- Whenever a net is driven by a signal, it takes the logic value of the signal
- When the signal source is tri-stated, the net too gets tri-stated
- In practice the net can have a capacitor associated with it, which can store the signal level even after the signal source dries up (*i.e.*, tri-stated)
- To account for this situation, a charge storage capacity is associated with the net
- Such nets are declared with the keyword **trireg**
- By virtue of the inherent capacitance associated with them, trireg nets can never be in the high impedance state – that is, they can assume 0, 1, or **x** value only

A **trireg** net can be in one of two possible states only:

Driven state:

When driven by a source or multiple sources, the net assumes the strength of the source. It can be any of the strengths specified in Table 1 except the high impedance value.

Capacitive state:

When the driven source (sources) is (are) tri-stated, the net retains the last value it was in – by virtue of the capacitance associated with it. The value can be 0, 1 or **x** (but not the high impedance value).

Table 1 Strength levels associated with outputs of gate primitives

Name	supply	strong	pull	weak	High impedance
Abbreviations	su1 su0	st1 st0	pu1 pu0	we1 we0	HiZ1 HiZ0
Strength	Strongest			Weakest	

- When in the capacitive state, a net can have a storage strength associated with it
- Three such storage strengths are possible – namely **large, medium,** and **small**
- When a storage strength is not specified, it is assigned the default value – **medium**
- For a **trireg** net one cannot assign storage strength capacity separately for the 0 and the 1 states
- A **trireg** net can be driven with possibilities of contention from two or more sources

Table 2 Capacitive storage strengths on nets

Name	`large`	`medium`	`small`
Strength	Strongest		Weakest

- Consider the design in Figure 1. As long as the signal control = 1, the signal out follows the signal in

- When control goes to 0, out is disconnected from the input and it '‘floats.'’ It retains the last value due to the capacitance storage capacity

- The storage strength is **medium,** signifying a medium value of capacitance

```
module charge(out,in,control);
output out;
trireg(medium)out;
input in,control;
bufif1 g1(out,in,control);
endmodule

module tst_charge; //TESTBENCH
reg in, control;
charge c1(out,in,control);
initial
    begin
    in =0;control =0;//when control=0 output is x
    #2 control =0;in =0;
    #2 control =1;in =0;
    #2 control =1;in =1;
    #2 control =0;in =0; // output is retained at
    end // the last value
initial $monitor($time ," in= %b ,control = %b , out=
%b " ,in,control,out);
initial #40$stop;
endmodule
```

```
output
        #     0 in = 0 , control = x , out=x
        #     2 in = 0 , control = 0 , out=x
        #     4 in = 0 , control = 1 , out=0
        #     6 in = 1 , control = 1 , out=1
        #     8 in = 0 , control = 0 , out=1
```

Figure 1 Illustration of net storage; the test bench and simulation results are also shown in the figure.