```
//TESTBENCH:
//ENCODER 4x2
                                          `timescale 1ns/1ps
module encoder4to2(i0,i1,i2,i3,y1,y0);
                                          module enco test;
input i0,i1,i2,i3;
                                          reg i0,i1,i2,i3;
output reg y1,y0;
                                          wire y1,y0;
always@*
                                          integer \square ;
case({i3,i2,i1,i0})
                                          encoder4to2 encoder(i0,i1,i2,i3,y1,y0); /*INSTANTIATE THE
4'b0001:{y1,y0}=2'b00;
                                          MODULE NAME (encoder4to2) THAT NEEDS BE TESTED WITH
4'b0010:{y1,y0}=2'b01;
                                          INSTANTIATION NAME encoder*/
4'b0100:{y1,y0}=2'b10;
                                          initial
4'b1000:{y1,y0}=2'b11;
                                          begin
default:{y1,y0}=2'bxx;
                                          \{i0,i1,i2,i3\}=0;
endcase
                                          for(i=1; i<16; i=i+1)
endmodule
                                          #5 \{i3,i2,i1,i0\} = \square;
                                          #150 $finish;
                                          end
                                          initial
                                          $monitor($time,"i0=%b, i1=%b, i2=%b, i3=%b, y1=%b,
                                          y0=\%b", \Box i0,i1,i2,i3,y1,y0);
                                          endmodule
```

1

```
module deco2to4(i0,i1,,y0,y1,y2,y3); input i0,i1; output reg y0,y1,y2,y3; always@(*) casex({i0,i1}) 3'b00:{y0,y1,y2,y3}=4'b1000; 3'b01:{y0,y1,y2,y3}=4'b0100; 3'b10:{y0,y1,y2,y3}=4'b0010; 3'b11:{y0,y1,y2,y3}=4'b0001; endcase endmodule
```

// DECODER 2x4

```
//TESTBENCH:
`timescale 1ns/1ps
module test decoder;
reg i0,i1;
wire y0,y1,y2,y3;
deco2to4 deco(i0,i1,y0,y1,y2,y3);
/*INSTANTIATE THE MODULE NAME(deco2to4) THAT NEEDS BE
TESTED
WITH INSTANTIATION NAME deco*/
initial
begin
{i0,i1}=0;
for(i=1;i<3;i=i+1);
#5 {i1,i0}=i;
end
initial
#150 $finish;
initial
$monitor($finish, "i0=%b,i1=%b,y0=%b,y1=%b,y2=%b,y3=%b",
i0,i1,y0,y1,y2,y3);
endmodule
```

2

PRIORITY ENCODER(BEHAVIOURAL)

w_3	w_2	w_1	w_0	y_1	y_0	z
0	0	0	0	d	d	0
0	0	0	1	0	0	1
0	0	1	x	0	1	1
0	1	x	X	1	0	1
1	X	x	X	1	1	1

```
module pe(w3,w2,w1,w0,y1,y0,z);
input w3,w2,w1,w0;
output y1,y0,z;
always@*
casex({w3,w2,w1,w0}) // note it is casex not case
4'b0000:{y1,y0,z}=3'b000;
4'b0001:{y1,y0,z}=3'b001;
4'b001x:{y1,y0,z}=3'b011;
4'b01xx:{y1,y0,z}=3'b101;
4'b1xxx:{y1,y0,z}=3'b111;
endcase
endmodule
```

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PRIORITY ENCODER(BEHAVIOURAL)

```
//Test bench
`timescale 1ns/1ps
module test_priority;
reg w3,w2,w1,w0;
wire y1,y0,z;
integer i;
pe encoder(w3,w2,w1,w0,y1,y0,z); /*INSTANTIATE THE MODULE NAME(pe)
THAT NEEDS BE TESTED WITH INSTANTIATION
NAME encoder*/
initial
begin
{w3,w2,w1,w0}=4'b0000;
for(i=1;i<16; i=i+1)
#5 {w3,w2,w1,w0}=i;
#150 $finish;
end
initial
monitor(time, w3=\%b, w2=\%b, w1=\%b, w0=\%b, y1=\%b, y0=\%b, z=\%b'', w3,w2,w1,w0,y1,y0,z);
endmodule
```

ZAKIR HUSSAIN Verilog HDL 4