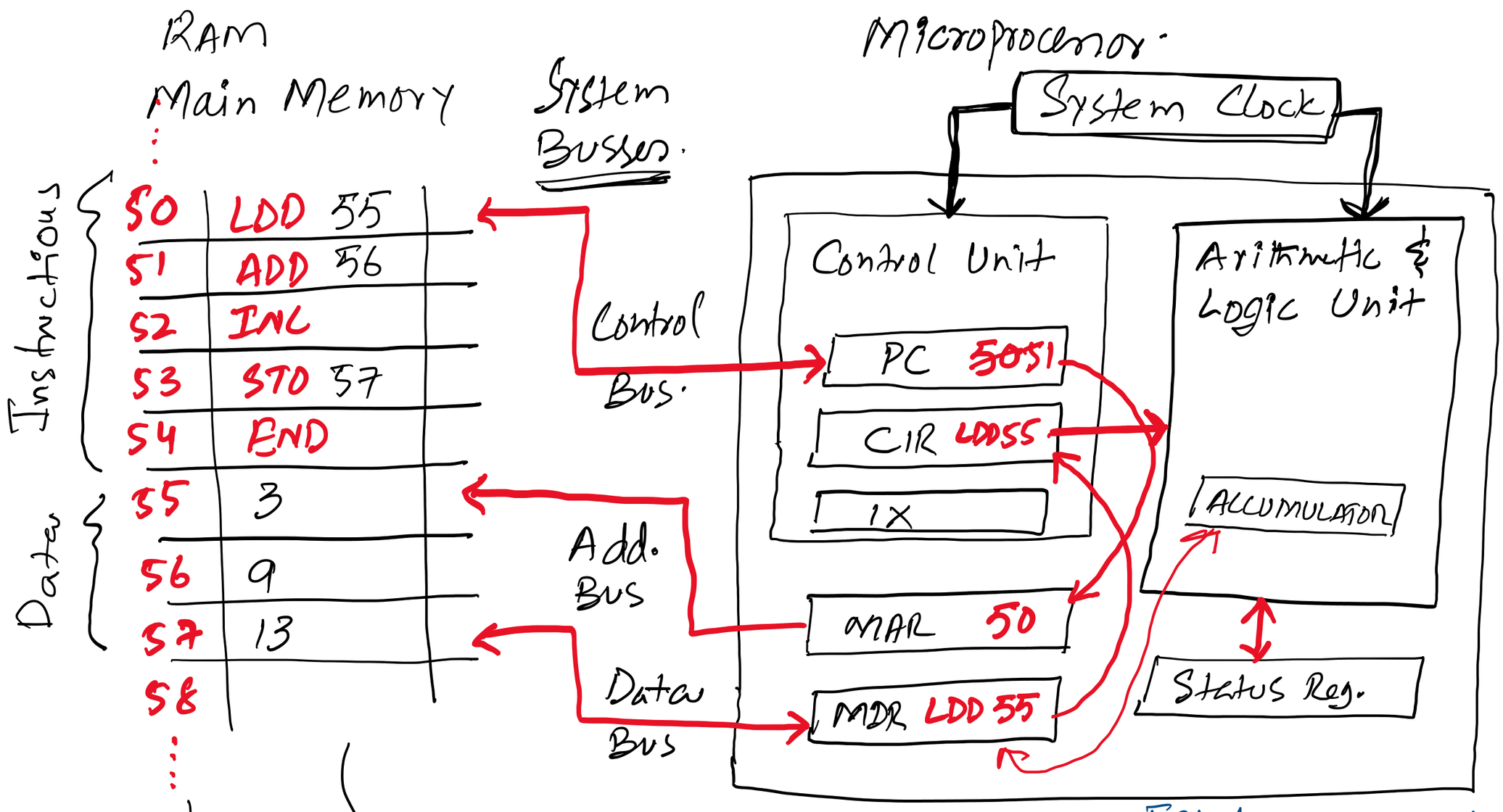
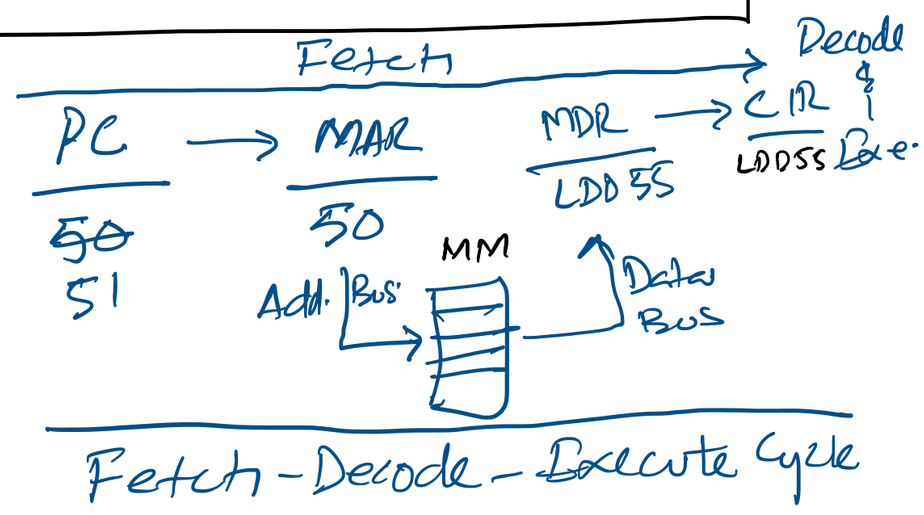
Processor Fundamentals:





Fetch - Decode - Execute cycle

Special Purpose

Accumulator: General purpose register that holds interim data.

Program Counter (PC): It holds the address of next inst.

Memory Address Register (MAR): It holds the addres of current inst.

Memory Data Register (MDR): It holds the inst. whose add. is saved in MAR. Curr. inst.

Current Inst. Register (CIR): It decodes, and executes the current inst.

FETCH, DECODE, EXECUTE CYCLE:

1) Addres of next instr. arrives in PC
2) From PC add. goes to MAR. It becomes current inst. address.
3) PC increments itself by 1.
4) Inst. at the add. in main memory, which is mentioned in MAR, arrives in MDR.
5) From MDR inst. goes to CIR.
6) CIR decodes and executes the inst.

Register transfer notation:

MAR ← [PC] [!]; The content of

PC ← [PC] + 1

MDR ← [[MAR]]

CIR ← [MDR]

[CIR]