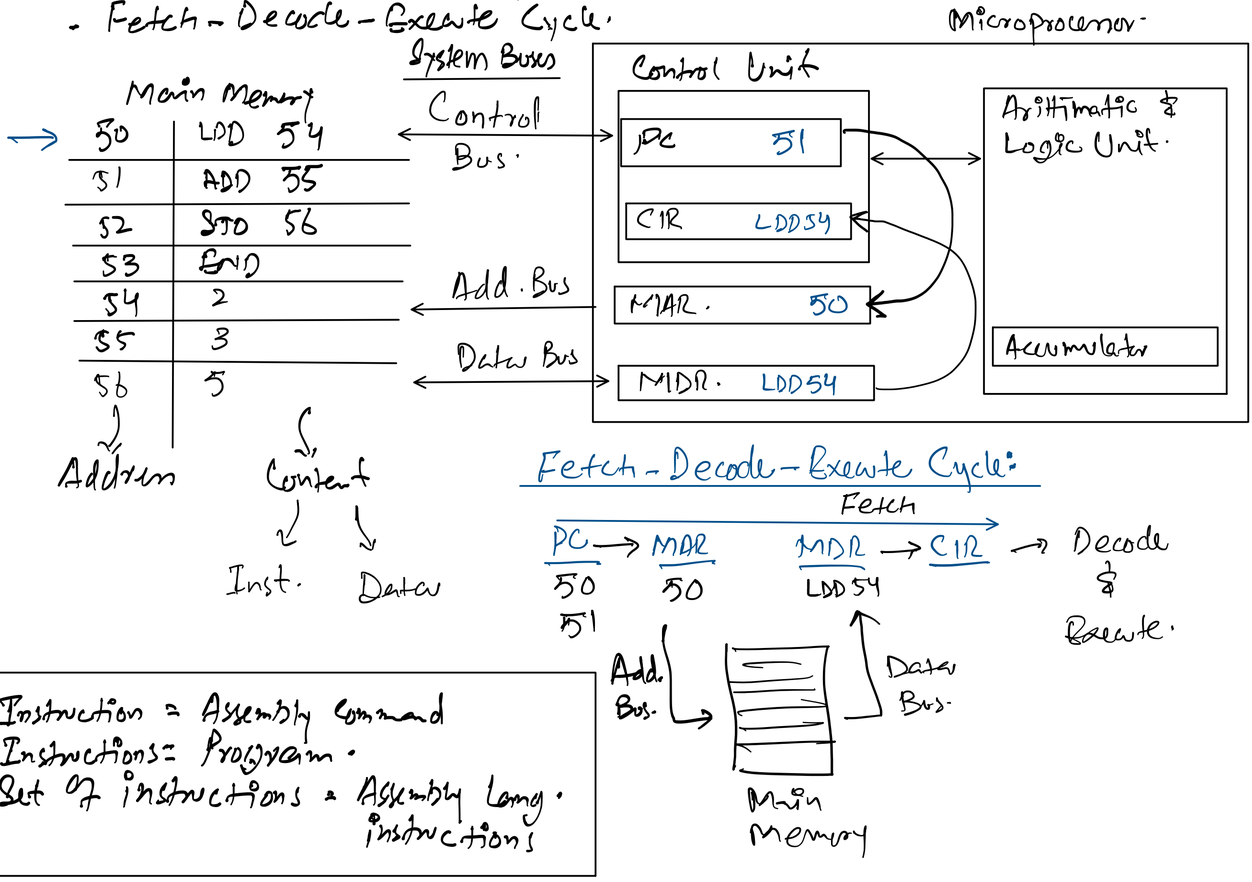
Architecture

Wednesday, 20 October 2021 4:27 PM

- Formation of microprocessor.
- CU, MU, ALU
- Registers: PC, CIR, MAR, MDR, Accumulator.
  Special Purpose General Purpose.
- Buses: Control, Addres, Data.
- Fetch - Decode - Execute Cycle.



Fetch - Decode - Execute Cycle:

Instruction = Assembly Command
Instructions = Program.
Set of instructions = Assembly Lang. instructions

Control Bus: It carries control signals from control unit to other parts of the system. It is bi-directional ↔

Address Bus: It carries address of the content in computer's main memory. It is uni-directional →

Data Bus: It carries the content back and forth b/w computer's microprocessor and main memory. It is bi-directional ↔.

CAIE Expectations:

1. FDEC
2. Registers
3. Buses.
4. FDEC practicle implementation.

Memory →
Microprocessor
MAR ← Add. 31
MDR ← Content. 9

MDR ← Value, Content 7
MAR ← Add. 33

30	8
31	9
32	2
33	7
34	5