Von Neumann Architecture.

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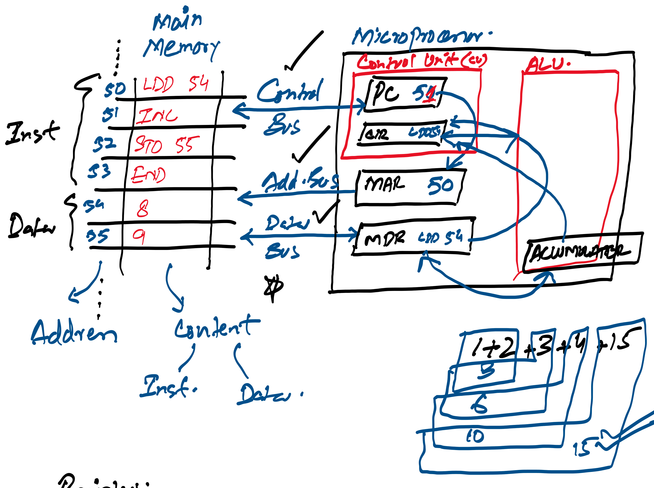
- VN Architecture
- Computer Architecture
- Architecture
- Idea of Stored program.

✓ - Definition
✓ - Fetch Decode Execute cycle FDEC.
✓ - Registers
- Buses.

Data & Instruction

Definition:

- Both the inst. & the data are indistinguishable when they are in binary form and should be kept in same main memory.
- Use of input, output & storage devices.
- It is a single processor made up of control unit (CU), memory unit (MU) & arithmetic & Logic unit (ALU).
- It is a serial machine.



Registers:

Special Purpose

- Program Counter (PC): It holds the address of next inst.
- Memory Address Register (MAR): It holds the add. of current inst.
- Current inst. Register (CIR): It decodes & executes inst.
- Memory Data Register (MDR): Inst. at the address mentioned in MAR arrives in MDR. It is the gateway b/w processor and memory.

General Purpose

- Accumulator: A general purpose register that keeps interim data

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Fetch Decode Execute Cycle:

FETCH

1. PC holds the add. of next. inst.
2. Add. from PC goes to MAR.
3. PC increases itself by 1.
4. MDR receives the instruction whose add. is saved in MAR.
5. From MDR current inst. goes to CIR.

Decode & Execute:

6. If the inst. has address part then it is copied to MAR.
7. CIR decodes & executes the current inst.

Buses:

Control Bus: It is used to send control signals.

Bi-directional
Two way

Address Bus: It carries the address to store data & inst. back & forth b/w processor & main memory.

Uni-directional
one-way.

Data Bus: It carries the data & instruction b/w processor & main memory.

Bi-directional
Two-way