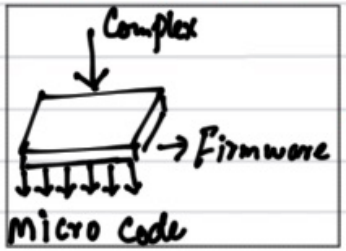
RISC CISC

MUL 23, 29, (#63 + #64), R4



CISC

C = Complex
I = Instruction
S = Set
C = Compuler

- Flexible inst. size
- Short code
- Compiler does less.
- Favourable for High level Languages
- Less effort for programmers
- procesor does more
- High heat generation
- Requires cooling system
- Desktops
- Bigger instruction set
- Memory to memory
  ↳ Load & store is built in.
- Complex production
- Expensive

RISC

R = Reduced
I = Instruction
S = Set
C = Compuler

LDM #63
ADD #64
PROD 29
PROD R4
STO 23

- fixed inst. size
- Large Code Size
- Compiler does more
- More effort for programmer
- Procesor has separate circuits for every instruction.
- procesor does less
- less heat generation
- Casings are enough to pacify the heat.
- Portable devices.
- less commands
- register to register
- Easy production methods
- Cheaper

Zak
ZAFAR ALI KHAN

CISC	RISC
C = Complex I = Instruction S = Set C = Computer	R = Reduced I = Instruction S = Set C = Computer
- Single instruction is executed in multiple cycles. - Uses control unit. ↳ Multiclock cycles per instruction.	- Single instruction is executed in single cycle. - Separate unit for every instruction. ↳ Single clock cycle per instruction.
- Many type of instructions are available for memory addressing.	- Only load and store instructions are available.
- Microprogrammed Control Unit	- Hard-wired control unit.
- Pipelining is difficult	- Pipelining is easier.