1.3.2 Computer architecture and the fetch execute cycle

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1.3.2 Computer

Computer Science 2210
Topical Past Papers

Zak ZAFAR ALI KHAN

Topic: 1.3.2 Computer architecture and the fetch execute cycle

Von Neumann Architecture:

1. (a) Describe what is meant by Von Neumann architecture. **[3]**
   (b) Explain the purpose of each of the following special registers in a processor.
   (i) Program Counter (Sequence Control Register) **[2]**
   (ii) Current Instruction Register. **[2]**
   (iii) Memory Address Register. **[2]**
   (iv) Memory Data Register. **[2]**
   (v) Accumulator

2. (a) Describe the purpose of the following registers in a processor:
   (i) Current instruction register (CIR), **[2]**
   (ii) Memory address register (MAR), **[2]**
   (iii) Program counter (PC), **[2]**
   (iv) Index register (IR). **[2]**

3. (a) Describe what is meant by Von Neumann architecture. **[2]**

4. (a) State the purpose of the Memory Address Register (MAR) in a computer. **[1]**
   (b) Describe two stages of the fetch/execute cycle which would change the contents of the MAR. State clearly, in each case, what the MAR contains. **[4]**

5. (a) (i) State what is held in the Program Counter (PC) during the fetch /execute cycle. **[1]**
   (ii) Explain how the contents of the PC change during the fetch/execute cycle. **[4]**
   (b) Describe the contents of the memory address register (MAR) during the fetch/execute cycle. **[4]**

6. (a) Describe basic Von Neumann processor architecture. **[3]**
   (b) At a particular point in a program, the program counter (PC) contains the value 200.
   (i) State the expected value contained in the PC after the instruction held at location 200 has been fetched.
   Explain your answer. **[2]**

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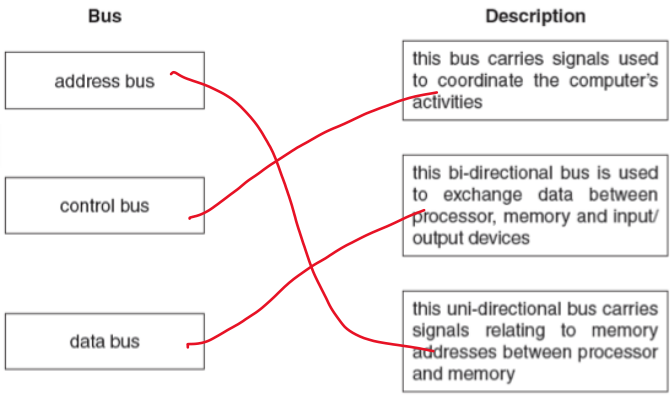
(ii) After the instruction is processed, the value in the PC is 180.
Explain why the value has changed to 180. **[2]**

7. State what is stored in each of the following special purpose registers in a computer and explainhow the contents are altered during the fetch/execute cycle.
   (i) MAR **[3]**
   (ii) MDR (or MBR) **[3]**
   (ii) CIR **[3]**

8. (a) Explain what is meant by Von Neumann architecture. **[3]**
   (b) (i) Explain what the accumulator holds and how the contents change during the fetch-execute cycle. **[2]**
   (ii) Explain what the program counter (PC) holds and how the contents change during the fetch-execute cycle. **[3]**

May/June 2015 P11 (2210)

7 (a) One of the key features of von Neumann computer architecture is the use of buses.
Three buses and three descriptions are shown below.
Draw a line to connect each bus to its correct description.



[2]

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(b) The seven stages in a von Neumann fetch-execute cycle are shown in the table below.
Put each stage in the correct sequence by writing the numbers 1 to 7 in the right hand column.
The first one has been done for you.

Stage	Sequence number
the instruction is then copied from the memory location contained in the MAR (memory address register) and is placed in the MDR (memory data register)	4
the instruction is finally decoded and is then executed	7
the PC (program counter) contains the address of the next instruction to be fetched	1
the entire instruction is then copied from the MDR (memory data register) and placed in the CIR (current instruction register)	5
the address contained in the PC (program counter) is copied to the	2

MAR (memory address register) via the address bus	2
the address part of the instruction, if any, is placed in the MAR (memory address register)	6
the value in the PC (program counter) is then incremented so that it points to the next instruction to be fetched	3

[6]

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Oct/Nov 2015 P13

3 A section of computer memory is shown below:

Address	Contents
1000 0000	0110 1110
1000 0001	0101 0001
1000 0010	1000 1101
1000 0011	1000 1100
⋮	⋮
1000 1100	
1000 1101	
1000 1110	
1000 1111	

MAR MDR.
Main Memory → Process.

(a) (i) The contents of memory location 1000 0001 are to be read.
Show the contents of the Memory Address Register (MAR) and the Memory Data Register (MDR) during this read operation:

MAR: 1 0 0 0 0 0 0 1

MDR: 0 1 0 1 0 0 0 1

[2]

(ii) The value 0111 1001 is to be written into memory location 1000 1110.
Show the contents of the MAR and MDR during this write operation:

Data

MAR: 1 0 0 0 1 1 1 0

MDR: 0 1 1 1 1 0 0 1

[2]

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(iii) Show any changes to the computer memory following the read and write operations in **part (a)(i)** and **part (a)(ii)**.

Address	Contents
1000 0000	0110 1110
1000 0001	0101 0001
1000 0010	1000 1101
1000 0011	1000 1100
⋮	⋮
1000 1100	
1000 1101	
1000 1110	0111 1001
1000 1111	

[1]

(b) Name **three** other registers used in computers. **[3]**

(c) The control unit is part of a computer system.
What is the function of the control unit? **[3]**

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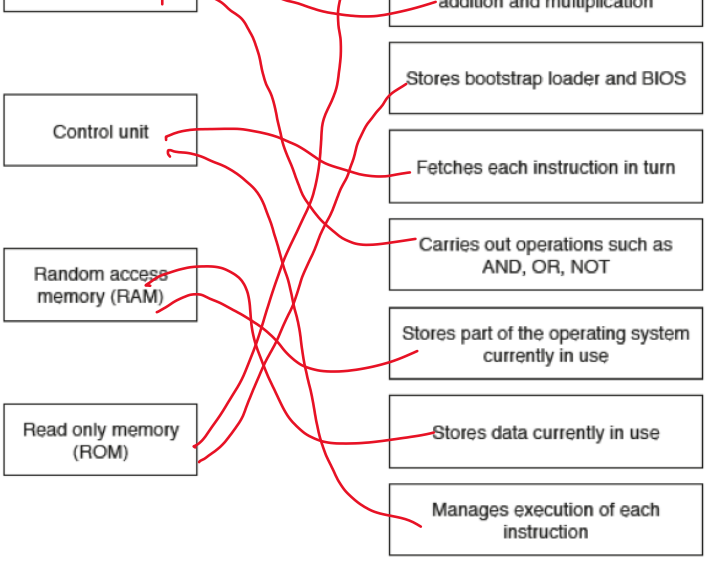
Oct/Nov 2016. P12

6 Four computer terms and **eight** descriptions are shown below.
Draw lines to connect each computer term to the correct description(s).

Computer term	Description
Arithmetic and logic unit (ALU)	Data can be read but not altered
	Carries out operations such as addition and multiplication



[4]

Oct/Nov 2016. P13

1 To process an instruction, a central processing unit (CPU) goes through a cycle that has three main stages.
Name each stage in this cycle. Fetch, Decode, Execute **[3]**

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May/June 2017. P11

6 Signals are sent to and from the components of a processor using buses.
Identify and describe the purpose of **two** different buses. **[6]**

May/June 2017. P12

1 Name **three** different buses that are used in the fetch-execute cycle. Control, Address, Data **[3]**

7 (c) A computer includes an Integrated Circuit (IC) and a Universal Serial Bus (USB) for data transmission.
Describe how the computer uses these for data transmission, including the type of data transmission used.

[4]

Oct/Nov 2017 P12(2210)

6 Selma writes the following **four** answers in her Computer Science examination.
State which computer terms she is describing.

"It is a signal. When the signal is received it tells the operating system that an event has occurred."
Selma is describing .....

"It takes source code written in a high level language and translates it into machine code. It translates the whole of the source code at once."
Selma is describing .....

"The part of the central processing unit (CPU) that carries out calculations."
Selma is describing ..... ALU

"When data is transmitted, if an error is detected in the data received a signal is sent to ask for the data to be retransmitted. This continues until the data received is correct."
Selma is describing .....

[4]

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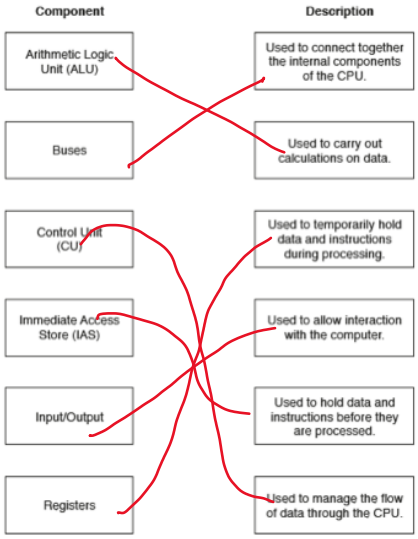
Oct/Nov 2017 P13(2210)

4 Six components of a computer system and **six** descriptions are shown.
Draw a line to match each component with the most suitable description.



[5]

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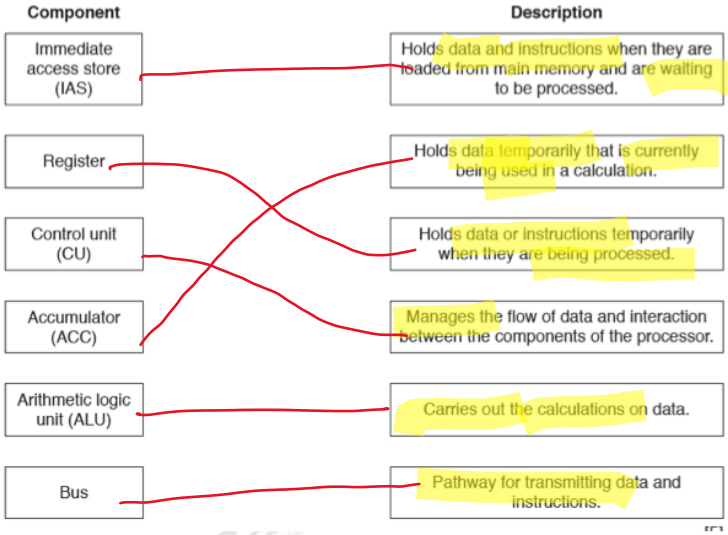
May/June 2018. P11

5 Six components of the Von Neumann model for a computer system and **six** descriptions are

given.
Draw a line to match each component to the most suitable description.



[5]

May/June 2018. P12

6 Kelvin correctly answers an examination question about the Von Neumann model.

Eight different terms have been removed from his answer.
Complete the sentences in Kelvin's answer, using the list given.
Not all items in the list need to be used.

- accumulator (ACC)
- address bus
- arithmetic logic unit (ALU)
- control unit (CU)
- data bus
- executed
- fetches
- immediate access store (IAS)
- memory address register (MAR)
- memory data register (MDR)
- program counter (PC)

- saved
- transmits

The central processing unit (CPU) ..... fetches .....
the data and instructions needed and stores them in the
..... main memory ; Immediate access store ..... to wait to be processed.
The ..... PC ..... holds the address of the next
instruction. This address is sent to the ..... MAR ..... .
The data from this address is sent to the ..... MDR ..... .
The instruction can then be decoded and ..... executed ..... .
Any calculations that are carried out on the data are done by the
..... ALU ..... . During calculations, the data is temporarily
held in a register called the ..... accumulator ..... .

[8]

Oct/Nov 2018 P13 (2210)
11
The fetch-execute cycle make use of registers.

(a) Describe the role of the Program Counter (PC).

- It holds the address of next inst.
- It increases itself by 1.

.....

.....[2]

(b) Describe the role of the Memory Data Register (MDR).

- It holds the current inst. whose address is placed in MAR
- It is supposed to be the gateway of microprocessor.

.....[2]