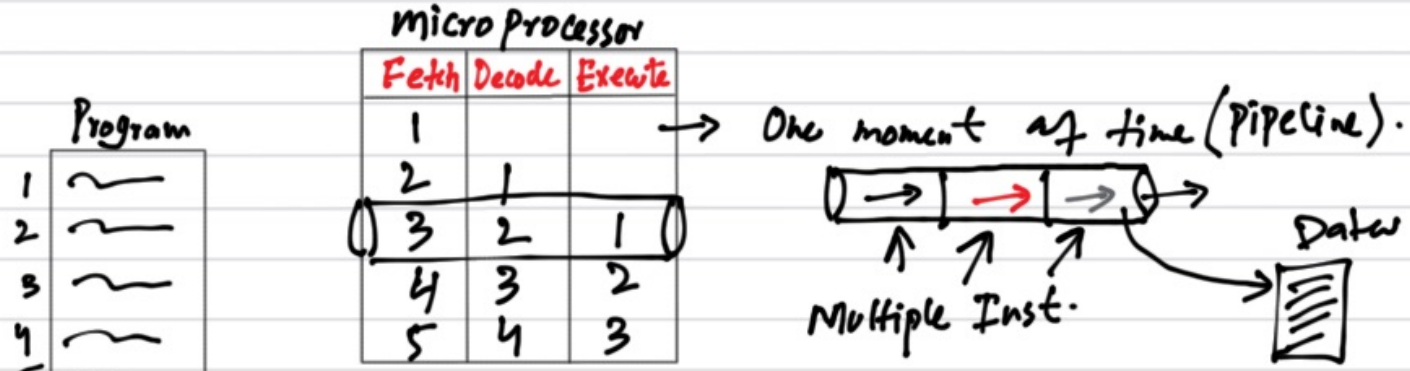
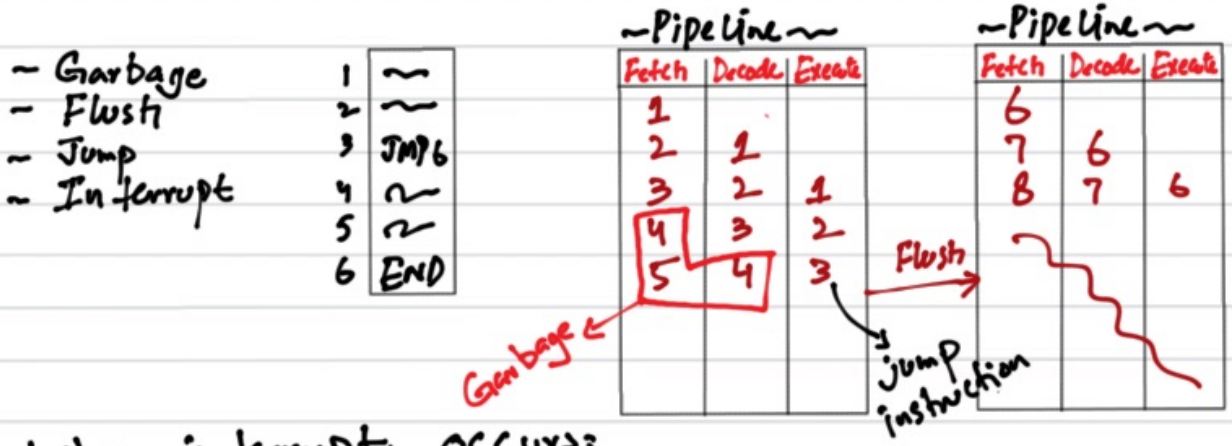
Pipelining

Fetch-Decode-Execute cycle:

Simple processors complete it once and then take next instruction.

In pipelining processor is divided into units, which perform FDEC steps simultaneously.

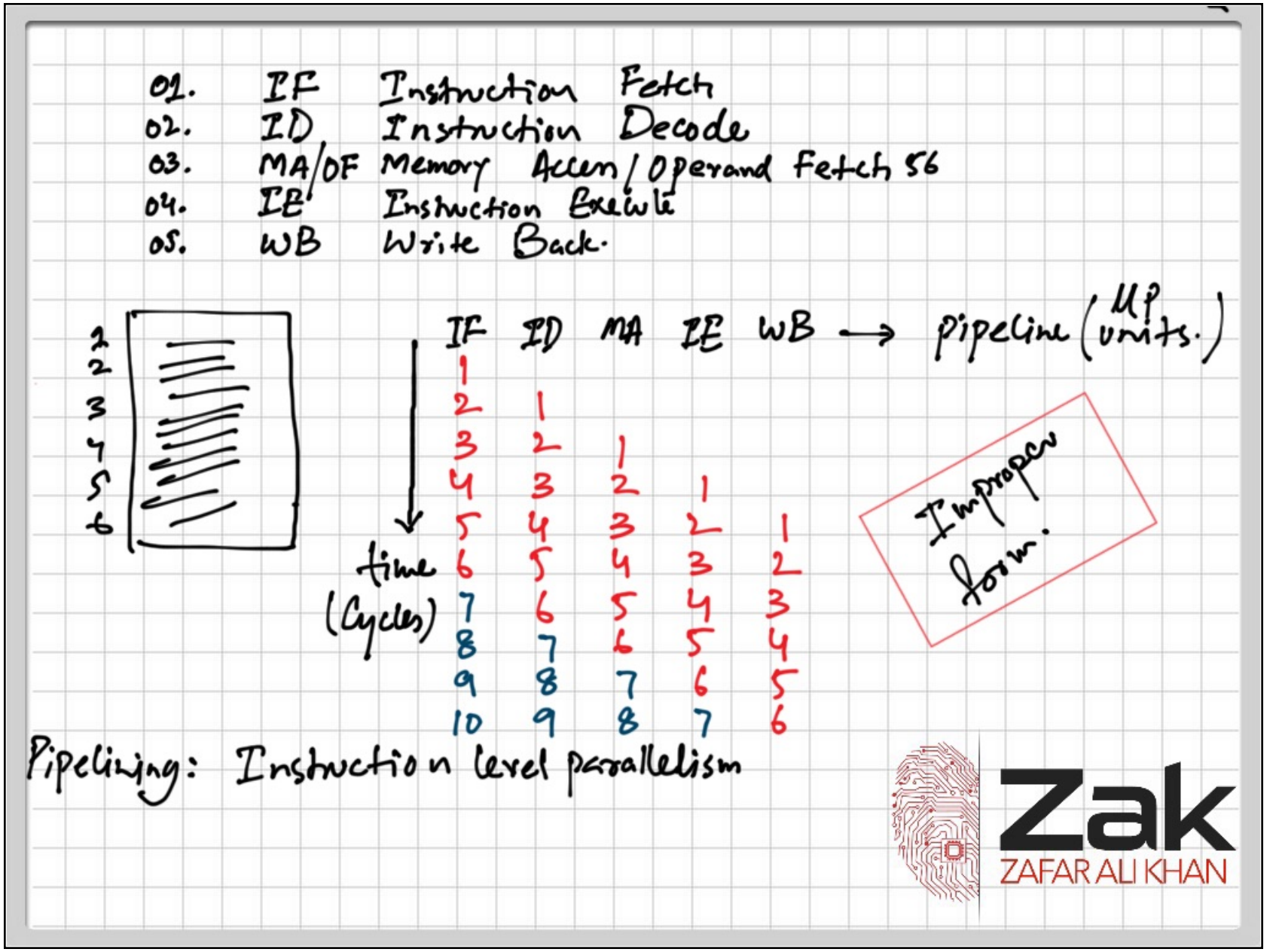


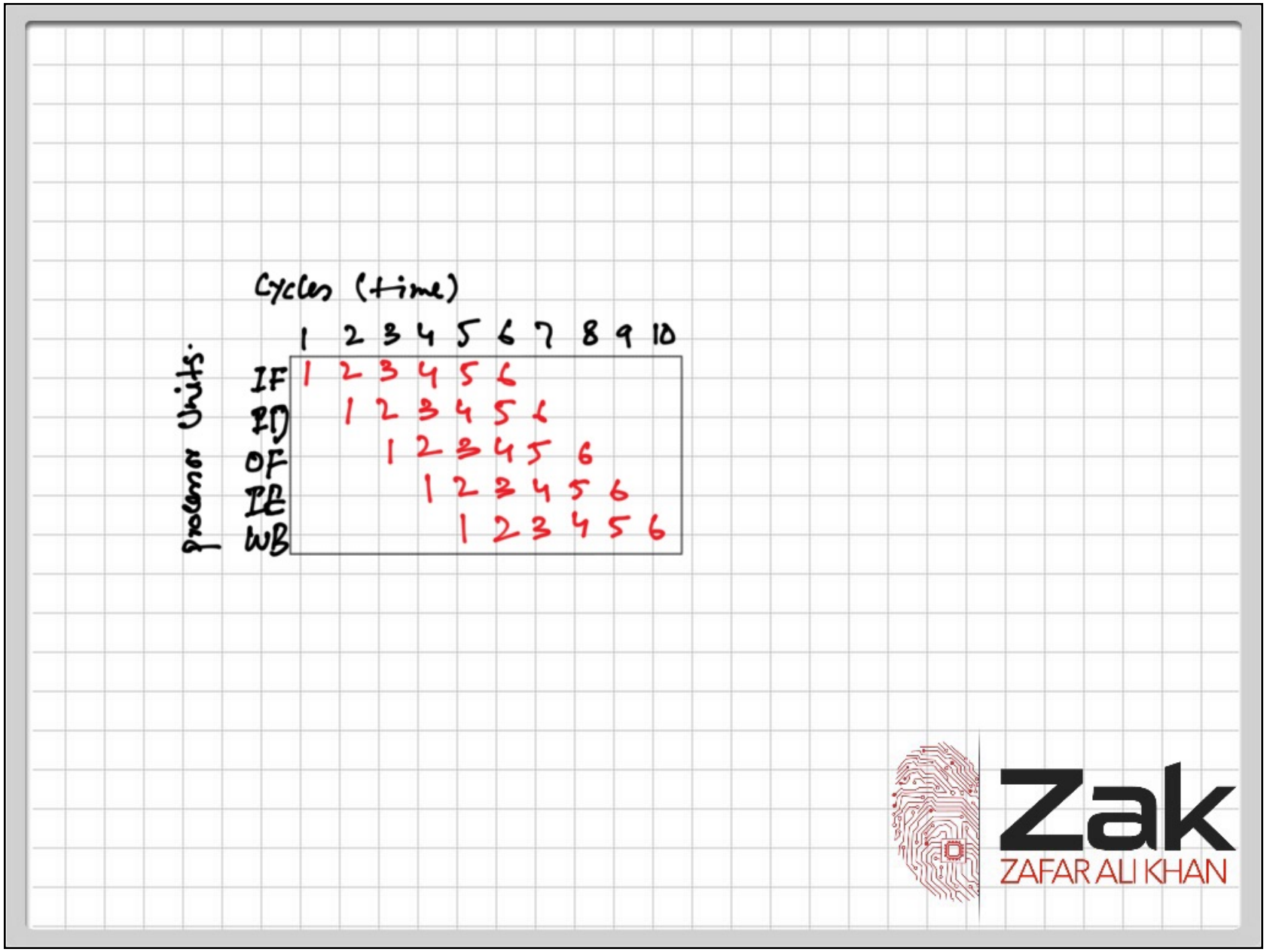


When 'interrupt occurs:

1) The inst. that is in execution will be completed and later along the inst. number from which the cycle will resume is saved in a memory stack and pipeline is flushed to take the program related to the interrupt.

2) There is another pipeline that will be used to handle the interrupt and current pipeline program related to is untouched and resume 'its working once interrupt related pipeline finishes working.


01. IF Instruction Fetch
02. ID Instruction Decode
03. MA/OF Memory Accen / Operand Fetch 56
04. IE Instruction Exewte
05. WB Write Back.
IF ID MA IE WB → pipeline (4 units.)
time (Cycles)
Improper flow.
Pipelining: Instruction level parallelism
Zak
ZAFAR ALI KHAN


Cycles (time)
1 2 3 4 5 6 7 8 9 10
Pipeline Units
IF
ID
OF
IE
WB
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