Memory Addressing Techniques

Monday, 4 October 2021 5:35 PM

Direct:

LDD
Load Direct.

100 | LDD 31

30	8
31	9
32	30
33	15

PC	MAR	MDR	CIR	ACC
100	100	LDD 31	LDD31	
101	31	9		9

Word Size:

Amount of data and number of bits a processor handles in one moment of time.
It is the size of bus, registers, address and constant.
Computer can input, process, output as much content. Computer instructions are of this size.

32 bits
$2^{32} = 4GB$

Mnemonic
OP-CODE OPERAND

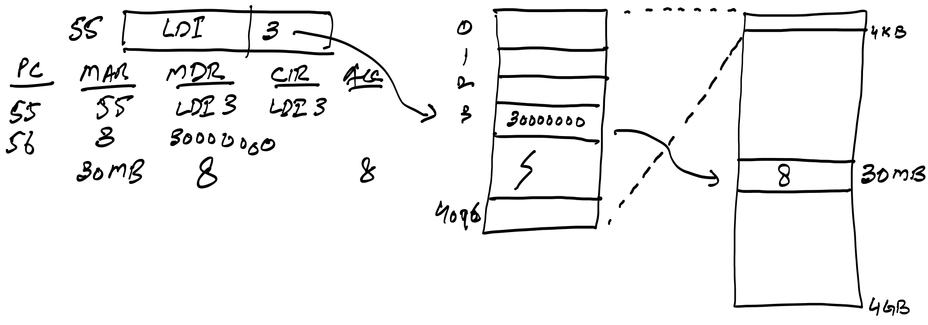
LDD | 31 — 32 bits

20 bits 5 : 3 12 bits

Add. Data
Empty

$2^{12} = 4096$
Direct Addresses

>4K
Indirectly Accessible Addresses.



Indirect Addressing:

LDI
Load Indirect

50 | LDI 33

30	8
31	9
32	11
33	30
34	2

PC	MAR	MDR	CIR	ACC
50	50	LDI 33	LDI 33	
51	33	30		
	30	8		8

Indexed:

IX
3
Index Register = IX

Offset / displacement

LDX
Indexed.

50 | LDX 31
Base Address

31 + 3 = 34
Actual Add.

30	8
31	6
32	2
33	1
34	9
35	100

PC	MAR	MDR	CIR	IX	ACC
50	50	LDX 31	LDX 31	4	
51	35	100			100