

**Bitwise Operators**  
 AND (check, clear)  
 OR (set)  
 XOR (invert)

Check:

00100100  
 AND 00000100  
 MASK 00000100

\* Accumulator is changed to an undesired value for checking. That's why we reload value.

clear:

01101110  
 AND 11011011  
 01001010

Set with OR:

00010011  
 OR 00100100  
 MASK 00100100  
 00110111

INVERT with XOR:

01101110  
 XOR 00100001  
 MASK 00100001  
 01001111

APPLICATIONS:

2's Complement:

-6 11111010  
 +6 00000110

256 | -6  
 257 | +6

LDD 256  
 XOR #255  
 INC  
 STD 257  
 END

ABSOLUTE ADDRESSING

1's Complement:

-6 11111010  
 XOR 11111111  
 00000101  
 ADD 00000001  
 +6 00000110

ACC  
 B1111010  
 B00000101  
 B00000110

ACC  
 250  
 5  
 6

\* When dealing with 2's numbers in bit manipulation use binary notations in registers.

LDD Num  
 XOR MASK1  
 INC  
 STD Num1  
 END  
 Num: -6  
 MASK1: 255  
 Num1:

SYMBOLIC ADDRESSING.

Shifting case Letter:

IN  
 STD LTR  
 AND MASK2  
 CMP #0  
 JPN LCW  
 UCW: LDD LTR  
 OR #32  
 STD LC  
 JMP STOP  
 LCW: LDD LTR  
 AND MASK1  
 STD UC  
 STOP: END

UC: B01000011  
 LC: B01100011  
 LTR: B01100011  
 MASK1: B11011111  
 MASK2: B00100000

INPUT a letter, LTR  
 CHECK the case,  
 IF LC Then convert to UC, UC  
 IF UC Then convert to LC, LC.

ACC Rough work

01000011  
 AND 00100000  
 MASK #32  
 00000000 IF0, UC  
 00100000 IF1, LC

01000011  
 OR 00100000  
 MASK 32  
 SET 01100011

01100011  
 AND 11011111  
 MASK 223  
 01000011