Pipelining.

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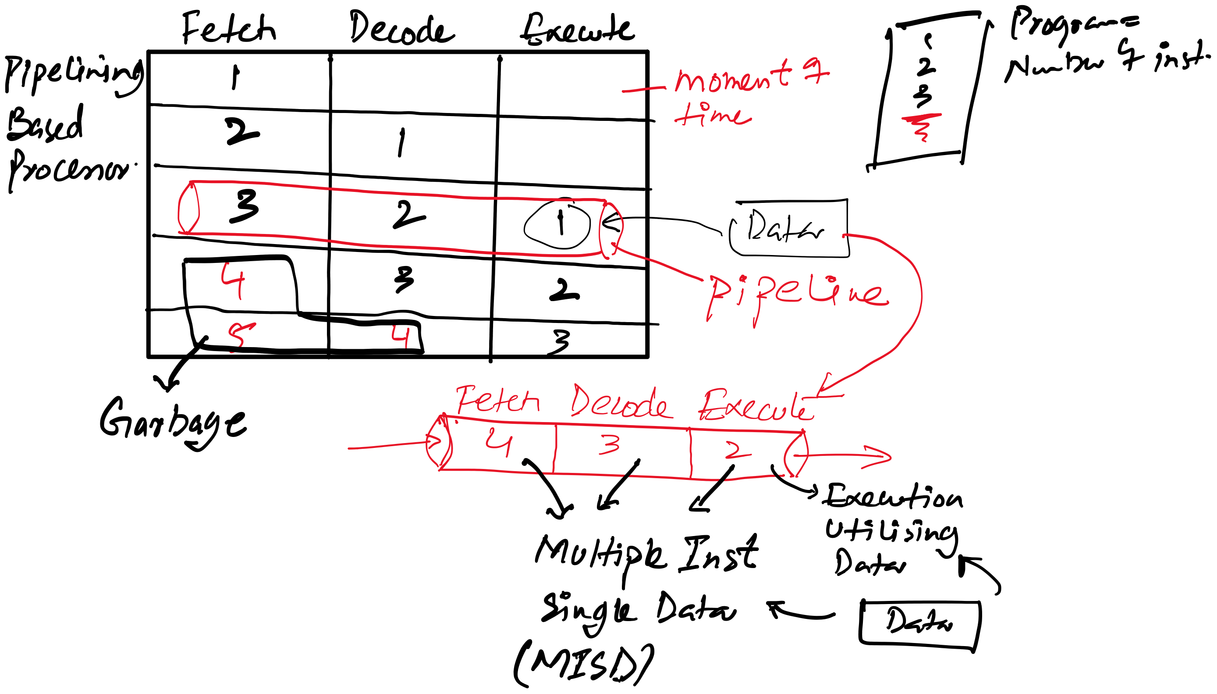
FDEC (Von-Neuman Architecture)

Fetch ← Next Inst.
↳ Decode
↳ Execute

One Complete FDEC then next.

In pipelining processor is divided into separate units for fetch, decode & execute. These units work in parallel.

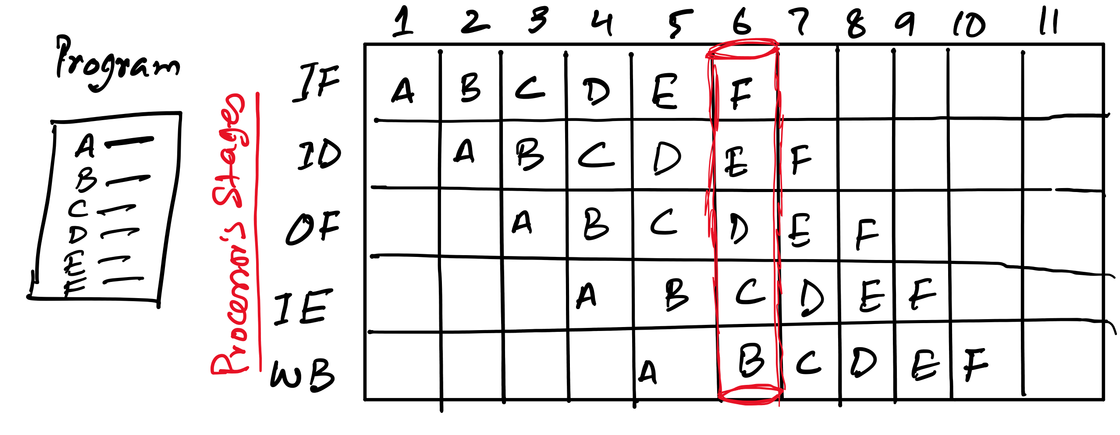


Instructions level parallelism.

Five Stages of execution:

1. inst. Fetch Cycle (IF)
2. inst. Decode Cycle (ID)
3. Operand Fetch Cycle (OF) / Memory Accen Cycle (MA)
4. inst. Execution Cycle (IE)
5. write back (WB)

CLOCK CYCLES.



Instructions: A, B, C, D, E, F #6
Regular VN Cycle: 6 × 5 = 30 clockcycles.
Pipelining: 10 clockcycles.