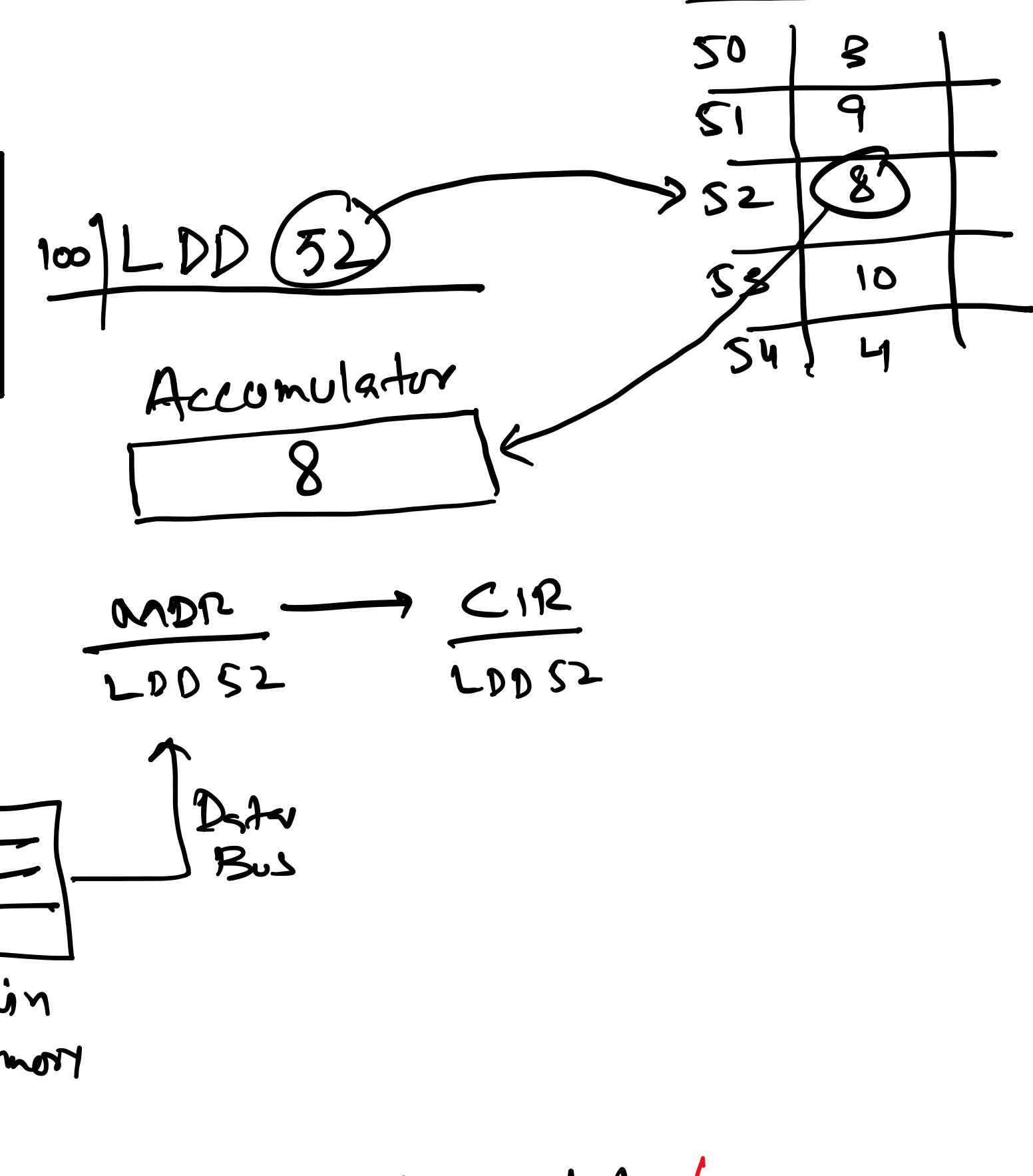


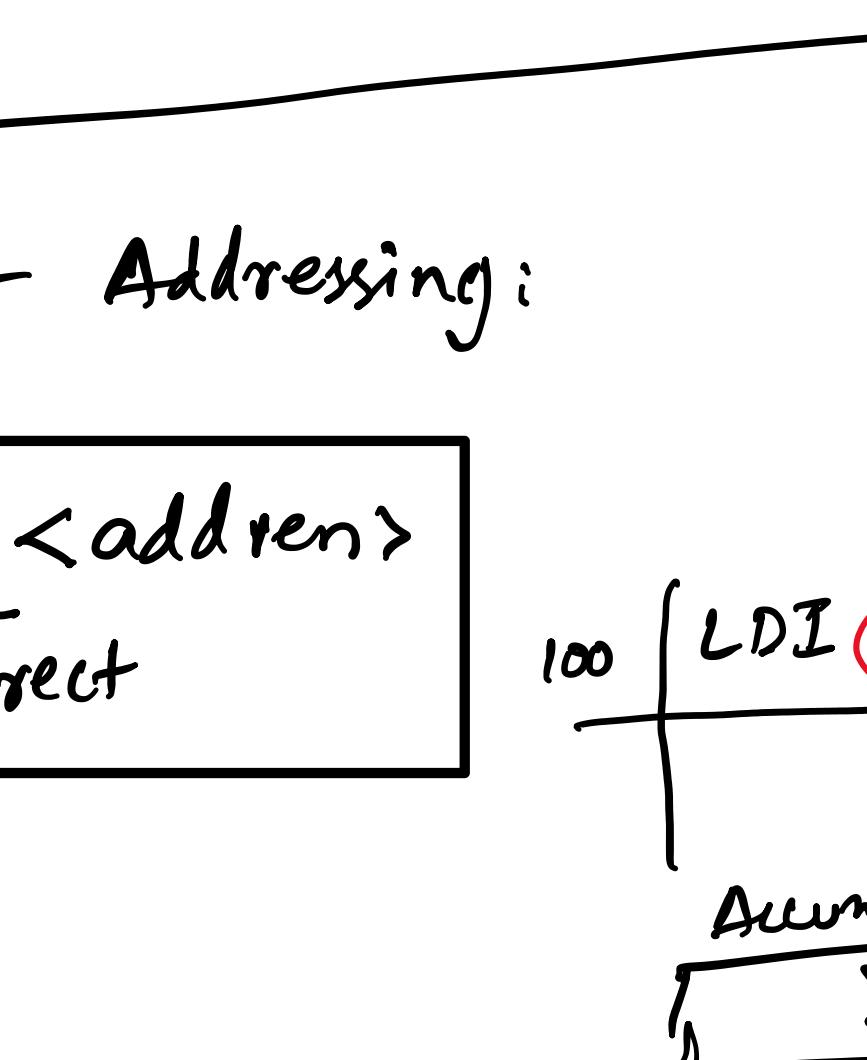
Modes of Addressing.

Direct Addressing:

LDD <address>
Load Direct



PC → MAR
100 → 100

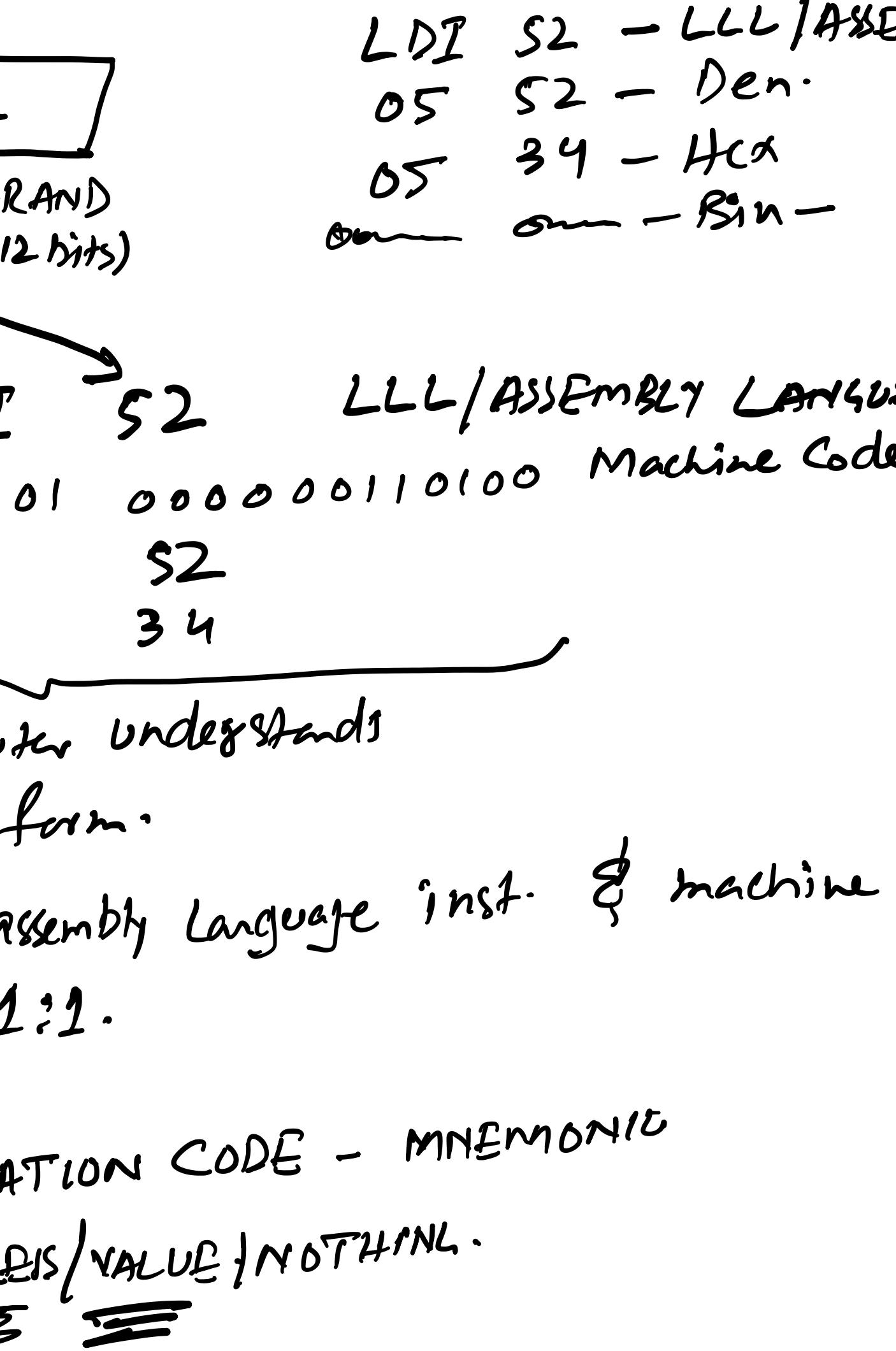


PC MAR MDR CIR Accumulator | Clock cycles
100 100 LDD 52 → LDD 52 8 | 4

Address Bus: 100 | 52
Data Bus: LDD 52 | 8

Indirect Addressing:

LDI <address>
Indirect



PC MAR MDR CIR Accumulator | Clock cycles
100 100 LDI 52 → LDI 52 2 | 5

ADDRESS BUS: 100 | 52 | 55
DATA BUS: LDI 52 | 55 | 2

WORD SIZE:

32 bits processor

$$2^{32} = 4\text{GB}$$

Max. Mem

CIR 32 bit
LDI 52 → 32 bits Instruction
Instruction Size 32 bits -

LDI S2 - LLL / ASSEMBLY -
05 S2 - Den.
05 34 - Hca
00000000000000000000000000000000 - Bin -

Instruction | LDI 52
OP-CODE | OPERAND
(20 bits) 5 : 3 (12 bits)

LDI 52

LLL / ASSEMBLY LANGUAGE → Machine Code.

B,00000000000000000000000000000000 000000010100 2,00000000000000000000000000000000 D-05 S2 II-05 34

Computer understands this form.

Relationship b/w assembly language inst. & machine language inst. is 1:1.

OP-CODE = OPERATION CODE - MNEMONIC

OPERAND = ADDRESS / VALUE / NOTHNGL.

A Computer inst. can only accm 4K addresses directly.

WORD size & Indirect Addressing:

OP-CODE 32 bits inst. size | LDD 202 | OPERAND 12 bits

$2^{12} = 4096 = 4K$.

MAX. MEM in 32 bits = 4GB

A Computer inst. can only accm 4K addresses directly.

Assembly

LDI 202 → 32 bits

Machine Code.

LDI 202 → 32 bits

Machine Code.