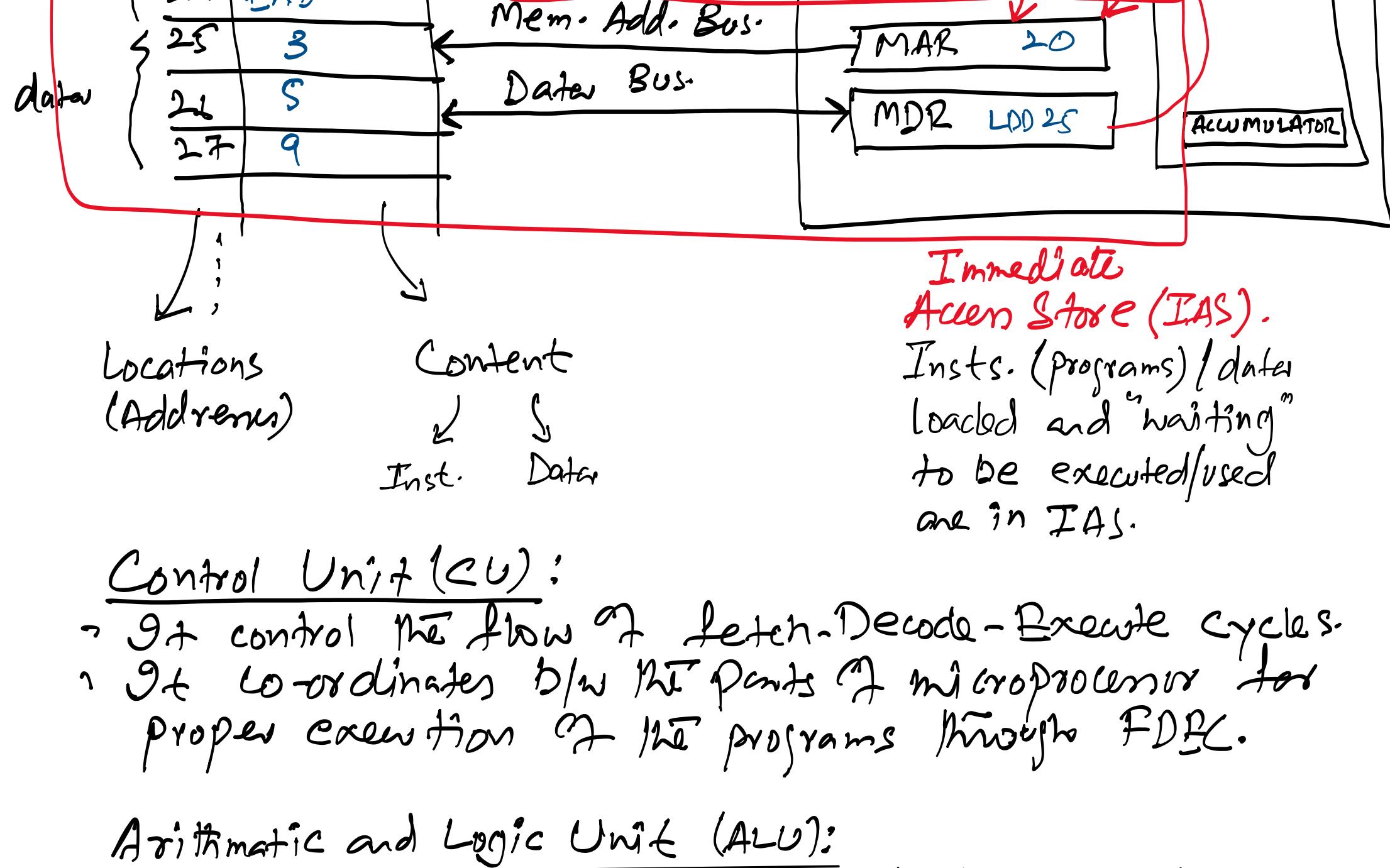


Computer Architecture AND Fetch Decode Execute Cycle.

Definition:

1. Both the inst. and data are in binary form and are indistinguishable. They are kept in same main memory.
2. A single processor, made up of 3 main parts. That is, **Control Unit (CU)**, Arithmetic & Logic Unit (ALU) and Memory Unit (MU).
3. It makes use of Input and output devices in addition to the storage devices. So, every code is stored for reuse. It is also called 'Idea of stored program'.
4. It is a serial machine.

Architecture:



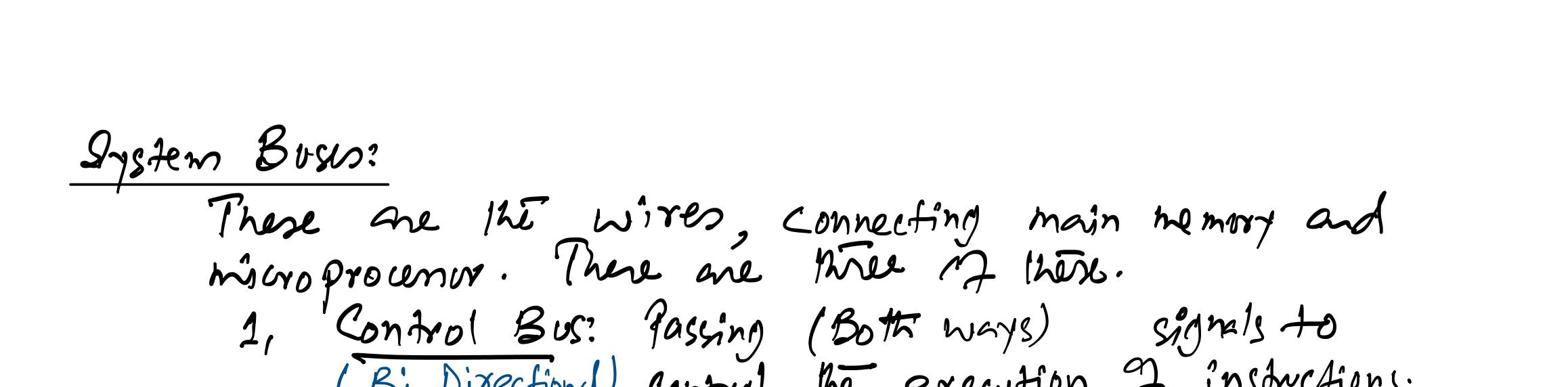
Control Unit (CU):

- It controls the flow of fetch-Decode-Execute cycles.
- It coordinates b/w the parts of microprocessor for proper execution of the programs through FDEC.

Arithmetic and Logic Unit (ALU):

- It does all the arithmetic operation (add, sub, mul, div)
- It does all the logical operations (AND, OR, NOT, XOR)
- It is supposed as "the hand" of microprocessor.

Registers:



System Bus:

These are the wires, connecting main memory and microprocessor. There are three of them.

- 1, Control Bus: Passing (Both ways) signals to (Bi-Directional) control the execution of instructions.
- 2, Mem. Add. Bus: It points to the current add. from (Uni-Directional) where the instruction will be fetched.
- 3, Data Bus: Carries the data/inst back and forth (Bi-Directional) b/w microprocessor and main memory.

Fetch-Decode-Execute (FDEC) Cycle:

1. PC holds the add. of next inst.
2. From PC add. goes to (Copy) MAR.
3. PC increments itself by 1.
4. Inst. from the add. mentioned MAR, arrives in MDR through data Bus.
5. Current Inst. in MDR arrives in (copy) CIR.

6. If the current inst. has add. part then it is copied to MAR.

7. Current inst. is decoded and executed.