

# UM0233 User manual

## STR91xFA firmware library

#### Introduction

#### **About this manual**

This document is the STR91xFA firmware library user manual. It describes the STR91xFA peripheral firmware library: a collection of routines, data structures and macros that cover the features of each peripheral.

This manual is structured as follows: some definitions, document conventions and firmware library rules are provided in *Section 1*. *Section 2* provides a detailed description of the Firmware library: The package content, the installation steps, the library structure and an example on how to use the library. Finally, Sections *3* to *20* describe the firmware library, peripheral configuration structure and functions description for each peripheral in detail.

#### **About STR91xFA library**

The STR91xFA Firmware library is a firmware package consisting of device drivers for all standard STR91xFA peripherals. You can use any STR91xFA device in applications without in-depth study of each peripheral specification. As a result, using this library can save you a lot of the time that you would otherwise spend in coding and also the cost of developing and integrating your application.

Each device driver consists of a set of functions covering the functionality of the peripheral. Since all the STR91xFA peripherals and their corresponding registers are memory-mapped, a peripheral can be easily controlled using 'C' code. The source code, developed in 'C', is fully documented. A basic knowledge of 'C' programming is required.

The library contains a complete firmware in 'C' that can be easily ported to any ARM compatible 'C' compiler.

Contents UM0233

# **Contents**

1	Docu	ument a	nd library rules
	1.1	Abbrev	iations
	1.2	Coding	rules
2	Firm	ware lib	rary
	2.1	Packag	e description
	2.2	Examp	les 18
	2.3	Library	
	2.4	Project	
	2.5	File de	scription
	2.6	How to	use the library
3	Perip	oheral fi	rmware overview
4	Flas	h memo	ry interface (FMI)24
	4.1	FMI reg	gister structure
		4.1.1	FMI register structure
	4.2	Firmwa	re library functions
		4.2.1	FMI_BankRemapConfig27
		4.2.2	FMI_Config
		4.2.3	FMI_EraseSector
		4.2.4	FMI_EraseBank
		4.2.5	FMI_WriteHalfWord
		4.2.6 4.2.7	FMI_WriteOTPHalfWord
			<del>-</del>
		4.2.8 4.2.9	FMI_ReadOTPData    34      FMI_GetFlagStatus    35
		4.2.10	FMI GetReadWaitStateValue
		4.2.11	FMI_GetWriteWaitStateValue
		4.2.12	FMI_SuspendEnable
		4.2.13	FMI_ResumeEnable
		4.2.14	FMI_ClearFlag
		4.2.15	FMI_WriteProtectionCmd38

UM0233 Contents

		4.2.16	FMI_WaitForLastOperation	. 39
		4.2.17	FMI_ReadRSIGData	. 40
5	Exte	rnal mei	mory interface (EMI)	41
	5.1	EMI reg	gister structure	41
		5.1.1	EMI register structure	. 41
	5.2	Firmwa	re library functions	44
		5.2.1	EMI_DeInit	. 44
		5.2.2	EMI_Init	. 44
		5.2.3	EMI_StructInit	. 49
		5.2.4	EMI_BCLKCmd	. 49
6	Syst	em cont	rol unit (SCU)	50
	6.1	Registe	er structure	50
		6.1.1	SCU register structure	. 50
	6.2	Firmwa	re library functions	53
		6.2.1	SCU_MCLKSourceConfig	. 54
		6.2.2	SCU_PLLFactorsConfig	. 55
		6.2.3	SCU_PLLCmd	. 55
		6.2.4	SCU_RCLKDivisorConfig	. 56
		6.2.5	SCU_HCLKDivisorConfig	. 56
		6.2.6	SCU_PCLKDivisorConfig	. 57
		6.2.7	SCU_FMICLKDivisorConfig	. 57
		6.2.8	SCU_EMIBCLKDivisorConfig	. 58
		6.2.9	SCU_BRCLKDivisorConfig	. 58
		6.2.10	SCU_TIMExtCLKCmd	. 59
		6.2.11	SCU_USBCLKConfig	. 59
		6.2.12	SCU_PHYCLKConfig	. 60
		6.2.13	SCU_APBPeriphClockConfig	. 60
		6.2.14	SCU_AHBPeriphClockConfig	. 61
		6.2.15	SCU_APBPeriphDebugConfig	. 61
		6.2.16	SCU_AHBPeriphDebugConfig	. 62
		6.2.17	SCU_APBPeriphIdleConfig	. 62
		6.2.18	SCU_AHBPeriphIdleConfig	. 62
		6.2.19	SCU_APBPeriphReset	. 63
		6.2.20	SCU_AHBPeriphReset	. 63
		6.2.21	SCU_EMIModeConfig	. 64

Contents UM0233

		6.2.22	SCU_EMIALEConfig64
		6.2.23	SCU_GetPLLFreqValue
		6.2.24	SCU_GetMCLKFreqValue65
		6.2.25	SCU_GetHCLKFreqValue
		6.2.26	SCU_GetPCLKFreqValue66
		6.2.27	SCU_GetRCLKFreqValue66
		6.2.28	SCU_WakeUpLineConfig67
		6.2.29	SCU_EnterIdleMode67
		6.2.30	SCU_EnterSleepMode67
		6.2.31	SCU_UARTIrDASelect
		6.2.32	SCU_PFQBCCmd69
		6.2.33	SCU_ITConfig
		6.2.34	SCU_GetFlagStatus70
		6.2.35	SCU_ClearFlag70
		6.2.36	SCU_EMIByte_Select_Pinconfig
		6.2.37	SCU_EMIclock_Pinconfig71
7	Gene	eral pur	pose I/O ports (GPIO)72
	7.1	GPIO r	register structure
	7.2	Firmwa	are library functions
		7.2.1	GPIO_DeInit
		7.2.2	GPIO_Init
		7.2.3	GPIO_StructInit78
		7.2.4	GPIO_ReadBit
		7.2.5	GPIO_Read
		7.2.6	GPIO_WriteBit
		7.2.7	GPIO_Write
		7.2.8	GPIO_ANAPinConfig
		7.2.9	GPIO_EMIConfig
8	Vecto	ored int	errupt controller (VIC)83
	8.1	VIC red	gister structure
	8.2	Ì	are library functions
	0.2	8.2.1	VIC_Delnit
		8.2.2	VIC_GetIRQStatus
		8.2.3	VIC_GetFIQStatus
		8.2.4	VIC_GetSourceITStatus
		0.2.4	vio_deloodicerrolalus00

UM0233 Contents

		8.2.5	VIC_ITCmd
		8.2.6	VIC_SWITCmd89
		8.2.7	VIC_ProtectionCmd
		8.2.8	VIC_GetCurrentISRAdd
		8.2.9	VIC_GetISRVectAdd90
		8.2.10	VIC_Config91
9	Wake	e-up inte	errupt unit (WIU)92
	9.1	WIU reg	gister structure
	9.2	Firmwa	re library functions 93
		9.2.1	WIU_Init
		9.2.2	WIU_DeInit96
		9.2.3	WIU_StructInit
		9.2.4	WIU_Cmd97
		9.2.5	WIU_GenerateSWInterrupt97
		9.2.6	WIU_GetFlagStatus
		9.2.7	WIU_ClearFlag98
		9.2.8	WIU_GetITStatus
		9.2.9	WIU_ClearITPendingBit
10	Real	time clo	ock (RTC)99
	10.1	RTC re	gister structure
	10.2	Firmwa	re library functions
		10.2.1	RTC_Delnit
		10.2.2	RTC_SetDate
		10.2.3	RTC_SetTime
		10.2.4	RTC_SetAlarm
		10.2.5	RTC_GetDate
		10.2.6	RTC_GetTime
		10.2.7	RTC_GetAlarm106
		10.2.8	RTC_TamperConfig106
		10.2.9	RTC_TamperCmd
		10.2.10	RTC_AlarmCmd107
		10.2.11	RTC_CalibClockCmd
		10.2.12	RTC_SRAMBattPowerCmd
		10.2.13	RTC_PeriodicIntConfig
		10.2.14	RTC_ITConfig

Contents UM0233

		10.2.15 10.2.16	RTC_GetFlagStatus
11	Watch	ndog tin	ner (WDG)
	11.1	WDG re	gister structure 111
	11.2	Firmwar	re library functions
		11.2.1	WDG_Init
		11.2.2	WDG_StructInit116
		11.2.3	WDG_StartWatchdogMode
		11.2.4	WDG_TimerModeCmd116
		11.2.5	WDG_ITConfig117
		11.2.6	WDG_GetITStatus
		11.2.7	WDG_ClearITPendingBit
		11.2.8	WDG_GetCounter
		11.2.9	WDG_GetFlagStatus
		11.2.10	WDG_GetFlagStatus
		11.2.11	WDG_Reload
12	16-bit	timer (	TIM)
		•	•
	12.1	TIM reg	ister structure
		TIM reg	re library functions
	12.1	TIM reg Firmwar 12.2.1	ister structure       121         re library functions       123         TIM_Delnit       124
	12.1	TIM reg Firmwar 12.2.1 12.2.2	ister structure       121         re library functions       123         TIM_DeInit       124         TIM_Init       124
	12.1	TIM reg Firmwar 12.2.1 12.2.2 12.2.3	ister structure       121         re library functions       123         TIM_Delnit       124         TIM_Init       124         TIM_StructInit       129
	12.1	TIM reg Firmwar 12.2.1 12.2.2 12.2.3 12.2.4	ister structure       121         re library functions       123         TIM_Delnit       124         TIM_Init       124         TIM_StructInit       129         TIM_PrescalerConfig       129
	12.1	TIM reg Firmwar 12.2.1 12.2.2 12.2.3 12.2.4 12.2.5	ister structure       121         re library functions       123         TIM_DeInit       124         TIM_Init       124         TIM_StructInit       129         TIM_PrescalerConfig       129         TIM_GetPrescalerValue       130
	12.1	TIM reg Firmwar 12.2.1 12.2.2 12.2.3 12.2.4 12.2.5 12.2.6	ister structure       121         re library functions       123         TIM_DeInit       124         TIM_Init       124         TIM_StructInit       129         TIM_PrescalerConfig       129         TIM_GetPrescalerValue       130         TIM_GetICAP1Value       130
	12.1	TIM reg Firmwar 12.2.1 12.2.2 12.2.3 12.2.4 12.2.5 12.2.6 12.2.7	ister structure       121         re library functions       123         TIM_DeInit       124         TIM_Init       124         TIM_StructInit       129         TIM_PrescalerConfig       129         TIM_GetPrescalerValue       130         TIM_GetICAP1Value       130         TIM_GetICAP2Value       131
	12.1	TIM reg Firmwar 12.2.1 12.2.2 12.2.3 12.2.4 12.2.5 12.2.6 12.2.7 12.2.8	ister structure       121         re library functions       123         TIM_DeInit       124         TIM_Init       124         TIM_StructInit       129         TIM_PrescalerConfig       129         TIM_GetPrescalerValue       130         TIM_GetICAP1Value       130         TIM_GetICAP2Value       131         TIM_GetPWMIPulse       131
	12.1	TIM reg Firmwar 12.2.1 12.2.2 12.2.3 12.2.4 12.2.5 12.2.6 12.2.7 12.2.8 12.2.9	ister structure       121         re library functions       123         TIM_Delnit       124         TIM_Init       124         TIM_StructInit       129         TIM_PrescalerConfig       129         TIM_GetPrescalerValue       130         TIM_GetICAP1Value       130         TIM_GetICAP2Value       131         TIM_GetPWMIPulse       131         TIM_GetPWMIPeriod       132
	12.1	TIM reg Firmwar 12.2.1 12.2.2 12.2.3 12.2.4 12.2.5 12.2.6 12.2.7 12.2.8 12.2.9 12.2.10	ister structure       121         re library functions       123         TIM_Delnit       124         TIM_Init       124         TIM_StructInit       129         TIM_PrescalerConfig       129         TIM_GetPrescalerValue       130         TIM_GetICAP1Value       130         TIM_GetICAP2Value       131         TIM_GetPWMIPulse       131         TIM_GetPWMIPeriod       132         TIM_CounterCmd       132
	12.1	TIM reg Firmwar 12.2.1 12.2.2 12.2.3 12.2.4 12.2.5 12.2.6 12.2.7 12.2.8 12.2.9 12.2.10 12.2.11	ister structure       121         re library functions       123         TIM_Delnit       124         TIM_Init       124         TIM_StructInit       129         TIM_PrescalerConfig       129         TIM_GetPrescalerValue       130         TIM_GetICAP1Value       130         TIM_GetICAP2Value       131         TIM_GetPWMIPulse       131         TIM_GetPWMIPeriod       132         TIM_CounterCmd       132         TIM_SetPulse       133
	12.1	TIM reg Firmwar 12.2.1 12.2.2 12.2.3 12.2.4 12.2.5 12.2.6 12.2.7 12.2.8 12.2.9 12.2.10 12.2.11 12.2.12	ister structure       121         re library functions       123         TIM_Delnit       124         TIM_Init       124         TIM_StructInit       129         TIM_PrescalerConfig       129         TIM_GetPrescalerValue       130         TIM_GetICAP1Value       130         TIM_GetICAP2Value       131         TIM_GetPWMIPulse       131         TIM_GetPWMIPeriod       132         TIM_CounterCmd       132         TIM_SetPulse       133         TIM_GetFlagStatus       133
	12.1	TIM reg Firmwar 12.2.1 12.2.2 12.2.3 12.2.4 12.2.5 12.2.6 12.2.7 12.2.8 12.2.9 12.2.10 12.2.11 12.2.12 12.2.13	ister structure       121         re library functions       123         TIM_DeInit       124         TIM_Init       124         TIM_StructInit       129         TIM_PrescalerConfig       129         TIM_GetPrescalerValue       130         TIM_GetICAP1Value       130         TIM_GetICAP2Value       131         TIM_GetPWMIPulse       131         TIM_GetPWMIPeriod       132         TIM_CounterCmd       132         TIM_SetPulse       133         TIM_GetFlagStatus       133         TIM_ClearFlag       134
	12.1	TIM reg Firmwar 12.2.1 12.2.2 12.2.3 12.2.4 12.2.5 12.2.6 12.2.7 12.2.8 12.2.9 12.2.10 12.2.11 12.2.12 12.2.13 12.2.14	ister structure       121         re library functions       123         TIM_Delnit       124         TIM_Init       124         TIM_StructInit       129         TIM_PrescalerConfig       129         TIM_GetPrescalerValue       130         TIM_GetICAP1Value       130         TIM_GetICAP2Value       131         TIM_GetPWMIPulse       131         TIM_GetPWMIPeriod       132         TIM_CounterCmd       132         TIM_SetPulse       133         TIM_GetFlagStatus       133         TIM_ClearFlag       134         TIM_ITConfig       134
	12.1	TIM reg Firmwar 12.2.1 12.2.2 12.2.3 12.2.4 12.2.5 12.2.6 12.2.7 12.2.8 12.2.9 12.2.10 12.2.11 12.2.12 12.2.13	ister structure       121         re library functions       123         TIM_DeInit       124         TIM_Init       124         TIM_StructInit       129         TIM_PrescalerConfig       129         TIM_GetPrescalerValue       130         TIM_GetICAP1Value       130         TIM_GetICAP2Value       131         TIM_GetPWMIPulse       131         TIM_GetPWMIPeriod       132         TIM_CounterCmd       132         TIM_SetPulse       133         TIM_GetFlagStatus       133         TIM_ClearFlag       134

UM0233 Contents

		12.2.17 TIM_DM	ACmd	. 137
13	DMA	controller (DMA	A)	138
	13.1	DMA register stru	ucture	138
	13.2	Firmware library	functions	142
		13.2.1 DMA_De	lnit	. 143
		13.2.2 DMA_Init	t	. 144
		13.2.3 DMA_Str	ructInit	. 150
		13.2.4 DMA_Cn	nd	. 150
		13.2.5 DMA_ITM	MaskConfig	. 151
		13.2.6 DMA_Ch	annelSRCIncConfig	. 152
		13.2.7 DMA_Ch	annelDESIncConfig	. 152
		13.2.8 DMA_Ge	etChannelActiveStatus	. 153
		13.2.9 DMA_ITO	Config	. 153
		13.2.10 DMA_Ge	etChannelStatus	. 154
		13.2.11 DMA_Ge	etITStatus	. 155
		13.2.12 DMA_Cle	earlT	. 157
		13.2.13 DMA_Sy	ncConfig	. 158
		13.2.14 DMA_Ge	etSReq	. 159
		13.2.15 DMA_Ge	otLSReq	. 159
		13.2.16 DMA_Ge	etBReq	. 160
		13.2.17 DMA_Ge	etLBReq	. 160
		13.2.18 DMA_Se	tSReq	. 160
		13.2.19 DMA_Se	tLSReq	. 161
		13.2.20 DMA_Se	tBReq	. 161
		13.2.21 DMA_Se	tLBReq	. 162
		13.2.22 DMA_Ch	annelCmd	. 162
		13.2.23 DMA_Ch	annelHalt	. 163
		13.2.24 DMA_Ch	annelBuffering	. 163
		13.2.25 DMA_Ch	annelLockTrsf	. 164
		13.2.26 DMA_Ch	annelCache	. 164
		13.2.27 DMA_Ch	annelProt0Mode	. 165
		13.2.28 DMA_LL	I_CCR_Init	. 165
14	Sync	nronous serial p	peripheral (SSP)	169
	14.1	SSP register stru	cture	169
	14.2	Firmware library	functions	171

Contents UM0233

		14.2.1	SSP_Delnit
		14.2.2	SSP_Init
		14.2.3	SSP_StructInit
		14.2.4	SSP_Cmd176
		14.2.5	SSP_ITConfig
		14.2.6	SSP_DMACmd178
		14.2.7	SSP_SendData
		14.2.8	SSP_ReceiveData179
		14.2.9	SSP_LoopBackConfig
		14.2.10	SSP_GetFlagStatus
		14.2.11	SSP_ClearFlag
		14.2.12	SSP_GetITStatus182
		14.2.13	SSP_ClearITPendingBit
		_	
15	Unive	-	ynchronous receiver transmitter (UART) 184
	15.1	UART re	egister structure 184
	15.2	Firmwai	re library functions
		15.2.1	UART_DeInit
		15.2.2	UART_Init
		15.2.3	UART_StructInit
		15.2.4	UART_Cmd193
		15.2.5	UART_ITConfig
		15.2.6	UART_DMAConfig
		15.2.7	UART_DMACmd195
		15.2.8	UART_LoopBackConfig
		15.2.9	UART_IrDALowPowerConfig
		15.2.10	UART_IrDACmd
		15.2.11	UART_IrDASetCounter197
		15.2.12	UART_SendData198
		15.2.13	UART_ReceiveData
		15.2.14	UART_SendBreak199
		15.2.15	UART_RTSConfig199
		15.2.16	UART_DTRConfig
		15.2.17	UART_GetFlagStatus
		15.2.18	UART_ClearFlag
		15.2.19	UART_GetITStatus
		15.2.20	UART_ClearITPendingBit

UM0233 Contents

16	I2C iı	nterface	module (I2C)	. 203
	16.1	I2C regi	ister structure	203
	16.2	Firmwa	re library functions	205
		16.2.1	I2C_Delnit	205
		16.2.2	I2C_Init	206
		16.2.3	I2C_StructInit	207
		16.2.4	I2C_Cmd	208
		16.2.5	I2C_GenerateSTART	208
		16.2.6	I2C_GenerateSTOP	209
		16.2.7	I2C_AcknowledgeConfig	209
		16.2.8	I2C_ITConfig	210
		16.2.9	I2C_ReadRegister	210
		16.2.10	I2C_GetFlagStatus	212
		16.2.11	I2C_ClearFlag	213
		16.2.12	I2C_Send7bitAddress	214
		16.2.13	I2C_SendData	214
		16.2.14	I2C_ReceiveData	215
		16.2.15	I2C_GetLastEvent	215
		16.2.16	I2C_CheckEvent	216
17	3-pha	ase indu	ction motor controller (MC)	. 217
	17.1	MC regi	ister structure	. 217
	17.2	Firmwa	re library functions	. 220
		17.2.1	MC Delnit	
		17.2.2	MC Init	
		17.2.3	_	
		17.2.4	MC_Cmd	
		17.2.5	MC_ClearPWMCounter	
		17.2.6	MC_ClearTachoCounter	
		17.2.7	MC_CtrlPWMOutputs	
		17.2.8	MC_ITConfig	
		17.2.9	MC_SetPrescaler	
		17.2.10	MC_SetPeriod	
		17.2.11	MC_SetPulseU	
		17.2.12	MC_SetPulseV	
		17.2.13	MC_SetPulseW	
		17.2.14		
				<b>-</b>

Contents UM0233

		17.2.15	MC_PWMModeConfig	233
		17.2.16	MC_SetDeadTime	233
		17.2.17	MC_EmergencyCmd	234
		17.2.18	MC_EmergencyClear	234
		17.2.19	MC_GetPeriod	235
		17.2.20	MC_GetPulseU	235
		17.2.21	MC_GetPulseV	236
		17.2.22	MC_GetPulseW	236
		17.2.23	MC_GetTachoCapture	237
		17.2.24	MC_ClearOnTachoCapture	237
		17.2.25	MC_ForceDataTransfer	238
		17.2.26	MC_SoftwarePreloadConfig	238
		17.2.27	MC_SoftwareTachoCapture	239
		17.2.28	MC_GetCountingStatus	239
		17.2.29	MC_GetFlagStatus	240
		17.2.30	MC_ClearFlag	241
		17.2.31	MC_GetITStatus	241
		17.2.32	MC_ClearITPendingBit	242
		17.2.33	MC_Lock	242
		17.2.34	MC_CounterModeConfig	243
		17.2.35	MC_DoubleUpdateMode	243
		17.2.36	MC_ADCTrigger	244
		17.2.37	MC_EnhancedStop	244
		17.2.38	MC_DebugOutputProtection	245
		17.2.39	MC_EmergencyStopPolarity	245
18	Contr	oller ar	ea network (CAN)	246
	18.1		gister structure	
	18.2	•	re library functions	
	10.2	18.2.1	CAN_Delnit	
		18.2.2	CAN_Init	
		18.2.3	CAN StructInit	
		18.2.4	CAN EnterInitMode	
		18.2.5	CAN LeaveInitMode	
		18.2.6	CAN_LeaveInitiviode	
		18.2.7	CAN_LeaveTestMode	
		18.2.8	CAN_SetBitrate	
		10.2.0	OAN_OUDITIALS	201

UM0233 Contents

		18.2.9	CAN_SetTiming
		18.2.10	CAN_SetUnusedMsgObj
		18.2.11	CAN_SetTxMsgObj
		18.2.12	CAN_SetRxMsgObj
		18.2.13	CAN_SetUnusedAllMsgObj
		18.2.14	CAN_ReleaseMessage
		18.2.15	CAN_ReleaseTxMessage
		18.2.16	CAN_ReleaseRxMessage
		18.2.17	CAN_UpdateMsgObj
		18.2.18	CAN_TransmitRequest
		18.2.19	CAN_SendMessage
		18.2.20	CAN_ReceiveMessage
		18.2.21	CAN_WaitEndOfTx
		18.2.22	CAN_BasicSendMessage
		18.2.23	CAN_BasicReceiveMessage
		18.2.24	CAN_GetMsgReceiveStatus
		18.2.25	CAN_GetMsgTransmitRequestStatus
		18.2.26	CAN_GetMsgInterruptStatus
		18.2.27	CAN_GetMsgValidStatus
		18.2.28	CAN_GetFlagStatus
		18.2.29	CAN_GetTransmitErrorCounter
		18.2.30	CAN_GetReceiveErrorCounter
10	A I -	- 4	wital a assessment (ADO)
19			gital converter (ADC)
	19.1	-	gister structure
	19.2		re library functions
		19.2.1	ADC_Delnit
		19.2.2	ADC_StructInit
		19.2.3	ADC_Init
		19.2.4	ADC_PrescalerConfig
		19.2.5	ADC_GetPrescalerValue
		19.2.6	ADC_GetFlagStatus
		19.2.7	ADC_ClearFlag
		19.2.8	ADC_GetConversionValue
		19.2.9	ADC_GetAnalogWatchdogResult
		19.2.10	ADC_ClearAnalogWatchdogResult
		19.2.11	ADC_GetWatchdogThreshold

Contents UM0233

21	Revis	sion his	tory
		20.2.6	AHBAPB_GetPeriphAddrError
		20.2.5	AHBAPB_ClearFlag
		20.2.4	AHBAPB_GetFlagStatus
		20.2.3	AHBAPB_StructInit
		20.2.2	AHBAPB_Init
		20.2.1	AHBAPB_DeInit
	20.2	Firmwa	re library functions
	20.1	AHBAP	B register structure
20	AHB/	APB Br	idges (AHBAPB)
		19.2.19	ADC_AutomaticClockGatedCmd
			ADC_DMACmd
			ADC_ExternalTrigCmd
		19.2.16	ADC_ExternalTrigConfig293
		19.2.15	ADC_ConversionCmd
		19.2.14	ADC_Cmd
		19.2.13	ADC_StandbyModeCmd291
		19.2.12	ADC_ITConfig

# 1 Document and library rules

The user manual document and the Firmware library use the conventions described in the sections below.

## 1.1 Abbreviations

The table below describes the different abbreviations used in this document.

Table 1. List of abbreviations

Acronym	Peripheral / unit
ADC	Analog-to-Digital Converter
CAN	Controller Area Network
SCU	System Control Unit
DMA	DMA Controller
VIC	Vectored Interrupt Controller
GPIO	General Purpose I/O Ports
12C	I <sup>2</sup> C Interface module
RTC	Real Time Clock
WIU	Wake-Up Interrupt Unit
AHBAPB	AHB/APB Bridges
MC	3-phase induction Motor Controller (MC)
FMI	Flash Memory Interface
EMI	External Memory Interface
SSP	Synchronous Serial Peripheral
TIM	Standard Timer
UART	Universal Asynchronous Receiver Transmitter
WDG	Watchdog Timer

13/303

The Firmware library uses the following naming conventions:

- **PPP** is used as reference to any peripheral acronym, e.g. **ADC**. See the section above for more information on peripheral acronyms.
- System and source/header file names are preceded by '91x\_', e.g. **91x\_conf.h**.
- Constants used in one file are defined within this file. A constant used in more than one file is defined in a header file.
- Registers are considered as constants. Their names are in upper case letters and have in most cases the same acronyms as in the STR91xFA reference manual document.
- Peripheral function names are preceded with the corresponding peripheral acronym in upper case followed by an underscore. The first letter in each word is upper case, e.g. SSP\_SendData. Only one underscore is allowed in a function name to separate the peripheral acronym from the rest of the function name.
- Functions for initializing PPP peripheral according to the specified parameters in the *PPP\_InitTypeDef* are named *PPP\_Init*, e.g. *TIM\_Init*.
- Functions for deinitializing PPP peripheral registers to their default reset values are named *PPP\_DeInit*, e.g. *TIM\_DeInit*.
- Functions for filling the PPP\_InitTypeDef structure with the reset value of each member are named PPP\_StructInit, e.g. UART\_StructInit.
- Functions for enabling or disabling the specified PPP peripheral are named PPP\_Cmd,
   e.g. SSP\_Cmd.
- Functions for enabling or disabling an interrupt source of the specified PPP peripheral are named *PPP\_ITConfig*, e.g. *DMA\_ITConfig*.
- Functions for enabling or disabling the DMA interface of the specified PPP peripheral are named **PPP\_DMACmd**, e.g. **SSP\_DMACmd**.
- Functions used to configure a peripheral function end with Config, e.g.
   UART\_DTRConfig.
- Functions for checking whether the specified PPP flag is set or not are named **PPP\_GetFlagStatus**, e.g. **I2C\_GetFlagStatus**.
- Functions for clearing a PPP flag are named PPP\_ClearFlag, e.g. I2C\_ClearFlag.
- Functions for checking whether the specified PPP interrupt has occurred or not are named PPP\_GetITStatus, e.g. DMA\_GetITStatus.
- Functions for clearing a PPP interrupt pending bit are named *PPP\_ClearITPendingBit*, e.g. WDG\_ClearITPendingBit.

### 1.2 Coding rules

The following rules are used in the Firmware library.

 Specific types are defined for variables whose type and size are fixed. These types are defined in the file 91x\_type.h:

```
typedef unsigned long
typedef unsigned short
                                1116:
typedef unsigned char
                               u8;
typedef signed long
                                s32;
typedef signed short
                                s16;
typedef signed char
typedef volatile unsigned long vu32;
typedef volatile unsigned short
typedef volatile unsigned char
typedef volatile signed long
                                vs32:
typedef volatile signed short
                                vs16;
typedef volatile signed char
```

bool type is defined in the file 91x\_type.h as:

```
typedef enum
{
  FALSE = 0,
  TRUE = !FALSE
} bool;
```

FlagStatus & ITStatus types are defined in the file 91x\_type.h. Two values can be assigned to this variable: SET or RESET.

```
typedef enum
{
  RESET = 0,
  SET = !RESET
} FlagStatus, ITStatus;
```

 FunctionalState type is defined in the file 91x\_type.h. Two values can be assigned to this variable: ENABLE or DISABLE.

```
typedef enum
{
   DISABLE = 0,
   ENABLE = !DISABLE
} FunctionalState;
```

ErrorStatus type is defined in the file 91x\_type.h. Two values can be assigned to this variable: SUCCESS or ERROR.

```
typedef enum
{
   ERROR = 0,
   SUCCESS = !ERROR
} ErrorStatus;
```

Pointers to peripherals are used to access the peripheral control registers. Peripheral pointers point to data structures that represent the mapping of the peripheral control registers. A structure is defined for each peripheral in the file 91x\_map.h. The example below illustrates the SSP register structure declaration:

```
/*-----Synchronous Serial Peripheral -------

*/
typedef struct
{
  vu16 CR0; /* Control Register 1 */
```

577

```
vu16 EMPTY1;
                 /* Control Register 2
                                                          * /
 vu16 CR1:
 vu16 EMPTY2;
                                                          */
 vu16 DR;
                 /* Data Register
 vu16 EMPTY3;
 vu16 SR;
                 /* Status Register
                                                          */
 vu16 EMPTY4;
 vu16 PR;
                 /* Clock Prescaler Register
                                                          * /
 vu16 EMPTY5;
 vul6 IMSCR;
                  /* Interrupt Mask Set or Clear Register */
 vul6 EMPTY6;
                                                          * /
 vu16 RISR;
                 /* Raw Interrupt Status Register
 vu16 EMPTY7;
                 /* Masked Interrupt Status Register
                                                          * /
 vu16 MISR:
 vu16 EMPTY8;
                 /* Interrupt Clear Register
                                                          * /
 vu16 ICR;
 vu16 EMPTY9;
                 /* DMA Control Register
                                                          * /
 vu16 DMACR;
 vu16 EMPTY10;
}SSP_TypeDef;
```

Register names are the register acronyms written in upper case for each peripheral. EMPTYi (i is an integer that indexes the reserved field) replaces a reserved field.

Peripherals are declared in **91x\_map.h** file. The following example shows the declaration of the *SSP* peripheral:

```
#ifndef EXT
#Define EXT extern
#endif
#define AHB_APB_BRDG1_U (0x5C000000) /* AHB/APB Bridge 1 UnBuffered Space */
#define AHB_APB_BRDG1_B (0x4C000000) /* AHB/APB Bridge 1 Buffered Space */
#define APB_SSP0_OFST
                         (0x00007000) /* Offset of SSP0 */
#ifndef Buffered
#define AHBAPB1_BASE
                            (AHB_APB_BRDG1_U)
#else /* Buffered */
#define AHBAPB1_BASE
                             (AHB_APB_BRDG1_B)
/* SSPO Base Address definition*/
#define SSP0_BASE
                    (AHBAPB1_BASE + APB_SSP0_OFST)
/* SSP0 peripheral declaration*/
#ifndef DEBUG
. . .
#define SSP0
                  ((SSP_TypeDef *) SSP0_BASE)
. . .
#else
#ifdef _SSP0
EXT SSP_TypeDef
                       *SSP0:
#endif /*_SSP0 */
. . .
```

To enter debug mode you have to define the label *DEBUG* in the file *91x\_conf.h*. Debug mode allows you to see the contents of peripheral registers but it uses more memory space. In both cases *SSP0* is a pointer to the first address of *SSP0* peripheral.

The *DEBUG* variable is defined in the file *91x conf.h* as follows:

```
#define DEBUG 1
```

*DEBUG* mode is initialized as follows in the *91x\_lib.c* file:

```
#ifdef DEBUG
void debug(void)
{
    ...
    #ifdef _SSP0
    SSP0 = (SSP_TypeDef *)SSP0_BASE;
    #endif /*_SSP0 */
    ...
}
#endif /* DEBUG*/
```

To include the *SSP* peripheral library in your application, define the label *\_SSP* and to access the *SSPn* peripheral registers, define the label *\_SSPn*, i.e to access the registers of *SSP1* peripheral, *\_SSP1* label must be defined in *91x\_conf.h* file. *\_SSP* and *\_SSPn* labels are defined in the file *91x\_conf.h* as follows:

```
#define _SSP
#define _SSPn
```

Each peripheral has several dedicated registers which contain different flags. Registers are defined within a dedicated structure for each peripheral. Flag definition is adapted to each peripheral case (In almost cases defined in **91x\_ppp.h** file). Flags are defined as acronyms written in upper case and prefixed by '**PPP\_Flag\_**' prefix.

577

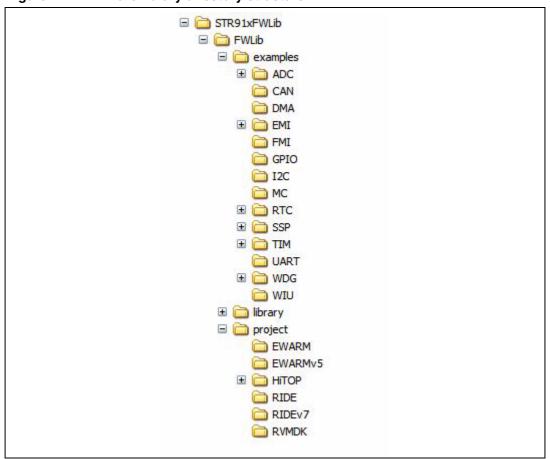
Firmware library UM0233

## 2 Firmware library

## 2.1 Package description

The Firmware library is supplied in one single zip package. The extraction of the zip file will give the one folder "STR91xFWLib\FWLib\FWLib\" containing the following sub-directories:

Figure 1. Firmware library directory structure



## 2.2 Examples

This directory contains for each peripheral sub-directory, the minimum set of files needed to run a typical example on how to use a peripheral:

- Readme.txt: a brief text file describing the example and how to make it work,
- 91x\_conf.h: the header file to configure the used peripherals and miscellaneous defines,
- 91x\_it.c: the source file containing the interrupt handlers (the function bodies may be empty if not used),
- *main.c*: the example program,

Note: All examples are independent from any software tool chain.

577

UM0233 Firmware library

### 2.3 Library

This directory contains all the subdirectories and files that form the core of the library:

- *inc* sub-directory contains the Firmware library header files that do not need to be modified by the user:
  - 91x\_type.h: Contains the common data types and enumeration used in all other files,
  - 91x\_map.h: Contains the peripheral memory mapping and register data structures,
  - 91x lib.h: Main header file including all other headers,
  - 91x\_ppp.h (one header file per peripheral): contains the function prototypes, data structures and enumeration.
- src sub-directory contains the Firmware library source files that do not need to be modified by the user:
  - 91x\_ppp.c (one source file per peripheral): contains the function bodies of each peripheral.

Note: All library files are independent from any software toolchain.

## 2.4 Project

This directory contains a standard template project program that compiles all library files and also all the user modifiable files needed to create a new project:

- **91x\_conf.h**: The configuration header file with all peripherals defined by default.
- 91x\_it.c: The source file containing the interrupt handlers (the function bodies are empty in this template).
- main.c: The main program body.
- **EWARM, EWARMv5, HiTOP, RIDE, RIDEv7, RVMDK:** For each toolchain usage, refer to the Readme.txt file available in the same sub-directory.

19/303

Firmware library UM0233

# 2.5 File description

The following table enumerates and describes the different files used in the Firmware library.

Table 2. Library files

File name	Description
91x_conf.h	Parameter configuration file. It should be modified by the user to specify several parameters to interface with the library before running any application. You can enable or disable peripherals if you use the template.
main.c	The main example program body.
91x_it.c	Peripheral interrupt functions file. You can modify it by including the code of interrupt functions used in your application. In case of multiple interrupt requests mapped on the same interrupt vector, the function polls the interrupt flags of the peripheral to establish the exact source of the interrupt. The names of these functions are already provided in the Firmware library.
91x_lib.h	Header file including all the peripheral header files. It is the only file to be included in the user application to interface with the library.
91x_lib.c	Debug mode initialization file. It includes the definition of variable pointers each one pointing to the first address of a specific peripheral and the definition of one function called when you choose to enter debug mode. This function initializes the defined pointers.
91x_map.h	This file implements memory mapping and physical registers address definition for both development and debug modes. This file is supplied with all peripherals.
91x_type.h	Common declarations file. It includes common types and constants used by all peripheral drivers.
91x_ppp.c	Driver source code file of PPP peripheral written in C language.
91x_ppp.h	Header file of PPP peripheral. It includes the definition of PPP peripheral functions and variables used within these functions.

UM0233 Firmware library

The Firmware library architecture and file inclusion relationship are shown in Figure 2.

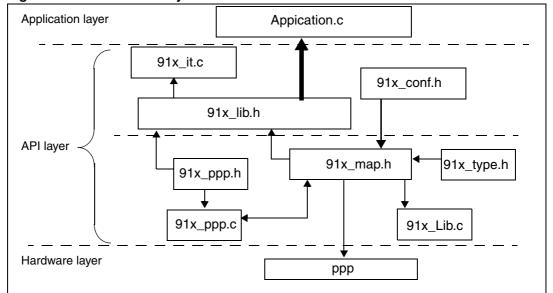


Figure 2. Firmware library file architecture

Each peripheral has a source code file **91x\_ppp.c** and a header file **91x\_ppp.h**. The **91x\_ppp.c** file contains all the firmware functions required to use the corresponding peripheral. A single memory mapping file **91x\_map.h** is supplied for all peripherals. This file contains all the register declarations for both development and debug modes.

The header file *91x\_lib.h* includes all the peripheral header files. This is the only file that needs to be included in the user application to interface with the library.

**577** 

Firmware library UM0233

### 2.6 How to use the library

This section describes step-by-step how to configure and initialize a PPP peripheral.

■ In your main application file, declare a *PPP\_InitTypeDef* structure, e.g: PPP\_InitTypeDef PPP\_InitStructure;

The PPP\_InitStructure is a working variable located in data memory that allows you to initialize one or more PPP instances.

■ Fill the PPP\_Initstructure variable with the allowed values of the structure member.

There are two ways of doing this:

Configuration of the whole structure: in this case you should proceed as follows:

```
PPP_InitStructure.member1 = val1;
PPP_InitStructure.member2 = val2;
PPP_InitStructure.memberN = valN; /* where N is the number of the structure members */
```

Note:

The previous initialization could be merged in only one line like the following:

```
PPP_InitTypeDef PPP_InitStructure = { val1, val2, ..., valN}
```

This reduces and optimizes code size.

Configuration of a few members of a structure: in this case you should modify the
 PPP\_InitStructure
 variable that has been already filled by a call to the
 PPP\_StructInit(..)
 function. This ensures that the other members of the
 PPP\_InitStructure
 variable have appropriate values (in most case their default
 values).

- You have to initialize the PPP peripheral by calling the **PPP\_Init(..)** function. PPP\_Init(PPP, &PPP\_InitStructure);
- At this stage the PPP peripheral is initialized and can be enabled (if applicable) by making a call to *PPP\_Cmd(..)* function.

```
PPP_Cmd(PPP, ENABLE);
```

To use the PPP peripheral, you can use a set of dedicated functions. These functions are specific to the peripheral and for more details refer to *Section 3 on page 23*.

Note: 1 Before configuring a peripheral, you have to enable its clock by calling the following function:

```
SCU_APBPeriphClockConfig(__PPP, ENABLE); /* For APB Peripheral */
OR:
    SCU_AHBPeriphClockConfig( PPP, ENABLE); /* For AHB Peripheral */
```

- 2 PPP\_DeInit(..) function can be used to set all PPP peripheral registers to their reset values:
  PPP\_DeInit(PPP);
- If after peripheral configuration, you want to modify one or more peripheral settings you should proceed as follows:

# 3 Peripheral firmware overview

The following chapters describe each peripheral Firmware library in detail. The related functions are fully documented. An example of use of the function is given and some important considerations are also provided.

Functions are described in the format below:

Function name	The name of the peripheral function
Function prototype	Prototype declaration
Behavior description	Brief explanation of how the functions are executed
Input parameter {x}	Description of the input parameters
Output parameter {x}	Description of the output parameters
Return Value	Value returned by the function
Required preconditions	Requirements before calling the function
Called functions	Other library functions called by the function

577

## 4 Flash memory interface (FMI)

The Flash Memory Interface of the STR91xFA contains two banks( with a total capacity of 256+32 ,512+32,1024+128 or 2048+128Kbytes) can be 32-bit burst read accessed and 16-bit write accessed.

## 4.1 FMI register structure

## 4.1.1 FMI register structure

The FMI register structure FMI\_TypeDef is defined in the 91x\_map.h file as follows:

```
typedef struct
{
  vu32 BBSR;
  vu32 NBBSR;
  vu32 EMPTY1;
  vu32 BBADR;
  vu32 NBBADR;
  vu32 CMPTY2;
  vu32 CR;
  vu32 SR;
  vu32 BCE5ADDR;
} FMI_TypeDef;
```

The following table presents the FMI registers:

Table 3. FMI registers

Register	Description
BBSR	Boot Bank Size Register
NBBSR	Non-Boot Bank Size Register
BBADR	Boot Bank Base Address Register
NBBADR	Non-Boot Bank Base Address Register
CR	Control Register
SR	Status Register
BCE5ADDR	BC Fifth Entry Target Address Register

The FMI interface are declared in the same file:

```
#ifndef EXT
  #define EXT extern
#endif /* EXT */
                  (0x54000000) /* FMI Unbuffered Space */
#define AHB_FMI_U
#define AHB_FMI_B
                          (0x44000000) /* FMI buffered Space */
#ifndef Buffered
#define FMI_BASE
                          (AHB_FMI_U)
#else /* Buffered */
#define FMI_BASE
                          (AHB_FMI_B)
#endif /* Buffered */
#ifndef DEBUG
#define FMI
                  ((FMI_TypeDef *)FMI_BASE)
. . .
#else
#ifdef _FMI
EXT FMI_TypeDef
                         *FMI;
#endif /* _FMI */
#endif
```

When debug mode is used, FMI pointer is initialized in *91x\_lib.c* file:

```
#ifdef _FMI
FMI = (FMI_TypeDef *)FMI_BASE
#endif /* _FMI */
```

\_FMI must be defined, in 91x\_conf.h file, to access the peripheral registers as follows:

```
...
#define _FMI
```

25/303

# 4.2 Firmware library functions

The following table enumerates the different functions of the FMI library.

Table 4. FMI library functions

Function name	Description
FMI_BankRemapConfig	Configures the sizes and addresses of bank 0 and bank 1.
FMI_Config	Configures the FMI.
FMI_EraseSector	Erases a sector.
FMI_EraseBank	Erases a bank.
FMI_WriteHalfWord	Writes a halfword to a Flash memory address.
FMI_WriteOTPHalfWord	Writes a halfword to an OTP sector address.
FMI_ReadWord	Reads the corresponding data.
FMI_ReadOTPData	Reads data from the OTP sector.
FMI_GetFlagStatus	Checks whether the specified FMI flag is set or not.
FMI_GetReadWaitStateValue	Gets the current Read wait state value.
FMI_GetWriteWaitStateValue	Gets the current write wait state value.
FMI_SuspendEnable	Enables the Suspend command.
FMI_ResumeEnable	Resumes the suspended command.
FMI_ClearFlag	Clears the FMI flags on the corresponding bank.
FMI_WriteProtectionCmd	Enables or disables the write protection for the specified sector.
FMI_WaitForLastOperation	Waits until the last Operation (Write halfword, Erase sector and Erase bank) completion.
FMI_ReadRSIGData	Reads the Electronic Signature stored in the user configuration sector of Bank 1.

## 4.2.1 FMI\_BankRemapConfig

Function name	FMI_BankRemapConfig	
Function prototype	void FMI_BankRemapConfig(u8 FMI_BootBankSize, u8 FMI_NonBootBankSize, u32 FMI_BootBankAddress, u32 FMI_NonBootBankAddress)	
Behavior description	Configures the addresses and sizes of bank 0 and bank 1.	
Input parameter1	FMI_BootBankSize: specifies the boot bank size. Refer to <i>Table 5: FMI_BootBankSize parameter values</i> for the allowed values of this parameter.	
Input parameter2	FMI_NonBootBankSize: specifies the non boot bank size.  Refer to Table 6: FMI_NonBootBankSize parameter values for the allowed values of this parameter.	
Input parameter3	FMI_BootBankAddress: specifies the boot bank address.	
Input parameter4	FMI_BootBankAddress: specifies the non boot bank address.	
Output parameter	None	
Return parameter	None	
Required preconditions		
Called functions	None	

Table 5. FMI\_BootBankSize parameter values

Value	Meaning
0	32 KBytes
1	64 KBytes
2	128 KBytes
3	256 KBytes
4	512 KBytes
0xB	64 MBytes

Table 6. FMI\_NonBootBankSize parameter values

Value	Meaning
0	8 KBytes
1	16 KBytes
2	32 KBytes
3	64 KBytes
0xD	64 MBytes

27/303

#### **Example:**

- Note: 1 When bank 1 is hardware remapped to address 0 (bank 1 is the boot bank), in the 91x\_conf.h file, the //#define Boot\_Bank\_1 line should be uncommented.
  - In the same file, you have also to uncomment either //#define Flash\_512KB\_256KB or //#define Flash\_2MB\_1MB lines to select your Flash size.

## 4.2.2 FMI\_Config

Function name	FMI_Config
Function prototype	<pre>void FMI_Config(u16 FMI_ReadWaitState, u32 FMI_WriteWaitState, u16 FMI_PWD, u16 FMI_LVDEN, u16 FMI_FreqRange)</pre>
Behavior description	Configures the FMI.
Input parameter 1	FMI_ReadWaitState: specifies the read wait state value.  Refer to <i>Table 7: FMI_ReadWaitState parameter values</i> " for the allowed values of this parameter.
Input parameter 2	FMI_WriteWaitState: specifies the read wait state value.  Refer to <i>Table 8: FMI_WriteWaitState parameter values</i> " for the allowed values of this parameter.
Input parameter 3	FMI_PWD: specifies the power down mode status.  Refer to <i>Table 9: FMI_PWD parameter values</i> " for the allowed values of this parameter.
Input parameter 4	FMI_LVDEN: specifies the low voltage detector mode status.  Refer to <i>Table 10: FMI_LVDEN parameter values</i> " for the allowed values of this parameter.
Input parameter 5	FMI_FreqRange: specifies the working frequency range.  Refer to <i>Table 11: FMI_FreqRange parameter values</i> " for the allowed values of this parameter.
Output parameter	None
Return parameter	None
Required preconditions	
Called functions	None

### Table 7. FMI\_ReadWaitState parameter values

FMI_ReadWaitState	Meaning
FMI_READ_WAIT_STATE_1	1 read wait state
FMI_READ_WAIT_STATE_2	2 read wait states
FMI_READ_WAIT_STATE_3	3 read wait states

#### Table 8. FMI\_WriteWaitState parameter values

FMI_WriteWaitState	Meaning
FMI_WRITE_WAIT_STATE_0	0 write wait state
FMI_WRITE_WAIT_STATE_1	1 write wait states

#### Table 9. FMI\_PWD parameter values

FMI_PWD	Meaning
FMI_PWD_ENABLE	Enable the PWD
FMI_PWD_DISABLE	Disable the PWD

29/303

Table 10. FMI\_LVDEN parameter values

FMI_LVDEN	Meaning
FMI_LVD_ENABLE	Enable the LVD
FMI_LVD_DISABLE	Disable the LVD

#### Table 11. FMI\_FreqRange parameter values

FMI_FreqRange	Meaning
FMI_FREQ_LOW	Low working frequency (up to 66 MHz)
FMI_FREQ_HIGH	High working frequency (above 66 MHz)

#### Example:

/\*To configure the FMI as follows: 2 read wait states, 1 write wait state, PWD enabled, LVD enabled and a low working frequency\*/
FMI\_Config(FMI\_READ\_WAIT\_STATE\_2, FMI\_WRITE\_WAIT\_STATE\_1, FMI\_PWD\_ENABLE, FMI\_LVD\_ENABLE, FMI\_FREQ\_LOW);

#### 4.2.3 FMI\_EraseSector

Function name	FMI_EraseSector
Function prototype	void FMI_EraseSector(vu32 FMI_Sector)
Behavior description	Erases a sector.
Input parameter	FMI_Sector: specifies the sector to be erased. Refer to <i>Table 12</i> and <i>Table 13</i> for the allowed values of this parameter.
Output parameter	None
Return parameter	None
Required preconditions	
Called functions	None

#### Table 12. FMI\_Sector values for devices with 1 MByte or 2 MByte internal Flash

Value	Meaning
FMI_B0S0FMI_B0S31	FMI bank 0 sector 0FMI bank 0 sector 31.
FMI_B1S0FMI_B1S7	FMI bank 1sector 0FMI bank 1 sector 7.

#### Table 13. FMI\_Sector values for devices with 256 KByte or 512 KByte internal Flash

Value	Meaning
FMI_B0S0FMI_B0S7	FMI bank 0 sector 0FMI bank 0 sector 7.
FMI_B1S0FMI_B1S3	FMI bank 1sector 0FMI bank 1 sector 3.

#### Example:

```
/*To erase sector 3 in bank 0*/
u8 FMI_Timeout_Status;
FMI_EraseSector(FMI_B0S3);
FMI_Timeout_Status = FMI_WaitForLastOperation(FMI_BANK_0);
```

577

#### 4.2.4 FMI\_EraseBank

Function name	FMI_EraseBank
Function prototype	void FMI_EraseBank(vu32 FMI_Bank)
Behavior description	Erases a bank.
Input parameter	FMI_Bank: specifies the bank to be erased. Refer to <i>Table 14</i> for the allowed values of this parameter.
Output parameter	None
Return parameter	None
Required preconditions	
Called functions	None

#### Table 14. FMI\_Bank parameter values

Value	Meaning
FMI_BANK_0	FMI bank 0
FMI_BANK_1	FMI bank 1

#### Example:

```
/*To erase bank 0*/
u8 FMI_Timeout_Status;
FMI_EraseBank(FMI_BANK_0);
FMI_Timeout_Status = FMI_WaitForLastOperation(FMI_BANK_0);
```

#### 4.2.5 FMI\_WriteHalfWord

Function name	FMI_WriteHalfWord
Function prototype	void FMI_WriteHalfWord(u32 FMI_Address, u16 FMI_Data)
Behavior description	Writes a halfword to a Flash memory address.
Input parameter1	FMI_Address: specifies the address offset where the data are to be written.
Input parameter2	FMI_Data: the data to be written.
Output parameter	None
Return parameter	None
Required preconditions	
Called functions	None

#### Example:

```
/*To write the data 0x1234 to the address 0x4000*/
u8 FMI_Timeout_Status;
FMI_WriteHalfWord(0x4000,0x1234);
FMI_Timeout_Status = FMI_WaitForLastOperation(FMI_BANK_0);
```

## 4.2.6 FMI\_WriteOTPHalfWord

Function name	FMI_WriteOTPHalfWord
Function prototype	void FMI_WriteOTPHalfWord(u8 FMI_OTPHWAddress, u16 FMI_OTPData)
Behavior description	Writes a halfword to the specified OTP sector address.
Input parameter1	FMI_OTPHWAddress: specifies the address offset where the data is to be written.  Refer to <i>Table 15: FMI_OTPHWAddress parameter values</i> " for the allowed values of this parameter.
Input parameter2	FMI_OTPData: the data to be written.
Output parameter	None
Return parameter	None
Required preconditions	
Called functions	None

Table 15. FMI\_OTPHWAddress parameter values

Value	Meaning
FMI_OTP_LOW_HALFWORD_0	FMI OTP low halfword 0
FMI_OTP_HIGH_HALFWORD_0	FMI OTP high halfword 0
FMI_OTP_LOW_HALFWORD_1	FMI OTP low halfword 1
FMI_OTP_HIGH_HALFWORD_1	FMI OTP high halfword 1
FMI_OTP_LOW_HALFWORD_2	FMI OTP low halfword 2
FMI_OTP_HIGH_HALFWORD_2	FMI OTP high halfword 2
FMI_OTP_LOW_HALFWORD_3	FMI OTP low halfword 3
FMI_OTP_HIGH_HALFWORD_3	FMI OTP high halfword 3
FMI_OTP_LOW_HALFWORD_4	FMI OTP low halfword 4
FMI_OTP_HIGH_HALFWORD_4	FMI OTP high halfword 4
FMI_OTP_LOW_HALFWORD_5	FMI OTP low halfword 5
FMI_OTP_HIGH_HALFWORD_5	FMI OTP high halfword 5
FMI_OTP_LOW_HALFWORD_6	FMI OTP low halfword 6
FMI_OTP_HIGH_HALFWORD_6	FMI OTP high halfword 6
FMI_OTP_LOW_HALFWORD_7	FMI OTP low halfword 7
FMI_OTP_HIGH_HALFWORD_7	FMI OTP high halfword 7

#### Example:

```
/*To write the data 0x1234 to the LSB of the word 2*/
u8 FMI_Timeout_Status;
FMI_WriteOTPHalfWord(FMI_OTP_LOW_HALFWORD_2,0x1234);
FMI_Timeout_Status = FMI_WaitForLastOperation(FMI_BANK_1);
```

**\_\_\_\_\_\_** 

#### 4.2.7 FMI\_ReadWord

Function name	FMI_ReadWord
Function prototype	u32 FMI_ReadWord(u32 FMI_Address)
Behavior description	Reads the corresponding data.
Input parameter	FMI_Address: specifies the address of the word to be read.
Output parameter	None
Return parameter	The data contained in the specified address.
Required preconditions	
Called functions	None

#### Example:

/\*To read the data contained in the address 0x6000\*/u32 DATA; DATA = FMI\_ReadWord(0x6000);

### 4.2.8 FMI\_ReadOTPData

Function name	FMI_ReadOTPData
Function prototype	u32 FMI_ReadOTPData(u8 FMI_OTPAddress)
Behavior description	Reads data from the OTP sector.
Input parameter	FMI_OTPAddress: specifies the address of the data to be read.  Refer to <i>Table 16: FMI_OTPAddress parameter values</i> " for the allowed values of this parameter.
Output parameter	None
Return parameter	The data to be read from the OTP sector.
Required preconditions	
Called functions	None

Table 16. FMI\_OTPAddress parameter values

Value	Meaning
FMI_OTP_WORD_0	FMI OTP word 0
FMI_OTP_WORD_1	FMI OTP word 1
FMI_OTP_WORD_2	FMI OTP word 2
FMI_OTP_WORD_3	FMI OTP word 3
FMI_OTP_WORD_4	FMI OTP word 4
FMI_OTP_WORD_5	FMI OTP word 5
FMI_OTP_WORD_6	FMI OTP word 6
FMI_OTP_WORD_7	FMI OTP word 7

#### Example:

/\*To read the 2nd word from the OTP sector\*/
vu16 OTP\_Data;
OTP\_Data= FMI\_ReadOTPData(FMI\_OTP\_WORD\_2);

#### 4.2.9 FMI\_GetFlagStatus

Function name	FMI_GetFlagStatus
Function prototype	FlagStatus FMI_GetFlagStatus(u8 FMI_Flag, vu32 FMI_Bank)
Behavior description	Checks whether the specified FMI flag is set or not.
Input parameter1	FMI_Flag: specifies the flag to check.  Refer to <i>Table 17: FMI_Flag parameter values</i> for the allowed values of this parameter.
Input parameter2	FMI_Bank: specifies the corresponding bank.  Refer to <i>Table 14: FMI_Bank parameter values on page 32</i> for the allowed values of this parameter.
Output parameter	None
Return parameter	The new state of FMI_Flag (SET or RESET).
Required preconditions	
Called functions	None

### Table 17. FMI\_Flag parameter values

Value	Meaning
FMI_FLAG_SPS	Sector protection status
FMI_FLAG_PSS	Program suspend status
FMI_FLAG_PS	Program status
FMI_FLAG_ES	Erase status
FMI_FLAG_ESS	Erase suspend status
FMI_FLAG_PECS	FPEC status

#### Example:

```
/*To get the FMI program status for bank 1*/
FlagStatus FMI_Flag;
FMI_Flag = GetFlagStatus(FMI_FLAG_PS, FMI_BANK_1);
```

35/303

#### 4.2.10 FMI\_GetReadWaitStateValue

Function name	FMI_GetReadWaitStateValue
Function prototype	u16 FMI_GetReadWaitStateValue(void)
Behavior description	Gets the current read wait state value.
Input parameter	None
Output parameter	None
Return parameter	The current read wait state value.
Required preconditions	
Called functions	None

#### Example:

/\*To get the current read wait state value\*/
u16 FMI\_ReadWaitState;
FMI\_ReadWaitState = FMI\_GetReadWaitStateValue();

#### 4.2.11 FMI\_GetWriteWaitStateValue

Function name	FMI_GetWriteWaitStateValue
Function prototype	u16 FMI_GetWriteWaitStateValue(void)
Behavior description	Gets the current write wait state value.
Input parameter	None
Output parameter	None
Return parameter	The current write wait state value.
Required preconditions	
Called functions	None

#### Example:

/\*To get the current write wait state value\*/
u16 FMI\_WriteWaitState;
FMI\_WriteWaitState = FMI\_GetWriteWaitStateValue();

## 4.2.12 FMI\_SuspendEnable

Function name	FMI_SuspendEnable
Function prototype	void FMI_SuspendEnable(vu32 FMI_Bank)
Behavior description	Enables the Suspend command.
Input parameter	FMI_Bank: specifies the bank to be suspended.  Refer to <i>Table 14: FMI_Bank parameter values on page 32</i> for the allowed values of this parameter.
Output parameter	None
Return parameter	None
Required preconditions	
Called functions	None

### Example:

/\*To suspend the current command in the bank  $1^{\star}/$  FMI\_SuspendEnanble(FMI\_BANK\_1);

## 4.2.13 FMI\_ResumeEnable

Function name	FMI_ResumeEnable
Function prototype	void FMI_ResumeEnable(vu32 FMI_Bank)
Behavior description	Resumes the suspended command.
Input parameter	FMI_Bank: specifies the suspended bank.  Refer to <i>Table 14: FMI_Bank parameter values on page 32</i> for the allowed values of this parameter.
Output parameter	None
Return parameter	None
Required preconditions	
Called functions	None

### Example:

/\*To resume the suspended command in the bank 1\*/  $\mbox{FMI}_{ResumeEnanble(FMI}_{BANK_1);}$ 

## 4.2.14 FMI\_ClearFlag

Function name	FMI_ClearFlag
Function prototype	void FMI_ClearFlag(vu32 FMI_Bank)
Behavior description	Clears the FMI flags in the corresponding bank.
Input parameter	FMI_Bank: specifies the corresponding bank.  Refer to <i>Table 14: FMI_Bank parameter values on page 32</i> for the allowed values of this parameter.
Output parameter	None
Return parameter	None
Required preconditions	
Called functions	None

### Example:

/\*To clear the status register on bank 0\*/ FMI\_ClearFlag(FMI\_BANK\_0);

## 4.2.15 FMI\_WriteProtectionCmd

Function name	FMI_WriteProtectionCmd
Function prototype	<pre>void FMI_WrieProtectionCmd(vu32 FMI_Sector, FunctionalState FMI_NewState)</pre>
Behavior description	Enables or disables the write protection for a specified sector.
Input parameter1	FMI_Sector: specifies the sector to be protected or unprotected.  Refer to <i>Table 12</i> and <i>Table 13 on page 31</i> for the allowed values of this parameter.
Input parameter2	NewState: specifies the protection status. This parameter can be: ENABLE or DISABLE.
Output parameter	None
Return parameter	None
Required preconditions	
Called functions	None

### Example:

/\*To disable the write protection of the sector  $3*/FMI\_WriteProtectionCmd(FMI\_BOS3, DISABLE);$ 

# 4.2.16 FMI\_WaitForLastOperation

Function name	FMI_WaitForLastOperation
Function prototype	u8 FMI_WaitForLastOperation(vu32 FMI_Bank)
Behavior description	Waits for the last operation (Write halfword, Write OTP halfword, Erase sector and Erase bank) to be completed.
Input parameter	FMI_Bank: specifies the corresponding bank.  Refer to <i>Table 14: FMI_Bank parameter values on page 32</i> for the allowed values of this parameter.
Output parameter	None
Return parameter	The timeout status. This parameter can be one of the following values:  - FMI_TIME_OUT_ERROR: Timeout error occurred.  - FMI_NO_TIME_OUT_ERROR: No timeout error.
Required preconditions	
Called functions	None

### Example:

```
/*To wait until the write operation completion*/
u8 FMI_Timeout_Status;
FMI_WriteProtectionCmd(FMI_B1S0, DISABLE);
FMI_WriteHalfWord(0x80000,0x1234);
FMI_Timeout_Status = FMI_WaitForLastOperation(FMI_BANK_1);
```

## 4.2.17 FMI\_ReadRSIGData

Function name	FMI_ReadRSIGData
Function prototype	u32 FMI_ReadRSIGData(u8 FMI_LSB_RSIGAddress)
Behavior description	Read the Electronic Signature stored in the user configuration sector of Bank 1.
Input parameter1	FMI_LSB_RSIGAddress: Specifies the low byte of the address to select the register. Refer to <i>Table 18: FMI_LSB_RSIGAddress</i> parameter values for the allowed values of this parameter.
Output parameter	None
Return parameter	The requested RSIG data.
Required preconditions	
Called functions	None

### Table 18. FMI\_LSB\_RSIGAddress parameter values

Value	Meaning
FMI_ReadRSIGData_0	Manufacturer Code
FMI_ReadRSIGData_1	Device Code
FMI_ReadRSIGData_2	Die Revision Code
FMI_ReadRSIGData_3	Protection Level 2 Register for 512KB Flash or Protection Level 1 Register (sectors of bank0) for 2MB flash.
FMI_ReadRSIGData_4	Protection Level 1 Register for 512KB Flash or Protection Level 1 Register (sectors of bank1) for 2MB flash.
FMI_ReadRSIGData_5	Protection Status Register(sectors of bank0) for 2MB flash or Flash Configuration Register for 512KB flash.
FMI_ReadRSIGData_6	Protection Status Register (sectors of bank1) (available only for 2MB flash)
FMI_ReadRSIGData_7	Flash Configuration Register(available only for 2MB flash).

### Example:

/\*To read the Flash configuration register for 512Kb Flash\*/
u16 FMI\_ConfigRegister;
FMI\_ConfigRegister = FMI\_ReadRSIGData(FMI\_ReadRSIGData\_5);

# 5 External memory interface (EMI)

The EMI provides an interface between the AHB system bus and external memory devices supporting up to four memory banks that you can configure independently. Each memory bank supports: SRAM (asynchronous memory), PSRAM (synchronous memory), ROM and Flash.

You can configure each memory bank to use 8-bit non multiplexed or 16-bit multiplexed data paths.

You can configure the EMI memory banks to support:

- Asynchronous Non-burst read and write accesses.
- Asynchronous page mode read accesses (supported in 8-bit non-multiplexed EMI configuration).
- Synchronous burst mode access (supported only in 16-bit mutliplexed mode on LFBGA package)

The first section describes the data structure used in the EMI Firmware library. The second one presents the Firmware library functions.

Note: Some EMI-related functions are defined in the SCU module (see Section 6.2 on page 53).

## 5.1 EMI register structure

### 5.1.1 EMI register structure

The EMI register structure EMI\_Bank\_TypeDef is defined in the 91x\_map.h file as follows:

```
typedef struct
{
    vu32 ICR;
    vu32 RCR;
    vu32 WCR;
    vu32 OECR;
    vu32 WECR;
    vu32 ECR;
    vu32 BCR;
    vu32 EMPTY1;
    vu32 BRDCR;
}
```

This structure defines the registers of one bank.

There are 4 banks in the EMI interface, so there are 28 registers without taking into account EMI\_CCR and SCU registers used to configure the EMI clock and GPIO mode for EMI bus.

Table 19. EMI registers

Register	Description
EMI_ICRx	Bankx Idle Cycle Control Register
EMI_RCRx	Bankx Read Wait State Control Register
EMI_WCRx	Bankx Write Wait State Control Register
EMI_OECRx	Bankx Output Enable Assertion Delay Control Register
EMI_WECRx	Bankx Write Enable Assertion Delay Control Register

Table 19. EMI registers (continued)

Register	Description
EMI_BCRx	Bankx Control Register
EMI_BRDCRx	Bankx burst Read wait Delay Control Register
EMI_CCR	Clock Control Register.

#### The EMI interface is declared in the same file:

```
#ifndef EXT
  #define EXT extern
#endif /* EXT */
                           (0x74000000) /* EMI UnBuffered Space */
#define AHB_EMI_U
                           (0x64000000) /* EMI Buffered Space
#define AHB_EMI_B
                                          /* Offset of EMI bank3 */
                            (0x00000040)
#define AHB_EMIB3_OFST
                                          /* Offset of EMI bank2 */
/* Offset of EMI bank1 */
#define AHB_EMIB2_OFST
                            (0x00000020)
#define AHB_EMIB1_OFST
                            (0x00000000)
#define AHB_EMIB0_OFST
                            (0x000000E0) /* Offset of EMI bank0 */
#ifndef Buffered
#define EMI_BASE
                            (AHB_EMI_U)
. . .
#else /* Buffered */
#define EMI_BASE
                            (AHB_EMI_B)
#endif /* Buffered */
/* Bank Base Address definition*/
#define EMI_Bank0_BASE (EMI_BASE + AHB_EMIB0_OFST)
#define EMI_Bank1_BASE (EMI_BASE + AHB_EMIB1_OFST)
#define EMI_Bank2_BASE (EMI_BASE + AHB_EMIB2_OFST)
#define EMI_Bank3_BASE (EMI_BASE + AHB_EMIB3_OFST)
#ifndef DEBUG
/* EMI peripheral declaration*/
#define EMI_Bank0
                          ((EMI_Bank_TypeDef *)EMI_Bank0_BASE)
#define EMI_Bank1
                          ((EMI_Bank_TypeDef *)EMI_Bank1_BASE)
#define EMI_Bank2
                          ((EMI_Bank_TypeDef *)EMI_Bank2_BASE)
                          ((EMI_Bank_TypeDef *)EMI_Bank3_BASE)
#define EMI_Bank3
      /* DEBUG */
#else
#ifdef _EMI_Bank0
EXT EMI_Bank_TypeDef
                           *EMI_Bank0;
#endif /* _EMI_Bank0 */
#ifdef _EMI_Bank1
EXT EMI_Bank_TypeDef
                           *EMI_Bank1;
#endif /* _EMI_Bank1 */
```

When debug mode is used, the EMI pointers are initialized in 91x\_lib.c file:

\_EMI, \_EMI\_Bankl0, \_EMI\_Bank1, \_EMI\_Bank2 and EMI\_Bank3 must be defined, in **91x\_conf.h** file, to access the peripheral registers as follows:

```
#define _EMI
#define _EMI_Bank0
#define _EMI_Bank1
#define _EMI_Bank2
#define __EMI_Bank3
```

# 5.2 Firmware library functions

Table 20. EMI library functions

Function name	Description
EMI_DeInit	Initializes the EMI peripheral registers to their default reset values.
EMI_Init	Initializes the EMI Bankx according to the specified parameters in the EMI_InitStruct.
EMI_StructInit	Fills each EMI_InitStruct member with its reset value.
EMI_BCLKCmd	Enable or Disable the activation of BCLK clock.

## 5.2.1 EMI\_Delnit

Function name	EMI_DeInit
Function prototype	void EMI_DeInit()
Behavior description	Initializes the EMI peripheral registers to their default reset values.
Input parameter	None
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	SCU_AHBPeriphReset()

### Example:

. .

 ${\tt EMI\_DeInit();}$  /\* set all EMI Peripheral registers to their reset value \*/

. . .

## 5.2.2 EMI\_Init

Function name	EMI_Init
Function prototype	<pre>void EMI_Init(EMI_Bank_TypeDef* EMI_Bankx, EMI_InitTypeDef* EMI_InitStruct)</pre>
Behavior description	Initializes the EMI_Bankx according to the specified parameters in the EMI_InitStruct.
Input parameter1	EMI_Bankx: where x can be 0,1,2 or 3 to select the EMI Bank.
Input parameter2	EMI_InitStruct: pointer to a EMI_InitTypeDef structure that contains the configuration information for the specified EMI_Bankx.  Refer to section "EMI_InitTypeDef on page 45" for more details on the allowed values of this parameter.
Output parameter	None
Return parameter	None
Required preconditions	
Called functions	None

### EMI\_InitTypeDef

The EMI\_InitTypeDef structure is defined in the *91x\_map.h* file:

```
typedef struct
u32 EMI_Bank_IDCY;
u32 EMI_Bank_WSTRD;
u32 EMI_Bank_WSTWR;
u32 EMI_Bank_WSTROEN;
u32 EMI_Bank_WSTWEN;
u32 EMI_Bank_BRDCR;
u32 EMI_Bank_MemWidth;
u32 EMI Bank WriteProtection;
u32 EMI_Burst_and_PageModeRead_TransferLength;
u32 EMI_Burst_and_PageModeRead_Selection;
u32 EMI_BurstModeWrite_TransferLength;
u32 EMI_BurstModeWrite_Selection;
u32 EMI_AccessRead_Support;
u32 EMI_AccessWrite_Support;
u32 EMI_ByteLane_Selection;
} EMI_InitTypeDef;
Example:
   EMI_InitTypeDef EMI_InitStruct;
   EMI_InitStruct.EMI_Bank_IDCY=0x0F ;
   EMI_InitStruct.EMI_Bank_WSTRD=0x1F ;
   EMI_InitStruct.EMI_Bank_WSTWR=0x1F ;
   EMI InitStruct.EMI Bank WSTROEN= 0x00;
   EMI_InitStruct.EMI_Bank_WSTWEN= 0x01;
   EMI_InitStruct.EMI_Bank_MemWidth= EMI_Width_Byte;
   EMI_InitStruct.EMI_Bank_WriteProtection= EMI_Bank_NonWriteProtect;
   EMI_InitStruct.EMI_Burst_and_PageModeRead_Selection=EMI_Burst_and_PageModeRead;
   EMI_InitStruct.EMI_Burst_and_PageModeRead_TransferLength=EMI_Read_4Data;
   EMI_Init (EMI_Bank0,&EMI_InitStruct);
```

#### EMI Bank IDCY

This member controls the number of bus turnaround cycles added between read and write accesses. It is coded with 4 bits, the minimum value is 0x3.

#### EMI Bank WSTRD

For SRAM and ROM, this member controls the number of wait states for read accesses, and the external wait assertion timing for reads. For burst ROM, it controls the number of wait states for the first read access only. It is coded with 5 bits (32 values: 0x01, 0x02, 0x03, .... 0x1F)

#### EMI Bank WSTWR

For SRAM, this member controls the number of wait states for write accesses, and the external wait assertion timing for writes.

It does not apply to read-only devices such as ROM.

It is coded with 5 bits (32 values: 0x01, 0x02, 0x03, .... 0x1F)

#### EMI\_Bank\_WSTROEN

Output enable assertion delay from chip select assertion.

It is coded with 4 bits (16 values: 0x01, 0x02, 0x03, ....0xF)

#### EMI\_Bank\_WSTWEN

Write Enable Assertion Delay From Chip Select Assertion.

It is coded with 4 bits (16 values: 0x01, 0x02, 0x03, ....0xF)

#### EMI\_Bank\_BRDCR

This member controls the number of wait states for burst read accesses after the first read.

It is coded with 5 bits (32 values: 0x01, 0x02, 0x03, .... 0x1F).

### EMI\_Burst\_and\_PageModeRead\_TransferLength

This member controls the page and burst read transfer length.

It can be one of the following values:

EMI_PageModeRead_TransferLength	Value	Meaning
EMI_Read_4Data	0x00000000	4 -transfer burst
EMI_Read_8Data	0x00000400	8-transfer burst
EMI_Read_16Data (only for burst mode)	0x00000800	16-transfers burst
EMI_Read_Continuous (only for burst mode)	0x00000C00	Continuous (synchronous only)

#### EMI\_Burst\_and\_PageModeRead\_Selection

Select or deselect burst and page mode read.

This member can be one of the following values:

EMI_PageModeRead_Selection	Value	Meaning
EMI_NormalMode	0x00000000	Normal Mode
EMI_Burst_and_PageModeRead	0x00000100	Page and burst Mode Read

#### EMI\_Bank\_MemWidth

This member controls the memory width.

This member can be one of the following values:

EMI_Bank_MemWidth	Value	Meaning
EMI_Width_Byte	0x00000000	8-bit width
EMI_Width_HalfWord	0x00000010	16-bit width

#### EMI\_Bank\_WriteProtect

This member controls the write protection feature.

This member can be one of the following values:

EMI_Bank_WriteProtect	Value	Meaning
EMI_Bank_NonWriteProtect	0x00000000	No write protection,
EMI_Bank_WriteProtection	0x00000008	Bank is write protected.

### EMI\_BurstModeWrite\_TransferLength

This member controls the burst write transfer length.

EMI_BurstModeWrite_TransferLength	Value	Meaning
EMI_Write_4Data	0x00000000	4 -transfer burst
EMI_Write_8Data	0x00040000	8-transfer burst
EMI_Write_Continuous	0x000C0000	Continuous (synchronous only)

#### EMI\_BurstModeWrite\_Selection

Select or deselect burst mode write.

This member can be one of the following values:

EMI_PageModeRead_Selection	Value	Meaning
EMI_NonBurstModeWrite	0x00000000	Non Burst Mode Write
EMI_BurstModeWrite	0x00010000	Burst Mode Write

### EMI\_AccessRead\_Support

This member controls the access read support.

This member can be one of the following values:

EMI_AccessRead_Support	Value	Meaning
EMI_Read_Asyn	0x00000000	Asynchronous access for read
EMI_Read_Syn	0x00000200	Synchronous access for read

### EMI\_AccessWrite\_Support

This member controls the access read support.

This member can be one of the following values:

EMI_AccessWrite_Support	Value	Meaning
EMI_Write_Asyn	0x00000000	Asynchronous access for write
EMI_Write_Syn	0x00020000	Synchronous access for write

577

### EMI\_ByteLane\_Selection

This member Enables or disables the byte select signals in 16-bit PSRAM bus mode.

This member can be one of the following values:

EMI_ByteLane_Selection	Value	Meaning
EMI_Byte_Select_disabled	0x00000000	Byte select disabled
EMI_Byte_Select_enabled	0x0000001	Byte select enabled

## 5.2.3 EMI\_StructInit

Function name	EMI_StructInit
Function prototype	void EMI_StructInit(EMI_InitTypeDef* EMI_InitStruct)
Behavior description	Fills each EMI_InitStruct member with its reset value.
Input parameter	EMI_InitStruct: pointer to a EMI_InitTypeDef structure which will be initialized.
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

### Example:

```
...
EMI_InitTypeDef EMI_InitStruct;
EMI_StructInit(&EMI_InitStruct);
```

# 5.2.4 EMI\_BCLKCmd

Function name	EMI_BCLKCmd
Function prototype	void EMI_BCLKCmd(FunctionalState NewState)
Behavior description	Enable or Disable the activation of BCLK clock (LFBGA only).
Input parameter	NewState : ENABLE or DISABLE
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

### Example:

```
...
EMI_BCLKCmd(ENABLE);
```

# 6 System control unit (SCU)

The System control unit (SCU) provides the control logic for the STR91xFA power, reset and clocks, also it controls a large number of miscellaneous features.

## 6.1 Register structure

### 6.1.1 SCU register structure

The SCU register structure SCU\_TypeDef is defined in the 91x\_map.h file as follows:

```
typedef struct
                             /* Clock Control Register
   vu32 CLKCNTR;
                                    /* PLL Configuration Register
   vu32 PLLCONF;
                                                                                                                               * /
   vu32 SYSSTATUS; /* System Status Register
vu32 PWRMNG; /* Power Management Register
   vu32 PWRMNG; /* Power Management Register
vu32 ITCMSK; /* Interrupt Mask Register
vu32 PCGR0; /* Peripheral Clock Gating Register 0
vu32 PCGR1; /* Peripheral Clock Gating Register 1
vu32 PRR0; /* Peripheral Software Reset Register 1
vu32 PRR1; /* Peripheral Software Reset Register 1
vu32 PRR1; /* Peripheral Software Reset Register 1
vu32 PCR0: /* Mask Cating Register 2
                                     /* Peripheral Software Reset Register 0
  Vu32 PRR1; /* Peripheral Software Reset Register 1

Vu32 MGR0; /* Mask Gating Register 0 */

Vu32 MGR1; /* Mask Gating Register 1 */

Vu32 PECGR0; /* Peripheral Emulation Clock Gating Register 0 */

Vu32 PECGR1; /* Peripheral Emulation Clock Gating Register 1 */

Vu32 SCR0; /* System Configuration Register 0 */
                                    /* Peripheral Software Reset Register 1
   vu32 EMPTY2:
   u32 EMPTY3;
   vu32 GPIOOUT[8]; /* GPIO Output Registers
   vu32 GPIOIN[8]; /* GPIO Input Registers
   vu32 GPIOTYPE[10]; /* GPIO Type Registers
   vu32 GPIOEMI; /* GPIO EMI Selector Register
   vu32 WKUPSEL;
                                     /* Wake-Up Selection Register
   u32 EMPTY4[2];
   vu32 GPIOANA;
                                    /* GPIO Analog mode
} SCU_TypeDef;
```

#### Table 21. SCU registers

Register	Description
CLKCNTR	Clock Control Register
PLLCONF	PLL Configuration Register
SYSSTATUS	System Status Register
PWRMNG	Power Management Register
ITMSK	Interrupt Mask Register
PCGRn	Peripheral Clock Gating Register (n =[0:1])
PRRn	Peripheral Reset Register (n=[0:1])
MGRn	Idle mode Mask Gating Register (n=[0:1])

577

Table 21. SCU registers

Register	Description
PECGRn	Peripheral Emulation Clock Gating (n=[0:1])
GPIOOUTn	GPIO Output Register (n=[0:7])
GPIOINn	GPIO Input Register (n=[0:7])
GPIOTYPEn	GPIO Type Register (n=[0:9])
GPIOEMI	GPIO External Memory Interface selector Register
SCR0	System Configuration Register
WKUPSEL	WakeUp Select Register
GPIOANA	GPIO Analog mode Register

#### The SCU is declared in the file below

```
#ifndef EXT
#Define EXT extern
#endif
#define AHB_APB_BRDG1_U (0x5C000000) /* AHB/APB Bridge 1 UnBuffered Space */
#define AHB_APB_BRDG1_B (0x4C000000) /* AHB/APB Bridge 1 Buffered Space */
#define APB_SCU_OFST
                           (0x00002000) /* Offset of SCU */
#ifndef Buffered
#define AHBAPB1_BASE
                                 (AHB_APB_BRDG1_U)
#else /* Buffered */
. . .
#define AHBAPB1_BASE
                                  (AHB_APB_BRDG1_B)
/* SCU Base Address definition*/
#define SCU_BASE (AHBAPB1_BASE + APB_SCU_OFST)
/* SCU peripheral declaration*/
#ifndef DEBUG
#define SCU
              ((SCU_TypeDef *) SCU_BASE)
#else
#ifdef _SCU
EXT SCU_TypeDef
                           *SCU;
\#endif /* \_SCU */
. . .
#endif
```

When debug mode is used, SCU pointer is initialized in *91x\_lib.c* file:

```
#ifdef _SCU
    SCU = (SCU_TypeDef *)SCU_BASE
#endif /* _SCU */
```

\_SCU must be defined, in *91x\_conf.h* file, to access the peripheral registers as follows:

#define SCU

. . .

# 6.2 Firmware library functions

Table 22. SCU library functions

Function name	Description
SCU_MCLKSourceConfig	Selects the Master clock source: OSC, PLL, or RTC
SCU_PLLFactorsConfig	Configures the PLL factors M,N and P
SCU_PLLCmd	Enables or disables the PLL
SCU_RCLKDivisorConfig	Configures the RCLK divisor: 1,2,4,8,16 or 1024
SCU_HCLKDivisorConfig	Configures the HCLK divisor: 1,2 or 4
SCU_PCLKDivisorConfig	Configures the PCLK divisor: 1,2,4 or 8
SCU_FMICLKDivisorConfig	Configures the FMI clock divisor: 1 or 2
SCU_EMIBCLKDivisorConfig	Configures the EMI bus clock divisor : 1 or 2
SCU_BRCLKDivisorConfig	Selects the Baud Rate clock divisor: 1 or 2
SCU_TIMExtCLKCmd	Enables or disables the TIMx clock source
SCU_USBCLKConfig	Selects the USBClock source: external 48MHz, MCLK or MCLK/2
SCU_PHYCLKConfig	Enables or disables the output PHY clock
SCU_APBPeriphClockConfig	Enables or disables the APB peripheral clocks
SCU_AHBPeriphClockConfig	Enables or disables the AHB peripheral clocks
SCU_APBPeriphIdleConfig	Enables or disables the APB peripheral clocks during Idle mode
SCU_AHBPeriphIdleConfig	Enables or disables the AHB peripherals clocks during Idle mode
SCU_APBPeriphDebugConfig	Enables or disables the APB peripherals clocks during debug mode
SCU_AHBPeriphDebugConfig	Enables or disables AHB peripheral clocks during debug mode
SCU_APBPeriphReset	Enables or disables Reset state for APB peripherals
SCU_AHBPeriphReset	Enables or disables Reset state for AHB peripherals
SCU_EMIModeConfig	Configures EMI mode : Multiplexed or Demultiplexed mode
SCU_EMIALEConfig	Configures EMI ALE signal length and polarity
SCU_GetPLLFreqValue	Gets the current PLL frequency value (unit = KHz)
SCU_GetMCLKFreqValue	Gets the current MCLK frequency value (unit = KHz)
SCU_GetHCLKFreqValue	Gets the current HCLK frequency value (unit = KHz)
SCU_GetPCLKFreqValue	Gets the current PCLK frequency value (unit = KHz)
SCU_GetRCLKFreqValue	Gets the current RCLK frequency value (unit = KHz)
SCU_WakeUpLineConfig	Configures an external interrupt as wake-up line
SCU_SpecIntRunModeConfig	Enables or disables the Special interrupt Run mode
SCU_EnterIdleMode	Puts the MCU in Idle mode
SCU_EnterSleepMode	Puts the MCU in Sleep mode
SCU_UARTIrDASelect	Selects UARTx operation : UART or IrDA

Table 22. SCU library functions

Function name	Description
SCU_PFQBCCmd	Enables or disables PFQBC
SCU_ITConfig	Enables or disables SCU interrupts
SCU_GetFlagStatus	Gets a flag status
SCU_ClearFlag	Clears a status flag
SCU_EMIByte_Select_Pinconfig	Enable or Disable the Byte selection pins behaviour(LFBGA only)
SCU_EMIclock_Pinconfig	Enable or Disable the BCLK pin clock driving (LFBGA only)

Note:

The SCU\_GPIOOUT, SCU\_GPIOIN, SCU\_GPIOTYPE, SCU\_GPIOEMI and SCU\_GPIOANA registers are not supported by the SCU library functions, they are supported by the GPIO driver functions.

## 6.2.1 SCU\_MCLKSourceConfig

Function name	SCU_MCLKSourceConfig
Function prototype	ErrorStatus SCU_MCLKSourceConfig(u32 MCLK_Source)
Behavior description	Selects the MCLK clock source: OSC, RTC, or PLL
Input parameter	MCLK_Source Refer to <i>Table 23: MCLK_Source parameter values</i> for the allowed values of this parameter.
Output parameter	None
Return parameter	ErrorStatus: ERROR or SUCCESS  - Function returns ERROR when selecting the PLL clock as MCLK source while PLL is either disabled or not locked.
Required preconditions	When selecting the PLL as MCLK clock source, make sure that the PLL is enabled and locked, you can do this using the SCU_PLLCmd(ENABLE) function.
Called functions	None

Table 23. MCLK\_Source parameter values

Value	Meaning
SCU_MCLK_PLL	MCLK source = PLL clock
SCU_MCLK_RTC	MCLK source = RTC clock
SCU_MCLK_OSC	MCLK source = Oscillator clock

## 6.2.2 SCU\_PLLFactorsConfig

Function name	SCU_PLLFactorsConfig
Function prototype	ErrorStatus SCU_PLLFactorsConfig(u8 PLLN, u8 PLLM, u8 PLLP)
Behavior description	Configures the PLL factors
Input parameter1	PLLN: PLL Feedback divider
Input parameter2	PLLM: PLL Pre-divider
Input parameter3	PLLP: PLL Post-divider
Output parameter	None
Return parameter	ErrorStatus: ERROR or SUCCESS  - Function returns ERROR when trying to set new PLL factors while PLL selected as MCLK source clock
Required preconditions	PLL must not be selected as MCLK clock
Called functions	SCU_PLLCmd(DISABLE) : Disables the PLL

Note:

This function disables the PLL before programming the PLL factors. To enable the PLL use the SCU\_PLLCmd(ENABLE) function after programming the PLL factors.

### 6.2.3 SCU\_PLLCmd

Function name	SCU_PLLCmd
Function prototype	ErrorStatus SCU_PLLConfig(FunctionnalState NewState)
Behavior description	Enables or disables the PLL
Input parameter	NewState : ENABLE or DISABLE
Output parameter	None
Return parameter	ErrorStatus: ERROR or SUCCESS The function returns ERROR when:  - Disabling the PLL while PLL is selected as MCLK source  - Enabling the PLL while PLL already enabled & locked
Required preconditions	<ul> <li>When enabling the PLL, you must have already configured the PLL factors using the SCU_PLLFactorsConfig function.</li> <li>When disabling the PLL, make sure that the PLL is not selected as MCLK.</li> </ul>
Called functions	None

Note:

After enabling the PLL, the PLL lock bit is polled to ensure that the PLL is locked before exiting the function.

Before disabling the PLL a "security" delay is inserted, this to guarantee that the system clock has already switched to OSC or RTC before disabling the PLL.

**577** 

# 6.2.4 SCU\_RCLKDivisorConfig

Function name	SCU_RCLKDivisorConfig
Function prototype	void SCU_RCLKDivisorConfig(u32 RCLK_Divisor)
Behavior description	Selects the RCLK divisor 1, 2, 4, 8, 16 or 1024
Input parameter	RCLK_Divisor Refer to <i>Table 24: RCLK_Divisor parameter values</i> for the allowed values of this parameter.
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

### Table 24. RCLK\_Divisor parameter values

RCLK_Divisor	Meaning
SCU_RCLK_Div1	RCLK Divisor = 1
SCU_RCLK_Div2	RCLK Divisor = 2
SCU_RCLK_Div4	RCLK Divisor = 4
SCU_RCLK_Div8	RCLK Divisor = 8
SCU_RCLK_Div16	RCLK Divisor = 16
SCU_RCLK_Div1024	RCLK Divisor = 1024

# 6.2.5 SCU\_HCLKDivisorConfig

Function name	SCU_HCLKDivisorConfig
Function prototype	void SCU_HCLKDivisorConfig(u32 HCLK_Divisor)
Behavior description	Selects the HCLK divisor: 1,2 or 4.
Input parameter	HCLK_Divisor  Refer to <i>Table 25: HCLK_Divisor parameter values</i> for the allowed values of this parameter.
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

Table 25. HCLK\_Divisor parameter values

Value	Meaning
SCU_HCLK_Div1	HCLK Divisor = 1
SCU_HCLK_Div2	HCLK Divisor = 2
SCU_HCLK_Div4	HCLK Divisor = 4

# 6.2.6 SCU\_PCLKDivisorConfig

Function name	SCU_PCLKDivisorConfig
Function prototype	void SCU_PCLKDivisorConfig(u32 PCLK_Divisor)
Behavior description	Selects the PCLK divisor: 1,2,4 or 8
Input parameter	PCLK_Divisor Refer to <i>Table 26: PCLK_Divisor parameter values</i> for the allowed values of this parameter.
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

### Table 26. PCLK\_Divisor parameter values

Value	Meaning
SCU_PCLK_Div1	PCLK Divisor = 1
SCU_PCLK_Div2	PCLK Divisor = 2
SCU_PCLK_Div4	PCLK Divisor = 4
SCU_PCLK_Div8	PCLK Divisor = 8

# 6.2.7 SCU\_FMICLKDivisorConfig

Function name	SCU_FMICLKDivisorConfig
Function prototype	void SCU_FMICLKDivisorConfig(u32 FMICLK_Divisor)
Behavior description	Selects the FMI clock Divisor: 1 or 2
Input parameter	FMICLK_Divisor Refer to <i>Table 27: FMICLK_Divisor parameter values</i> for the allowed values of this parameter.
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

### Table 27. FMICLK\_Divisor parameter values

Value	Meaning
SCU_FMICLK_Div1	FMICLK Divisor = 1
SCU_FMICLK_Div2	FMICLK Divisor = 2

## 6.2.8 SCU\_EMIBCLKDivisorConfig

Function name	SCU_EMIBCLKDivisorConfig
Function prototype	void SCU_EMIBCLKDivisorConfig(u32 EMIBCLK_Divisor)
Behavior description	Selects the EMI Bus clock Divisor: 1 or 2
Input parameter	EMIBCLK_Divisor Refer to <i>Table 28: EMIBCLK_Divisor parameter values</i> for the allowed values of this parameter.
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

### Table 28. EMIBCLK\_Divisor parameter values

Value	Meaning
SCU_EMIBCLK_Div1	EMIBCLK Divisor = 1
SCU_EMIBCLK_Div2	EMIBCLK Divisor = 2

# 6.2.9 SCU\_BRCLKDivisorConfig

Function name	SCU_BRCLKDivisorConfig
Function prototype	void SCU_BRCLKDivisorConfig(u32 BRCLK_Divisor)
Behavior description	Selects the Baud rate clock Divisor : 1 or 2
Input parameter	BRCLK_Divisor Refer to <i>Table 29: BRCLK_Divisor parameter values</i> for the allowed values of this parameter.
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

Table 29. BRCLK\_Divisor parameter values

Value	Meaning
SCU_BRCLK_Div1	BRCLK Divisor = 1
SCU_BRCLK_Div2	BRCLK Divisor = 2

## 6.2.10 SCU\_TIMExtCLKCmd

Function name	SCU_TIMExtCLKCmd
Function prototype	void SCU_TIMExtCLKCmd (u8 TIMx, FunctionalState NewState)
Behavior description	Enable or disable the TIMx external clock source.
Input parameter1	TIMx Refer to <i>Table 30: TIMx parameter values</i> for the allowed values of this parameter.
Input parameter2	NewState: ENABLE or DISABLE
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

### Table 30. TIMx parameter values

Value	Meaning
SCU_TIM01	TIMER 0 & 1
SCU_TIM23	TIMER 2 & 3

# 6.2.11 SCU\_USBCLKConfig

Function name	SCU_USBCLKConfig
Function prototype	void SCU_USBCLKConfig(u32 USBCLK_Source)
Behavior description	Selects the USB clock source
Input parameter	USBCLK_Source Refer to <i>Table 31: USBCLK_Source parameter values</i> for the allowed values of this parameter.
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

### Table 31. USBCLK\_Source parameter values

Value	Meaning
SCU_USBCLK_MCLK	USB clock = MCLK
SCU_USBCLK_MCLK2	USB clock = MCLK/2
SCU_USBCLK_EXT	USB clock = External 48MHz

# 6.2.12 SCU\_PHYCLKConfig

Function name	SCU_PHYCLKConfig
Function prototype	void SCU_PHYCLKConfig(FunctionnalState NewState)
Behavior description	Enables/disables the PHYCLK output
Input parameter	NewState: ENABLE or DISABLE
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

## 6.2.13 SCU\_APBPeriphClockConfig

Function name	SCU_APBPeriphClockConfig
Function prototype	void SCU_APBPeriphClockConfig(u32 APBPeriph, FunctionalState NewState)
Behavior description	Disables/ enables a clock for a peripheral or combination of peripherals (uses logical OR) on APB bus
Input parameter1	APBPeriph:PPP, example:RTC ,GPIO0, Refer to <i>APBPeriph on page 60</i> section for the list of allowed values.
Input parameter2	NewState: ENABLE or DISABLE
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

### **APBPeriph**

```
__TIM01, __TIM23, __MC, __UART0, __UART1, __UART2, __I2C0, __I2C1, __SSP0, __SSP1, __CAN, __ADC, __WDG, __WIU, __GPIO0, __GPIO1, __GPIO2, __GPIO3, __GPIO4, __GPIO5, __GPIO6, __GPIO7, __GPIO8, __GPIO9, __RTC.
```

## 6.2.14 SCU\_AHBPeriphClockConfig

Function name	SCU_AHBPeriphClockConfig
Function prototype	void SCU_AHBPeriphClockConfig(u32 AHBPeriph, FunctionalState NewState)
Behavior description	Disables / enables the clock for a peripheral or combination of peripherals (use logical OR) on AHB bus
Input parameter1	AHBPeriph:PPP, example:DMA,USB, Refer to <i>AHBPeriph on page 61</i> for the list of allowed values.
Input parameter2	NewState: ENABLE or DISABLE
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

### **AHBPeriph**

```
__FMI, __PFQBC, __SRAM, __SRAM_ARBITER, __VIC, __EMI, __EXT_MEM_CLK, __DMA, __USB, __USB48M , __ENET.
```

## 6.2.15 SCU\_APBPeriphDebugConfig

Function name	SCU_APBPeriphDebugConfig
Function prototype	void SCU_APBPeriphDebugConfig(u32 APBPeriph, FunctionalState NewState)
Behavior description	Enables/disables the clock for a peripheral during CPU Debug mode
Input parameter1	APBPeriph Refer to APBPeriph on page 60 for the list of allowed values.
Input parameter2	NewState: ENABLE or DISABLE
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

# 6.2.16 SCU\_AHBPeriphDebugConfig

Function name	SCU_AHBPeriphDebugConfig
Function prototype	void SCU_AHBPeriphDebugConfig(u32 AHBPeriph, FunctionalState NewState)
Behavior description	Enables/disables the clock for a peripheral during CPU Debug mode
Input parameter1	AHBPeriph Refer to AHBPeriph on page 61 for the list of allowed values.
Input parameter2	NewState: ENABLE or DISABLE
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

# 6.2.17 SCU\_APBPeriphIdleConfig

Function name	SCU_APBPeriphIdleConfig
Function prototype	<pre>void SCU_APBPeriphIdleConfig(u32 APBPeriph, FunctionalState NewState)</pre>
Behavior description	Enables/disables the clock for a peripheral during during Idle mode
Input parameter1	APBPeriph Refer to <i>APBPeriph on page 60</i> for the list of allowed values.
Input parameter2	NewState: ENABLE or DISABLE
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

# 6.2.18 SCU\_AHBPeriphIdleConfig

Function name	SCU_AHBPeriphIdleConfig	
Function prototype	<pre>void SCU_AHBPeripIdleConfig(u32 AHBPeriph, FunctionalState NewState)</pre>	
Behavior description	Enables/ disables the clock for a peripheral during Idle mode	
Input parameter1	AHBPeriph Refer to AHBPeriph on page 61 for the list of allowed values.	
Input parameter2	NewState: ENABLE or DISABLE	
Output parameter	None	
Return parameter	None	
Required preconditions	None	
Called functions	None	

## 6.2.19 SCU\_APBPeriphReset

Function name	SCU_APBPeriphReset
Function prototype	void SCU_APBPeriphReset(u32 APBPeriph, FunctionalState NewState)
Behavior description	Forces a peripheral into RESET
Input parameter1	APBPeriph Refer to APBPeriph on page 60 for the list of allowed values.
Input parameter2	NewState: ENABLE or DISABLE
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

# 6.2.20 SCU\_AHBPeriphReset

Function name	SCU_AHBPeriphReset
Function prototype	<pre>void SCU_AHBPeriphReset(u32 AHBResetPeriph, FunctionalState NewState)</pre>
Behavior description	Forces a peripheral into RESET
Input parameter1	AHBResetPeriph Refer to AHBResetPeriph on page 63 for the list of allowed values.
Input parameter2	NewState: ENABLE or DISABLE
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

### **AHBResetPeriph**

```
__FMI, __PFQBC, __SRAM, __SRAM_ARBITER, __VIC, __DMA,__USB, __ENET, __PFQBC_AHB.
```

## 6.2.21 SCU\_EMIModeConfig

Function name	SCU_EMIModeConfig
Function prototype	void SCU_EMIModeConfig(u32 SCU_EMIMODE)
Behavior description	Configures the EMI mode: multiplexed or demultiplexed
Input parameter	SCU_EMIMODE Refer to <i>Table 32: SCU_EMIMODE parameter values</i> for the allowed values of this parameter.
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

### Table 32. SCU\_EMIMODE parameter values

Value	Meaning
SCU_EMI_MUX	EMI mode = Multiplexed
SCU_EMI_DEMUX	EMI mode = Demultiplexed

# 6.2.22 SCU\_EMIALEConfig

Function name	SCU_EMIALEConfig
Function prototype	void SCU_EMIALEConfig(u32 SCU_EMIALE_LEN, u32 SCU_EMIALE_POL)
Behavior description	Configures EMI ALE signal length and polarity
Input parameter1	SCU_EMIALE_LEN Refer to <i>Table 33: SCU_EMIALE_LEN parameter values</i> for the allowed values of this parameter.
Input parameter2	SCU_EMIALE_POL Refer to <i>Table 34: SCU_EMIALE_POL parameter values</i> for the allowed values of this parameter.
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

## Table 33. SCU\_EMIALE\_LEN parameter values

Value	Meaning
SCU_EMIALE_LEN1	EMI ALE Length = 1 clock cycle
SCU_EMIALE_LEN2	EMI ALE length = 2 clock cycles

Table 34. SCU\_EMIALE\_POL parameter values

Value	Meaning
SCU_EMIALE_POLLow	EMI ALE Polarity = Low
SCU_EMIALE_POLHigh	EMI ALE Polarity = High

## 6.2.23 SCU\_GetPLLFreqValue

Function name	SCU_GetPLLFreqValue
Function prototype	u32 SCU_GetPLLFreqValue(void)
Behavior description	Gets the current generated PLL frequency
Input parameter	None
Output parameter	None
Return parameter	PLL frequency value (unit = KHz)
Required preconditions	None
Called functions	None

# 6.2.24 SCU\_GetMCLKFreqValue

Function name	SCU_GetMCLKFreqValue
Function prototype	u32 SCU_GetMCLKFreqValue(void)
Behavior description	Gets current MCLK frequency value
Input parameter	None
Output parameter	None
Return parameter	MCLK frequency value (unit = KHz)
Required preconditions	None
Called functions	None

# 6.2.25 SCU\_GetHCLKFreqValue

Function name	SCU_GetHCLKFreqValue	
Function prototype	u32 SCU_GetHCLKFreqValue(void)	
Behavior description	Gets current HCLK frequency value	
Input parameter	None	
Output parameter	None	
Return parameter	HCLK frequency value (unit = KHz)	
Required preconditions	None	
Called functions	None	

## 6.2.26 SCU\_GetPCLKFreqValue

Function name	SCU_GetPCLKFreqValue
Function prototype	u32 SCU_GetPCLKFreqValue(void)
Behavior description	Gets current PCLK frequency value
Input parameter	None
Output parameter	None
Return parameter	PCLK frequency value (unit = KHz)
Required preconditions	None
Called functions	None

# 6.2.27 SCU\_GetRCLKFreqValue

Function name	SCU_GetRCLKFreqValue	
Function prototype	u32 SCU_GetRCLKFreqValue(void)	
Behavior description	Gets current RCLK frequency value	
Input parameter	None	
Output parameter	None	
Return parameter	RCLK frequency (unit = KHz)	
Required preconditions	None	
Called functions	None	

# 6.2.28 SCU\_WakeUpLineConfig

Function name	SCU_WakeUpLineConfig
Function prototype	u32 SCU_WakeUpLineConfig(u8 EXTint)
Behavior description	Configures an external interrupt as wakeup line
Input parameter	EXTint (value from 0 to 31)
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

## 6.2.29 SCU\_EnterIdleMode

Function name	SCU_EnterIdleMode
Function prototype	void SCU_EnterIdleMode(void)
Behavior description	Puts MCU in Idle mode
Input parameter	None
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

# 6.2.30 SCU\_EnterSleepMode

Function name	SCU_EnterSleepMode	
Function prototype	void SCU_EnterSleepMode(void)	
Behavior description	Puts MCU in Sleep mode	
Input parameter	None	
Output parameter	None	
Return parameter	None	
Required preconditions	None	
Called functions	None	

# 6.2.31 SCU\_UARTIrDASelect

Function name	SCU_UARTIrdaSelect	
Function prototype	void SCU_UARTIrDASelect(u8 SCU_UARTx, u8 UART_IrDA_Mode)	
Behavior description	Configures UARTx as UART or IrDA	
Input parameter1	SCU_UARTx: SCU_UART[0:2]. Refer to <i>Table 36: SCU_UARTx</i> parameter values on page 68 for the allowed values of this parameter.	

Input parameter2	UART_IrDA Refer to <i>Table 35: UART_IrDA parameter values</i> for the allowed values of this parameter.
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

### Table 35. UART\_IrDA parameter values

Value	Meaning
SCU_UARTMode_IrDA	UARTMode = IrDA
SCU_UARTMode_UART	UARTMode = UART

### Table 36. SCU\_UARTx parameter values

Value	Meaning
SCU_UART0	UART0
SCU_UART1	UART1
SCU_UART2	UART2

## 6.2.32 SCU\_PFQBCCmd

Function name	SCU_PFQBCCmd
Function prototype	void SCU_PFQBCCmd(FunctionalState NewState)
Behavior description	Enables or Disables the PFQBC
Input parameter	NewState: ENABLE or DISABLE
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

# 6.2.33 SCU\_ITConfig

Function name	SCU_ITConfig
Function prototype	void SCU_ITConfig(u32 SCU_IT, FunctionalState NewState)
Behavior description	Enables or disables the specified SCU interrupts.
Input parameter1	SCU_IT: specifies the SCU interrupts sources to be enabled or disabled.  Refer to <i>Table 37: SCU_IT parameter values</i> for the allowed values of this parameter.
Input parameter2	NewState: new state of the specified SCU interrupts. This parameter can be: ENABLE or DISABLE.
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

## Table 37. SCU\_IT parameter values

Value	Meaning
SCU_IT_LVD_RST	LVD Reset interrupt
SCU_IT_SRAM_ERROR	SRAM error interrupt
SCU_IT_ACK_PFQBC	ACK_PFQBC interrupt
SCU_IT_LOCK_LOST	PLL LOCK Lost interrupt
SCU_IT_LOCK	PLL lock interrupt

# 6.2.34 SCU\_GetFlagStatus

Function name	SCU_GetFlagStatus
Function prototype	FlagStatus SCU_GetFlagStatus(u32 SCU_FLAG)
Behavior description	Checks whether the specified SCU flag is set or not.
Input parameter	SCU_FLAG: specifies the flag to check.  Refer to <i>Table 38: SCU_FLAG parameter values</i> for the allowed values of this parameter.
Output parameter	None
Return parameter	The new state of SCU_FLAG (SET or RESET).
Required preconditions	None
Called functions	None

### Table 38. SCU\_FLAG parameter values

SCU_FLAG	Meaning
SCU_FLAG_SRAM_ERR	SRAM error flag
SCU_FLAG_ACK_PFQBC	ACK_PFQBC flag
SCU_FLAG_LVD_RESET	LVD RESET flag
SCU_FLAG_WDG_RST	Watchdog RESET flag
SCU_FLAG_LOCK_LOST	PLL Lock lost flag
SCU_FLAG_LOCK	PLL Lock flag

# 6.2.35 SCU\_ClearFlag

Function name	SCU_ClearFlag
Function prototype	void SCU_ClearFlag(u32 SCU_FLAG)
Behavior description	Clears an SCU flag
Input parameter	SCU_FLAG: specifies the flag to clear.  Refer to <i>Table 38: SCU_FLAG parameter values</i> for the allowed values of this parameter.
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

# 6.2.36 SCU\_EMIByte\_Select\_Pinconfig

Function name	SCU_EMIByte_Select_Pinconfig
Function prototype	<pre>void SCU_EMIByte_Select_Pinconfig(FunctionalState NewState)</pre>
Behavior description	Enable or Disable the Byte selection pins behaviour(LFBGA only)
Input parameter	NewState : This parameter can be ENABLE or DISABLE
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

# 6.2.37 SCU\_EMIclock\_Pinconfig

Function name	SCU_EMIclock_Pinconfig
Function prototype	void SCU_EMIclock_Pinconfig(FunctionalState NewState)
Behavior description	Enable or Disable the BCLK pin clock driving (LFBGA only)
Input parameter	NewState :This parameter can be ENABLE or DISABLE
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

# 7 General purpose I/O ports (GPIO)

The GPIO driver may be used for several purposes, including pin configuration, reading a port pin and writing data into the port pin.

The first section describes the data structures used in the GPIO Firmware library. The second one presents the Firmware library functions.

## 7.1 GPIO register structure

The GPIO register structure *GPIO\_TypeDef* is defined in the *91x\_map.h* file as follows:

```
typedef struct
{

vu8 DR[1021]; /* Data Register */
vu32 DDR; /* Data Direction Register */
} GPIO_TypeDef;
```

#### Table 39. GPIO registers

Register	Description
GPIODATA	Data register
GPIODIR	Data direction register

The ten GPIO interfaces are declared in the same file:

```
#ifndef EXT
 #Define EXT extern
#endif
#define AHB_APB_BRDG0_U (0x58000000) /* AHB/APB Bridge 0 UnBuffered Space */
#define AHB_APB_BRDG0_B
                          (0x48000000) /* AHB/APB Bridge 0 Buffered Space
#define APB_GPIO0_OFST
                            (0x00006000) /* Offset of GPI00 */
#define APB_GPIO1_OFST
                            (0x00007000) /* Offset of GPI01 */
                            (0x00008000) /* Offset of GPIO2 */
#define APB_GPIO2_OFST
#define APB_GPIO3_OFST
                            (0x00009000)
                                          /* Offset of GPIO3 */
                                          /* Offset of GPIO4 */
#define APB_GPIO4_OFST
                            (0x0000A000)
                                          /* Offset of GPIO5 */
#define APB_GPIO5_OFST
                          (0x0000B000)
                                          /* Offset of GPIO6 */
#define APB_GPIO6_OFST
                         (0x0000D000) /* Offset of GPIO7 */
                          (0x0000C000)
#define APB_GPIO7_OFST
#define APB_GPIO8_OFST
                            (0x0000E000)
                                          /* Offset of GPIO8 */
                                          /* Offset of GPIO9 */
#define APB_GPIO9_OFST
                            (0x0000F000)
#ifndef Buffered
#define AHBAPB0_BASE
                              (AHB_APB_BRDG0_U)
#else /* Buffered */
#define AHBAPB0_BASE
                              (AHB_APB_BRDG0_B)
/* GPIO Base Address definition*/
#define GPIO0_BASE
                           (AHBAPB0_BASE + APB_GPIO0_OFST)
#define GPIO1_BASE
                           (AHBAPB0_BASE + APB_GPIO1_OFST)
```

577

```
#define GPIO2_BASE
                           (AHBAPB0_BASE + APB_GPIO2_OFST)
#define GPIO3_BASE
                           (AHBAPB0_BASE + APB_GPIO3_OFST)
#define GPIO4_BASE
                          (AHBAPB0_BASE + APB_GPIO4_OFST)
                          (AHBAPB0_BASE + APB_GPIO5_OFST)
#define GPIO5_BASE
                          (AHBAPB0_BASE + APB_GPIO6_OFST)
#define GPIO6_BASE
#define GPIO7_BASE
                           (AHBAPBO_BASE + APB_GPIO7_OFST)
                          (AHBAPBO_BASE + APB_GPIO8_OFST)
#define GPIO8_BASE
#define GPIO9_BASE
                          (AHBAPB0_BASE + APB_GPIO9_OFST)
/* GPIO peripheral declaration*/
#ifndef DEBUG
#define GPIO0
                ((GPIO_TypeDef *) GPIOO_BASE)
#define GPI01
                ((GPIO_TypeDef *) GPIO1_BASE)
                ((GPIO_TypeDef *) GPIO2_BASE)
#define GPIO2
#define GPIO3 ((GPIO_TypeDef *) GPIO3_BASE)
              ((GPIO_TypeDef *) GPIO8_BASE)
#define GPIO2
                ((GPIO_TypeDef *) GPIO9_BASE)
#define GPIO3
#else
. . .
#ifdef _GPIO0
EXT GPIO_TypeDef
                          *GPI00;
#endif /* _GPIO0 */
#ifdef _GPI01
EXT GPIO_TypeDef
                          *GPIO1;
#endif /* _GPIO1 */
#ifdef _GPIO2
EXT GPIO_TypeDef
                          *GPI02;
#endif /* _GPIO2 */
#ifdef _GPIO3
EXT GPIO_TypeDef
                          *GPI03;
#endif /* _GPIO3 */
#ifdef _GPIO8
EXT GPIO_TypeDef
                          *GPI08;
#endif /* _GPI08 */
#ifdef _GPIO9
EXT GPIO_TypeDef
                          *GPI09;
#endif /* _GPIO9 */
```

When debug mode is used, the GPIO pointers are initialized in the 91x\_lib.c file:

```
#ifdef _GPIO0
GPIO0 = (GPIO_TypeDef *)GPIO0_BASE;
#endif /*_GPIO0 */
#ifdef _GPIO1
GPIO0 = (GPIO_TypeDef *)GPIO1_BASE;
#endif /*_GPI01 */
#ifdef _GPIO2
GPIO0 = (GPIO_TypeDef *)GPIO2_BASE;
#endif /*_GPIO2 */
#ifdef _GPIO3
GPIO1 = (GPIO_TypeDef *)GPIO3_BASE;
#endif /*_GPIO3 */
#ifdef _GPIO8
GPIO1 = (GPIO_TypeDef *)GPIO8_BASE;
#endif /*_GPIO8 */
#ifdef _GPIO9
GPIO1 = (GPIO_TypeDef *)GPIO9_BASE;
#endif /*_GPIO9 */
```

\_GPIO, \_GPIO1,\_GPIO2 ....\_GPIO9 must be defined, in *91x\_conf.h* file, to access the peripheral registers as follows:

```
#define _GPIO
#define _GPIO0
#define _GPIO1
#define _GPIO2
...
#define _GPIO8
#define _GPIO9
```

5

# 7.2 Firmware library functions

Table 40. GPIO library functions

Function name	Description
GPIO_DeInit	Deinitializes the GPIOx peripheral registers to their default reset values.
GPIO_Init	Initializes the GPIOx peripheral according to the specified parameters in the GPIO_InitStruct.
GPIO_StructInit	Fills each GPIO_InitStruct member with its reset value.
GPIO_Read	Reads the specified GPIO data port
GPIO_ReadBit	Reads the specified port pin
GPIO_WriteBit	Sets or clears the selected data port bit.
GPIO_Write	Write data to the specified GPIO data port
GPIO_ANAPinConfig	Enables or disables pins from GPIO 4 in Analog mode.
GPIO_EMIConfig	Enables or disables GPIO 8 and 9 in EMI mode.

# 7.2.1 GPIO\_Delnit

Function name	GPIO_Delnit
Function prototype	void GPIO_DeInit(GPIO_TypeDef* GPIOx)
Behavior description	Deinitializes the GPIOx peripheral registers to their default reset values.
Input parameter	GPIOx: where x can be 0,1,,9 to select the GPIO peripheral.
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	SCU_APBPeriphReset()

### Example:

/\*Deinitializes the GPI00 peripheral registers to their default reset values\*/  $\mbox{GPIO\_DeInit(GPI00)};$ 

## 7.2.2 GPIO\_Init

Function name	GPIO_Init
Function prototype	<pre>void GPIO_Init(GPIO_TypeDef* GPIOx, GPIO_InitTypeDef* GPIO_InitStruct)</pre>
Behavior description	Initializes the GPIOx peripheral according to the specified parameters in the GPIO_InitStruct .
Input parameter1	GPIOx: where x can be 0,1,, 9 to select the GPIO peripheral.
Input parameter2	GPIO_InitStruct: pointer to a GPIO_InitTypeDef structure that contains the configuration information for the specified GPIO peripheral. Refer to section "GPIO_InitTypeDef on page 76" for more details on the allowed values of this parameter.
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

### **GPIO\_InitTypeDef**

The GPIO\_InitTypeDef structure is defined in the *91x\_GPIO.h* file:

```
typedef struct
{
vu8 GPIO_Pin;
vu8 GPIO_Direction;
vu8 GPIO_Type;
vu8 GPIO_IPInputConnected;
vu16 GPIO_Alternate;
} GPIO_InitTypeDef;
```

### GPIO\_Pin

Specifies GPIO pins to configure, (allows multiple pin configuration with the I operator).

This member can be one of the following values:

GPIO_Pin	Meaning
GPIO_Pin_None	No pin selected
GPIO_Pin_0	Pin 0 Selected
GPIO_Pin_1	Pin 1 Selected
GPIO_Pin_2	Pin 2 Selected
GPIO_Pin_3	Pin 3 Selected
GPIO_Pin_4	Pin 4 Selected
GPIO_Pin_5	Pin 5 Selected
GPIO_Pin_6	Pin 6 Selected
GPIO_Pin_7	Pin 7 Selected
GPIO_Pin_All	All pins Selected

### GPIO\_Direction

Specifies GPIO pin direction.

This member can be one of the following values:

GPIO_Direction	Meaning
GPIO_PinOutput	Configures corresponding pin to be an output.
GPIO_PinInput	Configures corresponding pin to be an input

### GPIO\_Type

Specifies the pin output type.

This member can be one of the following values:

GPIO_Type	Meaning
GPIO_Type_PushPull	Configures the GPIO in push pull type.
GPIO_Type_OpenCollector	Configures the GPIO in open collector type.

### GPIO\_IPInputConnected

Specifies the IP function to receive the input from a port pin. Only GPIO pins on P0 thru P7 use this function.

This member can be one of the following values:

GPIO_IPConnected	Meaning
GPIO_IPInputConnected_Enable	IP connected to the input
GPIO_IPInputConnected_Disable	IP unconnected to the input.

### GPIO\_Alternate

Specifies the IP function to be assigned to port pin. Only GPIO pins on P0 thru P7 use this function.

This member can be one of the following values:

GPIO_Out	Meaning
GPIO_InputAlt1	Configures the GPIO pin in input
GPIO_OutputAlt1	Configures the GPIO pin in output alternate function 1
GPIO_OutputAlt2	Configures the GPIO pin in output alternate function 2
GPIO_OutputAlt3	Configures the GPIO pin in output alternate function 3

#### Example:

```
/* Configure all the GPI00 in Input Push pull mode*/
GPI0_InitTypeDef GPI0_InitStruct;
GPI0_InitStruct.GPI0_Pin = GPI0_Pin_All;
GPI0_InitStruct.GPI0_Direction = GPI0_PinInput;
GPI0_InitStruct.GPI0_Type = GPI0_Type_PushPull;
GPI0_InitStruct.GPI0_IPInputConnected = GPI0_IPInputConnected_Disable;
GPI0_InitStruct.GPI0_Alternate = GPI0_InputAlt1;
GPI0_Init (GPI00, &GPI0_InitStruct);
```

## 7.2.3 **GPIO\_StructInit**

Function name	GPIO_StructInit
Function prototype	void GPIO_StructInit(GPIO_InitTypeDef* GPIO_InitStruct)
Behavior description	Fills each GPIO_InitStruct member with its reset value.
Input parameter	GPIO_InitStruct: pointer to a GPIO_InitTypeDef structure which will be initialized.
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

### Example:

/\*Initialize the GPIO Init Structure parameters\*/
GPIO\_InitTypeDef GPIO\_InitStruct;
GPIO\_StructInit(&GPIO\_InitStruct);

## 7.2.4 GPIO\_ReadBit

Function name	GPIO_ReadBit
Function prototype	u8 GPIO_ReadBit(GPIO_TypeDef* GPIOx, u8 GPIO_Pin)
Behavior description	Reads the specified data port bit.
Input parameter1	GPIOx: where x can be 0,1,,9 to select the GPIO peripheral.
Input parameter2	GPIO_Pin: Specifies the port bit to read.
Output parameter	None
Return parameter	The port pin value
Required preconditions	None
Called functions	None

### Example:

```
/* Reads the seventh pin of the GPIO1 and store it in Read_Value variable*/
u8 Read_Value;
Read_Value = GPIO_ReadBit(GPIO1, GPIO_Pin_7);
```

## 7.2.5 GPIO\_Read

Function name	GPIO_Read
Function prototype	u8 GPIO_Read(GPIO_TypeDef* GPIOx)
Behavior description	Reads the specified GPIO data port
Input parameter	GPIOx: where x can be 0,1,,9 to select the GPIO peripheral.
Output parameter	None
Return parameter	GPIO data port byte value.
Required preconditions	None
Called functions	None

### Example:

```
/* Read the GPIO2 data port and store it in Read_Value variable*/
u8 Read_Value;
Read_Value = GPIO_Read(GPIO2);
```

## 7.2.6 **GPIO\_WriteBit**

Function name	GPIO_WriteBit
Function prototype	<pre>void GPIO_WriteBit(GPIO_TypeDef* GPIOx,u8 GPIO_Pin, BitAction BitVal)</pre>
Behavior description	Sets or clears the selected data port bit
Input parameter1	GPIOx: where x can be 0,1,, 9 to select the GPIO peripheral.
Input parameter2	GPIO_Pin: specifies the port bit to be written.
Input parameter3	BitVal: this parameter specifies the value to be written to the selected bit.  Port_Val must be one of the BitAction enum values:  Bit_RESET: to clear the port pin  Bit_SET: to set the port pin
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

### Example:

/\*Set the GPI00 port pin 7\*/
GPI0\_WriteBit(GPI00, GPI0\_Pin\_7, Bit\_SET);

## 7.2.7 GPIO\_Write

Function name	GPIO_Write
Function prototype	<pre>void GPIO_Write(GPIO_TypeDef* GPIOx, u8 Port_Val)</pre>
Behavior description	Write the passed value in to the selected data GPIOx port register
Input parameter1	GPIOx: where x can be 0,1,, 9 to select the GPIO peripheral.
Input parameter2	Port_Val: The value to be written to the data port register.
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

### Example:

/\*Write data to GPIO0 data port\*/
GPIO\_Write(GPIO0, 0xFD);

## 7.2.8 **GPIO\_ANAPinConfig**

Function name	GPIO_ANAPinConfig
Function prototype	<pre>void GPIO_ANAPinConfig(u8 GPIO_ANAChannel, FunctionalState NewState)</pre>
Behavior description	Enables or disables pins from GPIO 4 in Analog mode.
Input parameter1	GPIO_ANAChannel: Specifies the port bit to be configured in Analog input. Refer to <i>Table 41: GPIO_ANAChannel parameter values</i> for the allowed values of this parameter.
Input parameter2	NewState: new state of the specified analog channel. This parameter can be: ENABLE or DISABLE.
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

### GPIO\_ANAChannel

Table 41. GPIO\_ANAChannel parameter values

· · · · · · · · · · · · · · · · · · ·	
Value	Meaning
GPIO_ANAChannel0	Configure the analog channel 0
GPIO_ANAChannel1	Configure the analog channel 1
GPIO_ANAChannel2	Configure the analog channel 2
GPIO_ANAChannel3	Configure the analog channel 3
GPIO_ANAChannel4	Configure the analog channel 4
GPIO_ANAChannel5	Configure the analog channel 5
GPIO_ANAChannel6	Configure the analog channel 6
GPIO_ANAChannel7	Configure the analog channel 7
GPIO_ANAChannelALL	Configure the all analog channel

### Example:

```
/* Enable Analog channel 3 */
GPIO_ANAPinConfig(GPIO_ANAChannel3, ENABLE);
```

# 7.2.9 **GPIO\_EMIConfig**

Function name	GPIO_EMIConfig
Function prototype	void GPIO_EMIConfig(FunctionalState NewState)
Behavior description	Enables or disables GPIO 8 and 9 in EMI mode.
Input parameter3	NewState: new state of the specified GPIO 8 and 9 is EMI interface. This parameter can be: ENABLE or DISABLE.
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

### Example:

/\* Enable GPIO 8 and 9 in EMI mode \*/
GPIO\_EMIConfig(ENABLE);

# 8 Vectored interrupt controller (VIC)

The driver may be used for several purposes, such as enabling and disabling interrupts (*IRQ*) and fast interrupts (*FIQ*), enabling and disabling individual *IRQ* channels, changing *IRQ* channel priorities, saving and restoring context and installing *IRQ* handlers.

The first section describes the data structures used in the VIC Firmware library. The second one presents the Firmware library functions.

## 8.1 VIC register structure

The VIC register structure VIC\_TypeDef is defined in the 91x\_map.h file as follows:

```
typedef struct
vu32 ISR;
vu32 FSR;
vu32 RINTSR;
vu32 INTSR;
vu32 INTER;
vu32 INTECR;
vu32 SWINTR
vu32 SWINTCR;
vu32 PER;
vu32 EMPTY1[3];
vu32 VAR;
vu32 DVAR;
vu32 EMPTY2[50];
vu32 VAiR[16];
vu32 EMPTY3[48];
vu32 VCiR[16];
} VIC_TypeDef;
```

### Table 42. VIC registers

Register	Description
ISR	IRQ Status Register
FSR	FIQ Status Register
RINTSR	Raw Interrupt Status Register
INTSR	Interrupt Select Register
INTER	Interrupt Enable Register
INTECR	Interrupt Enable Clear Register
SWINTR	Software Interrupt Register
SWINTCR	Software Interrupt clear Register
PER	Protection Enable Register
VAR	Vector Address Register
DVAR	Default Vector Address Register
VAiR	Vector Address 0-15 Register
VCiR	Vector Control 0-15 Register

577

The 2 VIC interfaces are declared in the same file:

```
#ifndef EXT
 #define EXT extern
#endif /* EXT */
                     (0xFC000000) /* Secondary VIC1 UnBuffered Space */
#define AHB_VIC1_U
                          (0xFFFFF000) /* Primary VICO UnBuffered Space */
#define AHB_VICO_U
#define VICO_BASE
                          (AHB_VICO_U)
#define VIC1_BASE
                          (AHB_VIC1_U)
#ifndef DEBUG
#define VIC0
                          ((VIC_TypeDef *)VIC0_BASE)
#define VIC1
                          ((VIC_TypeDef *)VIC1_BASE)
#else
#ifdef _VIC0
EXT VIC_TypeDef
                          *VIC0;
#endif /* _VIC0 */
#ifdef _VIC1
EXT VIC_TypeDef
                          *VIC1;
#endif /* _VIC1 */
#endif
```

When debug mode is used, VIC pointer is initialized in 91x\_lib.c file:

```
#ifdef __VIC0
   VIC0 = (VIC_TypeDef *)VIC0_BASE
#endif /* __VIC0 */

#ifdef __VIC1
   VIC1 = (VIC_TypeDef *)VIC1_BASE
#endif /* __VIC1 */
```

\_VIC, \_VIC0 and \_VIC1 must be defined, in  $91x\_conf.h$  file, to access the peripheral registers as follows:

```
#define _VIC
#define _VIC0
#define _VIC1
```

5

# 8.2 Firmware library functions

Table 43. VIC library functions

Function name	Description
VIC_DeInit	Deinitializes the VIC module registers to their default reset values.
VIC_GetIRQStatus	Gets the status of interrupts after IRQ masking.
VIC_GetFIQStatus	Gets the status of interrupts after FIQ masking.
VIC_GetSourceITStatus	Gets the status of the source interrupts before masking.
VIC_ITCmd	Enables or disables the interrupt request lines.
VIC_SWITConfig	Generates a software interrupt for the specific source interrupt before interrupt masking.
VIC_ProtectionCmd	Enables or disables the register access protection.
VIC_GetCurrentISRAdd	Gets the address of the currently active ISR.
VIC_GetISRVectAdd	Gets the ISR vector addresses.
VIC_Config	Configures the ISR, the line, the mode and the priority for each interrupt.

## 8.2.1 VIC\_Delnit

Function name	VIC_DeInit
Function prototype	void VIC_DeInit(void)
Behavior description	Deinitializes the VIC module registers to their default reset values.
Input parameter	None
Output parameter	None
Return parameter	None
Required preconditions	
Called functions	SCU_AHBPeriphReset()

### Example:

/\* Deinitialize the VIC \*/
VIC\_DeInit();

## 8.2.2 VIC\_GetIRQStatus

Function name	VIC_GetIRQStatus
Function prototype	FlagStatus VIC_GetIRQStatus(u16 VIC_Source)
Behavior description	Gets the status of interrupts after IRQ masking.
Input parameter	VIC_Source: specifies the number of the source line.  Refer to <i>Table 44: VIC_Source parameter values on page 86</i> for the allowed values of this parameter.
Output parameter	None
Return parameter	The status of the IRQ interrupt after masking (SET or RESET).
Required preconditions	
Called functions	None

The VIC\_Source parameter can take one of the following values defined in the *91x\_vic.h* file:

Table 44. VIC\_Source parameter values

Value	Meaning
WDG_ITLine	WDG interrupt line
SW_ITLine	Software interrupt line
ARMRX_ITLine	ARM RX interrupt line
ARMTX_ITLine	ARM TX interrupt line
TIM0_ITLine	TIM0 interrupt line
TIM1_ITLine	TIM1 interrupt line
TIM2_ITLine	TIM2 interrupt line
TIM3_ITLine	TIM3 interrupt line
USBHP_ITLine	High priority USB interrupt line
USBLP_ITLine	Low priority USB interrupt line
SCU_ITLine	SCU interrupt line
MAC_ITLine	MAC interrupt line
DMA_ITLine	DMA interrupt line
CAN_ITLine	CAN interrupt line
MC_ITLine	Motor Control interrupt line
ADC_ITLine	ADC interrupt line
UART0_ITLine	UART0 interrupt line
UART1_ITLine	UART1 interrupt line
UART2_ITLine	UART2 interrupt line
I2C0_ITLine	I2C0 interrupt line
I2C1_ITLine	I2C1 interrupt line
SSP0_ITLine	SSP0 interrupt line

Table 44. VIC\_Source parameter values (continued)

Value	Meaning
SSP1_ITLine	SSP1 interrupt line
LVD_ITLine	LVD interrupt line
RTC_ITLine	RTC interrupt line
WIU_ITLine	WIU interrupt line
EXTIT0_ITLine	EXTIT0 interrupt line
EXTIT1_ITLine	EXTIT1 interrupt line
EXTIT2_ITLine	EXTIT2 interrupt line
EXTIT3_ITLine	EXTIT3 interrupt line
USBWU_ITLine	USBWU interrupt line
PFQBC_ITLine	PFQBC interrupt line

### Example:

```
FlagStatus RTC_IT_Status;
/* Get the RTC interrupt status after IRQ masking */
RTC_IT_Status = VIC_GetIRQStatus(RTC_ITLine);
```

## 8.2.3 VIC\_GetFIQStatus

Function name	VIC_GetFIQStatus
Function prototype	FlagStatus VIC_GetFIQStatus(u16 VIC_Source)
Behavior description	Gets the status of interrupts after FIQ masking.
Input parameter	VIC_Source: specifies the number of the source line.  Refer to <i>Table 44: VIC_Source parameter values on page 86</i> for the allowed values of this parameter.
Output parameter	None
Return parameter	The status of the FIQ interrupt after masking (SET or RESET).
Required preconditions	
Called functions	None

### Example:

```
FlagStatus SSP1_IT_Status;
/* Get the SSP1 interrupt status after FIQ masking */
SSP1_IT_Status = VIC_GetFIQStatus(SSP1_ITLine);
```

### 8.2.4 VIC\_GetSourceITStatus

Function name	VIC_GetSourceITStatus
Function prototype	FlagStatus VIC_GetSourceITStatus(u16 VIC_Source)
Behavior description	Gets the status of the source interrupts before masking.
Input parameter	VIC_Source: specifies the number of the source line.  Refer to <i>Table 44: VIC_Source parameter values on page 86</i> for the allowed values of this parameter.
Output parameter	None
Return parameter	The status of the source interrupt before masking (SET or RESET).
Required preconditions	
Called functions	None

### Example:

```
FlagStatus RTC_IT_Status;
/* Get the RTC interrupt status before masking */
RTC_IT_Status = VIC_GetSourceITStatus(RTC_ITLine);
```

## 8.2.5 VIC\_ITCmd

Function name	VIC_ITCmd
Function prototype	void VIC_ITCmd(u16 VIC_Source, FunctionalState VIC_NewState)
Behavior description	Enables or disables the interrupt request lines.
Input parameter1	VIC_Source: specifies the number of the source line.  Refer to <i>Table 44: VIC_Source parameter values on page 86</i> for the allowed values of this parameter.
Input parameter2	VIC_NewState: specifies the line status. This parameter can be: ENABLE or DISABLE.
Output parameter	None
Return parameter	None
Required preconditions	
Called functions	None

### Example:

```
/* Enable the SSP1 interrupt request line */
VIC_ITCmd(SSP1_ITLine, ENABLE);
/* Disable the SSP2 interrupt request line */
VIC_ITCmd(SSP2_ITLine, DISABLE);
```

## 8.2.6 VIC\_SWITCmd

Function name	VIC_SWITCmd
Function prototype	void VIC_SWITCmd(u16 VIC_Source, FunctionalState VIC_NewState)
Behavior description	Generates a software interrupt for the specific source interrupt before interrupt masking.
Input parameter1	VIC_Source: specifies the number of the source line.  Refer to <i>Table 44: VIC_Source parameter values on page 86</i> for the allowed values of this parameter.
Input parameter2	VIC_NewState: specifies the software interrupt status. This parameter can be: ENABLE or DISABLE.
Output parameter	None
Return parameter	None
Required preconditions	
Called functions	None

### Example:

/\* Generate a software interrupt in the SSP1 interrupt request line before masking \*/  $VIC_SWITCmd(SSP1_ITLine, ENABLE)$ ;

/\* Generate a software interrupt in the SSP2 interrupt request line before masking \*/ VIC\_SWITCmd(SSP2\_ITLine, ENABLE);

## 8.2.7 VIC\_ProtectionCmd

Function name	VIC_ProtectionCmd
Function prototype	void VIC_ProtectionCmd(FuncionalState VIC_NewState)
Behavior description	Enables or disables the register access protection.
Input parameter	VIC_NewState: specifies the protection status. This parameter can be: ENABLE or DISABLE.
Output parameter	None
Return parameter	None
Required preconditions	
Called functions	None

### Example:

/\* Enable the registers access protection \*/
VIC\_ProtectionCmd(ENABLE);

### 8.2.8 VIC\_GetCurrentISRAdd

Function name	VIC_GetCurrentISRAdd
Function prototype	u32 VIC_GetCurrentISRAdd(VIC_TypeDef* VICx)
Behavior description	Gets the address of the current active ISR.
Input parameter	VICx: specifies the VIC peripheral. This parameter can one of the following values: - VIC0: To select VIC0 VIC1: To select VIC1.
Output parameter	None
Return parameter	The address of the active ISR.
Required preconditions	
Called functions	None

### Example:

```
u32 Address_Active_ISR
/* Get the address of the current active ISR for the VICO */
Address_Active_ISR = VIC_GetCurrentISRAdd(VICO);
```

Note: Lines 0 to 15 are mapped on VIC0 and Lines 16 to 31 are mapped on VIC1.

## 8.2.9 VIC\_GetISRVectAdd

Function name	VIC_GetISRVectAdd
Function prototype	u32 VIC_GetISRVectAdd(u16 VIC_Source, u16 VIC_Priority)
Behavior description	Configuration of the ISR vector addresses.
Input parameter1	VIC_Source: specifies the number of the source line.  Refer to <i>Table 44: VIC_Source parameter values on page 86</i> for the allowed values of this parameter.
Input parameter2	VIC_Priority: specifies the priority of the interrupt, it can be a value from 0 to 15, 0 is the highest priority.
Output parameter	None
Return parameter	The corresponding ISR vector address.
Required preconditions	
Called functions	None

#### Example:

```
u32 ISR_Address;
/* Get the ISR vector address of the RTC */
ISR_Address = VIC_GetISRVectAdd(RTC_ITLine, 0);
```

# 8.2.10 VIC\_Config

Function name	VIC_Config
Function prototype	void VIC_Config(u16 VIC_Source, VIC_ITLineMode VIC_LineMode, u8 VIC_Priority)
Behavior description	Configures the ISR, the line, the mode and the priority for each interrupt.
Input parameter1	VIC_Source: specifies the number of the source line.  Refer to <i>Table 44: VIC_Source parameter values on page 86</i> for the allowed values of this parameter.
Input parameter2	VIC_LineMode: specifies the type of interrupt of the source line. This parameter can be one of the following values: - VIC_IRQ: To configure the line as IRQ VIC_FIQ: To configure the line as FIQ.
Input parameter3	VIC_Priority: specifies the priority of the interrupt, it can be a value from 0 to 15, 0 is the highest priority.
Output parameter	None
Return parameter	None
Required preconditions	
Called functions	VIC_ITModeConfig VIC_ISRVecAddConfig VIC_VecEnableConfig VIC_ITSourceConfig

### Example:

```
void SSP1_ITHandler(void)
{
...
}
/* Configure the SSP1 interrupt as IRQ and set its priority to 5 */
VIC_Config(SSP1_ITLine, VIC_IRQ, 5);
```

# 9 Wake-up interrupt unit (WIU)

The WIU driver may be used for several purposes, such as enabling and disabling interrupt lines, selecting the edge sensitivity, interrupt or wake-up mode.

## 9.1 WIU register structure

The WIU register structure WIU\_TypeDef is defined in the 91x\_map.h file as follows:

### Table 45. WIU registers

Register	Description
CTRL	WIU Control register: used to enable input as wake-up or interrupt
MR	WIU Mask Register: used to mask generation of the interrupt or Wake- up event
TR	WIU Trigger register: used to specify whether the wake-up event is rising or falling edge triggered
PR	WIU Pending register: It is set when a wake-up input is pending
INTR	WIU Software Interrupt register: Software initiated interrupt

### The WIU is declared in the file below

```
#ifndef EXT
#Define EXT extern
#endif
#define AHB_APB_BRDGO_U (0x58000000) /* AHB/APB Bridge 0 UnBuffered Space */
#define AHB_APB_BRDG0_B
                          (0x48000000) /* AHB/APB Bridge 0 Buffered Space
                          (0x00001000) /* Offset of WIU */
#define APB_WIU_OFST
#ifndef Buffered
#define AHBAPB0_BASE
                              (AHB_APB_BRDG0_U)
#else /* Buffered */
#define AHBAPB0_BASE
                              (AHB_APB_BRDG0_B)
/* WIU Base Address definition*/
#define WIU_BASE
                   (AHBAPBO_BASE + APB_WIU_OFST)
/* WIU peripheral declaration*/
```

5

# 9.2 Firmware library functions

### Table 46. WIU library functions

Function name	Description
WIU_Init	Initializes the WIU according to the specified parameters in the WIU_InitTypeDef structure
WIU_DeInit	Deinitializes the WIU registers to their default reset values
WIU_StructInit	Fills each WIU_InitStruct member with its reset value.
WIU_Cmd	Enables or disables the WIU peripheral.
WIU_GetITStatus	Checks whether the specified WIU line is asserted or not
WIU_ClearITPendingBit	Clears the pending bit of the selected WIU line
WIU_GenerateSWInterrupt	Generates a Software interrupt for the specified line
WIU_GetFlagStatus	Checks whether the specified WIU line flag is set or not.
WIU_ClearFlag	Clears the WIU line pending flag.

## 9.2.1 WIU\_Init

Function name	WIU_Init
Function prototype	<pre>void WIU_Init(WIU_InitTypeDef* WIU_InitStruct)</pre>
Behavior description	Initializes WIU peripheral according to the specified parameters in the WIU_InitTypeDef structure.
Input parameter	WIU_InitStruct: Pointer to a WIU_InitTypeDef structure that contains the configuration information for the WIU peripheral. Refer to section "WIU_initTypeDef on page 94" for more details on the allowed values of this parameter.
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

### WIU\_initTypeDef

The WIU\_InitTypeDef structure defines the control setting for the WIU cell, it is defined in the <code>91x\_WIU.h</code>

```
typedef struct
{
u8 WIU_TriggerEdge;
u32 WIU_Line;
}WIU_InitTypeDef;
```

### WIU\_TriggerEdge

Specifies the triggering edge of the Wake-up line.

This member can be one of the following values.

WIU_TriggerEdge	Meaning
WIU_FallingEdge	Wake-up lines trigger on falling edge.
WIU_RisingEdge	Wake-up lines trigger on rising edge

WIU\_Line
Specifies the Wake-up line to be configured, it can be one of the following values:

Lines value	Corresponding Line
WIU_Line0	Wake-up line 0
WIU_Line1	Wake-up line 1
WIU_Line2	Wake-up line 2
WIU_Line3	Wake-up line 3
WIU_Line4	Wake-up line 4
WIU_Line5	Wake-up line 5
WIU_Line6	Wake-up line 6
WIU_Line7	Wake-up line 7
WIU_Line8	Wake-up line 8
WIU_Line9	Wake-up line 9
WIU_Line10	Wake-up line 10
WIU_Line11	Wake-up line 11
WIU_Line12	Wake-up line 12
WIU_Line13	Wake-up line 13
WIU_Line14	Wake-up line 14
WIU_Line15	Wake-up line 15
WIU_Line16	Wake-up line 16
WIU_Line17	Wake-up line 17
WIU_Line18	Wake-up line 18
WIU_Line19	Wake-up line 19
WIU_Line20	Wake-up line 20
WIU_Line21	Wake-up line 21
WIU_Line22	Wake-up line 22
WIU_Line23	Wake-up line 23
WIU_Line24	Wake-up line 24
WIU_Line25	Wake-up line 25
WIU_Line26	Wake-up line 26
WIU_Line27	Wake-up line 27
WIU_Line28	Wake-up line 28
WIU_Line29	Wake-up line 29
WIU_Line30	Wake-up line 30
WIU_Line31	Wake-up line 31

### **Example:**

```
The following example illustrates how to configure the WIU unit:

{
...
/* Set the WIU_InitTypeDef structure with the needed configuration */
WIU_InitStructure.WIU_Line = WIU_Line1;
WIU_InitStructure.WIU_TriggerEdge = WIU_FallingEdge;
/* Configure the WIU unit */
WIU_Init(&WIU_InitStructure);
...
}
```

### 9.2.2 WIU\_Delnit

Function name	WIU_DeInit
Function prototype	void WIU_DeInit(void)
Behavior description	Deinitalizes WIU peripheral registers to their default reset values
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	SCU_APBPeriphReset()

## 9.2.3 WIU\_StructInit

Function name	WIU_StructInit
Function prototype	<pre>void WIU_StructInit(WIU_InitTypeDef* WIU_InitStruct)</pre>
Behavior description	Fills each WIU_InitStruct member with its reset value.
Input parameter	WIU_InitStruct: pointer to a WIU_InitTypeDef structure which will be initialized.
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

## 9.2.4 WIU\_Cmd

Function name	WIU_Cmd
Function prototype	void WIU_Cmd(FunctionalState NewState)
Behavior description	Enables or disables the specified WIU peripheral.
Input parameter1	NewState: new state of the WIU peripheral. This parameter can be: ENABLE or DISABLE.
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

# 9.2.5 WIU\_GenerateSWInterrupt

Function name	WIU_GenerateSWInterrupt
Function prototype	void WIU_GenerateSWInterrupt(u32 WIU_Line)
Behavior description	Generates a software interrupt for the specified line.
Input parameter2	WIU_Line : Wake-up line.
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

### Example:

WIU\_GenerateSWInterrupt (WIU\_Line0);

## 9.2.6 WIU\_GetFlagStatus

Function name	WIU_GetFlagStatus
Function prototype	void WIU_GetFlagStatus(u32 WIU_Line)
Behavior description	Checks whether the specified WIU line flag is set or not
Input parameter2	WIU_Line: Wake-up line.
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

### Example:

WIU\_GetFlagStatus (WIU\_Line0);

577

## 9.2.7 WIU\_ClearFlag

Function name	WIU_ClearFlag
Function prototype	void WIU_ClearFlag(u32 WIU_Line)
Behavior description	Clears the WIU's line pending flag.
Input parameter2	WIU_Line : Wake-up line.
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

### Example:

WIU\_ClearFlag (WIU\_Line0);

## 9.2.8 WIU\_GetITStatus

Function name	WIU_GetITStatus
Function prototype	void WIU_GetITStatus(u32 WIU_Line)
Behavior description	Checks whether the specified WIU line is asserted or not.
Input parameter2	WIU_Line: Wake-up line
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

### Example:

WIU\_GetITStatus(WIU\_Line0);

## 9.2.9 WIU\_ClearITPendingBit

Function name	WIU_ClearITPendingBit
Function prototype	void WIU_ClearITPendingBit(u32 WIU_Line)
Behavior description	Clears the pending bit of the selected WIU line
Input parameter2	WIU_Line: Wake-up line to clear its pending bit.
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

### Example:

The following example clears the WIU line0 pending bit:

WIU\_ClearITPendingBit(WIU\_Line0);

# 10 Real time clock (RTC)

The RTC block combines a complete time of day clock with alarm, periodic interrupt, tamper detection and 9999-year calendar. The time is in 24 hour mode, and time/calendar values are stored in binary-coded decimal format.

## 10.1 RTC register structure

The RTC register structure RTC\_TypeDef is defined in the 91x\_map.h file as follows:

### Table 47. RTC registers

Register	Description
TR	Time register
DTR	Date register
ATR	Alarm Time register
CR	Control register
SR	Status register
MILR	Milliseconds register

#### The RTC is declared in the file below

```
#ifndef EXT
#Define EXT extern
#endif
#define AHB_APB_BRDG1_U
                           (0x5C000000) /* AHB/APB Bridge 1 UnBuffered Space */
                           (0x4C000000) /* AHB/APB Bridge 1 Buffered Space
#define AHB_APB_BRDG1_B
. . .
#define APB_RTC_OFST
                           (0x00001000) /* Offset of RTC */
#ifndef Buffered
                              (AHB_APB_BRDG1_U)
#define AHBAPB1_BASE
#else /* Buffered */
#define AHBAPB1_BASE
                               (AHB_APB_BRDG1_B)
/* RTC Base Address definition*/
#define RTC_BASE (AHBAPB1_BASE + APB_RTC_OFST)
/* RTC peripheral declaration*/
```

When debug mode is used, RTC pointer is initialized in *91x\_lib.c* file:

```
#ifdef _RTC
  RTC = (RTC_TypeDef *)RTC_BASE
#endif /* _RTC */
```

\_RTC must be defined, in  $\it 91x\_conf.h$  file, to access the peripheral registers as follows: #define \_RTC

. . .

**577** 

# 10.2 Firmware library functions

Table 48. RTC library functions

Function name	Description
RTC_DeInit	Resets RTC registers
RTC_SetDate	Sets Date (weekday, day, month, year* and century*) *example : 2006 , century = 20, year = 06.
RTC_SetTime	Sets Time (milliseconds, seconds, minutes, hours)
RTC_SetAlarm	Sets Alarm (alarm seconds, alarm minutes, alarm hour, alarm day)
RTC_GetDate	Gets current RTC date
RTC_GetTime	Gets current RTC time
RTC_GetAlarm	Gets configured alarm time
RTC_TamperConfig	Configures Tamper detection mode (level or edge) and polarity (high or low)
RTC_TamperCmd	Enables or disables Tamper detection
RTC_AlarmCmd	Enables or disables Alarm
RTC_CalibClockCmd	Enables or disables RTC Calibration Clock output
RTC_SRAMBattPowerCmd	Enables or Disables SRAM backup with VBAT
RTC_PeriodicIntConfig	Configures Periodic interrupt frequency
RTC_ITConfig	Enables or disables RTC interrupts
RTC_GetFlagStatus	Gets a flag status
RTC_ClearFlag	Clears a status flag

## 10.2.1 RTC\_Delnit

Function name	RTC_DeInit
Function prototype	void RTC_DeInit(void)
Behavior description	Resets RTC registers
Input parameter	None
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	SCU_APBPeriphReset()

## 10.2.2 RTC\_SetDate

Function name	RTC_SetDate
Function prototype	void RTC_SetDate (RTC_DATE Date)
Behavior description	Set Date : weekday, day, month, year and century.
Input parameter	Date: structure of type RTC_DATE
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

### RTC\_DATE

```
typedef struct
{
   u8 century;
   u8 year;
   u8 month;
   u8 day;
   u8 weekday;
}RTC_DATE;
```

### Structure members:

Member	Range
century	0- 99
year	0 - 99
month	1-12
day	1- 31
weekday	1-7

## 10.2.3 RTC\_SetTime

Function name	RTC_SetTime
Function prototype	void RTC_SetTime(RTC_TIME Time)
Behavior description	Set Time: milliseconds, seconds, minutes, hours
Input parameter	TIme: structure of type RTC_TIME
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

## RTC\_TIME

```
typedef struct
{
  u8 hours;
  u8 minutes;
  u8 seconds;
  u16 milliseconds;
}RTC_TIME;
```

### Structure members:

Member	Range
hours	0- 23
minutes	0- 59
seconds	0- 59
milliseconds	0 - 999

## 10.2.4 RTC\_SetAlarm

Function name	RTC_SetAlarm
Function prototype	void RTC_SetAlarm(RTC_ALARM Alarm)
Behavior description	Sets the Alarm time
Input parameter	Alarm: structure of type RTC_ALARM
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

### RTC\_ALARM

```
typedef struct
{
  u8 day;
  u8 hours;
  u8 minutes;
  u8 seconds;
}RTC_ALARM;
```

### Structure members:

Member	Range
day	1 - 31
hours	0 - 23
minutes	0 - 59
seconds	0 - 59

# 10.2.5 RTC\_GetDate

Function name	RTC_GetDate
Function prototype	void RTC_GetDate(u8 Format, RTC_DATE * Date)
Behavior description	Returns current RTC date
Input1 Parameter	Format: BINARY or BCD. Refer to <i>Table 49: Format parameter values on page 105</i> for the allowed values of this parameter.
Input2 Parameter	Date: pointer to structure of type RTC_DATE to be filled by function
Output parameter	Date
Return parameter	None
Required preconditions	None
Called functions	None

### Table 49. Format parameter values

Value	Meaning
BINARY	Binary coded values are returned
BCD	BCD coded values are returned

## 10.2.6 RTC\_GetTime

Function name	RTC_GetTime
Function prototype	void RTC_GetTime(u8 Format, RTC_TIME * Time)
Behavior description	Returns current RTC time
Input1 Parameter	Format: BINARY or BCD
Input2 Parameter	Time: pointer to a structure of type RTC_TIME to be filled by function
Output parameter	Time
Return parameter	None
Required preconditions	None
Called functions	None

## 10.2.7 RTC\_GetAlarm

Function name	RTC_GetAlarm
Function prototype	void RTC_GetAlarm(u8 Format, RTC_ALARM * Alarm)
Behavior description	Returns current RTC configured alarm time
Input1 Parameter	Format: BINARY or BCD
Input2 Parameter	Alarm: pointer to a structure of type <i>RTC_ALARM</i> to be filled by function
Output parameter	Alarm
Return parameter	None
Required preconditions	None
Called functions	None

# 10.2.8 RTC\_TamperConfig

Function name	RTC_TamperConfig
Function prototype	void RTC_TamperConfig(u32 TamperMode, u32 TamperPol)
Behavior description	Configures Tamper detection mode (level or edge) and polarity (high or low)
	TamperMode: Tamper detection mode (level or edge)
Input parameter1	Refer to <i>Table 50: TamperMode parameter values</i> section for the allowed values
	TamperPol: Tamper detection polarity (high or low)
Input parameter2	Refer to <i>Table 51: TamperPol parameter values</i> section for the allowed values.
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

Table 50. TamperMode parameter values

Value	Meaning
RTC_TamperMode_Edge	Tamper detection is on edge
RTC_TamperMode_Level	Tamper detection is on level

### Table 51. TamperPol parameter values

Value	Meaning
RTC_TamperPol_High	Tamper event triggered when Tamper input goes high
RTC_TamperPol_Low	Tamper event triggered when Tamper input goes low

## 10.2.9 RTC\_TamperCmd

Function name	RTC_TamperCmd
Function prototype	void RTC_TamperCmd(Function1State NewState)
Behavior description	Enables or disables RTC Tamper detection
Input parameter	NewState: ENABLE or DISABLE
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

## 10.2.10 RTC\_AlarmCmd

Function name	RTC_AlarmCmd
Function prototype	void RTC_AlarmCmd(Function1State NewState)
Behavior description	Enables or disables RTC Tamper detection
Input parameter	NewState: ENABLE or DISABLE
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

## 10.2.11 RTC\_CalibClockCmd

Function name	RTC_CalibClockCmd
Function prototype	void RTC_CalibClockCmd(FunctionalState NewState)
Behavior description	Enables or disables the RTC claibration clock output
Input parameter	NewState: ENABLE or DISABLE
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

## 10.2.12 RTC\_SRAMBattPowerCmd

Function name	RTC_SRAMBattPowerCmd
Function prototype	void RTC_SRAMBattPowerCmd(FunctionalState NewState)
Behavior description	Enables or disables SRAM power backup by VBAT
Input parameter	NewState: ENABLE or DISABLE
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

## 10.2.13 RTC\_PeriodicIntConfig

Function name	RTC_PeriodicIntConfig
Function prototype	void RTC_PeriodicIntConfig(u32 PeriodicClock)
Behavior description	Configures the Periodic clock frequency
Input parameter	PeriodicClock: Periodic Clock frequency Refer to <i>Table 52: PeriodicClock parameter values</i> section for the allowed values.
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

### Table 52. PeriodicClock parameter values

Value	Meaning
RTC_Per_2Hz	Periodic Clock = 2 Hz
RTC_Per_16Hz	Periodic Clock = 16 Hz

Table 52. PeriodicClock parameter values

Value	Meaning
RTC_Per_128Hz	Periodic Clock = 128 Hz
RTC_Per_1024Hz	Periodic Clock = 1024 Hz
RTC_Per_DISABLE	Periodic clock generation disabled

# 10.2.14 RTC\_ITConfig

Function name	RTC_ITConfig
Function prototype	void RTC_ITConfig(u32 RTC_IT, FunctionalState NewState)
Behavior description	Enables or disables the specified RTC interrupts.
Input parameter1	RTC_IT: specifies the RTC interrupts sources to be enabled or disabled. Refer to <i>Table 53: RTC_IT parameter values</i> section for the allowed values.
Input parameter2	NewState: new state of the specified RTC interrupts. This parameter can be: ENABLE or DISABLE.
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

Table 53. RTC\_IT parameter values

Value	Meaning
RTC_IT_Per	Periodic interrupt
RTC_IT_Alarm	Alarm interrupt
RTC_IT_Tamper	Tamper interrupt

## 10.2.15 RTC\_GetFlagStatus

Function name	RTC_GetFlagStatus
Function prototype	FlagStatus RTC_GetFlagStatus(u32 RTC_FLAG)
Behavior description	Checks whether the specified RTC flag is set or not.
Input parameter	RTC_FLAG: specifies the flag to check.  Refer to <i>Table 54: RTC_FLAG parameter values</i> section for the allowed values.
Output parameter	None
Return parameter	The new state of RTC_FLAG (SET or RESET).
Required preconditions	None
Called functions	None

## Table 54. RTC\_FLAG parameter values

Value	Meaning
RTC_FLAG_Per	Periodic interrupt flag
RTC_FLAG_Alarm	Alarm flag
RTC_FLAG_Tamper	Tamper flag

# 10.2.16 RTC\_ClearFlag

Function name	RTC_ClearFlag
Function prototype	void RTC_ClearFlag(u32 RTC_FLAG)
Behavior description	Clears a RTC flag
Input parameter2	RTC_FLAG: specifies the flag to clear.  Refer to <i>Table 54: RTC_FLAG parameter values</i> section for the allowed values.
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

# 11 Watchdog timer (WDG)

The Watchdog Timer peripheral can be used as free-running timer or as Watchdog to resolve processor malfunctions due to hardware or software failure.

The Watchdog supports the following features:

16-bit down-counter

8-bit clock prescaler

Safe reload sequence

Free-running timer mode

End of Count interrupt generation

The first section describes the data structure used in the WDG Firmware library. The second one presents the Firmware library functions.

### 11.1 WDG register structure

The WDG register structure  $WDG\_TypeDef$  is defined in the  $\textbf{91x\_map.h}$  file as follows:

```
typedef struct
 vu16 WDG_CR;
                    /* Control Register
 vu16 EMPTY1;
 vu16 WDG_PR;
                   /* Presclar Register
 vu16 EMPTY2;
 vu16 WDG_VR;
                   /* Pre-load Value Register */
 vu16 EMPTY3;
                   /* Counter Register
                                               * /
 vu16 WDG_CNT;
 vu16 EMPTY4;
 vu16 WDG_SR;
                   /* Status Register
 vu16 EMPTY5;
                   /* Mask Register
                                               * /
 vu16 WDG_MR;
 vu16 EMPTY6;
                    /* Key Register
 vu16 WDG_KR;
                                               * /
 vul6 EMPTY7;
} WDG_TypeDef;
```

#### Table 55. WDG registers

Register	Description
WDG_CR	This register controls and enables Watchdog Timer operations
WDG_PR	8-bit prescaler, WDG clock divider
WDG_VR	This register contains the 16-bit preload value to the WDG
WDG_CNT	This register contains the current counter value
WDG_SR	WDG Status register
WDG_MR	WDG Mask register
WDG_KR	Key Register: The WDG is loaded with VR value when the Key Register is written twice.

The WDG interface is declared in the same file:

```
#ifndef EXT
#Define EXT extern
#endif
#define AHB_APB_BRDG1_U (0x5C000000) /* AHB/APB Bridge 1 UnBuffered Space */
#define AHB_APB_BRDG1_B (0x4C000000) /* AHB/APB Bridge 1 Buffered Space */
                   (0x0000B000) /* Offset of WDG */
#define APB_WDG_OFST
#ifndef Buffered
#define AHBAPB1_BASE
                          (AHB_APB_BRDG1_U)
#else /* Buffered */
#define AHBAPB1_BASE
                           (AHB_APB_BRDG1_B)
/* WDG Base Address definition*/
#ifndef DEBUG
/* WDG peripheral declaration*/
#define WDG
                ((WDG_TypeDef *) WDG_BASE)
#else /* DEBUG */
#ifdef _WDG
EXT WDG_TypeDef
                      *WDG;
#endif /* _WDG */
#endif
```

When debug mode is used, WDG pointer is initialized in *91x\_lib.c* file:

```
#ifdef _WDG
WDG = (WDG_TypeDef *)WDG_BASE
#endif /* _WDG */
```

\_WDG must be defined, in  $\it 91x\_conf.h$  file, to access the peripheral registers as follows: #define \_WDG

477

# 11.2 Firmware library functions

Table 56. WDG library functions

Function name	Description	
WDG_Init	Initializes the WDG peripheral according to the specified parameters in the WDG_InitStruct.	
WDG_StructInit	Fills each WDG_InitStruct member with its reset value.	
WDG_StartWatchdogMode	Start the WDG in watchdog mode	
WDG_TimerModeCmd	Enables or disables WDG Timer mode	
WDG_ITConfig	Enables or disables the specified WDG interrupts.	
WDG_GetITStatus	Checks if the WDG End of Count(EC) interrupt is occurred or not.	
WDG_ClearITPendingBit	Clears the WDG End of Count(EC) interrupt pending bit.	
WDG_GetCounter	Gets the WDG counter value.	
WDG_GetFlagStatus	Checks whether the WDG End of Count(EC) flag is set or not.	
WDG_ClearFlag	Clears the WDG End of Count(EC) Flag.	
WDG_Reload	Reloads the watchdog counter in watchdog mode	

### 11.2.1 WDG\_Init

Function name	WDG_Init
Function prototype	void WDG_Init(void)
Behavior description	Initializes the WDG peripheral according to the specified parameters in the WDG_InitStruct.
Input parameter	None
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

### WDG\_InitTypeDef

The WDG\_InitTypeDef structure is defined in the *91x\_wdg.h* file:

```
typedef struct
{
  u16 WDG_ClockSource;
  u16 WDG_Prescaler;
  u16 WDG_Preload;
} WDG_InitTypeDef;
```

#### WDG\_ClockSource

This field specifies if the External clock (32 kHz RTC clock) or the APB clock signal will be used as counting clock.

This member can be one of the following values:

WDG_ClockSource	Value	Meaning
WDG_ClockSource_Rtc	0x0004	External clock (32 kHz RTC clock) will be used as counting clock.
WDG_ClockSource_Apb	0x0000	The APB clock signal will be used as counting clock.

#### WDG Prescaler

Specifies the Prescaler value to divide the clock source. The clock of the Watchdog Timer Counter is divided by PR[7:0] + 1.

This member must be a number between 0x00 and 0xFF.

#### WDG\_Preload

This value is loaded in the WDG Counter when it starts counting. The time ( $\mu$ s) needed to reach the end of count is given by:

$$\frac{Prescaler \times Preload \times Tclk}{1000}$$

where Tclk is the Clock period measured in ns.

This member must be a number between 0x0000 and 0xFFFF.

#### Example:

```
{
...
   WDG_InitTypeDef Init_Structure;
   Init_Structure.WDG_Prescaler = 0xF0;
   Init_Structure.WDG_Preload = 0xFF00;
   WDG_Init (&Init_Structure);
   ...
}
```

## 11.2.2 WDG\_StructInit

Function name	WDG_StructInit
Function prototype	void WDG_StructInit(WDG_InitTypeDef* WDG_InitStruct)
Behavior description	Fills each WDG_InitStruct member with its reset value.
Input parameter	WDG_InitStruct: pointer to a WDG_InitTypeDef structure which will be initialized.
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

### Example:

```
WDG_InitTypeDef WDG_InitStructure;
WDG_StructInit(&WDG_InitStructure);
```

## 11.2.3 WDG\_StartWatchdogMode

Function name	WDG_StartWatchdogMode
Function prototype	void WDG_StartWatchdogMode(void)
Behavior description	Start the WDG in watchdog mode
Input parameter	None
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

## 11.2.4 WDG\_TimerModeCmd

Function name	WDG_TimerModeCmd
Function prototype	void WDG_TimerModeCmd(FunctionalState NewState)
Behavior description	Enables or Disables the Watchdog Timer mode
Input parameter	NewState : This parameter can be: ENABLE or DISABLE.
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

## 11.2.5 WDG\_ITConfig

Function name	WDG_ITConfig
Function prototype	void WDG_ITConfig(FunctionalState NewState)
Behavior description	Enables or disables the WDG End of Count(EC) interrupt.
Input parameter1	NewState: This parameter can be: ENABLE or DISABLE.
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

#### Example:

WDG\_ITConfig(ENABLE);

## 11.2.6 WDG\_GetITStatus

Function name	WDG_GetFlagStatus
Function prototype	ITStatus WDG_GetITStatus(void)
Behavior description	Checks whether the WDG End of Count(EC) interrupt has occurred or not.
Input parameter1	None
Output parameter	None
Return parameter	The new state of WDG End of Count(EC) interrupt (SET or RESET).
Required preconditions	None
Called functions	None

### **Example:**

The following example illustrates how to test if the *end of count* flag is set or reset:

```
...
if (WDG_GetFlagStatus(WDG_U,WDG_IT_ECM) == SET)
...
```

57

## 11.2.7 WDG\_ClearITPendingBit

Function name	WDG_ClearITPendingBit
Function prototype	void WDG_ClearITPendingBit(void)
Behavior description	Clears the WDG End of Count(EC) interrupt pending bit.
Input parameter1	None
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

### **Example:**

The following example illustrates how to clear the end of count flag:

```
...
WDG_ClearITPendingBit();
```

## 11.2.8 WDG\_GetCounter

Function name	WDG_GetCounter
Function prototype	u16 WDG_GetCounter(void)
Behavior description	Gets the WDG current counter value.
Input parameter	None
Output parameter	None
Return parameter	WDG current counter value.
Required preconditions	None
Called functions	None

### Example:

The following example illustrates how to get the counter value of the WDG timer:

```
...
u16 CounterValue = WDG_GetCounter();
```

577

## 11.2.9 WDG\_GetFlagStatus

Function name	WDG_GetFlagStaus
Function prototype	FlagStatus WDG_GetFlagStatus(void)
Behavior description	Checks whether the WDG End of Count(EC) flag is set or not.
Input parameter	None
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

### **Example:**

### Example illustrating the use of WDG\_GetFlagStaus function:

/\*wait for the end of count on mode free running timer\*/
while(WDG\_GetFlagStatus() == RESET);

## 11.2.10 WDG\_GetFlagStatus

Function name	WDG_ClearFlag
Function prototype	void WDG_ClearFlag(void)
Behavior description	Clears the WDG End of Count(EC) Flag.
Input parameter	None
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

### Example:

```
WDG_ClearFlag();
```

## 11.2.11 WDG\_Reload

Function name	WDG_Reload
Function prototype	void WDG_Reload(void)
Behavior description	Reloads the watchdog counter in watchdog mode
Input parameter	None
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

# 12 16-bit timer (TIM)

The TIM driver may be used for a variety of purposes, including timing operation, Input capture, output compare and PWM generation.

## 12.1 TIM register structure

The TIM register structure *TIM\_TypeDef* is defined in the *91x\_map.h* file as follows:

```
typedef struct
  vu16 IC1R;
 vu16 EMPTY1;
 vu16 IC2R;
 vu16 EMPTY2;
 vul6 OC1R;
  vu16 EMPTY3;
 vu16 OC2R;
  vu16 EMPTY4;
 vul6 CNTR;
  vul6 EMPTY5;
  vu16 CR1;
  vul6 EMPTY6;
  vu16 CR2;
 vu16 EMPTY7;
  vu16 SR;
 vu16 EMPTY8;
} TIM_TypeDef;
```

#### Table 57. TIM registers

Register	Description
IC1R	Input Capture 1 Register
IC2R	Input Capture 2 Register
OC1R	Output Compare 1 Register
OC2R	Output Compare 2 Register
CNTR	Counter Register
CR1	Control Register 1
CR2	Control Register 2
SR	Status Register

The four TIM interfaces are declared in the same file:

```
#ifndef EXT
#Define EXT extern
#endif
...
#define AHB_APB_BRDGO_U (0x58000000) /* AHB/APB Bridge 0 UnBuffered Space */
#define AHB_APB_BRDGO_B (0x48000000) /* AHB/APB Bridge 0 Buffered Space */
...
#define APB_TIMO_OFST (0x00002000) /* Offset of TIMO */
```

```
#define APB_TIM1_OFST (0x00003000) /* Offset of TIM1 */
#define APB_TIM2_OFST (0x00004000) /* Offset of TIM0 */
#define APB_TIM3_OFST (0x00005000) /* Offset
#ifndef Buffered
#define AHBAPB0_BASE
                                (AHB_APB_BRDG0_U)
#else /* Buffered */
. . .
                                 (AHB_APB_BRDG0_B)
#define AHBAPB0_BASE
/* TIM Base Address definition*/
#define TIM1_BASE
                            (AHBAPBO_BASE + APB_TIM1_OFST)
                          (AHBAPB0_BASE + APB_TIM2_OFST)
#define TIM2_BASE
#define TIM3_BASE
                           (AHBAPBO_BASE + APB_TIM3_OFST)
/* TIM peripheral declaration*/
#ifndef DEBUG
#define TIM0
              ((TIM_TypeDef *) TIM0_BASE)
#define TIM1 ((TIM_TypeDef *) TIM1_BASE)
#define TIM2 ((TIM_TypeDef *) TIM2_BASE)
#define TIM3 ((TIM_TypeDef *) TIM3_BASE)
. . .
#else
#ifdef _TIM0
EXT TIM_TypeDef
                            *TIMO;
#endif /* _TIM0 */
#ifdef _TIM1
EXT TIM_TypeDef
                            *TIM1;
#endif /* _TIM1 */
#ifdef _TIM2
EXT TIM_TypeDef
                            *TIM2;
\#endif /* _TIM2 */
#ifdef _TIM3
EXT TIM_TypeDef
                            *TIM3;
\#endif /* _TIM3 */
#endif
```

#### When debug mode is used, TIM pointers are initialized in 91x\_lib.c file:

```
#ifdef _TIM0
TIM0 = (TIM_TypeDef *)TIM0_BASE;
#endif /*_TIM0 */
#ifdef _TIM1
TIM0 = (TIM_TypeDef *)TIM1_BASE;
#endif /*_TIM1 */
#ifdef _TIM2
TIM0 = (TIM_TypeDef *)TIM2_BASE;
#endif /*_TIM2 */
```

```
#ifdef _TIM3
TIM1 = (TIM_TypeDef *)TIM3_BASE;
#endif /*_TIM3 */
```

\_TIM, \_TIM0,\_TIM1,\_TIM2 and \_TIM3 must be defined, in **91x\_conf.h** file, to access the peripheral registers as follows:

```
#define _TIM
#define _TIM0
#define _TIM1
#define _TIM2
#define _TIM3
```

# 12.2 Firmware library functions

### Table 58. TIM library functions

Function name	Description
TIM_DeInit	Deinitializes TIM peripheral registers to their default reset values.
TIM_Init	Initializes TIM peripheral according to the specified parameters in the TIM_InitTypeDef structure.
TIM_StructInit	Fills a TIM_InitTypeDef structure with the reset value of each parameter (which depend on the register reset value)
TIM_ClockSourceConfig	Configures the TIM clock source.
TIM_PrescalerConfig	Configures the TIM prescaler Value.
TIM_GetPrescalerValue	Gets the TIM prescaler Value.
TIM_GetICAP1Value	Reads and returns the Input Capture 1 value.
TIM_GetICAP2Value	Reads and returns the Input Capture 2 value.
TIM_GetPWMIPulse	Reads and returns the PWM input pulse value.
TIM_GetPWMIPeriod	Reads and returns the PWM input period value.
TIM_CounterCmd	Configures the TIM counter.
TIM_SetPulse	Set the new pulse value.
TIM_GetFlagStatus	Checks whether the specified TIM flag is set or not.
TIM_ClearFlag	Clears the specified TIM flag.
TIM_ITConfig	Configures the TIM interrupts.
TIM_GetCounterValue	Gets the TIM counter value.
TIM_DMAConfig	Configures the TIM DMA source.
TIM_DMACmd	Enables or disables the TIMx DMA interface.

## 12.2.1 TIM\_Delnit

Function name	TIM_DeInit
Function prototype	<pre>void TIM_DeInit(TIM_TypeDef *TIMx);</pre>
Behavior description	Deinitializes the TIMx peripheral registers to their default reset values.
Input parameter	TIMx: where x can be 0,1, 2 or 3 to select the TIM peripheral.
Output parameter	None
Return parameter	None
Required preconditions	
Called functions	SCU_APBPeriphReset()

### Example:

```
/*To deinitialize the TIMO and TIM1*/
TIM_DeInit (TIMO);
TIM_DeInit (TIM1);
```

## 12.2.2 TIM\_Init

Function name	TIM_Init
Function prototype	<pre>void TIM_Init(TIM_TypeDef* TIMx, TIM_InitTypeDef* TIM_InitStruct)</pre>
Behavior description	Initializes the TIMx peripheral according to the specified parameters in the TIM_InitStruct .
Input parameter1	TIMx: where x can be 0,1, 2 or 3 to select the TIM peripheral.
Input parameter2	TIM_InitStruct: pointer to a TIM_InitTypeDef structure that contains the configuration information for the specified TIM peripheral. Refer to section "TIM_InitTypeDef on page 125" for more details on the allowed values of this parameter.
Output parameter	None
Return parameter	None
Required preconditions	
Called functions	None

### TIM\_InitTypeDef

The TIM\_InitTypeDef structure is defined in the *91x\_tim.h* file:

```
u16 TIM_Mode; /* Timer mode */
u16 TIM_OC1_Modes; /* Output Compare 1 Mode: Timing or Wave */
u16 TIM_OC2_Modes; /* Output Compare 2 Mode: Timing or Wave */
u16 TIM_Clock_Source; /* Timer Clock source APB/SCU/EXTERNAL */
u16 TIM_Clock_Edge; /* Timer Clock Edge: Rising or Falling Edge */
u16 TIM_OPM_INPUT_Edge; /* Timer Input Capture 1 Edge used in OPM Mode */
u16 TIM_ICAP1_Edge; /* Timer Input Capture 1 Edge used in ICAP1 Mode */
u16 TIM_ICAP2_Edge; /* Timer Input Capture 2 Edge used in ICAP2 Mode */
u8 TIM_Prescaler; /* Timer Prescaler factor */
u16 TIM_Pulse_Level_1; /* Level applied on the Output Compare Pin 1 */
u16 TIM_Pulse_Level_2; /* Level applied on the Output Compare Pin 2 */
u16 TIM_Period_Level; /* Level applied during the Period of a PWM Mode */
u16 TIM_Pulse_Length_1; /* Pulse 1 Length used in Output Compare 1 Mode */
u16 TIM_Pulse_Length_2; /* Pulse 2 Length used in Output Compare 2 Mode */
u16 TIM_Full_Period; /* Period Length used in PWM Mode */
U16 TIM_Full_Period; /* Period Length used in PWM Mode */
U16 TIM_InitTypeDef;
```

#### TIM\_Mode

Specifies the TIM operating mode. This parameter can be one of the following values:

TIM_Mode	Meaning
TIM_PWM	Pulse Width Modulation mode
TIM_OPM	One Pulse Mode
TIM_PWMI	Pulse Width Modulation Input Mode
TIM_OCM_CHANNEL_1	Output Compare Channel 1 Mode
TIM_OCM_CHANNEL_2	Output Compare Channel 2 Mode
TIM_OCM_CHANNEL_12	Output Compare Channels 1 & 2 Mode
TIM_ICAP_CHANNEL_1	Input Capture Channel 1 Mode
TIM_ICAP_CHANNEL_2	Input Capture Channel 2 Mode
TIM_ICAP_CHANNEL_12	Input Capture Channel 1 & 2 Mode

### TIM\_OC1\_Modes

Specifies the operating mode of the OCMP1 pin. This member can be one of the following values:

TIM_OC1_Modes	Meaning
TIM_Timing	OCMP1 pin is a general I/O
TIM_Wave	OCMP1 pin is dedicated to the OC1 capability of the TIM

577

#### TIM\_OC2\_Modes

Specifies the operating mode of the OCMP2 pin. This member can be one of the following values:

TIM_OC2_Modes	Meaning
TIM_Timing	OCMP2 pin is a general I/O
TIM_Wave	OCMP2 pin is dedicated to the OC2 capability of the TIM

#### TIM\_ICAP1\_EDGE

Specifies the trigger mode for Input Capture 1. This member can be one of the following values:

TIM_ICAP1_EDGE	Meaning
TIM_ICAP1_EDGE_RISING	A rising edge triggers the capture
TIM_ICAP1_EDGE_FALLING	A falling edge triggers the capture

#### TIM\_ICAP2\_EDGE

Specifies the trigger mode for Input Capture 1. This member can be one of the following values:

TIM_ICAP2_EDGE	Meaning
TIM_ICAP2_EDGE_RISING	A rising edge triggers the capture
TIM_ICAP2_EDGE_FALLING	A falling edge triggers the capture

#### TIM\_OPM\_INPUT\_Edge

Specifies the input edges for one pulse mode. This member can be one of the following values:

TIM_OPM_INPUT_Edge	Meaning
TIM_Rising	A rising edge triggers the counter initialization
TIM_Falling	A falling edge triggers the counter initialization

#### TIM\_Clock\_Source

Specifies the clock source of the TIM peripheral. This member can be one of the following values:

TIM_Clock_Source	Meaning
TIM_CLK_EXTERNAL	Reference clock source is used
TIM_CLK_APB	APB clock source is used

#### TIM\_Clock\_Edge

Specifies which type of level transition on the reference clock will trigger the counter. This member can be one of the following values:

TIM_Clock_Edge	Meaning
TIM_CLK_EDGE_RISING	A rising edge triggers the counter
TIM_CLK_EDGE_FALLING	A falling edge triggers the counter

#### TIM\_Prescaler

Specifies the Prescaler value to divide the APB clock. Timer clock will be equal to

$$\frac{f_{CPU}}{(Prescaler + 1)}$$

#### TIM\_Pulse\_Level\_1

When using PWM, OPM, OCM1 or OCM12 mode, this parameter specifies the pulse level of the signal generated on the OCMP1 pin. This member can be one of the following values:

TIM_Pulse_Level_1	Meaning
TIM_High	OLVL1 is High Level
TIM_Low	OLVL2 is High Level

#### TIM Pulse Level 2

When using OCM2 or OCM12 mode, this parameter specifies the pulse level of the signal generated on OCMP2 pin. This member can be one of the following values:

TIM_Pulse_Level_2	Meaning
TIM_High	OLVL2 is High Level
TIM_Low	OLVL1 is High Level

#### TIM\_Period\_Level

When using OPM mode, this parameter specifies the signal level after the pulse generated on the OCMP1 pin. This member can be one of the following values:

TIM_Period_Level	Meaning
TIM_High	OLVL1 is High Level
TIM_Low	OLVL1 is Low Level

#### TIM Pulse Length 1

When using PWM, OPM, OCM1 or OCM1&2 mode, this parameter specifies the pulse length to be loaded in the OC1R register.

#### TIM Pulse Length 2

When using OCM1 or OCM12 mode, this parameter specifies the pulse length to be loaded in the OC2R register.

#### TIM Full Period

Specifies the period to be loaded in the OC2R register, when PWM mode is used.

#### Example:

```
^{\prime \star} To configure the TIM3 peripheral as Output Compare Mode on channel 2 ^{\star \prime}
TIM_InitStruct
                    TIM_InitStructure;
TIM_InitStructure.TIM_Mode = TIM_OCM_CHANNEL_2;
TIM_InitStructure.TIM_Clock_Source = TIM_CLK_APB;
TIM_InitStructure.TIM_Prescaler = 0xFF;
TIM_InitStructure.TIM_OC2_Modes = TIM_WAVE ;
TIM_InitStructure.TIM_Pulse_Level_2 = TIM_HIGH;
TIM_InitStructure.TIM_Pulse_Length_2 = 0xFF00;
TIM_Init (TIM3, &TIM_InitStructure);
/*To configure the TIM2 peripheral as Input Capture Mode on channel1*/
TIM_InitStruct
                    TIM_InitStructure;
TIM InitStructure.TIM Mode = TIM ICAP CHANNEL 1;
TIM_InitStructure.TIM_Clock_Source = TIM_CLK_APB;
TIM_InitStructure.TIM_Prescaler = 0xFF;
TIM_InitStructure.TIM_ICAP1_Edge = TIM_ICAP1_EDGE_RISING;
TIM_Init (TIM2, &TIM_InitStructure);
/*To configure the TIMO peripheral in PWM Mode*/
TIM InitStruct TIM InitStructure;
TIM_InitStructure.TIM_Mode = TIM_PWM;
TIM_InitStructure.TIM_Clock_Source = TIM_CLK_APB;
TIM_InitStructure.TIM_Prescaler = 0xFF;
TIM_InitStructure.TIM_Pulse_Level_1 = TIM_HIGH;
TIM_InitStructure.TIM_Period_Level = TIM_LOW;
TIM_InitStructure.TIM_Pulse_Length_1 = 0x3FF;
TIM_InitStructure.TIM_Full_Period = 0xFFF;
TIM_Init (TIM0, &TIM_InitStructure);
/*To configure the TIM1 peripheral in PWMI Mode*/
TIM_InitStruct
                  TIM_InitStructure;
TIM_InitStructure.TIM_Mode = TIM_PWMI;
TIM_InitStructure.TIM_Clock_Source = TIM_CLK_APB;
TIM_InitStructure.TIM_Prescaler = 0x7F;
TIM_InitStructure.TIM_ICAP1_Edge = TIM_ICAP1_EDGE_RISING;
TIM_Init (TIM1, &TIM_InitStructure);
/*To configure the TIM2 peripheral in OPM Mode*/
TIM_InitStruct
                    TIM_InitStructure;
TIM_InitStructure.TIM_Mode = TIM_OPM;
TIM_InitStructure.TIM_OPM_INPUT_Edge = TIM_OPM_EDGE_RISING;
TIM_InitStructure.TIM_Clock_Source = TIM_CLK_APB;
TIM InitStructure.TIM Prescaler = 0xFF;
TIM_InitStructure.TIM_Pulse_Level_1 = TIM_HIGH;
TIM_InitStructure.TIM_Period_Level = TIM_LOW;
TIM_InitStructure.TIM_Pulse_Length_1 = 0xFFF;
TIM_Init (TIM2, &TIM_InitStructure);
```

## 12.2.3 TIM\_StructInit

Function name	TIM_StructInit
Function prototype	<pre>void TIM_StructInit(TIM_InitTypeDef* TIM_InitStruct)</pre>
Behavior description	Fills each TIM_InitStruct member with its reset value.
Input parameter	TIM_InitStruct: pointer to a TIM_InitTypeDef structure which will be initialized.
Output parameter	None
Return parameter	None
Required preconditions	
Called functions	None

### Example:

/\* To initialize the TIM structure \*/
TIM\_StructInit (&TIM\_InitStruct);

## 12.2.4 TIM\_PrescalerConfig

Function name	TIM_PrescalerConfig
Function prototype	<pre>void TIM_PrescalerConfig (TIM_TypeDef *TIMx, u8 TIM_Prescaler);</pre>
Behavior description	This routine is used to configure the TIM prescaler value.
Input parameter1	TIMx: where x can be 0,1, 2 or 3 to select the TIM peripheral.
Input parameter2	TIM_Prescaler: specifies the TIM prescaler value.
Output parameter	None
Return parameter	None
Required preconditions	
Called functions	None

### Example:

/\*To configure the TIM3 prescaler value to 0x7F\*/  $\texttt{TIM\_PrescalerConfig(TIM3, 0x7F)}$ 

## 12.2.5 TIM\_GetPrescalerValue

Function name	TIM_GetPrescalerValue
Function prototype	u8 TIM_GetPrescalerValue (TIM_TypeDef *TIMx)
Behavior description	This routine is used to get the Prescaler value.
Input parameter	TIMx: where x can be 0,1, 2 or 3 to select the TIM peripheral.
Output parameter	None
Return parameter	The prescaler value.
Required preconditions	
Called functions	None

#### Example:

/\*To get the Prescaler value of the TIM2 timer\*/
u8 MyPrescaler;
MyPrescaler = TIM\_GetPrescalerValue(TIM2);

### 12.2.6 TIM\_GetICAP1Value

Function name	TIM_GetICAP1Value
Function prototype	u8 TIM_GetICAPAValue (TIM_TypeDef *TIMx)
Behavior description	This routine is used to get the input capture 1 value.
Input parameter	TIMx: where x can be 0,1, 2 or 3 to select the TIM peripheral.
Output parameter	None
Return parameter	The input capture 1 value.
Required preconditions	
Called functions	None

### Example:

/\*To get the input capture 1value of the TIM2 timer\*/
u16 MyValue;
MyValue = TIM\_GetICAP1Value(TIM2);

## 12.2.7 TIM\_GetICAP2Value

Function name	TIM_GetlCAP2Value
Function prototype	u8 TIM_GetICAP2Value (TIM_TypeDef *TIMx)
Behavior description	This routine is used to get the input capture 2 value.
Input parameter	TIMx: where x can be 0,1, 2 or 3 to select the TIM peripheral.
Output parameter	None
Return parameter	The input capture 2 value.
Required preconditions	
Called functions	None

#### Example:

/\*To get the input capture 2 value of the TIM2 timer\*/
u16 MyValue;
MyValue = TIM\_GetICAP2Value(TIM2);

### 12.2.8 TIM\_GetPWMIPulse

Function name	TIM_GetPWMIPulse
Function prototype	u16 TIM_GetPWMIPulse (TIM_TypeDef *TIMx);
Behavior description	This routine is used to get the PWM input pulse value.
Input parameter	TIMx: where x can be 0,1, 2 or 3 to select the TIM peripheral.
Output parameter	None
Return parameter	The pulse of the external signal.
Required preconditions	
Called functions	None

### Example:

/\*To get the pulse of PWM input signal of the TIM3 timer\*/
u16 MyPWMIPulse;
MyPWMIPulse = TIM\_GetPWMIPulse(TIM3);

### 12.2.9 TIM\_GetPWMIPeriod

Function name	TIM_GetPWMIPeriod
Function prototype	u16 TIM_GetPWMIPeriod (TIM_TypeDef *TIMx);
Behavior description	This routine is used to get the PWM input period value.
Input parameter	TIMx: where x can be 0,1, 2 or 3 to select the TIM peripheral.
Output parameter	None
Return parameter	The period of the external signal.
Required preconditions	
Called functions	None

#### Example:

/\*To get the period of the PWM input signal of the TIM3 timer\*/
u16 MyPWMIPeriod;
MyPWMIPeriod = TIM\_GetPWMIPeriod(TIM3);

### 12.2.10 TIM\_CounterCmd

Function name	TIM_CounterCmd
Function prototype	<pre>void TIM_CounterCmd (TIM_TypeDef *TIMx, CounterOperations TIM_Operation);</pre>
Behavior description	This routine is used to control the TIM counter.
Input parameter1	TIMx: where x can be 0,1, 2 or 3 to select the TIM peripheral.
Input parameter2	TIM_Operation: specifies the operation of the counter TIM_STOP: Stops the TIM counter TIM_ENABLE: Enable or resume the TIM counter TIM_CLEAR: Clear the TIM counter value.
Output parameter	None
Return parameter	None
Required preconditions	
Called functions	None

### Example:

/\*To stop the TIM2 timer counter\*/
TIM\_CounterCmd(TIM2, TIM\_STOP);

## 12.2.11 TIM\_SetPulse

Function name	TIM_SetPulse
Function prototype	<pre>void TIM_SetPulse(TIM_TypeDef *TIMx, u16 TIM_Channel, u16 TIM_Pulse);</pre>
Behavior description	This routine is used to set the new pulse value.
Input parameter1	TIMx: where x can be 0,1, 2 or 3 to select the TIM peripheral.
Input parameter2	TIM_Channel: specifies the channel. This parameter can be one of the following: - TIM_PWM_OC1_Channel: PWM/Output Compare 1 Channel - TIM_OC2_Channel: Output Compare 2 Channel.
Input parameter3	TIM_Pulse: specifies the new TIM pulse value.
Output parameter	None
Return parameter	None
Required preconditions	
Called functions	None

#### Example:

/\*To set the pulse value of TIM2 on the channel 2 to 0xFFAA\*/ TIM\_SetPulse(TIM2, TIM\_OC2\_Channel,0xFFAA);

## 12.2.12 TIM\_GetFlagStatus

Function name	TIM_GetFlagStatus
Function prototype	FlagStatus TIM_GetFlagStatus(TIM_TypeDef* TIMx, u16 TIM_FLAG)
Behavior description	Checks whether the specified TIM flag is set or not.
Input parameter1	TIMx: where x can be 0,1, 2 or 3 to select the TIM peripheral.
Input parameter2	TIM_FLAG: specifies the flag to check.  Refer to <i>Table 59: TIM_FLAG parameter values</i> for the allowed values of this parameter.
Output parameter	None
Return parameter	The new state of TIM_FLAG (SET or RESET).
Required preconditions	
Called functions	None

Table 59. TIM\_FLAG parameter values

Values	Meaning
TIM_FLAG_IC1	Input Capture Flag channel 1
TIM_FLAG_OC1	Output Compare Flag channel 1

Table 59. TIM\_FLAG parameter values

Values	Meaning
TIM_FLAG_TO	Timer Overflow
TIM_FLAG_IC2	Input Capture Flag channel 2
TIM_FLAG_OC2	Output Compare Flag channel 2

#### Example:

```
/*To check the TIM1 overflow flag*/
FunctionalState OverFlowStatus ;
OverFlowStatus = TIM_GetFlagStatus(TIM1, TIM_FLAG_TO) ;
```

### 12.2.13 TIM\_ClearFlag

Function name	TIM_ClearFlag
Function prototype	void TIM_ClearFlag(TIM_TypeDef* TIMx, u16 TIM_FLAG)
Behavior description	Clears the TIMx pending flags.
Input parameter1	TIMx: where x can be 0,1, 2 or 3 to select the TIM peripheral.
Input parameter2	TIM_FLAG: specifies the flag to clear. To clear TIM flags, use a combination of one or more of the values in <i>Table 59: TIM_FLAG parameter values on page 133</i> .
Output parameter	None
Return parameter	None
Required preconditions	
Called functions	None

#### Example:

/\*To clear the TIM1 overflow flag\*/
TIM\_ClearFlag(TIM1, TIM\_FLAG\_TO);

## 12.2.14 TIM\_ITConfig

Function name	TIM_ITConfig
Function prototype	<pre>void TIM_ITConfig(TIM_TypeDef* TIMx, u16 TIM_IT, FunctionalState TIM_NewState)</pre>
Behavior description	Enables or disables the specified TIM interrupts.
Input parameter1	TIMx: where x can be 0,1, 2 or 3 to select the TIM peripheral.
Input parameter2	TIM_IT: specifies the TIM interrupts sources to be enabled or disabled. Refer to <i>Table 60: TIM_IT parameter values</i> for the allowed values of this parameter.
Input parameter3	TIM_NewState: new state of the specified TIMx interrupts. This parameter can be: ENABLE or DISABLE.
Output parameter	None
Return parameter	None

Required preconditions	
Called functions	None

To enable or disable TIM interrupts, use a combination of one or more of the following values:

Table 60. TIM\_IT parameter values

Value	Meaning
TIM_IT_IC1	Input Capture IT channel 1
TIM_IT_OC1	Output Compare IT channel 1
TIM_IT_TO	Timer Overflow IT
TIM_IT_IC2	Input Capture IT channel 2
TIM_IT_OC2	Output Compare IT channel 2

#### Example:

/\*To enable the overflow IT and the input capture 2 of the TIM3\*/ TIM\_ITConfig(TIM3, TIM\_IT\_TO | TIM\_IT\_IC2, ENABLE);

### 12.2.15 TIM\_GetCounterValue

Function name	TIM_GetCounterValue
Function prototype	u16 TIM_GetCounterValue(TIM_TypeDef* TIMx)
Behavior description	Gets the TIM counter value.
Input parameter	TIMx: where x can be 0,1, 2 or 3 to select the TIM peripheral.
Output parameter	None
Return parameter	The TIM counter value
Required preconditions	
Called functions	None

#### Example:

/\*To get the counter value of the TIM2\*/
u16 MyCounter;
MyCounter = TIM\_GetCounterValue(TIM2);

### 12.2.16 TIM\_DMAConfig

Function name	TIM_DMAConfig
Function prototype	<pre>void TIM_DMAConfig (TIM_TypeDef *TIMx, u16 TIM_DMA_Souces);</pre>
Behavior description	This routine is used to enable the DMA.
Input parameter1	TIMx: where x can be 0,1, 2 or 3 to select the TIM peripheral.
Input parameter2	TIM_DMASources: specifies the DMA source to be used.  Refer to <i>Table 61: TIM_DMASources parameter values</i> for the allowed values of this parameter.
Output parameter	None
Return parameter	None
Required preconditions	
Called functions	None

#### Table 61. TIM\_DMASources parameter values

Value	Meaning
TIM_DMA_IC1	Input Capture DMA channel 1
TIM_DMA_OC1	Output Compare DMA channel 1
TIM_DMA_IC2	Input Capture DMA channel 2
TIM_DMA_OC2	Output Compare DMA channel 2

#### Example:

/\*To configure the DMA for the TIMO peripheral and to choose ICAP1 as a DMA source\*/  $TIM_DMAConfig(TIMO, TIM_DMA_ICAP1);$ 

## 12.2.17 TIM\_DMACmd

Function name	TIM_DMACmd
Function prototype	<pre>void TIM_DMACmd(TIM_TypeDef* TIMx, FunctionalState TIM_NewState)</pre>
Behavior description	Enables or disables the TIMx DMA interface.
Input parameter1	TIMx: where x can be 0,1, 2 or 3 to select the TIM peripheral.
Input parameter2	TIM_NewState: new state of the DMA interface. This parameter can be: ENABLE or DISABLE.
Output parameter	None
Return parameter	None
Required preconditions	
Called functions	None

### Example:

/\*To enable TIM0 DMA interface\*/
TIM\_DMACmd(TIM0, ENABLE);
/\*To disable TIM0 DMA interface\*/
TIM\_DMACmd(TIM0, DISABLE);

## 13 DMA controller (DMA)

The DMA enables memory-to-memory, memory-to-peripheral, peripheral-to-memory, and peripheral-to-peripheral transactions. Each DMA stream provides unidirectional serial DMA transfers for a single source and destination. A bidirectional port requires one stream for transmit and one for receive. The source and destination areas can each be either a memory region or a peripheral.

## 13.1 DMA register structure

The DMA register structures <code>DMA\_TypeDef</code> and <code>DMA\_Channel\_TypeDef</code> are defined in the <code>91x\_map.h</code> file as follows:

 $/\,^\star$  there are forteen commun registers for the eight channels\*/

Table 62. DMA registers

Register	Description
DMA_SRCx	Channelx Source Address Register
DMA_DESx	Channelx Destination Address Register
DMA_LLIx	Channelx Linked List Item Register
DMA_CCx	Channelx Contol Register

Table 62. DMA registers (continued)

Register	Description
DMA_CCNFx	Channelx Configuration Register
DMA_ISR	Interrupt Status Register
DMA_TCISR	Terminal Count Interrupt Status Register
DMA_TCICR	Terminal Count Interrupt Clear Register
DMA_EISR	Error Interrupt Status Register
DMA_EICR	Error Interrupt Clear Register
DMA_TCRISR	Terminal Count Raw Interrupt Status Register
DMA_ERISR	Error Raw Interrupt Status Register
DMA_ENCSR	Enabled Channel Status Register
DMA_SBRR	Software Burst Request Register
DMA_SSRR	Software Single Request Register
DMA_SLBRR	Software Last Burst Request Register
DMA_SLSRR	Software Last Single Request Register
DMA_CNFR	Configuration Register
DMA_SYNR	Syncronization Register

#### The DMA interface is declared in the same file:

```
#ifndef EXT
  #define EXT extern
#endif /* EXT */
#define AHB_DMA_U
                            (0x78000000) /* DMA UnBuffered Space */
#define AHB_DMA_B
                            (0x68000000) /* DMA Buffered Space
#define AHB_DMA_Channel0_OFST
                                (0x00000100)
                                                /* Offset of Channel 0 */
                                                /* Offset of Channel 1 */
#define AHB_DMA_Channel1_OFST (0x00000120)
                                                /* Offset of Channel 2 */
/* Offset of Channel 3 */
#define AHB_DMA_Channel2_OFST
                                  (0x00000140)
#define AHB_DMA_Channel3_OFST
                                  (0x00000160)
#define AHB_DMA_Channel4_OFST (0x00000180)
                                                /* Offset of Channel 4 */
                                                /* Offset of Channel 5 */
#define AHB_DMA_Channel5_OFST (0x000001A0)
#define AHB_DMA_Channel6_OFST
                                                /* Offset of Channel 6 */
/* Offset of Channel 7 */
                                 (0x00001C0)
#define AHB_DMA_Channel7_OFST
                                  (0x000001E0)
#ifndef Buffered
#define DMA_BASE
                            (AHB_DMA_U)
#else /* Buffered */
#define DMA_BASE
                            (AHB_DMA_B)
#endif /* Buffered */
```

**577** 

```
/* Channel Base Address definition*/
#define DMA_Channel0_BASE (DMA_BASE + AHB_DMA_Channel0_OFST)
#define DMA_Channel1_BASE (DMA_BASE + AHB_DMA_Channel1_OFST)
#define DMA_Channel2_BASE (DMA_BASE + AHB_DMA_Channel2_OFST)
#define DMA_Channel3_BASE (DMA_BASE + AHB_DMA_Channel3_OFST)
#define DMA_Channel4_BASE (DMA_BASE + AHB_DMA_Channel4_OFST)
#define DMA_Channel5_BASE (DMA_BASE + AHB_DMA_Channel5_OFST)
#define DMA_Channel6_BASE (DMA_BASE + AHB_DMA_Channel6_OFST)
#define DMA_Channel7_BASE (DMA_BASE + AHB_DMA_Channel7_OFST)
#ifndef DEBUG
/* DMA peripheral declaration*/
#define DMA
                           ((DMA_TypeDef *)DMA_BASE)
#define DMA_Channel0
                           ((DMA_Channel_TypeDef *)DMA_Channel0_BASE)
#define DMA_Channel1
                           ((DMA_Channel_TypeDef *)DMA_Channel1_BASE)
                           ((DMA_Channel_TypeDef *)DMA_Channel2_BASE)
#define DMA_Channel2
                           ((DMA_Channel_TypeDef *)DMA_Channel3_BASE)
#define DMA_Channel3
#define DMA_Channel4
                           ((DMA_Channel_TypeDef *)DMA_Channel4_BASE)
                           ((DMA_Channel_TypeDef *)DMA_Channel5_BASE)
#define DMA_Channel5
#define DMA_Channel6
                           ((DMA_Channel_TypeDef *)DMA_Channel6_BASE)
                           ((DMA_Channel_TypeDef *)DMA_Channel7_BASE)
#define DMA_Channel7
      /* DEBUG */
#else
. . .
#ifdef _DMA
EXT DMA_TypeDef
                           *DMA;
#endif /* _DMA */
#ifdef _DMA_Channel0
EXT DMA_Channel_TypeDef
                           *DMA_Channel0;
#endif /* _DMA_Channel0 */
#ifdef _DMA_Channel1
EXT DMA_Channel_TypeDef
                           *DMA_Channel1;
#endif /* _DMA_Channel1 */
#ifdef _DMA_Channel2
EXT DMA_Channel_TypeDef
                          *DMA_Channel2;
\#endif /* _DMA_Channel0 */
#ifdef _DMA_Channel3
EXT DMA_Channel_TypeDef
                          *DMA_Channel3;
#endif /* _DMA_Channel0 */
#ifdef _DMA_Channel4
EXT DMA_Channel_TypeDef
                          *DMA_Channel4;
#endif /* _DMA_Channel4 */
#ifdef _DMA_Channel5
EXT DMA_Channel_TypeDef
                          *DMA_Channel5;
\#endif /* _DMA_Channel5 */
#ifdef _DMA_Channel6
EXT DMA_Channel_TypeDef
                           *DMA_Channel6;
#endif /* _DMA_Channel6 */
#ifdef _DMA_Channel7
EXT DMA_Channel_TypeDef *DMA_Channel7;
#endif /* _DMA_Channel7 */
```

When debug mode is used, DMA pointers are initialized in the 91x lib.c file:

```
#ifdef _DMA
 DMA = (DMA_TypeDef *)DMA_BASE;
#endif /* _DMA */
#ifdef _DMA_Channel0
 DMA_Channel0= (DMA_Channel_TypeDef *)DMA_Channel0_BASE;
#endif /* _DMA_Channel0 */
#ifdef _DMA_Channel1
 DMA_Channel1=
                      (DMA_Channel_TypeDef *)DMA_Channel1_BASE;
#endif /* _DMA_Channel1 */
#ifdef _DMA_Channel2
 DMA_Channel2 =
                      (DMA_Channel_TypeDef *)DMA_Channel2_BASE;
#endif /* _DMA_Channel2 */
#ifdef _DMA_Channel3
 DMA Channel3 =
                      (DMA_Channel_TypeDef *)DMA_Channel3_BASE;
#endif /* _DMA_Channel3 */
#ifdef _DMA_Channel4
DMA_Channel4 =
                     (DMA_Channel_TypeDef *)DMA_Channel4_BASE;
#endif /* _DMA_Channel4 */
#ifdef _DMA_Channel5
DMA_Channel5=
                     (DMA_Channel_TypeDef *)DMA_Channel5_BASE;
#endif /* _DMA_Channel5*/
#ifdef _DMA_Channel6
DMA_Channel6 =
                 (DMA_Channel_TypeDef *)DMA_Channel6_BASE;
#endif /* _DMA_Channel6 */
#ifdef _DMA_Channel7
DMA_Channel7 =
                     (DMA_Channel_TypeDef *)DMA_Channel7_BASE;
#endif /* _DMA_Channel7 */
```

\_DMA\_channel0,\_DMA\_channel1,\_DMA\_channel2, ....\_DMA\_channel7 must be defined, in *91x\_conf.h* file, to access the peripheral registers as follows:

```
#define _DMA #define _DMA_Channel0 #define _DMA_Channel1 #define _DMA_Channel2 #define _DMA_Channel3 #define _DMA_Channel4 #define _DMA_Channel5 #define _DMA_Channel6 #define _DMA_Channel7
```

# 13.2 Firmware library functions

Table 63. DMA library functions

Function name	Description
DMA_DeInit	Initializes the DMA peripheral registers to their default reset values.
DMA_Init	Initializes the DMA Channelx according to the specified parameters in the DMA_InitStruct.
DMA_StructInit	Fills each DMA_InitStruct member with its reset value.
DMA_Cmd	Enables or disables the DMA peripheral.
DMA_ITMaskConfig	Enables or disables the specified DMA Mask interrupt.
DMA_ITConfig	Enables or disables the Terminal count interrupt for specified DMA channelx.
DMA_SRCIncConfig	Enables or disables the source Address incrementing for the specified DMA channelx.
DMA_DESIncConfig	Enables or disables the destination Address incrementing for the specified DMA channelx.
DMA_GetITStatus	Checks the status of the specified interrupt.
DMA_ClearIT	Clears the pending bit of the specified interrupt.
DMA_SyncConfig	Enables or disables the synchronization logic for the corresponding DMA Request Signal.
DMA_GetSReq	Checks for a specific source if it requests a Single transfer or not.
DMA_GetLSReq	Checks for a specific source if it requests a Last Single transfer or not.
DMA_GetBReq	Checks for a specific source if it requests a Burst transfer or not.
DMA_GetLBReq	Checks for a specific source if it requests a Last Burst transfer or not.
DMA_SetSReq	Sets the DMA to generate a Single transfer request for the corresponding DMA Request Source.
DMA_SetLSReq	Sets the DMA to generate a Last Single transfer request for the corresponding DMA Request Source.
DMA_SetBReq	Sets the DMA to generate a Burst transfer request for the corresponding DMA Request Source.
DMA_SetLBReq	Sets the DMA to generate a Last Burst transfer request for the corresponding DMA Request Source.
DMA_ChannelCmd	Enables or disables the specified DMA Channelx
DMA_ChannelHalt	Enables DMA requests or ignore extra source DMA requests for the specified channelx.
DMA_ChannelBuffering	Enables or disables the access Cache ability for the specified channelx.
DMA_ChannelMode	Enables the access in User or Privileged mode for the specified channelx.

Table 63. DMA library functions

Function name	Description
DMA_ChannelLockTrsf	Enables or disables locked transfers.
DMA_ChannelCache	Enables or disables the access Cache ability for the specified channelx.
DMA_GetChannelActiveStatus	Checks if the DMA_Channelx FIFO is empty or not. Returns SET while the corresponding channel FIFO is not empty.
DMA_GetChannelStatus	Checks the status of DMA channelx (Enabled or Disabled)
DMA_LLI_CCR_Init	Returns linked list's control word according to the specified parameters in the LLI_CCR_InitStruct

## 13.2.1 DMA\_Delnit

Function name	DMA_DeInit
Function prototype	<pre>void DMA_DeInit()</pre>
Behavior description	Deinitializes the DMA peripheral registers to their default reset values.
Input parameter	None
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	SCU_AHBPeriphReset()

### Example:

## 13.2.2 **DMA\_Init**

Function name	DMA_Init
Function prototype	<pre>void DMA_Init(DMA_Channel_TypeDef * DMA_Channelx, DMA_InitTypeDef * DMA_InitStruct);</pre>
Behavior description	Initializes the DMA_Channelx according to the specified parameters in the DMA_InitStruct.
Input parameter1	DMA_Channelx: where x can be 0,1,2,3,4,5,6,or 7 to select the DMA Channel.
Input parameter2	DMA_InitStruct: pointer to a $DMA_InitTypeDef$ structure which contains the configuration information for the specified DMA_Channelx. Refer to section " $DMA_InitTypeDef$ : on page 145" for more details.
Output parameter	None
Return parameter	None
Required preconditions	
Called functions	None

### DMA\_InitTypeDef:

The DMA\_InitTypeDef structure is defined in the 91x\_dma.h file:

```
typedef struct
{
u32 DMA_Channel_SrcAdd;
u32 DMA_Channel_DesAdd;
u32 DMA_Channel_LLstItm;
u8 DMA_Channel_DesWidth;
u8 DMA_Channel_SrcWidth;
u8 DMA_Channel_SrcWidth;
u8 DMA_Channel_DesBstSize;
u8 DMA_Channel_TrsfSize;
u16 DMA_Channel_TrsfSize;
u8 DMA_Channel_FlowCntrl;
u8 DMA_Channel_Src;
u8 DMA_Channel_Src;
u8 DMA_Channel_Des;
```

#### DMA Channel SrcAdd

The current source address, (byte-aligned), of the data to be transferred.

#### DMA\_Channel\_DesAdd

The current destination address, (byte-aligned), of the data to be transferred.

## DMA\_Channel\_LLstltm

The word- aligned address for the next Linked List Item.

#### DMA Channel DesWidth

Destination transfer width.

This member can be one of the following values:

DMA_Channel_DesWidth	Value	Meaning
DMA_DesWidth_Byte	0x00000000	Destination Width is one Byte
DMA_DesWidth_HalfWord	0x00200000	Destination Width is one half word
DMA_DesWidth_Word	0x00400000	Destination Width is one Word

#### DMA\_Channel\_SrcWidth

Source transfer width.

This member can be one of the following values:

DMA_Channel_SrcWidth	Value	Meaning
DMA_SrcWidth_Byte	0x00000000	Source width is one Byte
DMA_SrcWidth_HalfWord	0x00040000	Source width is one Half Word
DMA_SrcWidth_Word	0x00080000	Source width is one Word

## DMA\_Channel\_DesBstSize

The destination burst size, which indicates the number of transfers that make up a destination burst transfer request.

This member can be one of the following values:

DMA_Channel_DesBstSize	Value	Meaning
DMA_DesBst_1Data	0x00000000	Destination Burst transfer request is 1 Data (DATA = destination transfer width)
DMA_DesBst_4Data	0x00008000	Destination Burst transfer request is 1 Data
DMA_Bst_8Data	0x00010000	Destination Burst transfer request is 4 Data
DMA_DesBst_16Data	0x00018000	Destination Burst transfer request is 8 Data
DMA_DesBst_32Data	0x00020000	Destination Burst transfer request is 16 Data
DMA_DesBst_64Data	0x00028000	Destination Burst transfer request is 32 Data
DMA_DesBst_128Data	0x00030000	Destination Burst transfer request is 128 Data
DMA_DesBst_256Data	0x00038000	Destination Burst transfer request is 256 Data

#### DMA\_Channel\_SrcBstSize

The source burst size indicates the number of transfers that make up a source burst.

This member can be one of the following values:

DMA_Channel_SrcBstSize	Value	Meaning
DMA_SrcBst_1Data	0x00000000	Source Burst transfer request is 1 Data (DATA = Source transfer width)
DMA_SrcBst_4Data	0x00001000	Source Burst transfer request is 4 Data
DMA_SrcBst_8Data	0x00002000	Source Burst transfer request is 8 Data
DMA_SrcBst_16Data	0x00003000	Source Burst transfer request is 16 Data
DMA_SrcBst_32Data	0x00004000	Source Burst transfer request is 32 Data
DMA_SrcBst_64Data	0x00005000	Source Burst transfer request is 64Data
DMA_SrcBst_128Data	0x00006000	Source Burst transfer request is 128 Data
DMA_SrcBst_256Data	0x00007000	Source Burst transfer request is 256 Data

#### DMA\_Channel\_TrsfSize

Transfer size indicates the size of the transfer when the DMA controller is the flow controller.

#### DMA\_Channel\_FlowCntrl

Flow control and transfer type: This value indicates the flow controller and transfer type. The flow controller can be the DMA, the source peripheral, or the destination peripheral. The transfer type can be memory to-memory, memory-to-peripheral, peripheral-to-memory, or peripheral to-peripheral.

This member can be one of the following values:

DMA_Channel_FlowCntrl	Value	Transfer Type	The flow controller
DMA_FlowCntrlt0_DMA	0x00000000	Memory-to-memory	DMA
DMA_FlowCntrl1_DMA	0x00000800	Memory-to-peripheral	DMA
DMA_FlowCntrl2_DMA	0x00001000	Peripheral-to-memory	DMA
DMA_FlowCntrl3_DMA	0x00001800	Source peripheral-to- destination peripheral	DMA
DMA_FlowCntrl_DestPerip	0x00002000	Source peripheral-to- destination peripheral	Destination peripheral
DMA_FlowCntrl_Perip1	0x00002800	Memory-to-peripheral	peripheral
DMA_FlowCntrl_Perip2	0x00003000	Peripheral-to-memory	peripheral
DMA_FlowCntrl_SrcPerip	0x00003800	Source peripheral-to- destination peripheral	Source peripheral

DMA controller (DMA) UM0233

## DMA\_Channel\_Src

Source peripheral. This value selects the DMA source request peripheral.

This field is ignored if the source of the transfer is from memory.

DMA_Channel_Src	Value	Description
DMA_SRC_USB_RX	0X00	
DMA_SRC_USB_TX	0x02	
DMA_SRC_TIM0	0x04	
DMA_SRC_TIM1	0x06	
DMA_SRC_UART0_RX	0x08	
DMA_SRC_UART0_TX	0x0A	
DMA_SRC_UART1_RX	0x0C	
DMA_SRC_UART1_TX	0x0E	2 out of 3 UARTs have DMA support (UART2 is not
DMA_SRC_External_Req0	0x10	supported by DMA)
DMA_SRC_External_Req1	0x12	
DMA_SRC_I2C0	0x14	
DMA_SRC_I2C1	0x16	
DMA_SRC_SSP0_RX	0x18	
DMA_SRC_SSP0_TX	0x1A	
DMA_SRC_SSP1_RX	0x1C	
DMA_SRC_SSP1_TX	0x1E	

#### DMA\_Channel\_Des

Destination peripheral. This value selects the DMA destination request peripheral. This field is ignored if the destination of the transfer is to memory.

DMA_Channel_Des	Value	Description
DMA_DES_USB_RX	0X00	
DMA_DES_USB_TX	0x40	
DMA_DES_TIM0	0x80	
DMA_DES_TIM1	0xC0	
DMA_DES_UARTO_RX	0x100	
DMA_DES_UARTO_TX	0x140	
DMA_DES_UART1_RX	0x180	
DMA_DES_UART1_TX	0x1C0	2 out of 3 UARTs have DMA support (UART2 is not
DMA_DES_External_Req0	0x200	supported by DMA)
DMA_DES_External_Req1	0x240	
DMA_DES_I2C0	0x280	
DMA_DES_I2C1	0x2C0	
DMA_DES_SSP0_RX	0x300	
DMA_DES_SSP0_TX	0x340	
DMA_DES_SSP1_RX	0x380	
DMA_DES_SSP1_TX	0x3C0	

#### **Example:**

```
/* Initialize the DMA Channel0 according to the DMA_InitStruct members */
DMA_InitTypeDef DMA_InitStruct;
...

DMA_InitStruct.DMA_Channel_SrcAdd= 0x4000000;
DMA_InitStruct.DMA_Channel_DesAdd= 0x4002000;
DMA_InitStruct.DMA_Channel_LLstItm =0;
DMA_InitStruct.DMA_Channel_DesWidth = DMA_Width_HalfWord;
DMA_InitStruct.DMA_Channel_DestBstSize = DMA_DesBst_4Data;
DMA_InitStruct.DMA_Channel_SrcBstSize= DMA_SrcBst_1Data;
DMA_InitStruct.DMA_Channel_TrsfSize = 0x14;
DMA_InitStruct.DMA_Channel_FlowCntrl= DMA_FlowCntrl_DMA;
...
DMA_Init(DMA_Channel0,&DMA_InitStruct);
```

# 13.2.3 DMA\_StructInit

Function name	DMA_StructInit
Function prototype	<pre>void DMA_StructInit(DMA_InitTypeDef* DMA_InitStruct)</pre>
Behavior description	Fills each DMA_InitStruct member with its reset value.
Input parameter	DMA_InitStruct: pointer to a DMA_InitTypeDef structure.
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

## Example:

```
/* define and Initialize a DMA_InitStruct */
DMA_InitTypeDef DMA_InitStruct;
DMA_StructInit(&DMA_InitStruct);
```

# 13.2.4 DMA\_Cmd

Function name	DMA_Cmd
Function prototype	void DMA_Cmd(FunctionalState NewState)
Behavior description	Enables or disables the DMA peripheral.
Input parameter1	NewState: new state of the DMA peripheral. This parameter can be: ENABLE or DISABLE.
Output parameter	None
Return parameter	None
Required preconditions	
Called functions	None

## Example:

```
/* Enable DMA */
...
DMA_Cmd(ENABLE);
...
```

577

# 13.2.5 DMA\_ITMaskConfig

Function name	DMA_ITMaskConfig
Function prototype	void DMA_ITMaskConfig(DMA_Channel_TypeDef * DMA_Channelx, u16 DMA_ITMask, FunctionalState NewState)
Behavior description	Enables or disables the specified DMA Mask interrupt.
Input parameter1	DMA_Channelx: where x can be 0,1,2,3,4,5,6,or 7 to select the DMA Channel.
Input parameter2	DMA_ITMask: specifies the DMA interrupt mask source to be enabled or disabled.  Refer to <i>Table 64: DMA_ITMask parameter values</i> for the allowed values of this parameter.
Input parameter3	NewState: new state of the specified DMA_Channelx mask interrupt. This parameter can be: ENABLE or DISABLE.
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

### Table 64. DMA\_ITMask parameter values

	<u> </u>	
DMA_ITMask	Value	Meaning
DMA_ITMask_IE	0x4000	Interrupt error mask.
DMA_ITMask_ITC	0x8000	Terminal count interrupt mask.
DMA_ITMask_ALL	0xC000	All DMA_Channelx interrupts enable/disable mask

### Example:

```
/* Terminal count interrupt Mask Enable for DMA_Channel2 */
...
DMA_ITMaskConfig(DMA_Channel2, DMA_ITMask_ITC, ENABLE);
...
```

DMA controller (DMA) UM0233

# 13.2.6 DMA\_ChannelSRCIncConfig

Function name	DMA_ChannelSRCIncConfig
Function prototype	<pre>void DMA_ChannelSRCIncConfig (DMA_Channel_TypeDef * DMA_Channelx, FunctionalState NewState);</pre>
Behavior description	Enables or disables the source Address incrementing for the specified DMA channelx.
Input parameter1	DMA_Channelx: where x can be 0,1,2,3,4,5,6,or 7 to select the DMA Channel.
Input parameter2	NewState: new state of the source incrementing feature. This parameter can be: ENABLE or DISABLE.
Output parameter	None
Return parameter	None
Required preconditions	
Called functions	None

#### Example:

```
/* Enable the source incrementation feature for the channel0 */ \dots DMA_ChannelSRCIncConfig (DMA_Channel0, ENABLE);
```

# 13.2.7 DMA\_ChannelDESIncConfig

Function name	DMA_ChannelDESIncConfig
Function prototype	<pre>void DMA_ChannelDESIncConfig (DMA_Channel_TypeDef * DMA_Channelx, FunctionalState NewState);</pre>
Behavior description	Enables or disables the source Address incrementing for the specified DMA channelx.
Input parameter1	DMA_Channelx: where x can be 0,1,2,3,4,5,6,or 7 to select the DMA Channel.
Input parameter2	NewState: new state of the destination incrementing feature. This parameter can be: ENABLE or DISABLE.
Output parameter	None
Return parameter	None
Required preconditions	
Called functions	None

#### Example:

```
/* Enable the destination incrementation feature for the channel0 */ ... \label{eq:DMA_ChannelDESIncConfig} $$(DMA\_Channel0, ENABLE);$$ ... $$
```

# 13.2.8 DMA\_GetChannelActiveStatus

Function name	DMA_GetChannelActiveStatus
Function prototype	FlagStatus DMA_GetChannelActiveStatus(DMA_Channel_TypeDef * DMA_Channelx)
Behavior description	Checks the DMA_Channelx FIFO if it is empty or not. Returns SET while the corresponding channel FIFO is not empty.
Input parameter1	DMA_Channelx: where x can be 0,1,2,3,4,5,6,or 7 to select the DMA Channel.
Output parameter	None
Return parameter	Returned status (SET or RESET).
Required preconditions	None
Called functions	None

## Example:

```
/* check the channel0 FIFO */
...
DMA_GetChannelActiveStatus(DMA_Channel0);
```

# 13.2.9 DMA\_ITConfig

Function name	DMA_ITConfig
Function prototype	<pre>void DMA_ITMaskConfig(DMA_Channel_TypeDef* DMA_Channelx, FunctionalState NewState)</pre>
Behavior description	Enables or disables the specified DMA_Channelx Terminal count.
Input parameter1	DMA_Channelx: where x can be 0,1,2,3,4,5,6,or 7 to select the DMA Channel.
Input parameter2	NewState: new state of the specified DMA_Channelx interrupts. This parameter can be: ENABLE or DISABLE.
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

DMA controller (DMA) UM0233

# 13.2.10 DMA\_GetChannelStatus

Function name	DMA_GetChannelStatus
Function prototype	FlagStatus DMA_GetChannelStatus(u8 ChannelIndx)
Behavior description	Check the status of DMA channelx (Enabled or Disabled)
Input parameter	ChannelIndx: specifies the DMA Channel to be checked.  Refer to section "ChannelIndx on page 154" for more details on the allowed values of this parameter.
Output parameter	None
Return parameter	Returned status (SET or RESET).
Required preconditions	
Called functions	None

## Channelindx

This Parameter is used as index for the channel to be checked (there are eight Channels)

ChannelIndx = Channel0=0

ChannelIndx = Channel1 =1

...

ChannelIndx = Channel7 = 7

# 13.2.11 DMA\_GetITStatus

Function name	DMA_GetITStatus
Function prototype	ITStatus DMA_GetITStatus(u8 ChannelIndx,u8 DMA_ITReq)
Behavior description	Checks the status of Terminal Count and Error interrupts request after and before Masking.
Input parameter1	ChannelIndx: specifies the DMA Channel to be checked.  Refer to section "ChannelIndx on page 154" for more details on the allowed values of this parameter.
Input parameter2	DMA_ITReq: specifies the DMA interrupt request status to be checked. Refer to <i>Table 65: DMA_ITReq parameter values on page 156</i> for the allowed values of this parameter.
Output parameter	None
Return parameter	Returned status (SET or RESET).
Required preconditions	
Called functions	None

## ChannelIndx

This Parameter is used as index for the channel to be checked (there are eight Channels)

ChannelIndx = Channel0 = 0

ChannelIndx = Channel1 = 1

• • •

ChannelIndx = Channel7 = 7

DMA controller (DMA) UM0233

## DMA\_ITReq:

Specifies the DMA interrupt request status to be checked and is coded as index for the register Status containing this interrupt request status.

To check the interrupt status, use a combination of one or more of the following values:

Table 65. DMA\_ITReq parameter values

DMA_ITReq	Value (code)	DMA register status	Meaning
DMA_IS	0x01	DMA_ISR	The status of the interrupts after masking.
DMA_TCS	0x02	DMA_TCISR	The status of the terminal count after masking.
DMA_ES	0x03	DMA_EISR	The status of the error request after masking
DMA_TCRS	0x04	DMA_TCRISR	Indicates if the DMA channel is requesting a transfer complete (terminal count Interrupt) prior to masking or Not.
DMA_ERS	0x05	DMA_ERISR	Indicates if the DMA channel is requesting an Error Interrupt prior to masking or Not.

#### Example:

```
/*Check the status of interrupts after masking on the channel0*/ \dots DMA_GetITStatus(Channel0,DMA_IS);
```

. . .

# 13.2.12 DMA\_ClearIT

Function name	DMA_ClearIT
Function prototype	void DMA_ClearIT(u8 ChannelIndx,u8 DMA_ITClr)
Behavior description	Clears The Interrupt pending bits for terminal count or Error interrupts for a specified DMA Channel.
Input parameter1	ChannelIndx: specifies the DMA Channel. Refer to section "ChannelIndx on page 155" for more details on the allowed values of this parameter.
Input parameter2	DMA_ITCIr: DMA interrupt pending. Refer to <i>Table 66: DMA_ITCIr</i> parameter values on page 157 for the allowed values of this parameter.
Output parameter	None
Return parameter	None
Required preconditions	
Called functions	None

## DMA\_ITCIr:

Specifies the DMA interrupt pending to be cleared and is coded as index for the register containing this interrupt pending bit.

To clear interrupts pending bits, use a combination of one or more of the following values:

Table 66. DMA\_ITCIr parameter values

DMA_ITCIr	Value (code)	DMA register status	Meaning
DMA_TCC	0X01	DMA_TCICR	Clear a Terminal Count Interrupt on the corresponding DMA channel
DMA_EC	0X02	DMA_EICR	Clear an Error Interrupt on the corresponding DMA channel

# 13.2.13 DMA\_SyncConfig

Function name	DMA_SyncConfig
Function prototype	void DMA_SyncConfig(u16 DMA_SrcReq, FunctionalState NewState)
Behavior description	enable or disable synchronization logic for the corresponding DMA Request Signal.
Input parameter1	DMA_SrcReq: specifies the DMA Request Source.  Refer to <i>Table 67: DMA_SrcReq parameter values on page 158</i> for the allowed values of this parameter.
Input parameter2	NewState: new state of the DMA peripheral. This parameter can be: ENABLE or DISABLE.
Output parameter	None
Return parameter	None
Required preconditions	
Called functions	None

Note:

You must use synchronization logic when the peripheral generating the DMA request runs on a different clock to the DMA. For peripherals running on the same clock as the DMA, disabling the synchronization logic improves the DMA request.

Table 67. DMA\_SrcReq parameter values

DMA_SrcReq	Value (code)
DMA_USB_RX_Mask	0x0001
DMA_USB_TX_Mask	0x0002
DMA_TIM0 _Mask	0x0004
DMA_TIM1_Mask	0x0008
DMA_UART0_RX_Mask	0x0010
DMA_UART0_TX_Mask	0x0020
DMA_UART1_RX_Mask	0x0040
DMA_UART1_TX_Mask	0x0080
DMA_External_Req0_Mask	0x0100
DMA_External_Req1_Mask	0x0200
DMA_I2C0_Mask	0x0400
DMA_I2C1_Mask	0x0800
DMA_SSP0_RX_Mask	0x1000
DMA_SSP0_TX_Mask	0x2000
DMA_SSP1_RX_Mask	0x4000
DMA_SSP1_TX_Mask	0x8000

# 13.2.14 DMA\_GetSReq

Function name	DMA_GetSReq
Function prototype	FlagStatus DMA_GetSReq(u16 DMA_SrcReq)
Behavior description	Checks for a specific source if it requests a Single transfer or not.
Input parameter	DMA_SrcReq: specifies the DMA Request Source.  Refer to <i>Table 67: DMA_SrcReq parameter values on page 158</i> for the allowed values of this parameter.
Output parameter	None
Return parameter	Returned status (SET or RESET).
Required preconditions	None
Called functions	None

# 13.2.15 DMA\_GetLSReq

Function name	DMA_GetLSReq
Function prototype	FlagStatus DMA_GetLSReq(u16 DMA_SrcReq)
Behavior description	Checks for a specific source if it requests a last Single transfer.
Input parameter	DMA_SrcReq: specifies the DMA Request Source.  Refer to <i>Table 67: DMA_SrcReq parameter values on page 158</i> for the allowed values of this parameter.
Output parameter	None
Return parameter	Returned status (SET or RESET).
Required preconditions	None
Called functions	None

# 13.2.16 DMA\_GetBReq

Function name	DMA_GetBReq
Function prototype	FlagStatus DMA_GetBReq(u16 DMA_SrcReq)
Behavior description	Checks for a specific source if it requests a Burst transfer.
Input parameter	DMA_SrcReq: specifies the DMA Request Source.  Refer to <i>Table 67: DMA_SrcReq parameter values on page 158</i> for the allowed values of this parameter.
Output parameter	None
Return parameter	Returned status (SET or RESET).
Required preconditions	None
Called functions	None

# 13.2.17 DMA\_GetLBReq

Function name	DMA_GetLBReq
Function prototype	FlagStatus DMA_GetLBReq(u16 DMA_SrcReq)
Behavior description	Checks for a specific source if it requests a Last Burst transfer.
Input parameter	DMA_SrcReq: specifies the DMA Request Source.  Refer to <i>Table 67: DMA_SrcReq parameter values on page 158</i> for the allowed values of this parameter.
Output parameter	None
Return parameter	Returned status (SET or RESET).
Required preconditions	None
Called functions	None

# 13.2.18 DMA\_SetSReq

Function name	DMA_SetSReq
Function prototype	void DMA_SetSReq(u16 DMA_SrcReq)
Behavior description	Sets the DMA to generate a Single transfer request for the corresponding DMA Request Source.
Input parameter	DMA_SrcReq: specifies the DMA Request Source.  Refer to <i>Table 67: DMA_SrcReq parameter values on page 158</i> for the allowed values of this parameter.
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

# 13.2.19 DMA\_SetLSReq

Function name	DMA_SetLSReq
Function prototype	void DMA_SetLSReq(u16 DMA_SrcReq)
Behavior description	Sets the DMA to generate a Last Single transfer request for the corresponding DMA Request Source.
Input parameter	DMA_SrcReq: specifies the DMA Request Source. Refer to <i>Table 67: DMA_SrcReq parameter values on page 158</i> for the allowed values of this parameter.
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

# 13.2.20 DMA\_SetBReq

Function name	DMA_SetBReq
Function prototype	void DMA_SetBReq(u16 DMA_SrcReq)
Behavior description	Sets the DMA to generate a Burst transfer request for the corresponding DMA Request Source.
Input parameter	DMA_SrcReq: specifies the DMA Request Source.  Refer to <i>Table 67: DMA_SrcReq parameter values on page 158</i> for the allowed values of this parameter.
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

# 13.2.21 DMA\_SetLBReq

Function name	DMA_SetLBReq
Function prototype	void DMA_SetLBReq(u16 DMA_SrcReq)
Behavior description	Sets the DMA to generate a Last Burst transfer request for the corresponding DMA Request Source.
Input parameter	DMA_SrcReq: specifies the DMA Request Source.  Refer to <i>Table 67: DMA_SrcReq parameter values on page 158</i> for the allowed values of this parameter.
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

# 13.2.22 DMA\_ChannelCmd

Function name	DMA_ChannelCmd
Function prototype	<pre>void DMA_ChannelCmd (DMA_Channel_TypeDef * DMA_Channelx, FunctionalState NewState)</pre>
Behavior description	Enables or disables the DMA_Channelx.
Input parameter1	DMA_Channelx: where x can be 0,1,2,3,4,5,6,or 7 to select the DMA Channel.
Input parameter2	NewState: new state of the DMA peripheral. This parameter can be: ENABLE or DISABLE.
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

## Example:

/\* Enable DMA\_Channel0 \*/
DMA\_ChannelCmd(DMA\_Channel0,ENABLE);

# 13.2.23 DMA\_ChannelHalt

Function name	DMA_ChannelHalt
Function prototype	void DMA_ChannelHalt (DMA_Channel_TypeDef * DMA_Channelx,FunctionalState NewState)
Behavior description	Enables or disables HALT Mode for the specified DMA_Channelx.
Input parameter1	DMA_Channelx: where x can be 0,1,2,3,4,5,6,or 7 to select the DMA Channel.
Input parameter2	NewState: new state of the DMA peripheral. This parameter can be: ENABLE or DISABLE.
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

#### Example:

/\* Enable Halt Mode for DMA\_Channel0 (ignore extra source DMA requests)\*/
DMA\_ChannelHalt(DMA\_Channel0,ENABLE);

# 13.2.24 DMA\_ChannelBuffering

Function name	DMA_ChannelBuffering
Function prototype	<pre>void DMA_ChannelBuffering (DMA_Channel_TypeDef * DMA_Channelx,FunctionalState NewState)</pre>
Behavior description	Enables or disables the Buffering Feature for the specified DMA_Channelx.
Input parameter1	DMA_Channelx: where x can be 0,1,2,3,4,5,6,or 7 to select the DMA Channel.
Input parameter2	NewState: new state of the DMA peripheral. This parameter can be: ENABLE or DISABLE.
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

#### Example

/\* Buffering feature enabled for the DMA\_Channel0 \*/  $\rm DMA\_ChannelBuffering(DMA\_Channel0,ENABLE);$ 

# 13.2.25 DMA\_ChannelLockTrsf

Function name	DMA_ChannelLockTrsf
Function prototype	void DMA_ChannelLockTrsf(DMA_Channel_TypeDef * DMA_Channelx,FunctionalState NewState)
Behavior description	Enables or disables the Locked Transfers Feature for the specified DMA_Channelx.
Input parameter1	DMA_Channelx: where x can be 0,1,2,3,4,5,6,or 7 to select the DMA Channel.
Input parameter2	NewState: new state of the DMA peripheral. This parameter can be: ENABLE or DISABLE.
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

#### Example:

/\* Enable the locked transfers feature for the DMA\_Channel0 \*/
DMA\_ChannelLockTrsf(DMA\_Channel0,ENABLE);

## 13.2.26 DMA\_ChannelCache

Function name	DMA_ChannelCache
Function prototype	void DMA_ChannelCache(DMA_Channel_TypeDef * DMA_Channelx,FunctionalState NewState)
Behavior description	Enables or disables the cache ability Feature for the specified DMA_Channelx.
Input parameter1	DMA_Channelx: where x can be 0,1,2,3,4,5,6,or 7 to select the DMA Channel.
Input parameter2	NewState: new state of the DMA peripheral. This parameter can be: ENABLE or DISABLE.
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

#### Example:

/\* Enable the cacheability for the DMA\_Channel0 \*/  $\mbox{DMA\_ChannelCache(DMA\_Channel0,ENABLE);}$ 

# 13.2.27 DMA\_ChannelProt0Mode

Function name	DMA_ChannelProt0Mode
Function prototype	<pre>void DMA_ChannelProt0Mode(DMA_Channel_TypeDef * DMA_Channelx,u32 Prot0Mode)</pre>
Behavior description	Sets User or Privileged mode for the specified DMA_Channelx.
Input parameter1	DMA_Channelx: where x can be 0,1,2,3,4,5,6,or 7 to select the DMA Channel.
Input parameter2	Prot0Mode: specifies the Privileged mode Or the User mode
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

## Prot0Mode:

Prot0Mode	Value	Meaning
DMA_PrivilegedMode	0X10000000	
DMA_UserMode	0XEFFFFFF	

# 13.2.28 DMA\_LLI\_CCR\_Init

Function name	DMA_LLI_CCR_Init
Function prototype	u32 DMA_LLI_CCR_Init(LLI_CCR_InitTypeDef * LLI_CCR_InitStruct);
Behavior description	Returns the control word of the linked list according to the specified parameters in the LLI_CCR_InitStruct structure.
Input parameter1	LLI_CCR_InitStruct: Pointer to LLI_CCR_InitTypeDef: on page 166 (Config structure to be loaded in DMA registers).
Output parameter	None
Return parameter	Control word
Required preconditions	
Called functions	None

DMA controller (DMA) UM0233

## LLI\_CCR\_InitTypeDef:

```
The LLI_CCR_InitTypeDef structure is defined in the \it 91x\_dma.h file: typedef struct
```

```
u32 LLI_TrsfSize;
u32 LLI_SrcBstSize;
u32 LLI_DesBstSize;
u32 LLI_SrcWidth;
u32 LLI_DesWidth;
u32 LLI_SrcIncrement;
u32 LLI_PROTO;
u32 LLI_PROT1;
u32 LLI_PROT2;
u32 LLI_PROT2;
u32 LLI_TCInterrupt;
} LLI_CCR_InitTypeDef;
```

#### LLI DesWidth

Destination transfer width.

This member can be one of the following values:

DMA_Channel_DesWidth	Value	Meaning
DMA_DesWidth_Byte	0x00000000	Destination Width is one Byte
DMA_DesWidth_HalfWord	0x00200000	Destination Width is one half word
DMA_DesWidth_Word	0x00400000	Destination Width is one Word

#### LLI\_SrcWidth

Source transfer width.

This member can be one of the following values:

DMA_Channel_SrcWidth	Value	Meaning
DMA_SrcWidth_Byte	0x00000000	Source width is one Byte
DMA_SrcWidth_HalfWord	0x00040000	Source width is one Half Word
DMA_SrcWidth_Word	0x00080000	Source width is one Word

## LLI\_DesBstSize

The destination burst size, which indicates the number of transfers that make up a destination burst transfer request.

This member can be one of the following values:

DMA_Channel_DesBstSize	Value	Meaning
DMA_DesBst_1Data	0x00000000	Destination Burst transfer request is 1 Data (DATA = destination transfer width)
DMA_DesBst_4Data	0x00008000	Destination Burst transfer request is 1 Data
DMA_Bst_8Data	0x00010000	Destination Burst transfer request is 4 Data
DMA_DesBst_16Data	0x00018000	Destination Burst transfer request is 8 Data
DMA_DesBst_32Data	0x00020000	Destination Burst transfer request is 16 Data
DMA_DesBst_64Data	0x00028000	Destination Burst transfer request is 32 Data
DMA_DesBst_128Data	0x00030000	Destination Burst transfer request is 128 Data
DMA_DesBst_256Data	0x00038000	Destination Burst transfer request is 256 Data

#### LLI\_SrcBstSize

The source burst size indicates the number of transfers that make up a source burst.

This member can be one of the following values:

DMA_Channel_SrcBstSize	Value	Meaning
DMA_SrcBst_1Data	0x00000000	Source Burst transfer request is 1 Data (DATA = Source transfer width)
DMA_SrcBst_4Data	0x00001000	Source Burst transfer request is 4 Data
DMA_SrcBst_8Data	0x00002000	Source Burst transfer request is 8 Data
DMA_SrcBst_16Data	0x00003000	Source Burst transfer request is 16 Data
DMA_SrcBst_32Data	0x00004000	Source Burst transfer request is 32 Data
DMA_SrcBst_64Data	0x00005000	Source Burst transfer request is 64Data
DMA_SrcBst_128Data	0x00006000	Source Burst transfer request is 128 Data
DMA_SrcBst_256Data	0x00007000	Source Burst transfer request is 256 Data

#### LLI\_TrsfSize

Transfer size indicates the size of the transfer when the DMA controller is the flow controller.

#### LLI SrcIncrement

Indicates that the source is incremented or not.

#### LLI DesIncrement

Indicates that the destination is incremented or not.

**577** 

#### LLI PROTO

Indicates that the access is cacheable or not.

#### LLI PROT1

Indicates that the access is bufferable or not.

#### LLI PROT2

Indicates that the mode is privileged or user.

#### LLI TCInterrupt

Activate the terminal count interrupt or not.

#### **Example:**

```
/*control word to generate*/
u32 control_word=0;
/* Initialize the DMA Channel0 according to the DMA_InitStruct members */
LLI_InitTypeDef LLI2_InitStructure;
LLI2_CCR_InitStruct.LLI_TrsfSize=10;
LLI2_CCR_InitStruct.LLI_SrcBstSize=DMA_SrcBst_4Data;
LLI2_CCR_InitStruct.LLI_DesBstSize=DMA_DesBst_1Data;
LLI2_CCR_InitStruct.LLI_SrcWidth=DMA_SrcWidth_HalfWord;
LLI2_CCR_InitStruct.LLI_DesWidth=DMA_DesWidth_HalfWord;
LLI2_CCR_InitStruct.LLI_SrcIncrement= DMA_SrcIncrement ;
LLI2_CCR_InitStruct.LLI_DesIncrement=DMA_DesIncrement;
LLI2_CCR_InitStruct.LLI_PROT0=DMA_CacheableAccess;
LLI2_CCR_InitStruct.LLI_PROT1=DMA_NonBufferableAccess;
LLI2_CCR_InitStruct.LLI_PROT2=DMA_UsermodeAccess;
LLI2_CCR_InitStruct.LLI_TCInterrupt=DMA_TCInterrupt;
control_word = DMA_LLI_CCR_Init(&LLI2_CCR_InitStruct);
```

# 14 Synchronous serial peripheral (SSP)

The SSP is a master or slave interface for synchronous serial communication with peripheral devices that have either Motorola SPI, National Semiconductor or Texas Instruments SSI synchronous serial interfaces.

The first section describes the data structure used in the SSP Firmware library. The second one presents the Firmware library functions.

## 14.1 SSP register structure

The SSP register structure SSP\_TypeDef is defined in the 91x\_map.h file as follows:

```
typedef struct
               /* Control Register 1
vu16 CR0;
                                                       * /
 vu16 EMPTY1;
 vu16 CR1;
                /* Control Register 2
 vu16 EMPTY2;
 vu16 DR;
                 /* Data Register
 vu16 EMPTY3;
 vu16 SR;
                /* Status Register
 vu16 EMPTY4;
               /* Clock Prescale Register
 vu16 PR:
 vu16 EMPTY5;
 vul6 IMSCR;
                  /* Interrupt Mask Set or Clear Register */
 vu16 EMPTY6;
                                                         * /
 vu16 RISR;
                 /* Raw Interrupt Status Register
 vu16 EMPTY7;
 vu16 MISR;
                 /* Masked Interrupt Status Register
 vu16 EMPTY8;
 vu16 ICR;
                /* Interrupt Clear Register
                                                        * /
 vu16 EMPTY9;
 vu16 DMACR;
                /* DMA Control Register
                                                         */
 vu16 EMPTY10;
} SSP_TypeDef;
```

Table 68. SSP registers

Register	Description
CR0	SSP Control Logic register 0
CR1	SSP Control Logic register 1
DR	SSP Data register
SR	SSP Status register
PR	SSP Clock Prescaler register
IMSCR	SSP Interrupt Mask Set and Clear register
RISR	SSP Raw Interrupt Status register

**577** 

Table 68. SSP registers

Register	Description
MISR	SSP Masked Interrupt Status register
ICR	SSP Interrupt Status register
DMACR	SSP DMA Control register

The two SSP interfaces are declared in the same file:

```
#ifndef EXT
#Define EXT extern
#endif
(0x00007000) /* Offset of SSP0 */
#define APB_SSP0_OFST
                      (0x00008000) /* Offset of SSP1 */
#define APB_SSP1_OFST
#ifndef Buffered
#define AHBAPB1_BASE
                         (AHB_APB_BRDG1_U)
#else /* Buffered */
#define AHBAPB1_BASE
                         (AHB_APB_BRDG1_B)
/* SSP Base Address definition*/
#define SSP1_BASE
                      (AHBAPB1_BASE + APB_SSP1_OFST)
/* SSP peripheral declaration*/
#ifndef DEBUG
#define SSP0 ((SSP_TypeDef *) SSP0_BASE)
#define SSP1 ((SSP_TypeDef *) SSP1_BASE)
#else
#ifdef _SSP0
EXT SSP_TypeDef
                      *SSP0;
\#endif /* \_SSP0 */
#ifdef _SSP1
EXT SSP_TypeDef
                      *SSP1;
#endif /* _SSP1 */
When debug mode is used, SSP pointers are initialized in 91x_1ib.c file:
#ifdef _SSP0
SSP0 = (SSP_TypeDef *)SSP0_BASE;
#endif /*_SSP0 */
#ifdef _SSP1
SSP1 = (SSP_TypeDef *)SSP1_BASE;
#endif /*_SSP1 */
```

\_SSP, \_SSP0 and \_SSP1 must be defined, in the  $\it 91x\_conf.h$  file, to access the peripheral registers as follows:

```
#define _SSP
#define _SSP0
#define _SSP1
```

# 14.2 Firmware library functions

The following table enumerates the functions of the SSP library.

Table 69. SSP library functions

Function name	Description
SSP_DeInit	Deinitializes the SSPx peripheral registers to their default reset values.
SSP_Init	Initializes the SSPx peripheral according to the specified parameters in the SSP_InitStruct.
SSP_StructInit	Fills each SSP_InitStruct member with its default value.
SSP_Cmd	Enables or disables the specified SSP peripheral.
SSP_ITConfig	Enables or disables the specified SSP interrupts.
SSP_DMACmd	Configures the SSP DMA interface.
SSP_SendData	Transmits a Data through the SSP peripheral.
SSP_ReceiveData	Returns the most recent received data by the SSP peripheral.
SSP_LoopBackConfig	Enables or disables Loop back mode for the selected SSP peripheral.
SSP_GetFlagStatus	Checks whether the specified SSP flag is set or not.
SSP_ClearFlag	Clears the SSPx pending flags.
SSP_GetITStatus	Checks whether the specified SSP interrupt has occurred or not.
SSP_ClearITPendingBit	Clears the SSPx interrupt pending bits.

57

# 14.2.1 SSP\_Delnit

Function name	SSP_DeInit
Function prototype	void SSP_DeInit(SSP_TypeDef* SSPx)
Behavior description	Deinitializes the SSPx peripheral registers to their default reset values.
Input parameter	SSPx: where x can be 0 or 1 to select the SSP peripheral.
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	SCU_APBPeriphReset()

#### **Example:**

```
/* Deinitialize the SSPO peripheral. */
SSP_DeInit(SSPO);
```

## 14.2.2 SSP\_Init

Function name	SSP_Init
Function prototype	<pre>void SSP_Init(SSP_TypeDef* SSPx, SSP_InitTypeDef* SSP_InitStruct)</pre>
Behavior description	Initializes the SSPx peripheral according to the specified parameters in the SSP_InitStruct .
Input parameter1	SSPx: where x can be 0 or 1 to select the SSP peripheral.
Input parameter2	SSP_InitStruct: pointer to a SSP_InitTypeDef structure that contains the configuration information for the specified SSP peripheral. Refer to section "SSP_InitTypeDef on page 172" for more details on the allowed values of this parameter.
Output parameter	None
Return parameter	None
Required preconditions	
Called functions	None

## SSP\_InitTypeDef

The SSP\_InitTypeDef structure is defined in the *91x\_SSP.h* file:

```
typedef struct
{
u16 SSP_FrameFormat ;
u16 SSP_Mode ;
u16 SSP_CPOL ;
u16 SSP_CPHA ;
u16 SSP_DataSize ;
u16 SSP_SlaveOutput ;
u8 SSP_ClockRate ;
u8 SSP_ClockPrescaler ;
} SSP_InitTypeDef;
```

#### SSP\_FrameFormat

Specifies whether the frame format is Motorola SPI or TI synchronous serial or Microwire. This member can be one of the following values:

SSP_FrameFormat	Meaning
SSP_FrameFormat_Motorola	Motorola frame format is selected
SSP_FrameFormat_TI	TI frame format is selected
SSP_FrameFormat_Microwire	Microwire frame format is selected

#### SSP\_Mode

Specifies the SSP operation mode. This member can be one of the following values:

SSP_Mode	Meaning
SSP_Mode_Master	SSP is configured as a master
SSP_Mode_Slave	SSP is configured as a slave

#### SSP\_CPOL

Specifies the steady state value of the serial clock. This member can be one of the following values:

SSP_CPOL	Meaning
SSP_CPOL_Low	Clock is active low
SSP_CPOL_High	Clock is active high

#### SSP\_CPHA

Specifies on which clock transition the bit capture is made. This member can be one of the following values:

SSP_CPHA	Meaning
SSP_CPHA_2Edge	Data is captured on the second edge
SSP_CPHA_1Edge	Data is captured on the first edge

577

#### SSP\_DataSize

Specifies the word length operation of the receive and transmit FIFO. This member can be one of the following values:

SSP_DataSize	Meaning
SSP_DataSize_16b	Data Size is 16 bits
SSP_DataSize_15b	Data Size is 15 bits
SSP_DataSize_14b	Data Size is 14 bits
SSP_DataSize_13b	Data Size is 13 bits
SSP_DataSize_12b	Data Size is 12 bits
SSP_DataSize_11b	Data Size is 11 bits
SSP_DataSize_10b	Data Size is 10 bits
SSP_DataSize_9b	Data Size is 9 bits
SSP_DataSize_8b	Data Size is 8 bits
SSP_DataSize_7b	Data Size is 7 bits
SSP_DataSize_6b	Data Size is 6 bits
SSP_DataSize_5b	Data Size is 5 bits
SSP_DataSize_4b	Data Size is 4 bits

## SSP\_SlaveOutput

Specifies whether the slave output is enabled or disabled. This is used especially in multiple-slave cases. This member can be one of the following values:

SSP_SlaveOutput	Meaning
SSP_SlaveOutput_Enable	Slave output enabled
SSP_SlaveOutput_Disable	Slave output disabled

## SSP\_ClockRate

Specifies the serial clock rate value used to configure the transmit and receive bit rate of SCK. This member must be a value from 2 to 254.

#### SSP ClockPrescaler

Specifies the division factor by which the input PCLK must be divided to be used by the SSP. This member must be an even number between 2 and 254. The least significant bit of the programmed number is hardcoded to zero. If an odd number is written the least significant bit is changed to zero by hardware.

	MOTOROLA Mode		TI Mode		Mirowire Mode	
Members	Master	Slave	Master	Slave	Master	Slave
SSP_FrameFormat	х	х	х	х	х	х
SSP_Mode	х	х	х	х	х	х
SSP_CPOL	х	х				
SSP_CPHA	х	х				
SSP_DataSize	х	х	х	х	х	х
SSP_SlaveOutput		х		х		х
SSP_ClockRate	х	(1)	х	(1)	х	(1)
SSP_ClockPrescaler	х	(1)	х	(1)	х	(1)

(1): the communication clock is derived from the master so no need to set the slave clock

#### Example:

```
/* Initialize the SSP0 according to the SSP_InitStructure members. */
SSP_InitTypeDef SSP_InitStructure;

SSP_InitStructure.SSP_FrameFormat = SSP_FrameFormat_TI;
SSP_InitStructure.SSP_Mode = SSP_Mode_Slave;
SSP_InitStructure.SSP_CPOL = SSP_CPOL_High;
SSP_InitStructure.SSP_CPHA = SSP_CPHA_1Edge;
SSP_InitStructure.SSP_DataSize = SSP_DataSize_8b;
SSP_InitStructure.SSP_SlaveOutput = SSP_SlaveOutput_Enable;
SSP_InitStructure.SSP_ClockRate = 0xB;
SSP_InitStructure.SSP_ClockPrescaler = 12;
SSP_Init(SSP0, &SSP_InitStructure);
```

## 14.2.3 SSP\_StructInit

Function name	SSP_StructInit
Function prototype	void SSP_StructInit(SSP_InitTypeDef* SSP_InitStruct)
Behavior description	Fills each SSP_InitStruct member with its default value, refer to the following table for more details.
Input parameter	SSP_InitStruct: pointer to a SSP_InitTypeDef structure which will be initialized.
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

577

Table 70. SSP\_InitStruct member default values

Member	Default value
SSP_FrameFormat	SSP_FrameFormat_Motorola
SSP_Mode	SSP_Mode_Master
SSP_CPOL	SSP_CPOL_Low
SSP_CPHA	SSP_CPHA_1Edge
SSP_DataSize	SSP_DataSize_8b
SSP_SlaveOutput	SSP_SlaveOutput_Enable
SSP_ClockRate	0
SSP_ClockPrescaler	0

#### Example:

```
/* Initialize a SSP_InitTypeDef structure. */
SSP_InitTypeDef SSP_InitStructure;
SSP_StructInit(&SSP_InitStructure);
```

# 14.2.4 SSP\_Cmd

Function name	SSP_Cmd
Function prototype	void SSP_Cmd(SSP_TypeDef* SSPx, FunctionalState NewState)
Behavior description	Enables or disables the specified SSP peripheral.
Input parameter1	SSPx: where x can be 0 or 1to select the SSP peripheral.
Input parameter2	NewState: new state of the SSPx peripheral. This parameter can be: ENABLE or DISABLE.
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

#### Example:

```
/* Enable the SSP0 peripheral */
SSP_Cmd(SSP0, ENABLE);
```

# 14.2.5 SSP\_ITConfig

Function name	SSP_ITConfig
Function prototype	<pre>void SSP_ITConfig(SSP_TypeDef* SSPx, u16 SSP_IT, FunctionalState NewState)</pre>
Behavior description	Enables or disables the specified SSP interrupts.
Input parameter1	SSPx: where x can be 0 or 1 to select the SSP peripheral.
Input parameter2	SSP_IT: specifies the SSP interrupts sources to be enabled or disabled.  Refer to section "SSP_IT" for more details on the allowed values of this parameter.  You can select more than one interrupt, by ORing them.
Input parameter3	NewState: new state of the specified SSP interrupts. This parameter can be: ENABLE or DISABLE.
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

# SSP\_IT

To enable or disable SSP interrupts, use a combination of one or more of the following values:

Table 71. SSP\_IT parameter values

Value	Meaning
SSP_IT_TxFifo	Transmit FIFO half empty or less condition interrupt
SSP_IT_RxFifo	Receive FIFO half full or less condition interrupt
SSP_IT_RxTimeOut	Receive timeout interrupt
SSP_IT_RxOverrun	Receive overrun interrupt

#### Example:

/\* Enable SSP0 Transmit FIFO and Receive FIFO interrupts. \*/
SSP\_ITConfig(SSP0, SSP\_IT\_TxFifo | SSP\_IT\_RxFifo, ENABLE);

# 14.2.6 SSP\_DMACmd

Function name	SSP_DMACmd
Function prototype	void SSP_DMACmd(SSP_TypeDef* SSPx,u16 SSP_DMAtransfer, FunctionalState NewState)
Behavior description	Configures the SSP DMA interface.
Input parameter1	SSPx: where x can be 0 or 1 to select the SSP peripheral.
Input parameter2	SSP_DMAtransfer: specifies the SSP DMA transfer to be enabled or disabled.  Refer to section "SSP_DMATransfer" for more details on the allowed values of this parameter.  You can select more than one interrupt, by ORing them.
Input parameter3	NewState: new state of SSP0 DMA transfer. This parameter can be: ENABLE or DISABLE.
Output parameter	None
Return parameter	None
Required preconditions	None

## SSP\_DMATransfer

To enable or disable SSP0 DMA transfer, use one of the following values:

Table 72. SSP0\_DMAtransfer parameter values

Value	Meaning
SSP0_DMA_Transmit	Transmit FIFO DMA transfer
SSP0_DMA_Receive	Receive FIFO DMA transfer

#### Example:

/\* Enable SSP0 transmit FIFO DMA transfer. \*/
SSP\_DMACmd(SSP0, SSP\_DMA\_Transmit, ENABLE);

# 14.2.7 SSP\_SendData

Function name	SSP_SendData
Function prototype	void SSP_SendData(SSP_TypeDef* SSPx, u16 Data)
Behavior description	Transmits a Data through the SSP peripheral.
Input parameter1	SSPx: where x can be 0 or 1 to select the SSP peripheral.
Input parameter 2	Data: word to be transmitted.
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

#### Example:

/\* Send 0xA5 through the SSP0 peripheral. \*/ SSP\_SendData(SSP0, 0xA5);

# 14.2.8 SSP\_ReceiveData

Function name	SSP_ReceiveData
Function prototype	u16 SSP_ReceiveData(SSP_TypeDef* SSPx)
Behavior description	Returns the most recent data received by the SSP peripheral.
Input parameter	SSPx: where x can be 0 or 1 to select the SSP peripheral.
Output parameter	None
Return parameter	The value of the received data.
Required preconditions	None
Called functions	None

### Example:

```
/* Read the most recent data received by the SSPO peripheral. */ u16 hReceivedData; hReceivedData = SSP_ReceiveData(SSPO);
```

# 14.2.9 SSP\_LoopBackConfig

Function name	SSP_LoopBackConfig
Function prototype	SSP_LoopBackConfig(SSP_TypeDef* SSPx, FunctionalState NewState)
Behavior description	Enables or disables the Loop back mode for the selected SSP peripheral.
Input parameter1	SSPx: where x can be 0 or 1 to select the SSP peripheral.
Input parameter2	NewState: new state of the Loop back mode. This parameter can be: ENABLE or DISABLE.
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

## Example:

/\* Enable the Loop back mode for the SSP0 peripheral. \*/ SSP\_LoopBackConfig(SSP0, ENABLE);

## 14.2.10 SSP\_GetFlagStatus

Function name	SSP_GetFlagStatus
Function prototype	FlagStatus SSP_GetFlagStatus(SSP_TypeDef* SSPx, u16 SSP_FLAG)
Behavior description	Checks whether the specified SSP flag is set or not.
Input parameter1	SSPx: where x can be 0 or 1 to select the SSP peripheral.
Input parameter2	SSP_FLAG: specifies the flag to check.  Refer to <i>Table 73: SSP_FLAG parameter values</i> for the allowed values of this parameter.
Output parameter	None
Return parameter	The new state of SSP_FLAG (SET or RESET).
Required preconditions	None
Called functions	None

## Table 73. SSP\_FLAG parameter values

SSP_FLAG	Meaning
SSP_FLAG_Busy	Busy flag
SSP_FLAG_RxFifoFull	Receive FIFO full flag
SSP_FLAG_RxFifoNotEmpty	Receive FIFO not empty flag
SSP_FLAG_TxFifoNotFull	Transmit FIFO not full flag
SSP_FLAG_TxFifoEmpty	Transmit FIFO empty flag
SSP_FLAG_TxFifo	Transmit FIFO Masked interrupt flag
SSP_FLAG_RxFifo	Receive FIFO Masked interrupt flag
SSP_FLAG_RxTimeOut	Receive timeout Masked interrupt flag
SSP_FLAG_RxOverrun	Receive overrun Masked interrupt flag

#### Example:

```
/* Get the Receive FIFO full flag status */
FlagStatus Status;
Status = SSP_GetFlagStatus(SSPO, SSP_FLAG_RxFifoFull);
```

## 14.2.11 SSP\_ClearFlag

Function name	SSP_ClearFlag
Function prototype	void SSP_ClearFlag(SSP_TypeDef* SSPx, u16 SSP_FLAG)
Behavior description	Clears the SSPx pending flags.
Input parameter1	SSPx: where x can be 0 or 1 to select the SSP peripheral.
Input parameter 2	SSP_FLAG: specifies the flag to clear.  Refer to <i>Table 74: SSP_FLAG parameter values</i> " for the allowed values of this parameter.
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

To clear the SSP flags, use one of the following values:

Table 74. SSP\_FLAG parameter values

SSP_FLAG	Meaning
SSP_FLAG_RxTimeOut	Receive timeout flag
SSP_FLAG_RxOverrun	Receive overrun flag

### Example:

/\* Clear the SSPO Receive timeout flag \*/
SSP\_ClearFlag(SSPO, SSP\_FLAG\_RxTimeOut);

## 14.2.12 SSP\_GetITStatus

Function name	SSP_GetITStatus
Function prototype	ITStatus SSP_GetITStatus(SSP_TypeDef* SSPx, u16 SSP_IT)
Behavior description	Checks whether the specified SSP interrupt has occurred or not.
Input parameter1	SSPx: where x can be 0 or 1 to select the SSP peripheral.
Input parameter2	SSP_IT: specifies the interrupt source to check.  Refer to <i>Table 75: SSP_IT parameter values</i> " for the allowed values of this parameter.
Output parameter	None
Return parameter	The new state of SSP_IT (SET or RESET).
Required preconditions	None
Called functions	None

#### Example:

```
/* Get the SSP0 Receive FIFO interrupt status */
ITStatus Status;
Status = SSP_GetITStatus(SSP0, SSP_IT_RxFifo);
```

## 14.2.13 SSP\_ClearITPendingBit

Function name	SSP_ClearITPendingBit
Function prototype	void SSP_ClearITPendingBit(SSP_TypeDef* SSPx, u16 SSP_IT)
Behavior description	Clears the SSPx's interrupt pending bits.
Input parameter1	SSPx: where x can be 0 or 1 to select the SSP peripheral.
Input parameter 2	SSP_IT: specifies the interrupt pending bit to clear. More than one interrupt can be cleared using the "I" operator.  Refer to <i>Table 75: SSP_IT parameter values</i> " for the allowed values of this parameter.
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

## SSP\_IT

To clear the SSP interrupt pending bits, use a combination of one or more of the following values:

Table 75. SSP\_IT parameter values

Value	Meaning
SSP_IT_RxTimeOut	Receive timeout interrupt
SSP_IT_RxOverrun	Receive overrun interrupt

#### Example:

/\* Clear the SSPO Receive timeout interrupt pending bit \*/
SSP\_ClearITPendingBit(SSPO, SSP\_IT\_RxTimeOut);

## 15 Universal asynchronous receiver transmitter (UART)

The UART interface provides hardware management of the CTS and RTS signals and has Full Modem interface (on UART0 only). It also supports IrDA mode that reduces the signal for IrDA by 3/16.

To optimize the data transfer between the processor and the peripheral, the UART has two FIFOs (receive/transmit) of 16 bytes each. The UART can be served by the DMA controller.

The first section describes the data structures used in the UART Firmware library. The second one presents the Firmware library functions.

## 15.1 UART register structure

The UART register structure *UART\_TypeDef* is defined in the *91x\_map.h* file as follows:

```
typedef struct
vu16 DR;
 vu16 EMPTY1;
  vu16 RSECR;
 vu16 EMPTY2[9];
  vu16 FR;
  vu16 EMPTY3[3]:
  vu16 ILPR;
  vul6 EMPTY4:
  vu16 IBRD;
  vu16 EMPTY5;
  vu16 FBRD;
  vul6 EMPTY6;
  vu16 LCR;
  vu16 EMPTY7;
  vu16 CR;
  vul6 EMPTY8;
  vu16 IFLS;
  vul6 EMPTY9;
  vul6 IMSC;
  vul6 EMPTY10;
  vu16 RIS;
  vu16 EMPTY11;
  vu16 MIS;
  vu16 EMPTY12;
  vul6 ICR;
  vu16 EMPTY13;
 vu16 DMACR;
  vu16 EMPTY14
} UART_TypeDef;
```

Table 76. UART registers

Register	Description
DR	Data Register
RSECR	Receive Status Register
FR	Flag Register
ILPR	IrDA Low-Power Counter Register
IBRD	Integer Baud Rate Divider Register
FBRD	Fractional Baud Rate Divider Register
LCR	Line Control Register
CR	Control Register
IFLS	Interrupt FIFO Level Select
IMSC	Interrupt Mask Set/Clear Register
RIS	Raw Interrupt Status
MIS	Masked Interrupt Status
ICR	Interrupt Clear Register
DMACR	DMA Control Register

#### The 3 UART interfaces are declared in the same file:

```
#ifndef EXT
#Define EXT extern
#endif
#define AHB_APB_BRDG1_U (0x5C000000) /* AHB/APB Bridge 1 UnBuffered Space */
\verb|#define AHB_APB_BRDG1_B| (0x4C000000) /* AHB/APB Bridge 1 Buffered Space */
                            (0x00004000) /* Offset of UARTO */
#define APB_UART0_OFST
#define APB_UART1_OFST
                           (0x00005000) /* Offset of UART1 */
#define APB_UART2_OFST
                          (0x00006000) /* Offset of UART2 */
#ifndef Buffered
#define AHBAPB1_BASE
                             (AHB_APB_BRDG1_U)
#else /* Buffered */
#define AHBAPB1_BASE
                             (AHB_APB_BRDG1_B)
/* UART Base Address definition*/
#define UARTO_BASE (AHBAPB1_BASE + APB_UARTO_OFST)
#define UART1_BASE
                          (AHBAPB1_BASE + APB_UART1_OFST)
#define UART2_BASE
                           (AHBAPB1_BASE + APB_UART2_OFST)
/* UART peripheral declaration*/
#ifndef DEBUG
```

```
#define UART0 ((UART_TypeDef *) UART0_BASE)
#define UART1 ((UART_TypeDef *) UART1_BASE)
#define UART2 ((UART_TypeDef *) UART2_BASE)
#else
#ifdef _UART0
EXT UART_TypeDef
                          *UART0;
#endif /* _UARTO */
#ifdef _UART1
EXT UART_TypeDef
                          *UART1;
#endif /* _UART1 */
#ifdef _UART2
                          *UART2;
EXT UART_TypeDef
#endif /* _UART2*/
```

### When debug mode is used, UART pointers are initialized in 91x\_lib.c file:

```
#ifdef _UART0
UART0 = (UART_TypeDef *)UART0_BASE;
#endif /*_UART0 */

#ifdef _UART1
UART1 = (UART_TypeDef *)UART1_BASE;
#endif /*_UART1 */

#ifdef _UART2
UART2 = (UART_TypeDef *)UART2_BASE;
#endif /*_UART2 */
```

# \_UART, \_UART0, \_UART1 and \_UART2 must be defined, in *91x\_conf.h* file, to access the peripheral registers as follows:

```
#define _UART
#define _UART0
#define _UART1
#define _UART2
```

# 15.2 Firmware library functions

Table 77. UART library functions

Function name	Description
UART_Delnit	Deinitializes the UARTx peripheral registers to their default reset values.
UART_Init	Initializes the UARTx peripheral according to the specified parameters in the UART_InitStruct.
UART_StructInit	Fills each UART_InitStruct member with its default value.
UART_Cmd	Enables or disables the specified UART peripheral.
UART_ITConfig	Enables or disables the specified UART interrupts.
UART_DMAConfig	Configures the UARTx DMA interface.
UART_DMACmd	Enables or disables the UARTx DMA interface.
UART_LoopBackConfig	Enables or disables the UARTx LoopBack mode.
UART_IrDALowPowerConfig	Sets the IrDA low power mode
UART_IrDASetCounter	Sets the IrDA counter divisor value in low power mode.
UART_IrDACmd	Enables or disables the UARTx IrDA interface
UART_SendData	Transmits a Byte of data through the UARTx peripheral.
UART_ReceiveData	Returns the most recent byte received by the UARTx peripheral.
UART_SendBreak	Transmits break characters.
UART_RTSConfig	Sets or resets the RTS signal (for UART0 only).
UART_DTRConfig	Sets or resets the DTR signal (for UART0 only).
UART_GetFlagStatus	Checks whether the specified UART flag is set or not.
UART_ClearFlag	Clears the UARTx pending flags.
UART_GetITStatus	Checks whether the specified UART interrupt has occurred or not.
UART_ClearITPendingBit	Clears the UARTx interrupt pending bits.

## 15.2.1 UART\_Delnit

Function name	UART_DeInit
Function prototype	void UART_DeInit(UART_TypeDef* UARTx)
Behavior description	Deinitializes the UARTx peripheral registers to their default reset values.
Input parameter	UARTx: where x can be 0,1 or 2 to select the UART peripheral.
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	SCU_APBPeriphReset()

#### **Example:**

/\* Deinitializes the UARTO registers to their default reset value \*/  ${\tt UART\_DeInit(UARTO)}\:;$ 

## 15.2.2 **UART\_Init**

Function name	UART_Init
Function prototype	void UART_Init(UART_TypeDef* UARTx, UART_InitTypeDef* UART_InitStruct)
Behavior description	Initializes the UARTx peripheral according to the specified parameters in the UART_InitStruct .
Input parameter1	UARTx: where x can be 0, 1 or 2 to select the UART peripheral.
Input parameter2	UART_InitStruct: pointer to a UART_InitTypeDef structure that contains the configuration information for the specified UART peripheral. Refer to section "UART_InitTypeDef" for more details on the allowed values of this parameter.
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

## UART\_InitTypeDef

The UART\_InitTypeDef structure is defined in the **91x\_uart.h** file:

```
typedef struct
{
  u16 UART_WordLength;
  u16 UART_StopBits;
  u16 UART_Parity;
  u32 UART_BaudRate;
  u16 UART_HardwareFlowControl;
  u16 UART_Mode;
  u16 UART_FIFO;
  UART_FIFOLEVEL UART_TXFIFOLEVEL;
  UART_FIFOLEVEL UART_RXFIFOLEVEL;
}UART_InitTypeDef;
```

### UART\_WordLength

Indicates the number of data bits transmitted or received in a frame.

This member can be one of the following values:

UART_WordLength	Meaning
UART_WordLength_5D	5 bits Data
UART_WordLength_6D	6 bits Data
UART_WordLength_7D	7 bits Data
UART_WordLength_8D	8 bits Data

### UART\_StopBits

Specifies the number of transmitted stop bits. This member can be one of the following values:

UART_StopBits	Meaning
UART_StopBits_1	One stop bit is transmitted at the end of frame
UART_StopBits_2	Tow stop bits are transmitted at the end of frame

### UART\_Parity

Specifies the parity mode. This member can be one of the following values:

UART_Parity	Meaning
UART_Parity_No	Parity Disable
UART_Parity_Even	Even Parity
UART_Parity_Odd	Odd Parity
UART_Parity_OddStick	1 is transmitted as bit parity
UART_Parity_EvenStick	0 is transmitted as bit parity

### UART\_BaudRate

Specifies the baudrate of the UART communication. The baudrate is computed with this formula :

IntegerDivider = ((APBClock) / (16 \* (UART\_InitStruct->UART\_BaudRate)))

FractionalDivider = ((IntegerDivider - ((u32) IntegerDivider)) \* 64 + 0.5)

#### UART\_HardFlowControl

Specifies whether hardware flow control mode is enabled or disabled.

This member can be one of the following values:

UART_HardFlowControl	Meaning
UART_HardwareFlowControl_None	HFC Disable
UART_HardwareFlowControl_RTS	RTS Enable
UART_HardwareFlowControl_CTS	CTS Enable
UART_HardwareFlowControl_RTS_CTS	CTS and RTS Enable

## UART\_Mode

Specifies whether receive and/or transmit mode is enabled or disabled.

This member can be a combination of one or more of the following values:

UART_Transmit	Meaning
UART_Mode_Rx	Receive Enable
UART_Mode_Tx	Transmit Enable
UART_Mode_Tx_Rx	Transmit and Receive Enable

## **UART\_FIFO**

Specifies whether the FIFOs (Rx and Tx FIFOs) are enabled or disabled.

This member can be one of the following values:

UART_Transmit	Meaning
UART_FIFO_Enable	FIFOs Enable
UART_FIFO_Disable	FIFOs Disable

### UART\_TxFIFOLevel

Specifies the level of the UART TxFIFO (not used when FIFOs are disabled).

This member can be one of the following values:

UART_TxFIFOLevel	Meaning
UART_FIFOLevel_1_8	FIFO becomes >= 1/8 full
UART_FIFOLevel_1_4	FIFO becomes >= 1/4 full
UART_FIFOLevel_1_2	FIFO becomes >= 1/2 full
UART_FIFOLevel_3_4	FIFO becomes >= 3/4 full
UART_FIFOLevel_7_8	FIFO becomes >= 7/8 full

### UART\_RxFIFOLevel

Specifies the level of the UART RxFIFO (not used when FIFOs are disabled).

This member can be one of the following values:

UART_RxFIFOLevel	Meaning
UART_FIFOLevel_1_8	FIFO becomes >= 1/8 full
UART_FIFOLevel_1_4	FIFO becomes >= 1/4 full
UART_FIFOLevel_1_2	FIFO becomes >= 1/2 full
UART_FIFOLevel_3_4	FIFO becomes >= 3/4 full
UART_FIFOLevel_7_8	FIFO becomes >= 7/8 full

#### Example:

```
/* The following example illustrates how to configure the UARTO */
    UART_InitTypeDef UART_InitStructure;

UART_InitStructure.UART_WordLength = UART_WordLength_8D;
    UART_InitStructure.UART_StopBits = UART_StopBits_1;
    UART_InitStructure.UART_Parity = UART_Parity_Odd;
    UART_InitStructure.UART_BaudRate = 9600;
    UART_InitStructure.UART_HardwareFlowControl = UART_HardwareFlowControl_RTS_CTS;
    UART_InitStructure.UART_Mode = UART_Mode_Tx_Rx;
    UART_InitStructure.UART_FIFO = UART_FIFO_Enable;
    UART_InitStructure.UART_TxFIFOLevel = UART_FIFOLevel_1_2;
    UART_InitStructure.UART_RxFIFOLevel = UART_FIFOLevel_1_2;
    UART_Init(UARTO, &UART_InitStructure);
```

#### **UART\_StructInit** 15.2.3

Function name	UART_StructInit
Function prototype	void UART_StructInit(UART_InitTypeDef* UART_InitStruct)
Behavior description	Fills each UART_InitStruct member with its default value, refer to the following table for more details.
Input parameter	UART_InitStruct: pointer to a UART_InitTypeDef structure which will be initialized.
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

#### **UART\_InitStruct** member default values Table 78.

Member	Default value
UART_WordLength	UART_WordLength_8D
UART_StopBits	UART_StopBits_1
UART_Parity	UART_Parity_Odd
UART_BaudRate	9600
UART_HardwareFlowControl	UART_HardwareFlowControl_None
UART_Mode	UART_Mode_Tx_Rx
UART_FIFO	UART_FIFO_Enable
UART_TxFIFOLevel	UART_FIFOLevel_1_2
UART_RxFIFOLevel	UART_FIFOLevel_1_2

### Example:

```
UART_InitTypeDef UART_InitStructure;
UART_StructInit(&UART_InitStructure);
```

## 15.2.4 **UART\_Cmd**

Function name	UART_Cmd	
Function prototype	void UART_Cmd(UART_TypeDef* UARTx, FunctionalState NewState)	
Behavior description	Enables or disables the specified UART peripheral.	
Input parameter1	UARTx: where x can be 0,1 or 2 to select the UART peripheral.	
Input parameter2	NewState: new state of the UARTx peripheral. This parameter can be: ENABLE or DISABLE.	
Output parameter	None	
Return parameter	None	
Required preconditions	None	
Called functions	None	

## Example:

/\* Enable the UARTO \*/
UART\_Cmd(UARTO, ENABLE);

## 15.2.5 **UART\_ITConfig**

Function name	UART_ITConfig	
Function prototype	void UART_ITConfig(UART_TypeDef* UARTx, u16 UART_IT, FunctionalState NewState)	
Behavior description	Enables or disables the specified UART interrupts.	
Input parameter1	UARTx: where x can be 0,1 or 2 to select the UART peripheral.	
Input parameter2	UART_IT: specifies the UART interrupts sources to be enabled or disabled.  Refer to <i>Table 79: UART_IT parameter values on page 194</i> " for the allowed values of this parameter.	
Input parameter3	NewState: new state of the specified UARTx interrupts. This parameter can be: ENABLE or DISABLE.	
Output parameter	None	
Return parameter	None	
Required preconditions	None	
Called functions	None	

## UART\_IT

To enable or disable UART interrupts, use a combination of one or more of the following values:

Table 79. UART\_IT parameter values

UART_IT	Meaning
UART_IT_OverrunError	Overrun Error interrupt mask
UART_IT_BreakError	Break Error interrupt mask
UART_IT_ParityError	Parity Error interrupt mask
UART_IT_FrameError	Frame Error interrupt mask
UART_IT_ReceiveTimeOut	Receive Time Out interrupt mask
UART_IT_Transmit	Transmit interrupt mask
UART_IT_Receive	Receive interrupt mask
UART_IT_DSR	DSR interrupt mask
UART_IT_DSD	DSD interrupt mask
UART_IT_CTS	CTS interrupt mask
UART_IT_RI	RI interrupt mask

## Example:

/\* Enables the UARTO transmit and receive interrupts \*/
UART\_ITConfig(UARTO, UART\_IT\_Transmit | UART\_IT\_Receive, ENABLE);

## 15.2.6 UART\_DMAConfig

Function name	UART_DMAConfig
Function prototype	void UART_DMAConfig(UART_TypeDef* UARTx, u16 UART_DMAOnError)
Behavior description	Configures the UARTx DMA interface.
Input parameter1	UARTx: where x can be 1 or 2 to select the UART peripheral.
Input parameter2	UART0_DMAOnError: specifies the DMA on error request.  Refer to <i>Table 80: UART_DMAOnError parameter values on page 195</i> for the allowed values of this parameter.
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

### UART\_DMAOnError

To select whether the DMA is enabled/disabled when an error ocurrs, use one of the following values:

Table 80. UART\_DMAOnError parameter values

Value	Meaning
UART_DMAOnError_Enable	DMA receive request enabled when the UART error interrupt is asserted.
UART_DMAOnError_Disable	DMA receive request disabled when the UART error interrupt is asserted.

#### Example:

/\* DMA configuration \*/
UART\_DMAConfig(UART1, UART\_DMAOnError\_Enable);

## 15.2.7 UART\_DMACmd

Function name	UART_DMACmd
Function prototype	void UART_DMACmd(UART_TypeDef* UARTx, u8 UART_DMAReq, FunctionalState NewState)
Behavior description	Enables or disables the UARTx's DMA interface.
Input parameter1	UARTx: where x can be 1 or 2 to select the UART peripheral.
Input parameter2	UART_DMAReq: specifies the DMA request.  Refer to <i>Table 81: UART_DMAReq parameter values</i> for the allowed values of this parameter.
Input parameter3	NewState: new state of the UARTx's DMA request. This parameter can be: ENABLE or DISABLE.
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

To select the DMA request to be enabled/disabled, use one of the following values:

Table 81. UART DMAReg parameter values

Value	Meaning
UART_DMAReq_Tx	Transmit DMA request
UART_DMAReq_Rx	Receive DMA request

## Example:

/\* Enable the DMA transfer on Rx action \*/
 UART\_DMACmd(UART1, ENABLE);

## 15.2.8 UART\_LoopBackConfig

Function name	UART_LoopBackConfig
Function prototype	void UART_LoopBackConfig(UART_TypeDef* UARTx, FunctionalState NewState)
Behavior description	Enables or disables the UARTx's LoopBack mode.
Input parameter1	UARTx: where x can be 0,1 or 2 to select the UART peripheral.
Input parameter2	NewState: new state of the UARTx's LoopBack mode. This parameter can be: ENABLE or DISABLE.
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

### Example:

/\* ENABLE the UART1 LoopBack mode \*/
UART\_LoopBackConfig(UART1, ENABLE);

## 15.2.9 UART\_IrDALowPowerConfig

Function name	UART_IrDALowPowerConfig
Function prototype	void UART_IrDALowPowerConfig(u8 IrDAx, FunctionalState NewState)
Behavior description	Sets the IrDA low power mode.
Input parameter1	IrDAx: where x can be 0,1 or 2 to select the IrDA.
Input parameter2	NewState: new state of the UARTx's IrDA interface. This parameter can be: ENABLE or DISABLE.
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

#### Example:

```
/* Enable IrDAO in low power*/
UART_IrDALowPowerConfig(IrDAO, ENABLE);
```

## 15.2.10 UART\_IrDACmd

Function name	UART_IrDACmd
Function prototype	void UART_IrDACmd(u8 IrDAx, FunctionalState NewState)
Behavior description	Enables or disables the IrDAx interface.
Input parameter1	IrDAx: where x can be 0, 1 or 2 to select the IrDA
Input parameter2	NewState: new state of the IrDAx's interface. This parameter can be: ENABLE or DISABLE.
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

## Example:

/\* Enable the IrDAO interface \*/
UART\_IrDACmd(IrDAO, ENABLE);

## 15.2.11 UART\_IrDASetCounter

Function name	UART_IrDASetCounter
Function prototype	void UART_IrDASetCounter(u8 IrDAx, u32 IrDA_Counter)
Behavior description	Sets the IrDA counter divisor value in low power mode.
Input parameter1	IrDAx: where x can be 0, 1 or 2 to select the IrDA
Input parameter2	IrDA_Counter:sets the IrDA counter divisor value(Hz).
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

#### Example:

/\* Sets IrDA0 counter \*/
UART\_IrDASetCounter(IrDA0, 1420000);

## 15.2.12 UART\_SendData

Function name	UART_SendData
Function prototype	void UART_SendData(UART_TypeDef* UARTx, u8 Data)
Behavior description	Transmits a byte of data through the UARTx peripheral.
Input parameter1	UARTx: where x can be 0,1 or 2 to select the UART peripheral.
Input parameter2	Data: the byte to transmit.
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

#### Example:

/\* Send one byte on UART1 \*/
UART\_SendData(UART1,0x22);

## 15.2.13 UART\_ReceiveData

Function name	UART_ReceiveData
Function prototype	vu8 UART_ReceiveData(UART_TypeDef* UARTx)
Behavior description	Returns the most recent byte received by the UARTx peripheral.
Input parameter	UARTx: where x can be 0,1 or 2 to select the UART peripheral.
Output parameter	None
Return parameter	The received data.
Required preconditions	None
Called functions	None

### Example:

```
/* Receive one byte on UART2 */
u8 RxData;
RxData = UART_ReceiveData(UART2);
```

## 15.2.14 UART\_SendBreak

Function name	UART_SendBreak
Function prototype	void UART_SendBreak(UART_TypeDef* UARTx)
Behavior description	Transmits break characters.
Input parameter	UARTx: where x can be 0,1 or 2 to select the UART peripheral.
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

### Example:

/\* Send break character on UART1 \*/
UART\_SendBreak(UART1);

## 15.2.15 UART\_RTSConfig

Function name	UART_RTSConfig
Function prototype	void UART_RTSConfig(UART_LevelTypeDef LevelState)
Behavior description	Sets or resets the RTS signal (for UART0 only).
Input parameter2	LevelState: new state of the RTS signal. This parameter can be: LowLevel or HighLevel.
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

### Example:

/\* Set the UARTO RTS signal \*/
UART\_RTSConfig(HighLevel);

## 15.2.16 UART\_DTRConfig

Function name	UART_DTRConfig	
Function prototype	void UART_RTSConfig(UART_LevelTypeDef LevelState)	
Behavior description	Sets or resets the DTR signal (for UART0 Only).	
Input parameter2	LevelState: new state of the DTR signal. This parameter can be: LowLevel or HighLevel.	
Output parameter	None	
Return parameter	None	
Required preconditions	None	
Called functions	None	

## Example:

/\* Set the UARTO DTR signal \*/
UART\_DTRConfig(HighLevel);

## 15.2.17 UART\_GetFlagStatus

Function name	UART_GetFlagStatus	
Function prototype	FlagStatus UART_GetFlagStatus(UART_TypeDef* UARTx, u16 UART_FLAG)	
Behavior description	Checks whether the specified UART flag is set or not.	
Input parameter1	UARTx: where x can be 0,1 or 2 to select the UART peripheral.	
Input parameter2	UART_FLAG: specifies the flag to check. Refer to <i>Table 82: UART_FLAG parameter values</i> " for the allowed values of this parameter.	
Output parameter	None	
Return parameter	The new state of UART_FLAG (SET or RESET).	
Required preconditions	None	
Called functions	None	

## Table 82. UART\_FLAG parameter values

Value	Meaning
UART_FLAG_OverrunError	Overrun error flag
UART_FLAG_Break	Break error flag
UART_FLAG_ParityError	Parity error flag
UART_FLAG_FrameError	Frame error flag
UART_FLAG_RI	Ring indicator flag
UART_FLAG_TxFIFOEmpty	Transmit FIFO Empty flag
UART_FLAG_RxFIFOFull	Receive FIFO Full flag
UART_FLAG_TxFIFOFull	Transmit FIFO Full flag

Table 82.

Value Meaning UART\_FLAG\_RxFIFOEmpty Receive FIFO Empty flag UART\_FLAG\_Busy Busy flag

**UART\_FLAG** parameter values (continued)

#### UART\_FLAG\_DCD DCD flag UART\_FLAG\_DSR DSR flag UART\_FLAG\_CTS CTS flag UART\_RawIT\_OverrunError Overrun Error interrupt flag UART\_RawIT\_BreakError Break Error interrupt flag UART\_RawIT\_ParityError Parity Error interrupt flag UART\_RawIT\_FrameError Frame Error interrupt flag UART\_RawIT\_ReceiveTimeOut ReceiveTimeOut interrupt flag UART\_RawIT\_Transmit Transmit interrupt flag UART\_RawIT\_Receive Receive interrupt flag UART\_RawIT\_DSR DSR interrupt flag UART\_RawIT\_DCD DCD interrupt flag UART\_RawIT\_CTS CTS interrupt flag UART\_RawIT\_RI RI interrupt flag

#### Example:

```
/\,^{\star} Check if the transmit FIFO is full or not ^{\star}/\,
FlagStatus Status;
Status = UART_GetFlagStatus(UART0, UART_TxFIF0Full);
```

#### 15.2.18 **UART\_ClearFlag**

Function name	UART_ClearFlag	
Function prototype	void UART_ClearFlag(UART_TypeDef* UARTx)	
Behavior description	Clears the UARTx pending flags.	
Input parameter1	UARTx: where x can be 0, 1or 2 to select the UART peripheral.	
Output parameter	None	
Return parameter	None	
Required preconditions	None	
Called functions	None	

#### Example:

```
/* Clear flag */
UART_ClearFlag(UART0);
```

## 15.2.19 UART\_GetITStatus

Function name	UART_GetITStatus	
Function prototype	ITStatus UART_GetITStatus(UART_TypeDef* UARTx, u16 UART_IT)	
Behavior description	Checks whether the specified UART interrupt has occurred or not.	
Input parameter1	UARTx: where x can be 0,1 or 2 to select the UART peripheral.	
Input parameter2	UART_IT: specifies the interrupt source to check. Refer to section "UART_IT on page 194" for more details on the allowed values of this parameter.	
Output parameter	None	
Return parameter	The new state of UART_IT (SET or RESET).	
Required preconditions	None	
Called functions	None	

#### Example:

```
/* Get the UARTO Overrun Error interrupt status */
ITStatus OverrunITStatus;
OverrunITStatus = UART_GetITStatus(UARTO, UART_IT_OverrunError);
```

## 15.2.20 UART\_ClearITPendingBit

Function name	UART_ClearITPendingBit
Function prototype	void UART_ClearITPendingBit(UART_TypeDef* UARTx, u16 UART_IT)
Behavior description	Clears the UARTx interrupt pending bits.
Input parameter1	UARTx: where x can be 0,1or 2 to select the UART peripheral.
Input parameter2	UART_IT: specifies the interrupt pending bit to clear. More than one interrupt can be cleared using the "I" operator.  Refer to section "UART_IT on page 194" for more details on the allowed values of this parameter.
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

## Example:

```
/* Clear the Overrun error interrupt pending bit */
UART_ClearITPendingBit(UARTO,UART_IT_OverrunError);
```

# 16 I<sup>2</sup>C interface module (I2C)

The I<sup>2</sup>C Bus interface module serves as interface between the microcontroller and the serial I<sup>2</sup>C bus. It provides both multi-master and slave functions, and controls all I<sup>2</sup>C bus-specific sequencing, protocol, arbitration and timing.

## 16.1 I<sup>2</sup>C register structure

The I<sup>2</sup>C register structure I2C\_TypeDef is defined in the **91x\_map.h** file as follows:

```
typedef struct
vu8 CR;
                        /* Control Register
                                                           * /
u8 EMPTY1[3];
vu8 SR1;
                        /* Status Register 1
                                                           * /
u8 EMPTY2[3];
vu8 SR2;
                        /* Status Register 2
u8 EMPTY3[3];
vu8 CCR;
                        /* Clock Control Register
u8 EMPTY4[3];
vu8 OAR1;
                        /* Own Address Register 1
u8 EMPTY5[3];
vu8 OAR2;
                        /* Own Address Register 2
u8 EMPTY6[3];
vu8 DR;
                        /* Data Register
u8 EMPTY7[3];
vu8 ECCR;
                        /* Extended Clock Control Register */
u8 EMPTY8[3];
} I2C_TypeDef;
```

#### Table 83. I2C registers

Register	Description
I2C_CR	Used to configure I <sup>2</sup> C mode operation
I2C_SR1	Used to check the I <sup>2</sup> C bus status
I2C_SR2	Used to check the I <sup>2</sup> C bus status
I2C_CCR	I <sup>2</sup> C clock control register
I2C_OAR1	Used to define the I <sup>2</sup> C bus address of the bus
I2C_OAR2	Used to define the $I^2C$ bus address of the bus (Bit 8 and 9) , and specify $I^2C$ bus setup/hold time
I2C_DR	This register contains the byte to be received or transmitted on the bus
I2C_ECCR	Specify the upper 5 bits of the 11-bit clock divider

#### The two I<sup>2</sup>C interfaces are declared in the same file:

```
#ifndef EXT
#Define EXT extern
#endif
#define AHB_APB_BRDG1_U (0x5C000000) /* AHB/APB Bridge 1 UnBuffered Space */
#define AHB_APB_BRDG1_B (0x4C000000) /* AHB/APB Bridge 1 Buffered Space */
                      (0x00007000) /* Offset of I2CO */
#define APB_I2C0_OFST
#define APB_I2C1_OFST
                        (0x00008000) /* Offset of I2C1 */
#ifndef Buffered
#define AHBAPB1_BASE
                            (AHB_APB_BRDG1_U)
#else /* Buffered */
#define AHBAPB1_BASE
                           (AHB_APB_BRDG1_B)
/* I2C Base Address definition*/
#define I2C0_BASE
                       (AHBAPB1_BASE + APB_I2C0_OFST)
#define I2C1_BASE
                        (AHBAPB1_BASE + APB_I2C1_OFST)
/* I2C peripheral declaration*/
#ifndef DEBUG
. . .
#else
EXT I2C_TypeDef
                      *I2C0;
EXT I2C_TypeDef
                       *I2C1;
#endif
```

## When debug mode is used, I<sup>2</sup>C pointers are initialized in *91x\_lib.c* file:

```
#ifdef _I2C0
I2C0 = (I2C_TypeDef *)I2C0_BASE;
#endif /*_I2C0 */
#ifdef _I2C1
I2C1 = (I2C_TypeDef *)I2C1_BASE;
#endif /*_I2C1 */
_I2C, _I2C0 and _I2C1 must be defined, in $91x_conf.h$ file, to access the peripheral registers as follows:
#define _I2C
#define _I2C0
#define _I2C0
```

# 16.2 Firmware library functions

Table 84. I2C library functions

Function name	Description
I2C_DeInit	Deinitializes the I2Cx peripheral registers to their default reset values.
I2C_Init	Initializes the I2Cx peripheral according to the specified parameters in the I2C_InitStruct.
I2C_StructInit	Fills each I2C_InitStruct member with its reset value.
I2C_Cmd	Enables or disables the I <sup>2</sup> C peripheral.
I2C_GenerateSTART	Generates I <sup>2</sup> C communication START condition.
I2C_GenerateSTOP	Generates I <sup>2</sup> C communication STOP condition.
I2C_AcknowledgeConfig	Enables or disables I <sup>2</sup> C acknowledge feature.
I2C_ITConfig	Enables or disables I <sup>2</sup> C interrupt.
I2C_ReadRegister	Reads any I <sup>2</sup> C register and return its value.
I2C_GetFlagStatus	Checks whether a I <sup>2</sup> C flag is set or not. The tested flag is passed as parameter of the function.
I2C_ClearFlag	Clears the specified I <sup>2</sup> C flag passed as parameter.
I2C_Send7bitAddress	Transmits the address byte to select the slave device.
I2C_SendData	Sends a data byte.
I2C_ReceiveData	Reads the received byte.
I2C_GetLastEvent	Gets the last I <sup>2</sup> C event that has occurred.
I2C_CheckEvent	Checks if the last occured event is equal to the one passed as parameter.

## 16.2.1 I2C\_Delnit

Function name	I2C_DeInit
Function prototype	void I2C_DeInit(I2C_TypeDef* I2Cx)
Behavior description	Resets all I <sup>2</sup> C registers to their default values.
Input parameter	I <sup>2</sup> Cx: where x can be 0,1, to select the I <sup>2</sup> C peripheral.
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	SCU_APBPeriphReset()

### Example:

```
/* Deinitialize the I2CO peripheral */
I2C_DeInit (I2CO);
```

**A**7/

## 16.2.2 I2C\_Init

Function name	I2C_Init	
Function prototype	<pre>void I2C_Init(I2C_TypeDef* I2Cx, I2C_InitTypeDef* I2C_InitStruct)</pre>	
Behavior description	Configures the selected I <sup>2</sup> C according to the choosen mode by writing the corresponding value to the I <sup>2</sup> C registers.	
Input parameter1	I2Cx: where x can be 0,1 to select the I <sup>2</sup> C peripheral to configure.	
Input parameter2	I2C_InitStruct: pointer to a I2C_InitTypeDef structure that contains the configuration information for the specified I <sup>2</sup> C peripheral. Refer to section "I2C_InitTypeDef on page 206" for more details on the allowed values of this parameter.	
Output parameter	None	
Return parameter	None	
Required preconditions	None	
Called functions	None	

## I2C\_InitTypeDef

The I2C\_InitTypeDef structure is defined in the **91x\_i2c.h** file:

```
typedef struct
typedef struct
{
   u32 I2C_CLKSpeed;
   u16 I2C_OwnAddress;
   u8 I2C_GeneralCall;
   u8 I2C_Ack;
}I2C_InitTypeDef;
```

## I2C\_Ack

Enable/Disable the I<sup>2</sup>C acknowledgement feature.

I2C_Ack	Meaning
I2C_Ack_Enable	Enable the Acknowledgement featue
I2C_Ack_Disable	Disable the Acknowledgement feature

## I2C\_OwnAddress

Select the device own address. It can be a 7-bit or 10-bit address.

## I2C\_GeneralCall

Enables/disables the General call feature. This member can be one of the following values:

I2C_GeneralCall	Meaning
I2C_GeneralCall_Enable	Enable the General call feature
I2C_GeneralCall_Disable	Disable the General call feature

### I2C\_CIkSpeed

Select the clock speed frequency, value must be under 400000

#### Example

```
/* Initialize the I2C peripheral according to the I2C_InitStructure members */
I2C_InitTypeDef I2C_InitStructure;

I2C_InitStructure.I2C_OwnAddress = 0xA8;
I2C_InitStructure.I2C_CLKSpeed = 100000;
I2C_InitStructure.I2C_GeneralCall = I2C_GeneralCall_Disable ;
I2C_InitStructure.I2C_Ack = I2C_Ack_Enable;
I2C_Init(&I2C_InitStructure);
```

## 16.2.3 I2C\_StructInit

Function name	I2C_StructInit
Function prototype	void I2C_StructInit(I2C_InitTypeDef* I2C_InitStruct)
Behavior description	Fills each I2C_InitStruct member with its reset value.
Input parameter	I2C_InitStruct: pointer to a I2C_InitTypeDef structure which will be initialized.
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

#### Table 85. I2C\_InitStruct member default values

Member	Default value	
I2C_CLKSpeed	5000	
I2C_OwnAddress	0	
I2C_GeneralCall	I2C_GeneralCall_Disable	
I2C_Ack	I2C_Ack_Disable	

### **Example:**

```
/* Initialize a I2C_InitTypeDef structure */
I2C_InitTypeDef I2C_InitStructure;
I2C_StructInit(&I2C_InitStructure);"
```

## 16.2.4 I2C\_Cmd

Function name	I2C_Cmd	
Function prototype	void I2C_Cmd(I2C_TypeDef* I2Cx, FunctionalState NewState)	
Behavior description	Enables or disables the I <sup>2</sup> C peripheral.	
Input parameter1	I2Cx: where x can be 0,1, to select the I <sup>2</sup> C peripheral.	
Input parameter2	NewState: new state of the I2Cx peripheral. This parameter can be: ENABLE or DISABLE.	
Output parameter	None	
Return parameter	None	
Required preconditions	None	
Called functions	None	

### **Example:**

```
/* To enable I2C0 */
I2C_Cmd (I2C0, ENABLE);
/* To disable I2C1 */
I2C_Cmd (I2C1, DISABLE);
```

## 16.2.5 I2C\_GenerateSTART

Function name	I2C_GenerateSTART	
Function prototype	void I2C_GenerateStart(I2C_TypeDef* I2Cx, FunctionalState NewState)	
Behavior description	Enables or disables the I <sup>2</sup> C start generation.	
Input parameter1	I2Cx: where x can be 0,1 to select the PPP peripheral.	
Input parameter2	NewState: specifies whether the start generation is Enabled or Disbaled. This parameter can be ENABLE or DISABLE	
Output parameter	None	
Return parameter	None	
Required preconditions	The specified I <sup>2</sup> C peripheral must be enabled	
Called functions	None	

## Example:

```
/*To enable the start generation for the I2C0*/
I2C_GenerateSTART (I2C0, ENABLE)
/*To disable the start generation for the I2C1*/
I2C_GenerateSTART (I2C1, DISABLE)
```

## 16.2.6 I2C\_GenerateSTOP

Function name	I2C_GenerateSTOP	
Function prototype	void I2C_GenerateSTOP(I2C_TypeDef* I2Cx, FunctionalState NewState)	
Behavior description	Enables or disables the STOP condition generation	
Input parameter 1	I2Cx : specifies the I <sup>2</sup> C to be configured	
Input parameter 2	NewState: specifies whether the stop generation is Enabled or Disbaled. This parameter can be ENABLE or DISABLE	
Output parameter	STOP bit in the I2C_CR is modified according to the NewState parameter	
Return parameter	None	
Required preconditions	The specified I <sup>2</sup> C peripheral must be enabled	
Called functions	None	

#### Example:

```
/*To enable the STOP condition generation for the I2C0*/
I2C_GenerateSTOP (I2C0, ENABLE);
/*To disable the STOP condition generation for the I2C1 /
I2C_GenerateSTOP (I2C1, DISABLE);
```

## 16.2.7 I2C\_AcknowledgeConfig

Function name	I2C_AcknowledgeConfig
Function prototype	<pre>void I2C_AcknowledgeConfig(I2c_TypeDef *I2Cx, FunctionalState NewState)</pre>
Behavior description	Enables or disables the I <sup>2</sup> C acknowlegement
Input parameter 1	I2Cx: specifies the I <sup>2</sup> C to be configured
Input parameter 2	NewState: specifies whether the acknowledgement is enabled or disabled. This parameter can be ENABLE or DISABLE
Output parameter	None
Return parameter	None
Required preconditions	The specified I <sup>2</sup> C peripheral must be enabled
Called functions	None

### Example:

```
/*To enable the acknowledgement feature for the I2C0*/
I2C_AcknowledgeConfig (I2C0, ENABLE);
/*To disable the acknowledgement feature for the I2C1*/
I2C_AcknowledgeConfig (I2C1, DISABLE);
```

## 16.2.8 I2C\_ITConfig

Function name	I2C_ITConfig	
Function prototype	<pre>void I2C_ITConfig(I2C_TypeDef *I2Cx, FunctionalState NewState)</pre>	
Behavior description	Enables or disables I <sup>2</sup> C interrupt feature	
Input parameter1	I2Cx: where x can be 0,1to select the I2C peripheral.	
Input parameter2	NewState: specifies whether the I2C interrupt is enabled or disabled. This parameter can be ENABLE or DISABLE	
Output parameter	ITE bit in the I2C_CR is modified according to condition parameter	
Return parameter	None	
Required preconditions	The specified I <sup>2</sup> C peripheral must be enabled	
Called functions	None	

## Example:

```
/*To enable the interrupt feature for the I2C0*/
I2C_ITConfig (I2C0, Enable);
/*To disable the interrupt feature for the I2C1*
I2C_ITConfig (I2C1, Enable);
```

## 16.2.9 I2C\_ReadRegister

Function name	I2C_ReadRegister	
Function prototype	u8 I2C_ReadRegister(I2C_TypeDef* I2Cx, u8 I2C_Register)	
Behavior description	Reads any I <sup>2</sup> C register and returns its value.	
Input parameter1	I2Cx: where x can be 0,1to select the I <sup>2</sup> C peripheral.	
Input parameter2	I2C_Register: specifies the register to be read.  Refer to <i>Table 86: I2C_Register parameter values on page 211</i> for the allowed values of this parameter.	
Output parameter	Access to register to be read	
Return parameter	None	
Required preconditions		
Called functions	None	

### Example:

```
/*Read the I2C_CR Register*/
u8 RegisterValue;
RegisterValue = I2C_RegisterRead (I2C0, I2C_CR);
```

Table 86. I<sup>2</sup>C\_Register parameter values

I <sup>2</sup> C registers	Meaning
I2C_CR	I2C_CR selected for read
I2C_SR1	I2C_SR1 selected for read
I2C_SR2	I2C_SR2 selected for read
I2C_CCR	I2C_CCR selected for read
I2C_OAR1	I2C_OAR1 selected for read
I2C_OAR2	I2C_OAR2 selected for read
I2C_DR	I2C_DR selected for read
I2C_ECCR	I2C_ECCR selected for read

## 16.2.10 I2C\_GetFlagStatus

Function name	I2C_GetFlagStatus	
Function prototype	Flagstatus I2C_GetFlagStatus(I2C_TypeDef* I2Cx, u16 I2C_FLAG)	
Behavior description	Checks whether the I2C flag is set or not.	
Input parameter 1	I2Cx: where x can be 0,1 to select the I <sup>2</sup> C peripheral.	
Input parameter 2	I2C_Flag: specifies the flag to check Refer to <i>Table 87: I2C_Flag parameter value</i> for the allowed values of this parameter.	
Output parameter	Access to register containing the flag to be checked.	
Return parameter	FlagStatus: the status of the specified I2C_Flag. It can be either: SET: if the tested flag is set RESET: if the tested flag is reset	
Required preconditions	None	
Called functions	None	

### Example:

/\*Get the I2C\_FLAG\_AF status \*/
FlagStatus Status;
Status = I2C\_GetFlagStatus (I2C0, I2C\_FLAG\_AF);

Table 87. I2C\_Flag parameter value

I2C_FLAG	Meaning
I2C_FLAG_SB	Start (Master mode) flag
I2C_FLAG_M_SL	Master/Slave flag
I2C_FLAG_ADSL	Address matched (Slave mode) flag
I2C_FLAG_BTF	Byte transfer finished flag
I2C_FLAG_BUSY	Bus busy flag
I2C_FLAG_TRA	Transmitter/Receiver flag
I2C_FLAG_ADD10	10-bit addressing in master mode flag
I2C_FLAG_EVF	Event flag
I2C_FLAG_GCAL	General call (slave mode) flag
I2C_FLAG_BERR	Bus error flag
I2C_FLAG_ARLO	Arbitration lost flag
I2C_FLAG_STOPF	Stop detection (slave mode) flag
I2C_FLAG_AF	Acknowledge failure flag
I2C_FLAG_ENDAD	End of address transmission flag
I2C_FLAG_ACK	Acknowledge enabled flag

## 16.2.11 I2C\_ClearFlag

Function name	I2C_ClearFlag	
Function prototype	void I2C_ClearFlag(I2C_TypeDef* I2Cx, u16 I2C_FLAG,)	
Behavior description	Clears the I <sup>2</sup> C pending flags.	
Input parameter1	I2Cx: where x can be 0,1 to select the I <sup>2</sup> C peripheral.	
Input parameter2	I2C_Flag: specifies the flag to be cleared. Refer to <i>Table 87: I2C_Flag parameter value on page 212</i> for the allowed values of this parameter.	
Input parameter3	Parameter needed in cases where a write to a register is needed to clear the flag.	
Output parameter	Some flags may be cleared when the register is read.	
Return parameter	None	
Required preconditions	None	
Called functions	I2C_Cmd	

## Example:

/\*Clears I2C\_FLAG\_STOPF flag \*/
I2C\_ClearFlag(I2C0, I2C\_FLAG\_STOPF);

## 16.2.12 I2C\_Send7bitAddress

Function name	I2C_Send7bitAddress	
Function prototype	void I2C_Send7bitAddress(I2C_TypeDef* I2Cx, u8 Address, u8 Direction)	
Behavior description	Transmits the address byte to select the slave device.	
Input parameter1	I2Cx: where x can be 0,1 to select the I <sup>2</sup> C peripheral.	
Input parameter2	Address: specifies the slave address which will be transmitted	
Input parameter3	Direction: specifies whether the I <sup>2</sup> C device will be a Transmitter or a Receiver. This parameter could be:  I2C_MODE_TRANSMITTER: Transmitter mode.  I2C_MODE_RECEIVER: Receiver mode.	
Output parameter	None	
Return parameter	None	
Required preconditions	None	
Called functions	None	

#### Example:

 $/\star$  Send from I2C0, as transmitter, the Slave device address 0xA8 in 7-bit addressing mode  $\star/$ 

I2C\_Send7bitAddress(I2C0, 0xA8, I2C\_MODE\_TRANSMITTER);

## 16.2.13 I2C\_SendData

Function name	I2C_SendData	
Function prototype	void I2C_SendData(I2C_TypeDef* I2Cx, u8 bData)	
Behavior description	Transmits a single byte	
Input parameter1	I2Cx: where x can be 0,1 to select the I <sup>2</sup> C peripheral.	
Input parameter2	bData: indicates the data to be transmitted (1 byte)	
Output parameter	I2C_DR register value will be modified	
Return parameter	None	
Required preconditions	None	
Called functions	None	

### Example:

/\*Transmits the byte 0xAF through the I2C1\*/
I2C\_SendData (I2C1, 0xAF);

## 16.2.14 I2C\_ReceiveData

Function name	I2C_ReceiveData	
Function prototype	u8 I2C_ReceiveData(I2C_TypeDef* I2Cx)	
Behavior description	Returns the most recent received byte	
Input parameter1	I2Cx: where x can be 0,1 to select the I <sup>2</sup> C peripheral.	
Output parameter	None	
Return parameter	I2C_DR register Value	
Required preconditions	None	
Called functions	None	

### Example:

```
/* I2C0 Receives a single byte */
u8 bByteReceived;
bByteReceived = I2C_ReceiveData(I2C0);
```

## 16.2.15 I2C\_GetLastEvent

Function name	I2C_GetLastEvent	
Function prototype	u16 I2C_GetLastEvent(I2C_TypeDef* I2Cx)	
Behavior description	Gets the last occurred I <sup>2</sup> C event.	
Input parameter1	I2Cx: where x can be 0,1 to select the I <sup>2</sup> C peripheral.	
Output parameter	None	
Return parameter	The last occurred event.	
Required preconditions	None	
Called functions	None	

### Example:

```
/*Get the I2C0 peripheral status*/
u16 LastEvent;
LastEvent=I2C_GetLastEvent (I2C0);
```

## 16.2.16 I2C\_CheckEvent

Function name	I2C_CheckEvent	
Function prototype	ErrorStatus I2C_CheckEvent(I2C_TypeDef* I2Cx, u16 I2C_Event	
Behavior description	Checks whether the last I <sup>2</sup> C event is equal to the one passed as parameter	
Input parameter1	I2Cx: where x can be 0,1 to select the I <sup>2</sup> C peripheral	
Input parameter2	I2C_EVENT: specifies the event to be checked. Refer to <i>Table 88:</i> I2C_EVENT parameter values for the allowed values of this parameter.	
Output parameter	None	
Return parameter	An ErrorStatus enumeration value: SUCCESS: Last event is equal to the I2C_Event ERROR: Last event is different from the I2C_Event	
Required preconditions	None	
Called functions	I2C_GetLastEvent()	

### Example:

/\*Checks if the last event is equal to I2C\_EVENT\_MASTER\_BYTE\_RECEIVED\*/ I2C\_CheckEvent (I2C0, I2C\_EVENT\_MASTER\_BYTE\_RECEIVED)

Table 88. I2C\_EVENT parameter values

Values	Meaning
I2C_EVENT_SLAVE_ADDRESS_MATCHED	EV1
I2C_EVENT_SLAVE_BYTE_RECEIVED	EV2
I2C_EVENT_SLAVE_BYTE_TRANSMITTED	EV3
I2C_EVENT_SLAVE_STOP_DETECTED	EV4
I2C_EVENT_MASTER_MODE_SELECT	EV5
I2C_EVENT_MASTER_MODE_SELECTED	EV6
I2C_EVENT_MASTER_BYTE_RECEIVED	EV7
I2C_EVENT_MASTER_BYTE_TRANSMITTED	EV8
I2C_EVENT_MASTER_MODE_ADDRESS10	EV9
I2C_EV31	EV3-1
I2C_EVENT_SLAVE_ACK_FAILURE	

# 17 3-phase induction motor controller (MC)

The MC controller is designed for variable speed motor control applications. Three PWM outputs are available for controlling a three-phase motor drive. Rotor speed feedback is provided by capturing a tachogenerator input signal.

The first section describes the data structures used in the MC Firmware library. The second one presents the Firmware library functions.

## 17.1 MC register structure

The MC register structure MC\_TypeDef is defined in the 91x\_map.h file as follows:

```
typedef struct
vul6 TCPT;
u16 EMPTY1;
vu16 TCMP;
u16 EMPTY2;
vu16 IPR;
u16 EMPTY3;
vul6 TPRS;
u16 EMPTY4;
vul6 CPRS;
u16 EMPTY5;
vu16 REP;
u16 EMPTY6;
vu16 CMPW;
u16 EMPTY7;
vul6 CMPV;
u16 EMPTY8;
vu16 CPMU;
u16 EMPTY9;
vul6 CMP0;
u16 EMPTY10;
vul6 PCR0;
u16 EMPTY11;
vul6 PCR1;
u16 EMPTY12;
vu16 PCR2;
u16 EMPTY13;
vu16 PSR;
u16 EMPTY14;
vu16 OPR;
u16 EMPTY15;
vu16 IMR;
u16 EMPTY16:
vu16 DTG;
u16 EMPTY17;
vul6 ESC;
u16 EMPTY18;
vu16 ECR;
vu16 EMPTY19;
vul6 LOK;
vu16 EMPTY20;
} MC_TypeDef;
```

Table 89. MC registers

Register	Description	
TCPT	Tacho capture register	
TCMP	Tacho compare register	
IPR	Interrupt pending register	
TPRS	Tacho prescaler register	
CPRS	PWM counter prescaler register	
REP	Repetition counter register	
CMPW	Compare phase W preload register	
CMPV	Compare phase V preload register	
СМРИ	Compare phase U preload register	
CMP0	Compare 0 preload register	
PCR0	Peripheral control register 0	
PCR1	Peripheral control register 1	
PCR2	Peripheral control register 2	
PSR	Polarity selection register	
OPR	Output peripheral register	
IMR	Interrupt mask register	
DTG	Dead time generator register	
ESC	Emergency stop clear register	
ECR	Enhanced control register	
LOK	Lock register	

### The MC is declared in the file below

```
#ifndef EXT
#Define EXT extern
#endif
#define AHB_APB_BRDG1_U (0x5C000000) /* AHB/APB Bridge 1 UnBuffered Space */
#define AHB_APB_BRDG1_B (0x4C000000) /* AHB/APB Bridge 1 Buffered Space */
#define APB_MC_OFST
                      (0x00003000) /* Offset of MC */
#ifndef Buffered
#define AHBAPB1_BASE
                             (AHB_APB_BRDG1_U)
#else /* Buffered */
#define AHBAPB1_BASE
                             (AHB_APB_BRDG1_B)
/* MC Base Address definition*/
#define MC_BASE
                       (AHBAPB1_BASE + APB_MC_OFST)
/* MC peripheral declaration*/
```

When debug mode is used, the MC pointer is initialized in the *91x\_lib.c* file:

```
#ifdef _MC
   MC = (MC_TypeDef *)MC_BASE
#endif /* _MC */
```

\_MC must be defined, in  $91x\_conf.h$  file, to access the peripheral registers as follows:  $\#define \_MC$ 

# 17.2 Firmware library functions

Table 90. MC library functions

Function name	Description
MC_DeInit	Deinitializes the MC peripheral registers to their default reset values.
MC_Init	Initializes the MC peripheral according to the specified parameters in the MC_InitStruct.
MC_StructInit	Fills each MC_InitStruct member with its default value.
MC_Cmd	Enables or disables the MC peripheral.
MC_ClearPWMCounter	Clears the MC PWM Counter.
MC_ClearTachoCounter	Clears the MC Tacho Counter.
MC_CtrlPWMOutputs	Enables or disables MC peripheral Main Outputs.
MC_ITConfig	Enables or disables the MC interrupts.
MC_SetPrescaler	Sets the MC PWM prescaler value.
MC_SetPeriod	Sets the MC period value.
MC_SetPulseU	Sets the PWM pulse U value.
MC_SetPulseV	Sets the PWM pulse V value.
MC_SetPulseW	Sets the PWM pulse W value.
MC_SetTachoCompare	Sets the MC Tacho compare value.
MC_PWMModeConfig	Selects the MC PWM Counter Mode.
MC_SetDeadTime	Sets the MC dead time value.
MC_EmergencyCmd	Enables or disables the MC emergency feature.
MC_EmergencyClear	Clears the MC emergency register.
MC_GetPeriod	Gets the MC period value.
MC_GetPulseU	Gets the MC pulse U value.
MC_GetPulseV	Gets the MC pulse V value.
MC_GetPulseW	Gets the MC pulse W value.
MC_GetTachoCapture	Gets the MC Tacho capture value.
MC_ClearOnTachoCapture	Enables or disables the Clear on Capture of Tacho counter.
MC_ForceDataTransfer	Sets the MC outputs default states.
MC_SoftwarePreloadConfig	Enables the software data transfer.
MC_SoftwareTachoCapture	Enables the software Tacho capture.
MC_GetCountingStatus	Checks whether the PWM counter is counting UP or DOWN.
MC_GetFlagStatus	Checks whether the specified MC flag is set or not.
MC_ClearFlag	Clears the MC pending flags.
MC_GetITStatus	Checks whether the specified MC interrupt is occurred or not.
MC_ClearITPendingBit	Clears the MC interrupt pending bits.

Table 90. MC library functions (continued)

Function name	Description
MC_Lock	Enables the lock of control register bits.
MC_CounterModeConfig	Selects the 10-bits mode for the dead time counter and/or selects the 16-bits mode for the PWM counter.
MC_DoubleUpdateMode	Enables or disables the Double Update Mode for the MC.
MC_ADCTrigger	Enables or disables the Triggers to the ADC conversion.
MC_EnhancedStop	Enables or disables the Enhanced Motor Stop feature.
MC_DebugOutputProtection	Allows the output phases to follow the polarity set by PSR if enabled or they remain in their last known state if disabled.
MC_EmergencyStopPolarity	Enables or disables the Enhanced Stop Polarity feature.

# 17.2.1 MC\_Delnit

Function name	MC_DeInit
Function prototype	void MC_DeInit(void)
Behavior description	Deinitializes the MC peripheral registers to their default reset values.
Input parameter	None
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	SCU_APBPeriphReset()

## **Example:**

 $/^{\star}$  Deinitializes the MC registers to their default reset value  $^{\star}/$  MC\_DeInit ();

## 17.2.2 MC\_Init

Function name	MC_Init
Function prototype	void MC_Init(MC_InitTypeDef* MC_InitStruct)
Behavior description	Initializes the MC peripheral according to the specified parameters in the MC_InitStruct.
Input parameter	MC_InitStruct: pointer to a MC_InitTypeDef structure that contains the configuration information for the MC peripheral. Refer to section ": MC_InitTypeDef on page 222" for more details on the allowed values of this parameter.
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

## MC\_InitTypeDef

The MC\_InitTypeDef structure is defined in the **91x\_mc.h** file:

```
typedef struct
u16 MC_OperatingMode;
u16 MC_TachoMode;
u16 MC_TachoEventMode;
u8 MC_Prescaler;
u16 MC_TachoPrescaler;
u16 MC_PWMMode;
u16 MC_Complementary;
u8 MC_ForcedPWMState;
u16 MC_Emergency;
u16 MC_Period;
u8 MC_TachoPeriod;
u16 MC_Channel;
u16 MC_PulseU;
u16 MC_PulseV;
u16 MC_PulseW;
u16 MC_PolarityUL;
u16 MC_PolarityUH;
u16 MC_PolarityVL;
u16 MC_PolarityVH;
u16 MC_PolarityWL;
u16 MC_PolarityWH;
u16 MC_TachoPolarity;
u16 MC_DeadTime;
u8 MC_RepetitionCounter;
} MC_InitTypeDef;
```

## MC\_OperatingMode

Specifies the MC operating mode. This member can be one of the following values:

MC_Mode	Meaning
MC_HardwareOperating_Mode	Hardware operating Mode
MC_SoftwareOperating_Mode	Software operating Mode

## MC\_TachoMode

Specifies the MC Tacho mode. This member can be one of the following values:

MC_TachoMode	Meaning
MC_TachoOneShot_Mode	One Shot Tacho Mode
MC_TachoContinuous_Mode	Continuous Tacho Mode

#### MC\_TachoEventMode

Specifies the MC Tacho mode. This member can be one of the following values:

MC_TachoEventMode	Meaning
MC_TachoEvent_Hardware_Mode	Tacho Hardware event Mode
MC_TachoEvent_Software_Mode	Tacho Software event Mode

### MC\_Prescaler

Specifies the Prescaler value to divide the MC Input clock. The clock of the PWM Counter is divided by MC\_Prescaler + 1.

This member must be a number between 0x00 and 0xFF.

### MC\_TachoPrescaler

Specifies the Prescaler value to divide the Tacho Input clock. The clock of the Tacho Counter is divided by MC\_TachoPrescaler + 1.

This member must be a number between 0x000 and 0xFFF.

### MC\_PWMMode

Specifies the MC PWM mode. This member can be one of the following values:

MC_PWMMode	Meaning
MC_PWMClassical_Mode	Classical PWM Mode
MC_PWMZeroCenterd_Mode	Zero Centered Mode

## **MC\_Complementary**

Enables or disables the complementary MC feature. This member can be one of the following values:

MC_Complementary	Meaning
MC_Complementary_Enable	MC Complementary Mode Enable.
MC_Complementary_Disable	MC Complementary Mode Disable.

## MC\_ForcedPWMState

Specifies the default PWM signal states. This member can be one of the following values:

MC_ForcedPWMState	Meaning
MC_Polarity_Inverted	PWM signal polarity inverted
MC_Polarity_NonInverted	PWM signal polarity non-inverted

### MC\_Emergency

Enables or disables the Emergency MC feature. This member can be one of the following values:

MC_Emergency	Meaning
MC_Emergency_Enable	MC Emergency Enable.
MC_Emergency_Disable	MC Emergency Disable.

### MC\_Period

Specifies the period value to be loaded in the active Auto-Reload Register at the next update event. This member must be a number between 0x0000 and 0xFFFF.

## MC\_TachoPeriod

Specifies the Tacho Compare period. This member must be a number between 0x00 and 0xFF.

### MC\_Channel

Specifies the MC Channel to be used. This member can be one of the following values:

MC_Channel	Meaning
MC_Channel_U	MC Channel U is used.
MC_Channel_V	MC Channel V is used.
MC_Channel_W	MC Channel W is used.
MC_Channel_ALL	MC Channel U, V and W are used.

#### MC PulseU

Specifies the Pulse U value to be loaded in the CMPU Register.

The MC\_PulseU presents the DutyCycle value. This member must be a number between 0x000 and 0x7FF.

### MC PulseV

Specifies the Pulse V value to be loaded in the CMPV Register.

The MC\_PulseV presents the DutyCycle value. This member must be a number between 0x000 and 0x7FF.

#### MC PulseW

Specifies the Pulse W value to be loaded in the CMPW Register.

The MC\_PulseW presents the DutyCycle value. This member must be a number between 0x000 and 0x7FF.

## MC\_PolarityUL

Specifies the Channel UL signal Polarity. This member can be one of the following values:

MC_PolarityUL	Meaning
MC_Polarity_Inverted	Channel UL signal polarity inverted
MC_Polarity_NonInverted	Channel UL signal polarity non-inverted

## MC\_PolarityUH

Specifies the Channel UH signal Polarity. This member can be one of the following values:

MC_PolarityUH	Meaning
MC_Polarity_Inverted	Channel UH signal polarity inverted
MC_Polarity_NonInverted	Channel UH signal polarity non-inverted

## MC\_PolarityVL

Specifies the Channel VL signal Polarity. This member can be one of the following values:

MC_PolarityVL	Meaning
MC_Polarity_Inverted	Channel VL signal polarity inverted
MC_Polarity_NonInverted	Channel VL signal polarity non-inverted

### MC\_PolarityVH

Specifies the Channel VH signal Polarity. This member can be one of the following values:

MC_PolarityVH	Meaning
MC_Polarity_Inverted	Channel VH signal polarity inverted
MC_Polarity_NonInverted	Channel VH signal polarity non-inverted

#### MC PolarityWL

Specifies the Channel WL signal Polarity. This member can be one of the following values:

MC_PolarityWL	Meaning
MC_Polarity_Inverted	Channel WL signal polarity inverted
MC_Polarity_NonInverted	Channel WL signal polarity non-inverted

### MC\_PolarityWH

Specifies the Channel WH signal Polarity. This member can be one of the following values:

MC_PolarityWH	Meaning
MC_Polarity_Inverted	Channel WH signal polarity inverted
MC_Polarity_NonInverted	Channel WH signal polarity non-inverted

#### MC\_TachoPolarity

Specifies the Tacho Input signal Polarity. This member can be one of the following values:

MC_TachoPolarity	Meaning
MC_Polarity_Inverted	Tacho Input signal polarity inverted
MC_Polarity_NonInverted	Tacho Input signal polarity non-inverted

### MC\_DeadTime

Specifies the dead time for managing the time between the switching-off and the switching-on instants of the outputs.

## MC\_RepetitionCounter

Specifies the repetition counter value. Each time the RER down-counter reaches zero, an update event is generated and it restarts counting from RER value.

#### Example:

```
/* The following example illustrates how to configure the MC hardware operating
complementary Mode */
MC_InitStructure.MC_OperatingMode = MC_HardwareOperating_Mode;
MC_InitStructure.MC_TachoMode = MC_TachoContinuous_Mode;
MC_InitStructure.MC_Prescaler = 0x00;
MC_InitStructure.MC_TachoPrescaler = 0x000;
MC_InitStructure.MC_PWMMode = MC_PWMZeroCentered_Mode;
MC_InitStructure.MC_Complementary = MC_Complementary_Enable;
MC_InitStructure.MC_Emergency = MC_Emergency_Enable;
MC_InitStructure.MC_Period = 0x3FF;
MC_InitStructure.MC_TachoCompare = 0xFF;
MC_InitStructure.MC_Channel = MC_Channel_ALL;
MC_InitStructure.MC_PulseU = 0x1FF;
MC_InitStructure.MC_PulseV = 0xFF;
MC_InitStructure.MC_PulseW = 0x7F;
MC_InitStructure.MC_PolarityUL = MC_Polarity_Inverted;
MC_InitStructure.MC_PolarityUH = MC_Polarity_Inverted;
MC_InitStructure.MC_PolarityVL = MC_Polarity_NonInverted;
MC_InitStructure.MC_PolarityVH = MC_Polarity_NonInverted;
MC_InitStructure.MC_PolarityWL = MC_Polarity_Inverted;
```

```
MC_InitStructure.MC_PolarityWH = MC_Polarity_Inverted;
MC_InitStructure.MC_TachoPolarity = MC_TachoEventEdge_Falling;
MC_InitStructure.MC_DeadTime = 0x0F;
MC_InitStructure.MC_RepetitionCounter = 0x0;
MC_Init(&MC_InitStructure);
```

# 17.2.3 MC\_StructInit

Function name	MC_StructInit
Function prototype	<pre>void MC_StructInit(MC_InitTypeDef* MC_InitStruct)</pre>
Behavior description	Fills each MC_InitStruct member with its default value.
Input parameter	MC_InitStruct: pointer to an MC_InitTypeDef structure which will be initialized.
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

### Example:

/\* The following example illustrates how to initialize a MC\_InitTypeDef structure \*/
MC\_InitTypeDef MC\_InitStructure;
MC\_StructInit(&MC\_InitStructure);

## 17.2.4 MC\_Cmd

Function name	MC_Cmd
Function prototype	void MC_Cmd(FunctionalState NewState)
Behavior description	Enables or disables the MC peripheral.
Input parameter	NewState: new state of the MC peripheral. This parameter can be: ENABLE or DISABLE.
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

## Example:

```
/* Enable the MC */
MC_Cmd(ENABLE);
```

# 17.2.5 MC\_ClearPWMCounter

Function name	MC_ClearPWMCounter
Function prototype	void MC_ClearPWMCounter(void)
Behavior description	Clears the MC PWM counter.
Input parameter	None
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

#### Example:

/\* Clears the PWM Counter\*/
MC\_ClearPWMCounter();

## 17.2.6 MC\_ClearTachoCounter

Function name	MC_ClearTachoCounter
Function prototype	void MC_ClearTachoCounter(void)
Behavior description	Clears the MC Tacho counter.
Input parameter	None
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

## Example:

/\* Clears the Tacho Counter\*/
MC\_ClearTachoCounter();

# 17.2.7 MC\_CtrlPWMOutputs

Function name	MC_CtrlPWMOutputs
Function prototype	void MC_CtrlPWMOutputs(FunctionalState Newstate)
Behavior description	Enables or disables MC peripheral Main Outputs.
Input parameter	NewState: new state of the MC peripheral outputs. This parameter can be: ENABLE or DISABLE.
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

## Example:

/\* Enable the MC Outputs \*/  $\mbox{MC\_CtrlPWMOutputs(ENABLE);}$ 

# 17.2.8 MC\_ITConfig

Function name	MC_ITConfig
Function prototype	void MC_ITConfig(u16 MC_IT, FunctionalState NewState)
Behavior description	Enables or disables the MC interrupts.
Input parameter1	MC_IT: specifies the MC interrupts sources to be enabled or disabled.  Refer to <i>Table 91: MC_IT parameter values</i> for the allowed values of this parameter.
Input parameter2	NewState: new state of the MC interrupts. This parameter can be: ENABLE or DISABLE.
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

## MC\_IT

To enable or disable MC interrupts, use a combination of one or more of the following values:

Table 91. MC\_IT parameter values

Value	Meaning
MC_IT_CMPW	Compare W interrupt
MC_IT_CMPV	Compare V interrupt
MC_IT_CMPU	Compare U interrupt
MC_IT_ZPC	Zero of PWM counter interrupt
MC_IT_ADT	Automatic data transfer interrupt
MC_IT_OTC	Overflow of tacho counter interrupt
MC_IT_CPT	Capture of tacho counter interrupt
MC_IT_CM0	Compare 0 interrupt

## Example:

```
/* Enables the MC Output Compare W Interrupt */
MC_ITConfig(MC_IT_CMPW, ENABLE);
```

# 17.2.9 MC\_SetPrescaler

Function name	MC_SetPrescaler
Function prototype	void MC_SetPrescaler(u8 MC_Prescaler)
Behavior description	Sets the MC prescaler value.
Input parameter	MC_Prescaler: PWM prescaler new value.
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

### Example:

```
/* Sets the MC new Prescaler value */
u8 MCPrescaler = 0xFF;
MC_SetPrescaler( MCPrescaler);
```

# 17.2.10 MC\_SetPeriod

Function name	MC_SetPeriod
Function prototype	void MC_SetPeriod(u16 MC_Period)
Behavior description	Sets the MC period value.
Input parameter	MC_Period: MC period new value.
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

```
/* Sets the MC new Period value */
u16 MCPeriod = 0x3FF;
MC_SetPrescaler(MCPeriod);
```

# 17.2.11 MC\_SetPulseU

Function name	MC_SetPulseU
Function prototype	void MC_SetPulseU(u16 MC_PulseU)
Behavior description	Sets the MC pulse U value.
Input parameter	MC_PulseU: MC pulse U new value.
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

### Example:

```
/* Sets the MC new Channel U Pulse value */
u16 MCPulse = 0x00F0;
MC_SetPulseU(MCPulse);
```

# 17.2.12 MC\_SetPulseV

Function name	MC_SetPulseV
Function prototype	void MC_SetPulseV(u16 MC_PulseV)
Behavior description	Sets the MC pulse V value.
Input parameter	MC_PulseV: MC pulse V new value.
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

```
/* Sets the MC new Channel V Pulse value */
u16 MCPulse = 0x00F0;
MC_SetPulseV(MCPulse);
```

## 17.2.13 MC\_SetPulseW

Function name	MC_SetPulseW
Function prototype	void MC_SetPulseW(u16 MC_PulseW)
Behavior description	Sets the MC pulse W value.
Input parameter	MC_PulseW: MC pulse W new value.
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

#### **Example:**

```
/* Sets the MC new Channel W Pulse value */
u16 MCPulse = 0x00F0;
MC_SetPulseW(MCPulse);
```

# 17.2.14 MC\_SetTachoCompare

Function name	MC_SetTachoCompare
Function prototype	void MC_SetTachoCompare(u8 MC_Compare)
Behavior description	Sets the MC Tacho compare value.
Input parameter	MC_Compare: MC Tacho compare value.
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

```
/* Sets the MC Tacho Compare value */
u8 MCTachoCompare = 0x0F;
MC_SetTachoCompare(MCTachoCompare);
```

# 17.2.15 MC\_PWMModeConfig

Function name	MC_PWMModeConfig
Function prototype	void MC_PWMModeConfig(u16 MC_PWMMode)
Behavior description	Configures the MC PWM Mode.
Input parameter	MC_PWMMode: MC PWM Mode.  Refer to section : MC_PWMMode on page 223 for more details on the allowed values of this parameter.
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

## **Example:**

```
/* Configures the MC to generate a Zero Centred PWM Mode */
MC_PWMModeConfig(MC_PWMZeroCenterd_Mode);
```

# 17.2.16 MC\_SetDeadTime

Function name	MC_SetDeadTime
Function prototype	void MC_SetDeadTime(u16 DeadTime)
Behavior description	Sets the MC Dead Time value.
Input parameter	DeadTime: MC Dead Time value.
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

## Example:

```
/* Sets the MC new Dead Time value */
u16 MCDeadTime = 0x00F;
MC_SetDeadTime(MCDeadTime);
```

# 17.2.17 MC\_EmergencyCmd

Function name	MC_EmergencyCmd
Function prototype	void MC_EmergencyCmd(FunctionalState NewState)
Behavior description	Enables or disables the MC emergency feature.
Input parameter	NewState: new state of the MC peripheral Emergency Input. This parameter can be: ENABLE or DISABLE.
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

## Example:

```
/* Enables the MC Emergency Input */
MC_EmergencyCmd( ENABLE);
```

# 17.2.18 MC\_EmergencyClear

Function name	MC_EmergencyClear
Function prototype	void MC_EmergencyClear(void)
Behavior description	Clears the MC emergency register.
Input parameter	None
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

```
/* Clears the MC Emergency Register*/
MC_EmergencyClear();
```

# 17.2.19 MC\_GetPeriod

Function name	MC_GetPeriod
Function prototype	u16 MC_GetPeriod(void);
Behavior description	Gets the MC period value.
Input parameter	None
Output parameter	None
Return parameter	MC period value.
Required preconditions	None
Called functions	None

### Example:

```
/* Gets the MC Period value */
u16 MCPeriod = 0x000;
MCPeriod = MC_GetPeriod();
```

# 17.2.20 MC\_GetPulseU

Function name	MC_GetPulseU
Function prototype	u16 MC_GetPulseU(void);
Behavior description	Gets the MC pulse U value.
Input parameter	None
Output parameter	None
Return parameter	MC pulse U value.
Required preconditions	None
Called functions	None

## Example:

```
/* Gets the MC Channel U Pulse value */
u16 MCPulse = 0x000;
MCPulse = MC_GetPulseU();
```

# 17.2.21 MC\_GetPulseV

Function name	MC_GetPulseV
Function prototype	u16 MC_GetPulseV(void);
Behavior description	Gets the MC pulse V value.
Input parameter	None
Output parameter	None
Return parameter	MC pulse V value.
Required preconditions	None
Called functions	None

### Example:

```
/* Gets the MC Channel V Pulse value */
u16 MCPulse = 0x000;
MCPulse = MC_GetPulseV();
```

# 17.2.22 MC\_GetPulseW

Function name	MC_GetPulseW
Function prototype	u16 MC_GetPulseW(void);
Behavior description	Gets the MC pulse W value.
Input parameter	None
Output parameter	None
Return parameter	MC pulse W value.
Required preconditions	None
Called functions	None

```
/* Gets the MC Channel W Pulse value */
u16 MCPulse = 0x000;
MCPulse = MC_GetPulseW();
```

# 17.2.23 MC\_GetTachoCapture

Function name	MC_GetTachoCapture
Function prototype	u16 MC_GetTachoCapture(void)
Behavior description	Gets the MC Tacho capture value.
Input parameter	None
Output parameter	None
Return parameter	MC Tacho capture value.
Required preconditions	None
Called functions	None

#### **Example:**

```
/* Gets the MC Tacho Capture value */
u16 MCTachoCapture = 0x0000;
MCTachoCapture = MC_GetTachoCapture();
```

# 17.2.24 MC\_ClearOnTachoCapture

Function name	MC_ClearOnTachoCapture
Function prototype	void MC_ClearOnTachoCapture(void)
Behavior description	Enables or disables the clear on capture of Tacho counter.
Input parameter	NewState: new state of the CCPT Bit. This parameter can be: ENABLE or DISABLE.
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

## Example:

```
/* Enables the Clear on capture of Tacho Counter */ \mbox{MC\_ClearOnTachoCapture(ENABLE)};
```

## 17.2.25 MC\_ForceDataTransfer

Function name	MC_ForceDataTransfer
Function prototype	void MC_ForceDataTransfer(u8 MC_ForcedData)
Behavior description	Sets the MC Outputs default states.
Input parameter	MC_ForcedData: MC outputs new states.
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

### **Example:**

/\* Sets the MC PWM forced state: all outputs on high level\*/

MC\_ForceDataTransfer(0x2F);

# 17.2.26 MC\_SoftwarePreloadConfig

Function name	MC_SoftwarePreloadConfig
Function prototype	<pre>void MC_SoftwarePreloadConfig(void)</pre>
Behavior description	Enables the software data transfer.
Input parameter	None
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

## Example:

/\* Enables the software Data Transfer \*/
MC\_SoftwarePreloadConfig();

# 17.2.27 MC\_SoftwareTachoCapture

Function name	MC_SoftwareTachoCapture
Function prototype	void MC_SoftwareTachoCapture(void)
Behavior description	Enables the software Tacho Capture.
Input parameter	None
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

## Example:

/\* Enables the software Tacho Capture \*/
MC\_SoftwareTachoCapture();

# 17.2.28 MC\_GetCountingStatus

Function name	MC_GetCountingStatus
Function prototype	CountingStatus MC_GetCountingStatus(void)
Behavior description	Checks whether the PWM Counter is counting Up or Down.
Input parameter	None
Output parameter	None
Return parameter	The new state of the PWM Counter (DOWN or UP).
Required preconditions	None
Called functions	None

## Example:

/\* Gets the MC counting state \*/
CountingStatus MC\_CounterStatus = DOWN;
MC\_CounterStatus = MC\_GetCountingStatus();
MC\_EmergencyStopPolarity

# 17.2.29 MC\_GetFlagStatus

Function name	MC_GetFlagStatus
Function prototype	FlagStatus MC_GetFlagStatus(u16 MC_FLAG)
Behavior description	Checks whether the MC flag is set or not.
Input parameter	MC_FLAG: specifies the flag to check.  Refer to <i>Table 92: MC_FLAG parameter values</i> for the allowed values of this parameter.
Output parameter	None
Return parameter	The new state of MC_FLAG (SET or RESET).
Required preconditions	None
Called functions	None

## Table 92. MC\_FLAG parameter values

MC_FLAG	Meaning
MC_FLAG_CMPW	Compare W pending bit
MC_FLAG_CMPV	Compare V pending bit
MC_FLAG_CMPU	Compare U pending bit
MC_FLAG_ZPC	Zero of PWM counter pending bit
MC_FLAG_ADT	Automatic data transfer pending bit
MC_FLAG_OTC	Overflow of tacho counter pending bit
MC_FLAG_CPT	Capture of tacho counter pending bit
MC_FLAG_CM0	Compare 0 of PWM pending bit
MC_FLAG_EST	Emergency stop pending bit

## Example:

```
/* Check if the MC Overflow of Tacho counter (OTC)flag is set or reset */
if (MC_GetFlagStatus(MC_FLAG_OTC) == SET)
   {
   }
```

# 17.2.30 MC\_ClearFlag

Function name	MC_ClearFlag
Function prototype	void MC_ClearFlag(u16 MC_FLAG)
Behavior description	Clears the MC pending flags.
Input parameter	MC_FLAG: specifies the flags to clear.  Refer to <i>Table 92: MC_FLAG parameter values on page 240</i> for the allowed values of this parameter
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

### Example:

```
/* Clear the MC Output Compare W flag */
    MC_ClearFlag(MC_IT_CMPW);
```

# 17.2.31 MC\_GetITStatus

Function name	MC_GetITStatus
Function prototype	ITStatus MC_GetITStatus(u16 MC_IT)
Behavior description	Checks whether the specific MC interrupt has occurred or not.
Input parameter	MC_IT: specifies the interrupt to check.  Refer to <i>Table 91: MC_IT parameter values on page 229</i> for the allowed values of this parameter.
Output parameter	None
Return parameter	The new state of MC_IT (SET or RESET).
Required preconditions	None
Called functions	None

## **Example:**

```
/* Gets the MC output compare W interrupt state */
ITStatus MC_ITStatus = RESET;
MC_ITStatus = MC_GetITStatus(MC_IT_CMPW);
```

# 17.2.32 MC\_ClearITPendingBit

Function name	MC_ClearITPending Bit
Function prototype	void MC_ClearITPendingBit(u16 MC_IT)
Behavior description	Clears the MC's interrupt pending bits.
Input parameter	MC_IT: specifies the pending bit to clear. Refer to <i>Table 91: MC_IT parameter values on page 229</i> for the allowed values of this parameter.
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

### Example:

/\* Clear the MC Output Compare W interrupt pending bit \*/
 MC\_ClearITPendingBit (MC\_IT\_CMPW);

## 17.2.33 MC\_Lock

Function name	MC_Lock
Function prototype	void MC_Lock(u16 MC_LockLevel)
Behavior description	Enables the lock of certain control register bits.
Input parameter	MC_LockLevel: Specifies the level to be locked.  Refer to <i>Table 93: MC_LockLevel parameter values</i> for the allowed values of this parameter.
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

## Table 93. MC\_LockLevel parameter values

Value	Meaning
MC_LockLevel4	Lock the dead time generator register
MC_LockLevel3	Lock the output peripheral register
MC_LockLevel2	Lock the phase polarity bits
MC_LockLevel1	Lock the emergency stop disable bit
MC_LockLevel0	Lock the dead time counter enable and the output dead time counter Selection bits.

## Example:

/\*Enable the lock for the output peripheral register bit\*/  $\mbox{MC\_Lock}(\mbox{MC\_LockLevel3})\;;$ 

# 17.2.34 MC\_CounterModeConfig

Function name	MC_CounterModeConfig
Function prototype	void MC_CounterModeConfig(u16 MC_Counter)
Behavior description	Enables the 10 bits mode for the dead time counter or enables or enables the 16 bits mode for the PWM counter.
Input parameter	MC_Counter: specifies the counter Refer to <i>Table 94: MC_Counter parameter values</i> for the allowed values of this parameter.
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

## Table 94. MC\_Counter parameter values

MC_Counter	Meaning
MC_DT_Counter	Dead time counter
MC_PWM_Counter	PWM counter

#### Example:

/\*Enable the 16 bit-mode for the PWM counter\*/
MC\_CounterModeConfig(MC\_PWM\_Counter);

# 17.2.35 MC\_DoubleUpdateMode

Function name	MC_DoubleUpdateMode
Function prototype	void MC_DoubleUpdateMode(FunctionalState NewState)
Behavior description	Enables or disables the double update mode
Input parameter	NewState: new state of the MC counter mode bits. This parameter can be: ENABLE or DISABLE.
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

## **Example:**

/\*Enable the double update mode\*/
MC\_DoubleUpdateMode(ENABLE);

# 17.2.36 MC\_ADCTrigger

Function name	MC_ADCTrigger
Function prototype	void MC_ADCTrigger(u16 IMC_Event, FunctionalState NewState)
Behavior description	Enables or disables the trigger to the ADC conversion
Input parameter	IMC_Event: the IMC event used to trigger the ADC conversion.  Refer to <i>Table 95: IMC_Event parameter values</i> for the allowed values of this parameter.  NewState: new state of the ADC trigger.  This parameter can be: ENABLE or DISABLE.
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

## Table 95. IMC\_Event parameter values

Value	Meaning
MC_ZPC	When the PWM counter reaches zero
MC_CM0	When the PWM counter reaches its maximum count
MC_ADT	When the PWM counter equals zero and the repetition down counter equals zero.

## **Example:**

/\*Trigger the ADC conversion when the PWM counter reaches zero\*/  $\mbox{MC\_ADC\_Trigger}(\mbox{MC\_ZPC, ENABLE});$ 

## 17.2.37 MC\_EnhancedStop

Function name	MC_EnhancedStop
Function prototype	void MC_EnhancedStop(FunctionalState NewState)
Behavior description	Enables or disables the enhanced motor stop feature.
Input parameter	NewState: new state of the output phases. This parameter can be: ENABLE or DISABLE.
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

### Example:

/\*Enable the Enhanced Motor Stop feature\*/
MC\_EnhancedStop(ENABLE);

# 17.2.38 MC\_DebugOutputProtection

Function name	MC_DebugOutputProtection
Function prototype	void MC_DebugOutputProtection(FunctionalState NewState)
Behavior description	Allows the output phases to follow the polarity set by PSR if enabled or they remain in their last known state if disabled.
Input parameter	NewState: new state of the output phases. This parameter can be: ENABLE or DISABLE.
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

## **Example:**

/\*The output phases follow the polarity set by PSR\*/  $\mbox{MC\_DebugOutputProtection(ENABLE)};$ 

# 17.2.39 MC\_EmergencyStopPolarity

Function name	MC_EmergencyStopPolarity
Function prototype	void MC_EmergencyStopPolarity(FunctionalState NewState)
Behavior description	Enables or disables an Emergency Stop Polarity.
Input parameter	NewState: new state of the output phases. This parameter can be: ENABLE or DISABLE.
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

## **Example:**

/\*Enable the Emergency Stop Polarity\*/
MC\_EmergencyStopPolarity(ENABLE);

# 18 Controller area network (CAN)

This peripheral performs communication according to the CAN protocol version 2.0 part A and B. The bitrate can be programmed to values up to 1Mbit/s. Another main feature of this cell is that 32 message objects are implemented which can be fully configured with 2 interfaces.

The first section describes the data structures used in the CAN Firmware library. The second one presents the Firmware library functions.

Note:

Before using any CAN function, the I/O ports linked to the CAN RX and CAN TX pins must be set up as follows: GPIO 1.5 (CAN RX pin) must be input Tri-state CMOS, and GPIO 1.6 (CAN TX pin) must be output alternate push-pull.

# 18.1 CAN register structure

The structures of the *CAN\_TypeDef* and *CAN\_MsgObj\_TypeDef* registers are defined in the *91x\_map.h* file as follows:

```
typedef volatile struct
  vu16 CRR;
  u16 EMPTY1;
  vu16 CMR;
  u16 EMPTY2;
  vu16 M1R;
 u16 EMPTY3;
  vu16 M2R;
  u16 EMPTY4;
  vu16 A1R;
  1116 EMPTY5:
  vu16 A2R;
  u16 EMPTY6;
  vul6 MCR;
  u16 EMPTY7;
  vu16 DA1R;
  u16 EMPTY8;
  vu16 DA2R;
  u16 EMPTY9;
  vu16 DB1R:
  u16 EMPTY10;
  vu16 DB2R;
  u16 EMPTY11[27];
} CAN_MsgObj_TypeDef;
typedef volatile struct
  vu16 CR;
 u16 EMPTY1;
  vul6 SR;
  u16 EMPTY2;
  vu16 ERR;
  u16 EMPTY3;
  VII16 BTR:
  u16 EMPTY4;
  vu16 IDR;
  u16 EMPTY5;
  vul6 TESTR;
  u16 EMPTY6;
```

```
vu16 BRPR;
  u16 EMPTY7[3];
  CAN_MsgObj_TypeDef sMsgObj[2];
  u16 EMPTY8[16];
  vu16 TXR1R;
u16 EMPTY9;
  vu16 TXR2R;
  u16 EMPTY10[13];
  vu16 ND1R;
  u16 EMPTY11;
  vu16 ND2R;
  u16 EMPTY12[13];
  vu16 IP1R;
  u16 EMPTY13;
  vu16 IP2R;
  u16 EMPTY14[13];
  vu16 MV1R;
 u16 EMPTY15;
 vu16 MV2R;
u16 EMPTY16;
} CAN_TypeDef;
```

## Table 96. CAN registers

Register	Description
CR	CAN Control Register
SR	CAN Status Register
ERR	CAN Error counter Register
BTR	CAN Bit Timing Register
IDR	CAN Interrupt Identifier Register
TESTR	CAN Test Register
BRPR	CAN BRP Extension Register
CRR	CAN IF1 Command Request Register
CMR	CAN IF1 Command Mask Register
M1R	CAN IF1 Message Mask 1 Register
M2R	CAN IF1 Message Mask 2 Register
A1R	CAN IF1 Message Arbitration 1 Register
A2R	CAN IF1 Message Arbitration 2 Register
MCR	CAN IF1 Message Control Register
DA1R	CAN IF1 DATA A 1 Register
DA2R	CAN IF1 DATA A 2 Register
DB1R	CAN IF1 DATA B 1 Register
DB2R	CAN IF1 DATA B 2 Register
CRR	CAN IF2 Command request Register
CMR	CAN IF2 Command Mask Register
M1R	CAN IF2 Message Mask 1 Register
M2R	CAN IF2 Message Mask 2 Register

Table 96. CAN registers (continued)

Register	Description
A1R	CAN IF2 Message Arbitration 1 Register
A2R	CAN IF2 Message Arbitration 2 Register
MCR	CAN IF2 Message Control Register
DA1R	CAN IF2 DATA A 1 Register
DA2R	CAN IF2 DATA A 2 Register
DB1R	CAN IF2 DATA B 1 Register
DB2R	CAN IF2 DATA B 2 Register
TXR1R	CAN Transmission Request 1 Register
TXR2R	CAN Transmission Request 2 Register
ND1R	CAN New Data 1 Register
ND2R	CAN New Data 2 Register
IP1R	CAN Interrupt Pending 1 Register
IP2R	CAN Interrupt Pending 2 Register
MV1R	CAN Message Valid 1 Register
MV2R	CAN Message Valid 2 Register

#### The CAN is declared in the file below

```
#ifndef EXT
 #Define EXT extern
#endif
#define AHB_APB_BRDG1_U (0x5C000000) /* AHB/APB Bridge 1 UnBuffered Space */
#define AHB_APB_BRDG1_B (0x4C000000) /* AHB/APB Bridge 1 Buffered Space */
#define APB_CAN_OFST (0x00009000) /* Offset of CAN */
#ifndef Buffered
                                (AHB_APB_BRDG1_U)
#define AHBAPB1_BASE
#else /* Buffered */
#define AHBAPB1_BASE
                                (AHB_APB_BRDG1_B)
/* CAN Base Address definition*/
#define CAN_BASE (AHBAPB1_BASE + APB_CAN_OFST)
/* CAN peripheral declaration*/
#ifndef DEBUG
#define CAN ((CAN_TypeDef *) CAN_BASE)
#else
EXT CAN_TypeDef
                            *CAN;
```

#endif

When debug mode is used, CAN pointer is initialized in *91x\_lib.c* file:

```
#ifdef _CAN
    CAN = (CAN_TypeDef *)CAN_BASE
#endif /* _CAN */
```

\_CAN must be defined, in  $\it 91x\_conf.h$  file, to access the peripheral registers as follows: #define \_CAN

. .

# 18.2 Firmware library functions

Table 97. CAN library functions

Function name	Description
CAN_DeInit	Deinitializes the CAN peripheral registers to their default reset values.
CAN_Init	Initializes the CAN cell and sets the bitrate.
CAN_StructInit	Fills each CAN_InitStruct member with its default value.
CAN_EnterInitMode	Switches the CAN to initialization mode.
CAN_LeaveInitMode	Leaves initialization mode (switches to normal mode).
CAN_EnterTestMode	Switches the CAN to test mode.
CAN_LeaveTestMode	Leaves the current test mode (switches to normal mode).
CAN_SetBitrate	Sets up a standard CAN bitrate.
CAN_SetTiming	Sets up the CAN timing with specific parameters.
CAN_SetUnusedMsgObj	Configures the message object as unused.
CAN_SetTxMsgObj	Configures the message object as TX.
CAN_SetRxMsgObj	Configures the message object as RX.
CAN_SetUnusedAllMsgObj	Configures all the message objects as unused.
CAN_ReleaseMessage	Releases the message object.
CAN_ReleaseTxMessage	Releases the transmit message object.
CAN_ReleaseRxMessage	Releases the receive message object.
CAN_UpdateMsgObj	Updates the message object
CAN_TransmitRequest	Requests the transmission of a message object. A data or remote frame is sent.
CAN_SendMessage	Starts transmission of a message.
CAN_ReceiveMessage	Gets the message, if received.
CAN_WaitEndOfTx	Waits until current transmission is finished.
CAN_BasicSendMessage	Starts transmission of a message in BASIC mode.

Table 97. CAN library functions (continued)

Function name	Description
CAN_BasicReceiveMessage	Gets the message in BASIC mode, if received.
CAN_GetMsgReceiveStatus	Tests the waiting status of a received message.
CAN_GetMsgTransmitRequest Status	Tests the request status of a transmitted message.
CAN_GetMsgInterruptStatus	Tests the interrupt status of a message object.
CAN_GetMsgValidStatus	Tests the validity of a message object (ready to use).
CAN_GetFlagStatus	Returns the state of the CAN flags: TxOK, RxOK, EPASS, EWARN and BOFF
CAN_GetTransmitErrorCounter	Gets the CAN transmit Error counter
CAN_GetReceiveErrorCounter	Gets the CAN receive Error counter

# 18.2.1 CAN\_Delnit

Function name	CAN_DeInit
Function prototype	void CAN_DeInit(void)
Behavior description	Deinitializes the CAN peripheral registers to their default reset values.
Input parameter	None
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	SCU_APBPeriphReset()

## Example:

This example illustrates how to initialize the CAN registers.

```
{
/* Initialize CAN registers*/
    CAN_DeInit ();
}
```

# 18.2.2 **CAN\_Init**

Function name	CAN_Init
Function prototype	void CAN_Init(CAN_InitTypeDef* CAN_InitStruct)
Behavior description	Initializes the CAN peripheral according to the specified parameters in the CAN_InitStruct.
Input parameter	CAN_InitStruct: pointer to a CAN_InitTypeDef structure that contains the configuration information for the CAN peripheral.  Refer to section "CAN_InitTypeDef on page 251" for more details on the allowed values of this parameter.
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	CAN_EnterInitMode() CAN_SetBitrate() CAN_LeaveInitMode() CAN_LeaveTestMode()

## CAN\_InitTypeDef

The CAN\_InitTypeDef structure is defined in the **91x\_can.h** file:

```
typedef struct
{
   u8   CAN_ConfigParameters;
   u32   CAN_Bitrate;
}CAN_InitTypeDef;
```

## CAN\_ConfigParameters

Specifies the CAN configuration parameters. This member can be any combination of the following values:

CAN_ConfigParameters	Meaning
CAN_CR_TEST	Test mode enable
CAN_CR_CCE	Configuration change enable
CAN_CR_DAR	Disable automatic retransmission
CAN_CR_EIE	Error interrupt enable
CAN_CR_SIE	Status change interrupt enable
CAN_CR_IE	Module interrupt enable
CAN_CR_INIT	Initialization

### **CAN Bitrate**

Specifies the CAN bit rate. This member can be one of the following values:

CAN_Bitrate	Meaning
CAN_BITRATE_100K	100 kbit/s bit rate
CAN_BITRATE_125K	125 kbit/s bit rate
CAN_BITRATE_250K	250 kbit/s bit rate
CAN_BITRATE_500K	500 kbit/s bit rate
CAN_BITRATE_1M	1 Mbit/s bit rate

## Example:

This example illustrates how to initialize the CAN at 100 kbit/s and enable the interrupts.

```
/* Init Structure declarations for CAN*/
CAN_InitTypeDef CAN_InitStructure;

/*Configure CAN registers*/
CAN_InitStructure.CAN_ConfigParameters = CAN_CR_IE;
CAN_InitStructure.CAN_Bitrate = CAN_BITRATE_100K;
CAN_Init(&CAN_InitStructure);
```

## 18.2.3 CAN\_StructInit

Function name	CAN_StructInit
Function prototype	<pre>void CAN_StructInit(CAN_InitTypeDef* CAN_InitStruct)</pre>
Behavior description	Fills each CAN_InitStruct member with its default value.
Input parameter	CAN_InitStruct: pointer to a CAN_InitTypeDef structure which will be initialized.
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

#### Example:

This example illustrates how to initialize CAN init structure.

```
/* Init Structures declarations for CAN */
CAN_InitTypeDef CAN_InitStructure;

/*Initialize CAN structure*/
CAN_StructInit (&CAN_InitStructure);
```

# 18.2.4 CAN\_EnterInitMode

Function name	CAN_EnterInitMode
Prototype	void CAN_EnterInitMode(u8 InitMask)
Behavior description	Switches the CAN into initialization mode. This function must be used in conjunction with CAN_LeaveInitMode().
Input parameter	InitMask: specifies the CAN configuration in normal mode.  Refer to <i>Table 98: InitMask parameter values</i> " for the allowed values of this parameter.
Output parameter	None
Return Value	None
Required preconditions	None
Called functions	None

Note:

This function sets the INIT bit in the Control register, ORed with the mask and resets the Status register.

### InitMask

Specifies the CAN configuration which will be set after the initialisation in normal mode. This member can be any combination of the following values:

Table 98. InitMask parameter values

Table 00. Illimater parameter value	
Value	Meaning
CAN_CR_CCE	Configuration change enable
CAN_CR_DAR	Disable automatic retransmission
CAN_CR_EIE	Error interrupt enable
CAN_CR_SIE	Status change interrupt enable
CAN_CR_IE	Module interrupt enable

### Example:

This example illustrates how to initialize the CAN enable interrupts.

```
CAN_EnterInitMode(CAN_CR_IE);
}
```

# 18.2.5 CAN\_LeaveInitMode

Function name	CAN_LeaveInitMode
Prototype	void CAN_LeaveInitMode()
Behavior description	Leaves initialization mode (switch into normal mode). This function must be used in conjunction with CAN_EnterInitMode().
Input parameter	None
Output parameter	None
Return Value	None
Required preconditions	None
Called functions	None

Note:

This function clears the INIT and CCE bits in the Control register.

## Example:

```
This example illustrates how to leave CAN init mode.
```

```
{
   CAN_LeaveInitMode();
}
```

## 18.2.6 CAN\_EnterTestMode

Function name	CAN_EnterTestMode
Prototype	<pre>void CAN_EnterTestMode(u8 TestMask);</pre>
Behavior description	Switches the CAN into test mode. This function must be used in conjunction with CAN_LeaveTestMode().
Input parameter	TestMask: specifies the configuration in test modes.  Refer to <i>Table 99: TestMask parameter values</i> " for the allowed values of this parameter.
Output parameter	None
Return Value	None
Required preconditions	None
Called functions	None

Note:

This function sets the TEST bit in the Control register to enable test mode and updates the Test register by ORing its value with the mask.

#### TestMask

Specifies the CAN configuration in test modes. This member can be any combination of the following values:

Table 99. TestMask parameter values

TestMask	Meaning
CAN_TESTR_LBACK	Loopback mode enabled
CAN_TESTR_SILENT	Silent mode enabled
CAN_TESTR_BASIC	Basic mode enabled

### Example:

This example illustrates how to switch the CAN into Loopback mode, i.e. RX is disconnected from the bus, and TX is internally linked to RX.

```
{
    CAN_EnterTestMode(CAN_TESTR_LBACK);
}
```

# 18.2.7 CAN\_LeaveTestMode

Function name	CAN_LeaveTestMode
Prototype	void CAN_LeaveTestMode()
Behavior description	Leaves the current test mode (switches into normal mode). This function must be used in conjunction with CAN_EnterTestMode().
Input parameter	None
Output parameter	None
Return Value	None
Required preconditions	None
Called functions	None

Note:

This function sets the TEST bit in the Control register to enable write access to the Test register, clears the LBACK, SILENT and BASIC bits in the Test register and clears the TEST bit in the Control register to disable write access to the Test register.

## Example:

```
{
CAN_LeaveTestMode();
}
```

# 18.2.8 CAN\_SetBitrate

Function name	CAN_SetBitrate
Prototype	<pre>void CAN_SetBitrate(u32 bitrate);</pre>
Behavior description	Sets up a standard CAN bitrate.
Input parameter	BitRate: specifies the bit rate.  Refer to <i>Table 100: BitRate parameter values</i> " for the allowed values of this parameter.
Output parameter	None
Return Value	None
Required preconditions	CAN_EnterInitMode() must have been called before. The APB clock must be 8 MHz
Called functions	None

Note:

This function writes the predefined timing value in the Bit Timing register and clears the BRPR register.

Table 100. BitRate parameter values

BitRate	Meaning
CAN_BITRATE_100K	100 kbit/s
CAN_BITRATE_125K	125 kbit/s
CAN_BITRATE_250K	250 kbit/s
CAN_BITRATE_500K	500 kbit/s
CAN_BITRATE_1M	1 Mbit/s

#### Example:

This example illustrates how to enable the configuration change bit, to be able to set the bitrate

```
{
CAN_EnterInitMode(CAN_CR_CCE);
CAN_SetBitrate(CAN_BITRATE_100K);
CAN_LeaveInitMode();
}
```

## 18.2.9 CAN\_SetTiming

Function name	CAN_SetTiming
Prototype	<pre>void CAN_SetTiming(u32 tseg1, u32 tseg2, u32 sjw, u32 brp);</pre>
Behavior description	Sets up the CAN timing with specific parameters.
Input parameter 1	tseg1: Time Segment before the sample point position. It can take values from 1 to 16.
Input parameter 2	tseg2: Time Segment after the sample point position. It can take values from 1 to 8.
Input parameter 3	sjw: Synchronization Jump Width. It can take values from 1 to 4.
Input parameter 4	brp: Baud Rate Prescaler. It can take values from 1 to 1024.
Output parameter	None
Return Value	None
Required preconditions	CAN_EnterInitMode() must have been called before.
Called functions	None

Note:

This function writes the timing value in the Bit Timing register, from the tseg1, tseg2, sjw parameters and bits 5..0 of brp parameter and writes the BRPR register with bits 9..0 of brp parameter; and all written values are the real values decremented by one unit.

#### Example:

This example illustrates how to enable the configuration change bit, to be able to set the specific timing parameters: TSEG1=11, TSEG2=4, SJW=4, BRP=5

```
{
CAN_EnterInitMode(CAN_CR_CCE);
CAN_SetTiming(11, 4, 4, 5);
CAN_LeaveInitMode();
}
```

## 18.2.10 CAN\_SetUnusedMsgObj

Function name	CAN_SetUnusedMsgObj
Prototype	ErrorStatus CAN_SetUnusedMsgObj(u32 msgobj);
Behavior description	Configure the message object as unused.
Input parameter	msgobj The message object number, from 0 to 31.
Output parameter	None
Return Value	None
Required preconditions	An ErrorStatus enumeration value: - SUCCESS: Found Interface to treat the message - ERROR: No interface found to treat the message
Called functions	CAN_GetFreeIF()

Note:

This function searches for a free message interface from IF0 and IF1, sets the WR/RD, Mask, Arb, Control, DataA and DataB bits in the Command Mask register, clears the Mask1 and Mask2 registers, clears the Arb1 and Arb2 register, clears the Message Control register, clears the DataA1, DataA2, DataB1, DataB2 registers and writes the value 1+msgobj in the Command Request register.

#### Example:

This example illustrates how to invalidate the message objects from 16 to 31: these objects will not be used by the hardware

```
{
for (i=16; i<=31; i++) CAN_SetUnusedMsgObj(i);
}</pre>
```

## 18.2.11 CAN\_SetTxMsgObj

Function name	CAN_SetTxMsgObj
Prototype	ErrorStatus CAN_SetTxMsgObj(u32 msgobj, u32 idType, FunctionalState RemoteEN)
Behavior description	Configures the message object as TX.
Input parameter 1	msgobj: The message object number, from 0 to 31.
Input parameter 2	idType: The identifier type of the frames that will be transmitted using this message object. The value is one of the following:  CAN_STD_ID (standard ID, 11-bit)  CAN_EXT_ID (extended ID, 29-bit)
Input parameter 3	RemoteEN: This parameter can be: ENABLE or DISABLE. Remote functionality is enabled if ENABLE,else it's disabled.
Output parameter	None
Return Value	An ErrorStatus enumeration value: - SUCCESS: Interface to treat the message - ERROR: No interface to treat the message
Required preconditions	None
Called functions	CAN_GetFreeIF()

#### Note:

- 1 This function: Search for a free message interface from IF0 and IF1. Set the WR/RD, Mask, Arb, Control, DataA and DataB bits in the Command Mask register. Clear the Mask1 and Arb1 registers. Set the MDir bit in the Mask2 register, also the MXtd bit if extended ID is used. Set the MsgVal and Dir bits in the Arb2 register, also the Xtd bit if extended ID is used. Set the TxIE and EoB bits in the Message Control register. Clear the DataA1, DataA2, DataB1, DataB2 registers. Write the value 1+msgobj to the Command Request register to copy the registers into the message RAM.
- When defining which message object number to use for TX or RX, you must take into account the priority levels when processing the objects. The lower number (0) has the highest priority and the higher number (31) has the lowest priority, whatever their type. Also, for optimum performance, it is not recommended to have "holes" in the object list.

#### Example:

This example illustrates how to define transmit message object 0 with standard identifiers and disable remote functionality.

```
{
    CAN_SetTxMsgObj(0, CAN_STD_ID, DISABLE);
}
```

## 18.2.12 CAN\_SetRxMsgObj

Function name	CAN_SetRxMsgObj
Prototype	ErrorStatus CAN_SetRxMsgObj(u32 msgobj, u32 idType, u32 idLow, u32 idHigh, bool singleOrFifoLast);
Behavior description	Configures the message object as RX.
Input parameter 1	msgobj: The message object number, from 0 to 31.
Input parameter 2	idType: The identifier type of the frames that will be transmitted using this message object. The value is one of the following:  CAN_STD_ID (standard ID, 11-bit)  CAN_EXT_ID (extended ID, 29-bit)
Input parameter 3	idLow: The low part of the identifier range used for acceptance filtering. It can take values from 0 to 0x7FF for standard ID, and values from 0 to 0x1FFFFFFF for extended ID.
Input parameter 4	idHigh: The high part of the identifier range used for acceptance filtering.  It can take values from 0 to 0x7FF for standard ID, and values from 0 to 0x1FFFFFFF for extended ID. idHigh must be above idLow.  For convenience, use one of the following values to set the maximum ID: CAN_LAST_STD_ID or CAN_LAST_EXT_ID
Input parameter 5	singleOrFifoLast: End-of-buffer indicator, it can take the following values:  -TRUE for a single receive object or a FIFO receive object that is the last one in the FIFO  -FALSE for a FIFO receive object that is not the last one
Output parameter	None
Return Value	An ErrorStatus enumeration value: - SUCCESS: Interface to treat the message - ERROR: No interface to treat the message
Required preconditions	None
Called functions	CAN_GetFreeIF()

### Note:

- This function: Search for a free message interface from IF0 and IF1. Set the WR/RD, Mask, Arb, Control, DataA and DataB bits in the Command Mask register. Write the ID mask value formed from idLow and idHigh in the Mask1 and Mask2 registers, and also set the MXtd bit in the Mask2 register if extended ID is used. Write the ID arbitration value formed from idLow and idHigh in the Arb1 and Arb2 registers, set the MsgVal bit, and also Xtd bit in the Arb2 register if extended ID is used. Set the RxIE and UMask bits in the Message Control register, and also the EoB bit if the parameter singleOrFifoLast is TRUE. Clear the DataA1, DataA2, DataB1, DataB2 registers. Write the value 1+msgobj to the Command Request register to copy the selected registers into the message RAM.
- 2 Care must be taken when defining an ID range: all combinations of idLow and idHigh will not always produce the expected result, because of the way identifiers are filtered by the hardware. The criteria applied to keep a received frame is as follows: (received ID) AND (ID mask) = (ID arbitration), where AND is a bitwise operator. Consequently, for idLow, it is generally better to choose a value with some LSBs cleared, and for idHigh a value that

"logically contains" idLow and with the same LSBs set. Example: the range 0x100-0x3FF will work, but the range 0x100-0x2FF will not because 0x100 is not logically contained in 0x2FF (i.e. 0x100 & 0x2FF = 0).

## Example:

```
This example illustrates how to define FIFOs and acceptance filtering
```

```
{
    /*Define a receive FIFO of depth 2 (objects 0 and 1) for standard identifiers, in which IDs are filtered in the range 0x400-0x5FF*/
    CAN_SetRxMsgObj(0, CAN_STD_ID, 0x400, 0x5FF, FALSE);
    CAN_SetRxMsgObj(1, CAN_STD_ID, 0x400, 0x5FF, TRUE);
    /*Define a single receive object for extended identifiers, in which all IDs are filtered in*/
    CAN_SetRxMsgObj(2, CAN_EXT_ID, 0, CAN_LAST_EXT_ID, TRUE);
}
```

## 18.2.13 CAN\_SetUnusedAllMsgObj

Function name	CAN_SetUnusedAllMsgObj
Prototype	ErrorStatus CAN_SetUnusedAllMsgObj();
Behavior description	Configures all the message objects as unused.
Input parameter	None
Output parameter	None
Return Value	An ErrorStatus enumeration value: - SUCCESS: Interface to treat all messages - ERROR: No interface to treat one message
Required preconditions	None
Called functions	CAN_SetUnusedMsgObj()

#### Example:

```
{
    CAN_SetUnusedAllMsgObj();
```

# 18.2.14 CAN\_ReleaseMessage

Function name	CAN_ReleaseMessage
Prototype	<pre>void CAN_ReleaseMessage(u32 msgobj);</pre>
Behavior description	Releases the message object.
Input parameter	msgobj The message object number, from 0 to 31.
Output parameter	None
Return Value	None
Required preconditions	None
Called functions	CAN_GetFreeIF()

### Note: This function:

Search for a free message interface from IF0 and IF1.

Set the bits ClrIntPnd and TxRqst/NewDat in the Command Mask register.

Write the value 1+msgobj to the Command Request register to copy the selected registers into the message RAM.

#### Example:

This example illustrates how to release the message object 0.

```
{
CAN_ReleaseMessage(0);
}
```

## 18.2.15 CAN\_ReleaseTxMessage

Function name	CAN_ReleaseTxMessage
Prototype	<pre>void CAN_ReleaseTxMessage(u32 msgobj);</pre>
Behavior description	Releases the transmit message object.
Input parameter	msgobj: The message object number, from 0 to 31.
Output parameter	None
Return Value	None
Required preconditions	The message interface 0 must not be busy.
Called functions	None

### Note: This function:

Sets the ClrIntPnd and TxRqst/NewDat bits in the Command Mask register of message interface 0.

Writes the value 1+msgobj to the Command Request register to copy the selected registers into the message RAM.

### Example:

```
This example illustrates how to release transmit message object 0. 
 \{ 
 /*It is assumed that message interface 0 is always used for transmission*/ 
 /*Release the transmit message object 0*/ 
 CAN_ReleaseTxMessage(0);
```

## 18.2.16 CAN\_ReleaseRxMessage

Function name	CAN_ReleaseRxMessage
Prototype	<pre>void CAN_ReleaseRxMessage(u32 msgobj);</pre>
Behavior description	Releases the receive message object.
Input parameter	msgobj: The message object number, from 0 to 31.
Output parameter	None
Return Value	None
Required preconditions	The message interface 1 must not be busy.
Called functions	None

### Note: This function:

Sets the bits ClrIntPnd and TxRqst/NewDat in the Command Mask register of message interface 1.

Writes the value 1+msgobj to the Command Request register to copy the selected registers into the message RAM.

### Example:

This example illustrates how to release the receive message object 0.

```
{
/*It is assumed that message interface 1 is always used for reception*/
/*Release the receive message object 0*/
CAN_ReleaseRxMessage(0);
}
```

# 18.2.17 CAN\_UpdateMsgObj

Function name	CAN_UpdateMsgObj
Function prototype	ErrorStatus CAN_UpdateMsgObj(u32 msgobj, canmsg* pCanMsg);
Behavior description	Updates the message object passed in parameter with the pCanMsg.
Input parameter 1	msgobj: message object number, from 0 to 31.
Input parameter 2	pCanMsg: pointer to the canmsg structure that contains the data to transmit: ID type, ID value, data length, data values.
Output parameter	None
Return Value	An ErrorStatus enumeration value: - SUCCESS: Interface to treat the message - ERROR: No interface to treat the message
Required preconditions	It is assumed that message interface 0 is used to update a can message object.
Called functions	None

### Example:

The following example illustrates how to update a message object already configured to transmit.

```
{
...
canmsg CanMsg = { CAN_STD_ID, 0x111, 4, {0x10, 0x20, 0x40, 0x80} };
/* Update CAN Message 0 */
CAN_UpdateMsgObj(0, &CanMsg);
...
}
```

# 18.2.18 CAN\_TransmitRequest

Function name	CAN_TransmitRequest
Prototype	ErrorStatus CAN_TransmitRequest( u32 msgobj);
Behavior description	Starts the transmission of a messsage object. A data frame is transmitted if the message object is configured in transmission mode. A remote frame is transmitted if the message object is configured in reception mode.
Input parameter	msgobj: The message object number, from 0 to 31.
Output parameter	None
Return Value	An ErrorStatus enumeration value: - SUCCESS: IF found to treat the message - ERROR: No IF found to treat the message
Required preconditions	The message object must have been set up properly.

## Example:

The following example illustrates how to request the transmission of a data frame.

```
{
...
/* Message object 0 has been already configured for transmission*/
/* Request the transmission of a data frame */
CAN_TransmitRequest(0);
...
```

## 18.2.19 CAN\_SendMessage

Function name	CAN_SendMessage
Prototype	ErrorStatus CAN_SendMessage(u32 msgobj, canmsg* pCanMsg);
Behavior description	Starts transmission of a message.
Input parameter 1	msgobj: The message object number, from 0 to 31.
Input parameter 2	pCanMsg: Pointer to the canmsg structure that contains the data to transmit: ID type, ID value, data length, data values.
Output parameter	None
Return Value	An ErrorStatus enumeration value: - SUCCESS: Transmission OK - ERROR: No transmission
Required preconditions	The message object must have been set up properly.
Called functions	CAN_UpdateMsgObj CAN_TransmitRequest

#### Note: This function:

Waits for message interface 0 to be free.

Read the Arbitration and Message Control registers.

Waits for message interface 0 to be free.

Updates the Arbitration, Message Control, DataA and DataB registers with the message contents.

Writes the value 1+msgobj to the Command Request register to copy the selected registers into the message RAM and to start the transmission.

#### Example:

```
This example illustrates how to send a standard ID data frame containing 4 data value.
```

```
{
canmsg CanMsg = { CAN_STD_ID, 0x111, 4, {0x10, 0x20, 0x40, 0x80} };
/*Send a standard ID data frame containing 4 data values*/
CAN_SendMessage(0, &CanMsg);
}
```

## 18.2.20 CAN\_ReceiveMessage

Function name	CAN_ReceiveMessage
Prototype	<pre>ErrorStatus CAN_ReceiveMessage(u32 msgobj, bool release, canmsg* pCanMsg);</pre>
Behavior description	Gets the message, if received.
Input parameter 1	msgobj: The message object number, from 0 to 31.
Input parameter 2	Release: The message release indicator, it can take the following values: -TRUE: the message object is released at the same time as it is copied from message RAM, then it is free for next reception -FALSE: the message object is not released, it is to the caller to do it
Input parameter 3	pCanMsg: Pointer to the canmsg structure where the received message is copied.
Output parameter	None
Return Value	An ErrorStatus enumeration value: - SUCCESS: Transmission OK - ERROR: No transmission
Required preconditions	The message object must have been set up properly.
Called functions	CAN_GetMsgReceiveStatus()

#### Note: This function:

Test the bit corresponding to the message object number in the NewData registers.

Clear the bit RxOk in the Status register.

Copy the message contents from the message RAM to the registers and to the structure, and release the message object if asked.

#### Example:

This example illustrates how to receive a message.

```
{
  canmsg CanMsg;
/*Receive a message in the object 0 and ask for release*/
  if (CAN_ReceiveMessage(CAN0, 0, TRUE, &CanMsg))
  {
    /*Check or copy the message contents*/
  }
  else
  {
    /* Error handling*/
  }
}
```

## 18.2.21 CAN\_WaitEndOfTx

Function name	CAN_WaitEndOfTx
Prototype	ErrorStatus CAN_WaitEndOfTx(void);
Behavior	Tests the TxOk bit in the Status register, and loops until it is set. Clears this bit to prepare the next transmission.
Input parameter	None
Output parameter	None
Return Value	An ErrorStatus enumeration value: - SUCCESS: Transmission ended - ERROR: Transmission did not occur yet
Required preconditions	A message must have been sent before.
Called functions	None

## Example:

This example illustrates how to send frames.

```
{
/*Send consecutive data frames using message object 0*/
for (i = 0; i < 10; i++)
{
    CAN_SendMessage(0, CanMsgTable[i]);
    CAN_WaitEndOfTx();
}</pre>
```

# 18.2.22 CAN\_BasicSendMessage

Function name	CAN_BasicSendMessage
Prototype	ErrorStatus CAN_BasicSendMessage(canmsg* pCanMsg);
Behavior description	Starts transmission of a message in BASIC mode. This mode does not use the message RAM.
Input parameter	pCanMsg: Pointer to the canmsg structure that contains the data to transmit: ID type, ID value, data length, data values.
Output parameter	None
Return Value	An ErrorStatus enumeration value: - SUCCESS: Transmission OK - ERROR: No transmission
Required preconditions	The CAN must have been switched into BASIC mode.
Called functions	None

Note:

This function:

Clears the bit NewDat in message interface 1.

Writes the Arbitration, Message Control, DataA and DataB registers of message interface 0, with the message contents.

Writes the value 1+msgobj to the Command Request register to start the transmission.

## Example:

This example illustrates how to send frames.

```
{
/*Send consecutive data frames using message object 0*/
for (i = 0; i < 10; i++)
{
   CAN_SendMessage(0, CanMsgTable[i]);
   CAN_WaitEndOfTx();
}</pre>
```

## 18.2.23 CAN\_BasicReceiveMessage

Function name	CAN_BasicReceiveMessage
Prototype	ErrorStatus CAN_BasicReceiveMessage(canmsg* pCanMsg);
Behavior description	Gets the message in BASIC mode, if received. This mode does not use the message RAM.
Input parameter	pCanMsg: Pointer to the canmsg structure where the received message is copied.
Output parameter	None
Return Value	An ErrorStatus enumeration value: - SUCCESS: Reception OK - ERROR: No message pending
Required preconditions	The CAN must have been switched into BASIC mode.
Called functions	None

#### Note: This function:

Tests the bit NewDat in the Message Control register of message interface 1.

Clears the bit RxOk in the Status register.

Copies the message contents from the message interface 1 registers to the structure.

### Example:

This example illustrates how to receive frame in basic mode.

```
{
  canmsg CanMsg;
/*Receive a message in BASIC mode*/
if (CAN_BasicReceiveMessage(&CanMsg))
{
   /* Check or copy the message contents*/
}
else
{
   /* Error handling*/
}
```

## 18.2.24 CAN\_GetMsgReceiveStatus

Function name	CAN_GetMsgReceiveStatus
Function prototype	FlagStatus CAN_GetMsgReceiveStatus(u32 msgobj);
Behavior description	Tests the waiting status of a received message.
Input parameter	msgobj: message object number, from 0 to 31.
Output parameter	None
Return Value	SET if the corresponding message object has received a message waiting to be copied, else RESET.
Required preconditions	The corresponding message object must have been set as RX.
Called functions	None

### Note: This function:

Tests the corresponding bit in the NewData 1 or 2 registers.

## Example:

This example illustrates how to test the new data registers for the message object 0.

# 18.2.25 CAN\_GetMsgTransmitRequestStatus

Function name	CAN_GetMsgTransmitRequestStatus
Prototype	FlagStatus CAN_GetMsgTransmitRequestStatus(u32 msgobj);
Behavior description	Tests the request status of a transmitted message.
Input parameter	msgobj: The message object number, from 0 to 31.
Output parameter	None
Return Value	SET if the corresponding message is requested to transmit, else RESET.
Required preconditions	A message must have been sent before.
Called functions	None

### Note: This function:

Tests the corresponding bit in the Transmission Request 1 or 2 registers.

## Example:

This example illustrates how to test the transmit request.

```
{
    /*Send a message using object 0*/
    CAN_SendMessage(0, &CanMsg);
    /*Wait for the end of transmit request*/
    while (CAN_GetMsgTransmitRequestStatus(0));
    /*Now, the message is being processed by the priority handler of the CAN cell, and ready to be emitted on the bus*/
}
```

# 18.2.26 CAN\_GetMsgInterruptStatus

Function name	CAN_GetMsgInterruptStatus
Prototype	FlagStatus CAN_GetMsgInterruptStatus(u32 msgobj);
Behavior description	Tests the interrupt status of a message object.
Input parameter	msgobj: The message object number, from 0 to 31.
Output parameter	None
Return Value	SET if the corresponding message has an interrupt pending, else RESET.
Required preconditions	The interrupts must have been enabled.
Called functions	None

This function Tests the corresponding bit in the Interrupt Pending 1 or 2 registers.

## Example:

This example illustrates how to test interrupt pending.

```
{
/*Send a message using object 0*/
CAN_SendMessage(0, &CanMsg)
/* Wait for the TX interrupt*/
while (!CAN_GetMsgInterruptStatus(0));
```

# 18.2.27 CAN\_GetMsgValidStatus

Function name	CAN_GetMsgValidStatus
Prototype	FlagStatus CAN_GetMsgValidStatus(u32 msgobj);
Behavior description	Tests the validity of a message object (ready to use).  A valid object means that it has been set up either as TX or as RX, and so is used by the hardware.
Input parameter	msgobj: The message object number, from 0 to 31.
Output parameter	None
Return Value	SET if the corresponding message object is valid, else RESET.
Required preconditions	None
Called functions	None

Note:

This function tests the corresponding bit in the Message Valid 1 or 2 registers.

## Example:

This example illustrates how to test the validity of message object 10.

```
{
if (CAN_GetMsgValidStatus(10))
{
   /* Do something with message object 10*/
}
}
```

# 18.2.28 CAN\_GetFlagStatus

Function name	CAN_GetFlagStatus
Prototype	FlasgStatus CAN_GetFlagStatus( u32 CAN_Flag);
Behavior description	Returns the state of the CAN flags: TxOK, RxOK, EPASS, EWARN and BOFF
Input parameter	One of the following: - CAN_SR_TXOK - CAN_SR_RXOK - CAN_SR_EPASS - CAN_SR_EWARN - CAN_SR_BOFF
Output parameter	None
Return Value	SET if the flag passed in parameter is set else RESET
Required preconditions	None
Called functions	None

## Example:

The following example illustrates how to read the Ewarning status of the CAN cell.

```
...
/* if CAN cell has reached the Ewarning status */
if (CAN_GetFlagStatus(CAN_SR_EWARN))
{
    /* Error handling*/
}
else
{
    /*continue */
}
...
}
```

# 18.2.29 CAN\_GetTransmitErrorCounter

Function name	CAN_GetTransmitErrorCounter
Prototype	u32 CAN_GetTransmitErrorCounter( void );
Behavior description	Returns the transmit error counter content
Input parameter	None
Output parameter	None
Return Value	Transmit Error Counter value
Required preconditions	None
Called functions	None

### Example:

The following example illustrates how to read the CAN transmit Error Counter .

```
{
...
/* raed the transmit error counter */
if (CAN_GetTransmitErrorCounter() > 10)
{
    /* Error handling */
}
...
}
```

# 18.2.30 CAN\_GetReceiveErrorCounter

Function name	CAN_GetReceiveErrorCounter
Prototype	u32 CAN_GetReceiveErrorCounter( void );
Behavior description	Returns the receive error counter content
Input parameter	None
Output parameter	None
Return Value	Receive Error Counter value
Called functions	None

### Example:

The following example illustrates how to read the CAN Receive Error Counter .

```
{
...
/* raed the receive error counter */
if (CAN_GetReceiveErrorCounter() > 20)
{
   /* Error handling*/
}
...
}
```

# 19 Analog-to-digital converter (ADC)

The 10-bit ADC is a simple successive approximation based ADC that has 8 analog inputs. The analog inputs are just a simple analog switch (mux). Only one channel can be active at a time.

# 19.1 ADC register structure

The ADC register structure ADC\_TypeDef is defined in the 91x\_map.h file as follows:

```
typedef struct
 vul6 CR;
  vu16 EMPTY1;
 vu16 CCR;
  vul6 EMPTY2;
 vu16 HTR;
  vu16 EMPTY3;
  vu16 LTR;
  vul6 EMPTY4;
  vu16 CRR;
  vu16 EMPTY5;
  vu16 DR0;
  vu16 EMPTY6:
  vu16 DR1;
 vul6 EMPTY7;
  vu16 DR2;
  vul6 EMPTY8;
  vu16 DR3;
  vul6 EMPTY9;
  vu16 DR4;
  vu16 EMPTY10;
  vu16 DR5;
  vu16 EMPTY11;
  vu16 DR6;
  vu16 EMPTY12;
  vu16 DR7;
  vu16 EMPTY13;
  vul6 PRS;
  vu16 EMPTY14;
  vu16 DDR;
 vu16 EMPTY15;
  vu16 CR2;
  vu16 EMPTY16;
} ADC_TypeDef;
```

#### Table 101. ADC registers

<u> </u>	
Register	Description
CR	Control Register
CCR	Channel Configuration Register
HTR	Higher Threshold Register
LTR	Lower Threshold Register
CRR	Compare Result Register

Table 101. ADC registers (continued)

Register	Description
DR0	Data Register for Channel 0
DR1	Data Register for Channel 1
DR2	Data Register for Channel 2
DR3	Data Register for Channel 3
DR4	Data Register for Channel 4
DR5	Data Register for Channel 5
DR6	Data Register for Channel 6
DR7	Data Register for Channel 7
PRS	Prescaler Value Register
DDR	ADC DMA Data Register
CR2	ADC Control Register 2

### The ADC is declared in the file below

```
#ifndef EXT
   #Define EXT extern
#endif
\verb|#define AHB_APB_BRDG1_U & (0x5C000000) /* AHB/APB Bridge 1 UnBuffered Space */ AH
#define AHB_APB_BRDG1_B
                                                                                                                  (0x4C000000) /* AHB/APB Bridge 1 Buffered Space */
#define APB_ADC_OFST
                                                                                                             (0x0000A000) /* Offset of ADC */
#ifndef Buffered
#define AHBAPB1_BASE
                                                                                                                               (AHB_APB_BRDG1_U)
#else /* Buffered */
#define AHBAPB1_BASE
                                                                                                                                 (AHB_APB_BRDG1_B)
/* ADC Base Address definition*/
#define ADC_BASE
                                                                                    (AHBAPB1_BASE + APB_ADC_OFST)
/* ADC peripheral declaration*/
#ifndef DEBUG
                                                                               ((ADC_TypeDef *) ADC_BASE)
#define ADC
#else
#ifdef _ADC
EXT ADC_TypeDef
                                                                                                              *ADC;
#endif /* _ADC */
 . . .
#endif
```

When debug mode is used, ADC pointer is initialized in *91x\_lib.c* file:

```
#ifdef _ADC
ADC = (ADC_TypeDef *)ADC_BASE
#endif /* _ADC */
```

\_ADC must be defined, in the  $\it 91x\_conf.h$  file, to access the peripheral registers as follows:  $\tt \#define\_ADC$ 

. . .

# 19.2 Firmware library functions

## Table 102. ADC library functions

Function name	Description
ADC_DeInit	Reset all the ADC registers to their default values.
ADC_StructInit	Reset all the Init struct parameters to their default values.
ADC_Init	Configure the ADC according to the input passed parameters.
ADC_PrescalerConfig	Configure the ADC prescaler value.
ADC_GetPrescalerValue	Get the ADC prescaler value.
ADC_GetFlagStatus	Check whether the specified ADC flag is set or not.
ADC_ClearFlag	Clear the ADC pending flags.
ADC_GetConversionValue	Read the result of conversion from the appropriate data register.
ADC_GetAnalogWatchdogResult	Return the result of the comparison on the selected Analog Watchdog.
ADC_ClearAnalogWatchdogResult	Clear result of the comparison on the selected Analog Watchdog.
ADC_GetWatchdogThreshold	Get the Higher or the Lower thresholds values of the watchdog.
ADC_ITConfig	Enable /Disable the specified ADC interrupts.
ADC_StandbyModeConfig	Enable/disable the standby mode.
ADC_Cmd	Power on or put in the Reset mode the ADC peripheral.
ADC_ConversionCmd	Start or stop the ADC conversion in the selected mode.
ADC_ExternalTrigConfig	Source and edge selection of external trigger.
ADC_ExternalTrigCmd	Enable or disable the external trigger feature.
ADC_DMACmd	Enable or disable the DMA request for ADC.
ADC_AutomaticClockGatedCmd	Enables or disables the Automatic clock gated mode( Only in Rev H).

# 19.2.1 ADC\_Delnit

Function name	ADC_DeInit
Function prototype	void ADC_DeInit(void)
Behavior description	Deinitializes the ADC peripheral registers to their default reset values.
Input parameter	None
Output parameter	None
Return parameter	None
Required preconditions	
Called functions	SCU_APBPeriphReset()

### Example:

/\* To initialize the ADC registers to their default values \*/  $\mbox{ADC\_DeInit()}\;;$ 

## 19.2.2 ADC\_StructInit

Function name	ADC_StructInit
Function prototype	void ADC_StructInit(ADC_InitTypeDef* ADC_InitStruct)
Behavior description	Fills each ADC_InitStruct member with its reset value.
Input parameter	ADC_InitStruct: pointer to a ADC_InitTypeDef structure which will be initialized.
Output parameter	None
Return parameter	None
Required preconditions	
Called functions	None

## Example:

/\* Initialize the ADC structure \*/
ADC\_StructInit(&ADC\_InitStruct);

## 19.2.3 ADC\_Init

Function name	ADC_Init
Function prototype	void ADC_Init(ADC_InitTypeDef* ADC_InitStruct)
Behavior description	Initializes the ADC peripheral according to the specified parameters in the ADC_InitStruct.
Input parameter	ADC_InitStruct: pointer to a ADC_InitTypeDef structure that contains the configuration information for the specified ADC peripheral. Refer to section "ADC_InitTypeDef on page 282" for more details on the allowed values of this parameter.
Output parameter	None
Return parameter	None
Required preconditions	
Called functions	None

## ADC\_InitTypeDef

### The ADC\_InitTypeDef structure is defined in the 91x\_ADC.h file:

```
typedef struct
{
  u16 ADC_WDG_High_Threshold;
  u16 ADC_WDG_Low_Threshold;
  u16 ADC_Channel_0_Mode;
  u16 ADC_Channel_1_Mode;
  u16 ADC_Channel_3_Mode;
  u16 ADC_Channel_3_Mode;
  u16 ADC_Channel_4_Mode;
  u16 ADC_Channel_5_Mode;
  u16 ADC_Channel_5_Mode;
  u16 ADC_Channel_5_Mode;
  u16 ADC_Channel_7_Mode;
  u16 ADC_Channel_7_Mode;
  u16 ADC_Select_Channel;
  FunctionalState ADC_Scan_Mode;
  u16 ADC_Conversion_Mode;
}ADC_InitTypeDef;
```

#### ADC\_WDG\_High\_Threshold

The high threshold value of the watchdog. It can be a value between 0 and 0x3FF.

#### ADC\_WDG\_Low\_Threshold

The low threshold value of the watchdog. It can be a value between 0 and ADC\_WDG\_High\_Threshold.

#### ADC\_Channel\_i\_Mode

The channel i conversion mode. It can take one of the following values.

ADC_Channel_i_Mode	Meaning
ADC_NoThreshold_Conversion	Channel i is converted without watchdog
ADC_HighThreshold_Conversion	Channel i is converted with watchdog on the higher threshold
ADC_LowThreshold_Conversion	Channel i is converted with watchdog on the lower threshold
ADC_NoConversion	Channel i is never converted

### ADC\_Select\_Channel

The channel to be converted when scan mode is disabled. It can be one of the following values.

ADC_Select_Channel	Meaning
ADC_Channel_0	ADC Channel 0
ADC_Channel_1	ADC Channel 1
ADC_Channel_2	ADC Channel 2
ADC_Channel_3	ADC Channel 3
ADC_Channel_4	ADC Channel 4
ADC_Channel_5	ADC Channel 5
ADC_Channel_6	ADC Channel 6
ADC_Channel_7	ADC Channel 7

### ADC\_Scan\_Mode

The scan mode status. It can be one of the following values.

ADC_Scan_Mode	Meaning
ENABLE	Scan mode is enabled, all the ADC inputs are converted.
DISABLE	Scan mode is disabled, only the selected channel is converted.

#### ADC\_Conversion\_Mode

The type of the conversion. It can be one of the following values.

ADC_Conversion_Mode	Meaning
ADC_Continuous_Mode	The conversion is restarted continuously
ADC_Single_Mode	One single conversion

#### Example:

# 19.2.4 ADC\_PrescalerConfig

Function name	ADC_PrescalerConfig
Function prototype	<pre>void ADC_PrescalerConfig(u8 ADC_Prescaler);</pre>
Behavior description	Configures the ADC prescaler value.
Input parameter	ADC_Prescaler: specifies the prescaler value. This parameter can be a value from 0x0 to 0xFF.
Output parameter	None
Return parameter	None
Required preconditions	
Called functions	None

## Example:

/\* Configure the ADC prescaler to 0xF \*/ ADC\_PrescalerConfig(0xF);

# 19.2.5 ADC\_GetPrescalerValue

Function name	ADC_GetPrescalerValue
Function prototype	u8 ADC_GetPrescalerValue(void);
Behavior description	Gets the ADC prescaler value.
Input parameter	None
Output parameter	None
Return parameter	The prescaler value.
Required preconditions	
Called functions	None

## Example:

```
u8 ADC_Prescaler;
/* Get the ADC prescaler value */
ADC_Prescaler = ADC_GetPrescalerValue();
```

# 19.2.6 ADC\_GetFlagStatus

Function name	ADC_GetFlagStatus
Function prototype	FlagStatus ADC_GetFlagStatus(u16 ADC_Flag)
Behavior description	Checks whether the specified ADC flag is set or not.
Input parameter	ADC_Flag: specifies the flag to check.  Refer to <i>Table 103: ADC_Flag parameter values</i> " for the allowed values of this parameter.
Output parameter	None
Return parameter	The new state of ADC_FLAG (SET or RESET).
Required preconditions	
Called functions	None

## Table 103. ADC\_Flag parameter values

Value	Meaning
ADC_FLAG_OV_CH_0	Conversion overflow status for channel 0
ADC_FLAG_OV_CH_1	Conversion overflow status for channel 1
ADC_FLAG_OV_CH_2	Conversion overflow status for channel 2
ADC_FLAG_OV_CH_3	Conversion overflow status for channel 3
ADC_FLAG_OV_CH_4	Conversion overflow status for channel 4
ADC_FLAG_OV_CH_5	Conversion overflow status for channel 5
ADC_FLAG_OV_CH_6	Conversion overflow status for channel 6
ADC_FLAG_OV_CH_7	Conversion overflow status for channel 7
ADC_FLAG_ECV	End of conversion status
ADC_FLAG_AWD	Analog watchdog status

## Example:

```
/* To get the end of conversion flag */
FlagStatus ADC_ECV_Status;
ADC_ECV_Status = ADC_GetFlagStatus(ADC_FLAG_ECV);
```

# 19.2.7 ADC\_ClearFlag

Function name	ADC_ClearFlag
Function prototype	void ADC_ClearFlag(16 ADC_Flag)
Behavior description	Clears the ADC pending flags.
Input parameter	ADC_Flag: specifies the flag to clear.  Refer to <i>Table 104: ADC_Flag parameter values</i> " for the allowed values of this parameter.
Output parameter	None
Return parameter	None
Required preconditions	
Called functions	None

## ADC\_Flag

To clear ADC flags, use a combination of one or more of the following values:

Table 104. ADC\_Flag parameter values

Value	Meaning
ADC_FLAG_ECV	End of conversion status
ADC_FLAG_AWD	Analog watchdog status
ADC_FLAG_ORD	DMA overrun status

#### Example:

/\* To clear the end of conversion flag \*/  $ADC\_ClearFlag(ADC\_FLAG\_ECV);$ 

# 19.2.8 ADC\_GetConversionValue

Function name	ADC_GetConversionValue
Function prototype	u16 ADC_GetConversionValue(u16 ADC_Channel)
Behavior description	Reads the result of conversion from the appropriate data register.
Input parameter	ADC_Channel: the corresponding channel of the ADC peripheral.  Refer to <i>Table 105: ADC channel parameter values</i> " for the allowed values of this parameter.
Output parameter	None
Return parameter	Returns the result of the conversion for the specific channel.
Required preconditions	
Called functions	None

## Table 105. ADC channel parameter values

Value	Meaning
ADC_Channel_0	ADC Channel 0
ADC_Channel_1	ADC Channel 1
ADC_Channel_2	ADC Channel 2
ADC_Channel_3	ADC Channel 3
ADC_Channel_4	ADC Channel 4
ADC_Channel_5	ADC Channel 5
ADC_Channel_6	ADC Channel 6
ADC_Channel_7	ADC Channel 7

#### Example:

```
/* To get the conversion value of channel 1 */
u16 ADC_Conversion_Value;
ADC_Conversion_Value = ADC_GetConversionValue(ADC_Channel_1);
```

# 19.2.9 ADC\_GetAnalogWatchdogResult

Function name	ADC_GetAnalogWatchdogResIt
Function prototype	FlagStatus ADC_GetAnalogWatchdogResult(u16 ADC_Channel)
Behavior description	Returns the result of the comparison on the selected Analog Watchdog
Input parameter	ADC_Channel: the corresponding channel of the ADC peripheral.  Refer to <i>Table 105: ADC channel parameter values on page 287</i> " for the allowed values of this parameter.
Output parameter	None
Return parameter	The state of the comparison (SET or RESET)
Required preconditions	
Called functions	None

## Example:

```
/* To get the watchdog result of channel 1 */
FlagStatus ADC_Analog_WDG_Status;
ADC_Analog_WDG_Status = ADC_GetAnalogWatchdogResult(ADC_Channel_1);
```

# 19.2.10 ADC\_ClearAnalogWatchdogResult

Function name	ADC_ClearAnalogWatchdogResult
Function prototype	void ADC_ClearAnalogWatchdogResult(u16 ADC_Channel)
Behavior description	Clear the result of the comparison on the selected Analog Watchdog
Input parameter	ADC_Channel: the corresponding channel of the ADC peripheral.  Refer to <i>Table 105: ADC channel parameter values on page 287</i> " for the allowed values of this parameter.
Output parameter	None
Return parameter	None
Required preconditions	
Called functions	None

# Example:

/\* To clear the watchdog result of the channel 2 \*/ ADC\_ClearAnalogWatchdogResult(ADC\_Channel\_2);

# 19.2.11 ADC\_GetWatchdogThreshold

Function name	ADC_GetWatchdogThreshold
Function prototype	u16 ADC_GetWatchdogThreshold(ADC_ThresholdType ADC_Threshold)
Behavior description	Gets the higher or the lower threshold values of the watchdog.
Input parameter	ADC_Threshold: The lower or the higher threshold.  Refer to <i>Table 106: ADC_ThresholdType parameter values</i> " for the allowed values of this parameter.
Output parameter	None
Return parameter	The selected threshold.
Required preconditions	
Called functions	None

# Table 106. ADC\_ThresholdType parameter values

Value	Meaning
ADC_HighThreshold	The high threshold of the watchdog
ADC_LowThreshold	The low threshold of the watchdog

#### Example:

/\* To get the high threshold of the watchdog\*/
u16 ADC\_High\_Threshold;
ADC\_High\_Threshold = ADC\_GetWatchdogThreshold(ADC\_HighTreshold);

# 19.2.12 ADC\_ITConfig

Function name	ADC_ITConfig	
Function prototype	<pre>void ADC_ITConfig(u16 ADC_IT, FunctionalState ADC_NewState)</pre>	
Behavior description	Enables or disables the specified ADC interrupts.	
Input parameter1	ADC_IT: specifies the ADC interrupt sources to be enabled or disabled. Refer to <i>Table 107: ADC_IT parameter values</i> " for the allowed values of this parameter.	
Input parameter2	ADC_NewState: new state of the specified ADC interrupts. This parameter can be: ENABLE or DISABLE.	
Output parameter	None	
Return parameter	None	
Required preconditions		
Called functions	None	

# ADC\_IT

To enable or disable ADC interrupts, use a combination of one or more of the following values:

Table 107. ADC\_IT parameter values

Value	Meaning
ADC_IT_ECV	End of conversion interrupt
ADC_IT_AWD	Analog watchdog interrupt
ADC_IT_ORD	Overun DMA Interrupt

### Example:

/\* To enable the end of conversion interrupt \*/  $\tt ADC\_ITConfig(ADC\_IT\_ECV, ENABLE);$ 

# 19.2.13 ADC\_StandbyModeCmd

Function name	ADC_StandbyModeCmd
Function prototype	void ADC_StandbyModeCmd(FunctionalState ADC_NewState)
Behavior description	Enables or disables ADC standby mode.
Input parameter	ADC_NewState: new state of the ADC standby mode. This parameter can be: ENABLE or DISABLE.
Output parameter	None
Return parameter	None
Required preconditions	
Called functions	None

### Example:

/\* To enable the standby mode \*/  $\mbox{ADC\_StandbyModeCmd}(\mbox{ENABLE});$ 

# 19.2.14 ADC\_Cmd

Function name	ADC_Cmd
Function prototype	void ADC_Cmd(FunctionalState ADC_NewState)
Behavior description	Powers on or puts the ADC peripheral in reset mode.
Input parameter	ADC_NewState: new state of the ADC peripheral. This parameter can be: ENABLE or DISABLE.
Output parameter	None
Return parameter	None
Required preconditions	
Called functions	None

### Example:

/\* To power on the ADC \*/
ADC\_Cmd(ENABLE);

# 19.2.15 ADC\_ConversionCmd

Function name	ADC_ConversionCmd
Function prototype	void ADC_ConversionCmd(u16 ADC_Conversion)
Behavior description	Start or stop the ADC conversion in the selected mode.
Input parameter	ADC_Conversion: the conversion command of the ADC peripheral.  Refer to <i>Table 108: ADC_Conversion parameter values</i> " for the allowed values of this parameter.
Output parameter	None
Return parameter	None
Required preconditions	
Called functions	None

# Table 108. ADC\_Conversion parameter values

Value	Meaning
ADC_Conversion_Start	Start the conversion
ADC_Conversion_Stop	Stop the conversion

### Example:

/\* To start the conversion \*/
ADC\_ConversionCmd(ADC\_Conversion\_Start);

# 19.2.16 ADC\_ExternalTrigConfig

Function name	ADC_ExternalTrigConfig
Function prototype	<pre>void ADC_ExternalTrigConfig(u16 ADC_ExtTrig_Src , u16 ADC_ExtTrig_Edge)</pre>
Behavior description	Source and edge selection of external trigger
Input parameter1	ADC_ExtTrig_Src: The ADC external trigger source Refer to <i>Table 109: ADC_ExtTrig_Src parameter values</i> " for the allowed values of this parameter.
Input parameter2	ADC_ExtTrig_Edge:The ADC external trigger edge Refer to <i>Table 110: ADC_ExtTrig_Edge parameter values</i> " for the allowed values of this parameter.
Output parameter	None
Return parameter	None
Required preconditions	
Called functions	None

# Table 109. ADC\_ExtTrig\_Src parameter values

Value	Meaning
ADC_PWM_Trig	PWM Trigger
ADC_TIM_Trig	Timer Trigger
ADC_PIN_Trig	External Trigger on Pin P4.7

# ADC\_ExtTrig\_Edge

The ADC external trigger edges that can be selected are listed in the following table:

Table 110. ADC\_ExtTrig\_Edge parameter values

Value	Meaning
Falling_ETE	Falling edge of trigger
Rising_ETE	Rising edge of trigger

### Example:

/\*External Pin trigger with rising edge\*/
ADC\_ExternalTrigConfig(ADC\_PIN\_Trig , Rising\_ETE);

# 19.2.17 ADC\_ExternalTrigCmd

Function name	ADC_ExternalTrigCmd
Function prototype	void ADC_ExternalTrigCmd(FunctionalState ADC_NewState)
Behavior description	Enable or disable the external trigger feature.
Input parameter	ADC_NewState: new state of the ADC external trigger . This parameter can be: ENABLE or DISABLE.
Output parameter	None
Return parameter	None
Required preconditions	
Called functions	None

# Example:

/\*Enable ADC external trigger\*/
ADC\_ExternalTrigCmd(ENABLE);

# 19.2.18 ADC\_DMACmd

Function name	ADC_DMACmd
Function prototype	<pre>void ADC_DMACmd(FunctionalState ADC_NewState);</pre>
Behavior description	Enables or disables the DMA request for ADC
Input parameter	ADC_NewState: new state of the ADC DMA . This parameter can be: ENABLE or DISABLE.
Output parameter	None
Return parameter	None
Required preconditions	
Called functions	None

### Example:

/\*Enable ADC-DMA Request\*/
ADC\_DMACmd(ENABLE);

# 19.2.19 ADC\_AutomaticClockGatedCmd

Function name	ADC_AutomaticClockGatedCmd
Function prototype	void ADC_AutomaticClockGatedCmd(FunctionalStateADC_NewState)
Behavior description	Enables or disables the Automatic clock gated mode( Only in Rev H)
Input parameter	ADC_NewState: new state of the ADC DMA . This parameter can be: ENABLE or DISABLE.
Output parameter	None
Return parameter	None
Required preconditions	
Called functions	None

# Example:

/\*Fast Trigger mode enable(in Rev H devices)\*/
ADC\_AutomaticClockGatedCmd(ENABLE);

# 20 AHB/APB Bridges (AHBAPB)

The AHB/APB bridge provides a completely asynchronous connection between the AHB with the APB buses. The AHB/APB clock ratio could be typically around 1/10. As a consequence, an APB read access will need more than 20 AHB cycle to be done.

The first section below describes the data structures used in the AHBAPB Firmware library. The second one presents the Firmware library functions.

# 20.1 AHBAPB register structure

The AHBAPB register structure *AHBAPB\_TypeDef* is defined in the *91x\_map.h* file as follows:

The following table presents the AHBAPB registers:

Table 111. AHBAPB register structure

Register	Description
AHBAPB_BSR	Bridge Status Register
AHBAPB_BCR	Bridge Configuration Register
AHBAPB_PAER	Peripheral Address Error Register

#### The 2 AHBAPB interfaces are declared in the same file:

```
#define AHB APB BRDG0 B
                           (0x48000000)
#define AHB_APB_BRDG1_B
                           (0x4C000000)
#define AHB_APB_BRDG0_U
                           (0x58000000)
#define AHB_APB_BRDG1_U
                           (0x5C000000)
#ifndef Buffered
#define AHBAPB0_BASE
                                (AHB_APB_BRDG0_U)
#define AHBAPB1_BASE
                                (AHB_APB_BRDG1_U)
#else /* Buffered */
#define AHBAPB0_BASE
                               (AHB_APB_BRDG0_B)
#define AHBAPB1_BASE
                               (AHB_APB_BRDG1_B)
#endif
#ifndef DEBUG
#define AHBAPB0
                               ((AHBAPB_TypeDef *)AHBAPB0_BASE)
#define AHBAPB1
                               ((AHBAPB_TypeDef *)AHBAPB1_BASE)
```

57

```
#else
...
#ifdef _AHBAPB0
EXT AHBAPB_TypeDef *AHBAPB0;
#endif /* _AHBAPB0 */

#ifdef _AHBAPB1
EXT AHBAPB_TypeDef *AHBAPB1;
#endif /*_AHBAPB1 */
```

When debug mode is used, the AHBAPB pointer is initialized in the *91x\_lib.c* file:

```
#ifdef _AHBAPB0
AHBAPB0 = (AHBAPB_TypeDef *)AHBAPB0_BASE;
#endif /*_AHBAPB0 */
#ifdef _AHBAPB1
AHBAPB1 = (AHBAPB_TypeDef *)AHBAPB1_BASE;
#endif /*_AHBAPB1 */
```

\_AHBAPB, \_AHBAPB0, \_AHBAPB1 must be defined, in the *91x\_conf.h* file, to access the peripheral registers as follows:

```
#define _AHBAPB
#define _AHBAPB0
#define _AHBAPB1
```

# 20.2 Firmware library functions

### Table 112. AHBAPB library functions

Function name	Description
AHBAPB_DeInit	Deinitializes the AHBAPBx peripheral registers to their default reset values.
AHBAPB_Init	Initializes the AHBAPBx peripheral according to the specified parameters in the AHBAPB_InitStruct.
AHBAPB_StructInit	Fills each AHBAPB_InitStruct member with its reset value.
AHBAPB_GetFlagStatus	Checks whether the specified AHBAPB flag is set or not.
AHBAPB_ClearFlag	Clears the AHBAPBx's pending flags.
AHBAPB_GetPeriphAddrError	Gets the AHBAPB error address peripherals.

# 20.2.1 AHBAPB\_Delnit

Function name	AHBAPB_DeInit
Function prototype	void AHBAPB_DeInit(AHBAPB_TypeDef* AHBAPBx)
Behavior description	Deinitializes the AHBAPBx peripheral registers to their default reset values.
Input parameter	AHBAPBx: where x can be 0 or1 to select the AHBAPB peripheral.
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

#### **Example:**

/\*Deinitializes the AHPABP0 peripheral registers to their default reset values\*/AHBAPB\_DeInit(AHBAPB0);

# 20.2.2 AHBAPB\_Init

Function name	AHBAPB_Init
Function prototype	void AHBAPB_Init(AHBAPB_TypeDef* AHBAPBx, AHBAPB_InitTypeDef* AHBAPB_InitStruct)
Behavior description	Initializes the AHBAPBx peripheral according to the specified parameters in the AHBAPB_InitStruct.
Input parameter1	AHBAPBx: where x can be 0 or1 to select the AHBAPB peripheral.
Input parameter2	AHBAPB_InitStruct: pointer to an AHBAPB_InitTypeDef structure that contains the configuration information for the specified AHBAPB peripheral. Refer to section "AHBAPB_InitTypeDef on page 298" for more details on the allowed values of this parameter.
Output parameter	None
Return parameter	None
Required preconditions	None
Called functions	None

# AHBAPB\_InitTypeDef

The AHBAPB\_InitTypeDef structure is defined in the *91x\_AHBAPB.h* file:

```
typedef struct
{
u32 AHBAPB_Error;
  u32 AHBAPB_SetTimeOut;
u32 AHBAPB_Split;
  u8 AHBAPB_SplitCounter;
} AHBAPB_InitTypeDef;
```

#### AHBAPB\_SetTimeOut

Sets the Time-out, in terms of APB clock periods, that the bridge can wait for a target completion, before asserting the time-out error, allowed values are from 0 to 31. When the time-out counter = 0, is disabled.

5//

#### AHBAPB Error

Enables or disables error generation.

This member can be one of the following values:

AHBAPB_Error	Meaning
AHBAPB_Error_Enable	Enables error generation.
AHBAPB_Error_Disable	Disable error generation.

Note:

If AHBAPB\_Error\_Disable is used, AHBAPB\_SetTimeOut struct member has no effect.

### AHBAPB Split

Enables or disables accesses to be split after the number of AHB cycles.

This member can be one of the following values:

AHBAPB_Split	Meaning
AHBAPB_Split_Enable	Enable accesses to be split after the number of AHB cycles.
	Disable accesses to be split after the number of AHB cycles. The bridge will provide the bus with HREADY or a timeout condition

Note:

If AHBAPB\_Split\_Disable is used, AHBAPB\_SplitCounter struct member has no effect.

#### AHBAPB\_SplitCounter

Sets the number of AHB cycle to be performed before returning a split to the arbiter.

Allowed values are from 0 to 31.

#### Example:

```
/* Configure AHBAPB0 bridge */
AHBAPB_InitTypeDef AHBAPB_InitStructure;
AHBAPB_InitStructure.AHBAPB_SetTimeOut = 0x0F;
AHBAPB_InitStructure.AHBAPB_Error= AHBAPB_Error_Enable;
AHBAPB_InitStructure.AHBAPB_Split = AHBAPB_Split_Enable;
AHBAPB_InitStructure.AHBAPB_SplitCounter = 0x0E;
AHBAPB_Init(AHBAPB0, &AHBAPB_InitStructure);
```

### 20.2.3 AHBAPB\_StructInit

Function name	AHBAPB_StructInit
Function prototype	void AHBAPB_StructInit(AHBAPB_InitTypeDef* AHBAPB_InitStruct)
Behavior description	Fills each AHBAPB_InitStruct member with its reset value.
Input parameter	AHBAPB_InitStruct: pointer to a AHBAPB_InitTypeDef structure which will be initialized.
Output parameter	None
Return parameter	None

57

Required preconditions	None
Called functions	None

The AHBAPB\_InitStruct members default values are as follows:

Member	Default value
AHBAPB_Split	AHBAPB_Split_Enable
AHBAPB_SplitCounter	0xFF
AHBAPB_Error	AHBAPB_Error_Enable
AHBAPB_SetTimeOut	0xFF
AHBAPB_IsoFrequency	AHBAPB_IsoFrequency_Enable

### Example:

/\*Initialize the AHBAPBO Init Structure parameters\*/
AHBAPB\_InitTypeDef AHBAPB\_InitStruct;
AHBAPB\_StructInit(AHBAPB\_InitStructure);

# 20.2.4 AHBAPB\_GetFlagStatus

Function name	AHBAPB_GetFlagStatus	
Function prototype	GetFlagStatus AHBAPB_FlagStatus(AHBAPB_TypeDef* AHBAPBx, u8 AHBAPB_FLAG)	
Behavior description	Checks whether the specified AHBAPB flag is set or not.	
Input parameter1	AHBAPBx: where x can be 0 or 1 to select the AHBAPB peripheral.	
Input parameter2	AHBAPB_FLAG: specifies the flag to check.  Refer to <i>Table 113: AHBAPB_FLAG parameter values</i> for the allow values of this parameter.	
Output parameter	None	
Return parameter	The new state of AHBAPB_FLAG (SET or RESET).	
Required preconditions	None.	
Called functions	None.	

### Table 113. AHBAPB\_FLAG parameter values

Value	Meaning
AHBAPB_FLAG_ERROR	A previous access has been aborted because it generates an error.
AHBAPB_FLAG_OUTM	An access out of memory has been attempted.
AHBAPB_FLAG_APBT	A peripheral did not answer before the time out.
AHBAPB_FLAG_RW	The type of access that generate the error conditions: read/write.

#### Example:

```
/* Get the error flag status */
FlagStatus Status;
Status = AHBAPB_GetFlagStatus(AHBAPB0, AHBAPB_FLAG_ERROR);
```

# 20.2.5 AHBAPB\_ClearFlag

Function name	AHBAPB_ClearFlag	
Function prototype	void AHBAPB_ClearFlag(AHBAPB_TypeDef* AHBAPBx, u8 AHBAPB_FLAG)	
Behavior description	Clears the AHBAPBx's pending flags.	
Input parameter1	AHBAPBx: where x can be 0,1 to select the AHBAPB peripheral.	
Input parameter2	AHBAPB_FLAG: specifies the flag to clear. To clear AHBAPB flags, us a combination of one or more of the values in <i>Table 114:</i> AHBAPB_FLAG parameter values.	
Output parameter	None	
Return parameter	None	
Required preconditions	None	
Called functions	None	

# Table 114. AHBAPB\_FLAG parameter values

AHBAPB_FLAG	Meaning
AHBAPB_FLAG_ERROR	A previous access has been aborted because it generates an error.
AHBAPB_FLAG_OUTM	An access out of memory has been attempted.
AHBAPB_FLAG_APBT	A peripheral did not answer before the time out.

#### Example:

/\* Clear the AHBAPB0 error flag\*/
AHBAPB\_ClearFlag(AHBAPB0, AHBAPB\_FLAG\_ERROR);

# 20.2.6 AHBAPB\_GetPeriphAddrError

Function name	AHBAPB_GetPeriphAddrError	
Function prototype	u32 AHBAPB_GetPeriphAddr(AHBAPB_TypeDef* AHBAPBx)	
Behavior description	Gets the AHBAPB peripheral address error.	
Input parameter	AHBAPBx: where x can be 0,1 to select the AHBAPB peripheral.	
Output parameter	None	
Return parameter	AHBAPB peripheral address error.	
Required preconditions	None	
Called functions	None	

#### Example:

/\* return AHBAPB0 pheripheral address error \*/
AHBAPB\_GetPeriphAddrError(AHBAPB0);

577

Revision history UM0233

# 21 Revision history

Table 115. Document revision history

Date	Revision	Changes
15-May-2006	1	Initial release.
28-May-2007	2	Section 8: Vectored interrupt controller (VIC) updated. Section 9: Wake-up interrupt unit (WIU) updated. Section 12: 16-bit timer (TIM) updated. Section 13: DMA controller (DMA) updated. Section 14: Synchronous serial peripheral (SSP) updated. Section 15: Universal asynchronous receiver transmitter (UART) updated.
21-Jan-2008	3	Section 4: Flash memory interface (FMI) updated. Section 5: External memory interface (EMI) updated. Section 6: System control unit (SCU) updated. Section 7: General purpose I/O ports (GPIO) updated. Section 11: Watchdog timer (WDG) updated. Section 12: 16-bit timer (TIM) updated. Section 13: DMA controller (DMA) updated. Section 17: 3-phase induction motor controller (MC) updated. Section 18: Controller area network (CAN) updated. Section 19: Analog-to-digital converter (ADC) updated.
05-Feb-2009	4	Modified Figure 1: Firmware library directory structure on page 18 Updated Section 6.1.1: SCU register structure on page 50 Modified Section 8.2.9: VIC_GetISRVectAdd on page 90 Removed function WDG Deinit in Section 11: Watchdog timer (WDG)

#### Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST's terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST'S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

UNLESS EXPRESSLY APPROVED IN WRITING BY AN AUTHORIZE REPRESENTATIVE OF ST, ST PRODUCTS ARE NOT DESIGNED, AUTHORIZED OR WARRANTED FOR USE IN MILITARY, AIR CRAFT, SPACE, LIFE SAVING, OR LIFE SUSTAINING APPLICATIONS, NOR IN PRODUCTS OR SYSTEMS, WHERE FAILURE OR MALFUNCTION MAY RESULT IN PERSONAL INJURY, DEATH, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

© 2009 STMicroelectronics - All rights reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com

