KAUNAS UNIVERSITY OF TECHNOLOGY

THE FIRST PRPICNICPLE OF DIGITAL LOGIC

LAB 1: Latches and Flip-flops

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Introductory Theory:

- In digital logic a flip-flop or latch is a circuit that has two stable states and can be used to store information. It is the most basic memory element that can store one bit of information. The circuit can be made to change state by signals applied to control inputs and will have one or two outputs. There are several types of latches (flip-flops) according to control inputs. In practice common types are SR, JK, D and T.

In this laboratory work, we are going to show the D type.
Assignment number 21

- D Latch

D latches, as well as all other types of latches, are made from a simple SR latch. Gated D latches are made by connecting a complement of S (S) signal to input R as shown in Figure 1.

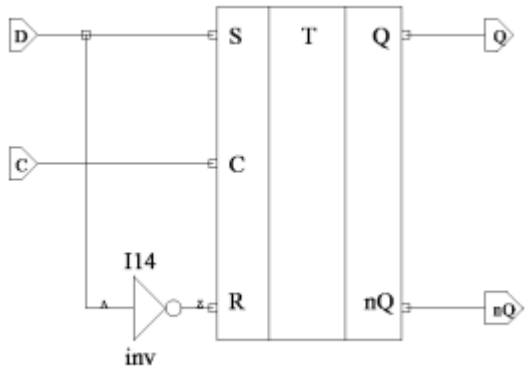


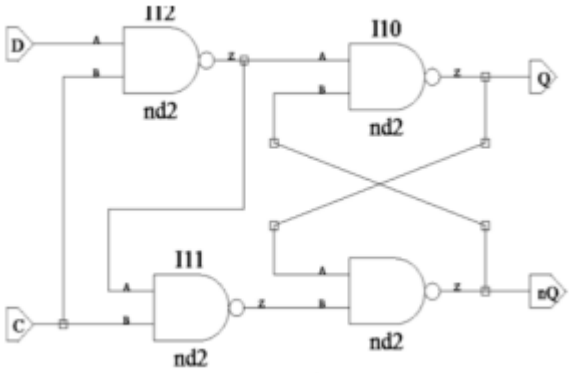
Figure 1.

This type of latch has one input - D (data) and a synchronization signal C (clock). When C = 1 signal propagates directly from the input D to the output Q. When C = 0 a latch holds the state that was last set in active mode. A truth table for D latch is presented in Table 1.

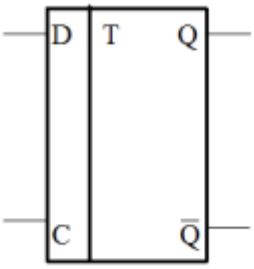
C	D	Q_t	Q_{t+1}	**Action**
0	x	0	0	Hold state
0	x	1	1	
1	0	0	0	Set output
1	0	1	0	
1	1	0	1	
1	1	1	1	

Table 1

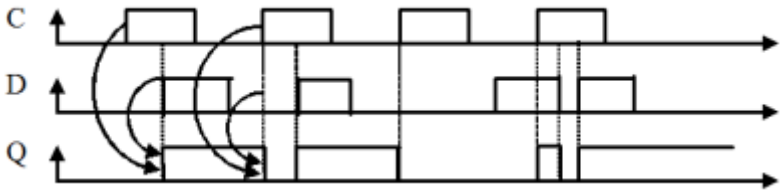
Characteristic equation of a D type gated latch is: Qt+1 = !CQt ∪ CD.
where !CQt represents holding the current state and CD shows ”next” state’s dependency on the D value, when C = 1.



Schematic of D Latch



Symbol of D Latch



Timing Diagram of D Latch

- **Master-Slave Latch:**

A masterâĂŞslave latch is created by connecting two gated SR latches in series, and inverting the synchronization (clock) signal to one of them, as shown in Figure 3.9. The name masterâĂŞslave comes from the second latch (slave) being responsive from the change in the first (master) latch. This type is often called MS latch.

- **Flip Flops:**

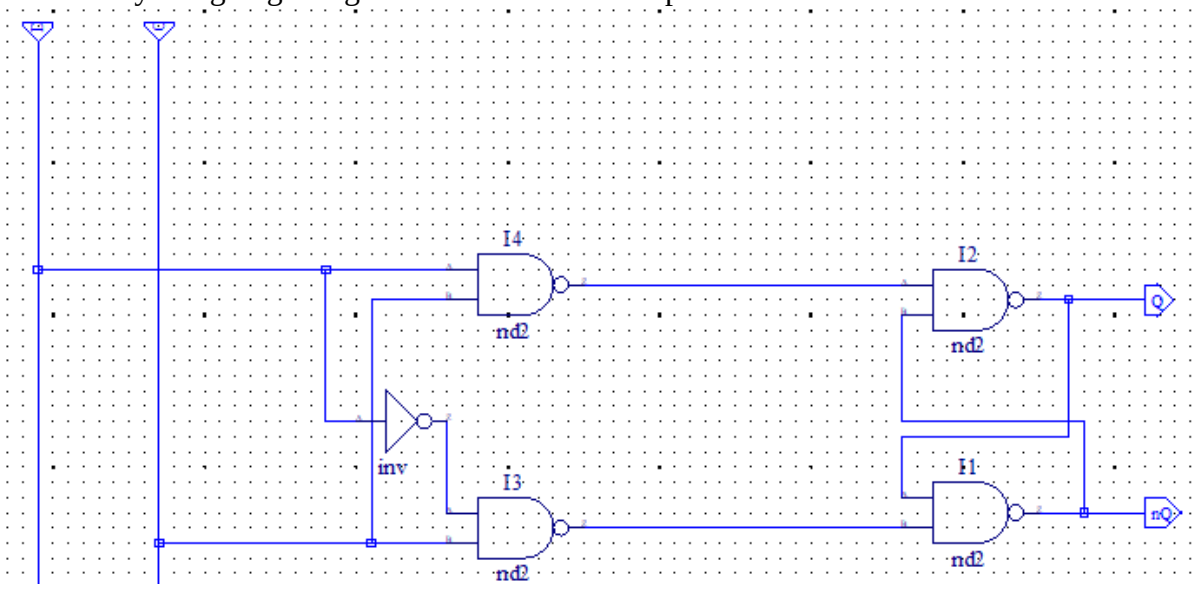
The word latch is mainly used for level-sensitive memory elements, whereas a flip-flop is edge-sensitive. That is, when a latch is enabled it becomes transparent, while a flip flop’s output only changes when clock goes form 0 to 1 (positive-edge) or from 1 to 0 (negative edge).

Implementation:

Design process for a Latches and Flip-Flops:

1. Design a gated latch D
2. Design a master-slave gated latch of type D
3. Design a flip flop of type D
4. Connect the schematic, using D flip-flop from elements library (use fd1sdx from Lattice Diamond). Determine functionality of the circuit.

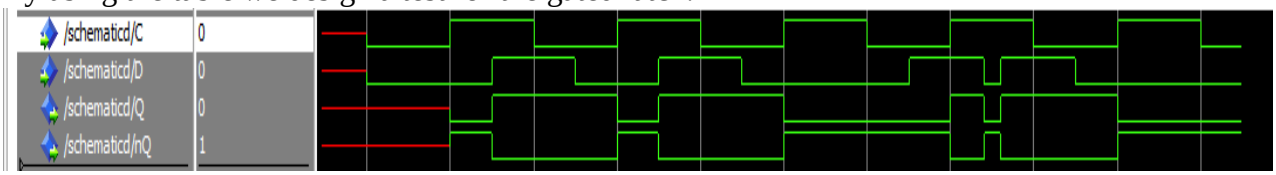
We start by designing a D gated latch with a data input D and clock C.



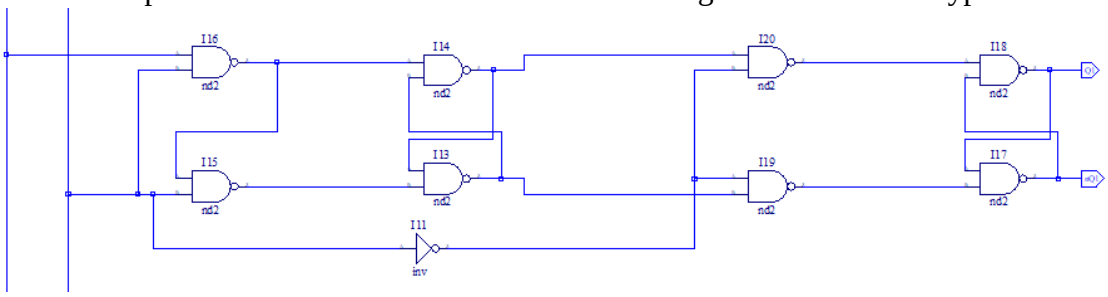
The functionality of the latch is described by the D latch truth table:

C	D	Q_t	Q_{t+1}	**Action**
0	x	0	0	Hold state
0	x	1	1	
1	0	0	0	Set output
1	0	1	0	
1	1	0	1	
1	1	1	1	

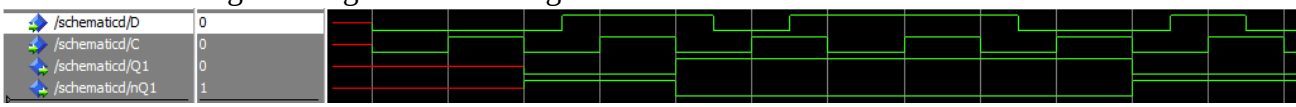
By using the table we design a test for the gated latch.



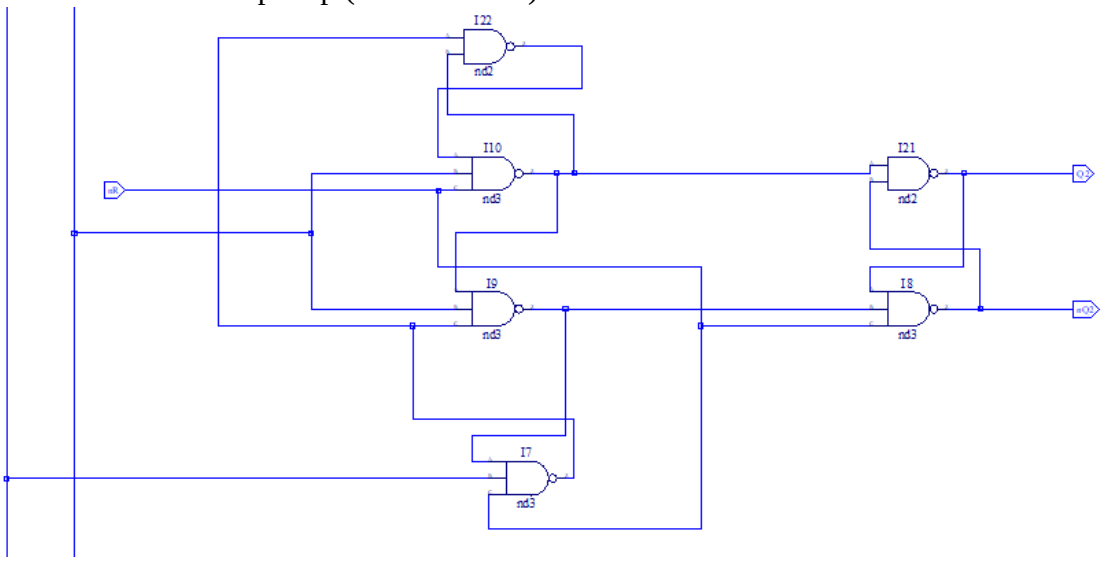
For the completion of the next exercise we have to design a Master-Slave type D latch.



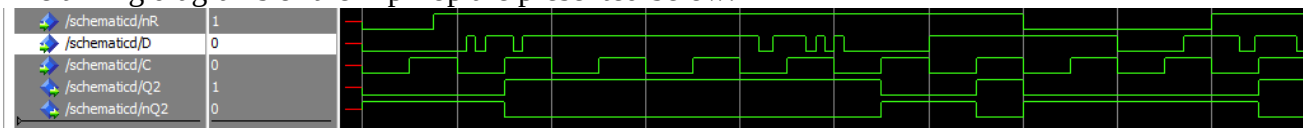
Once a test is designed we get the following simulation results:



The schematic of a flip-flop (D in this case):

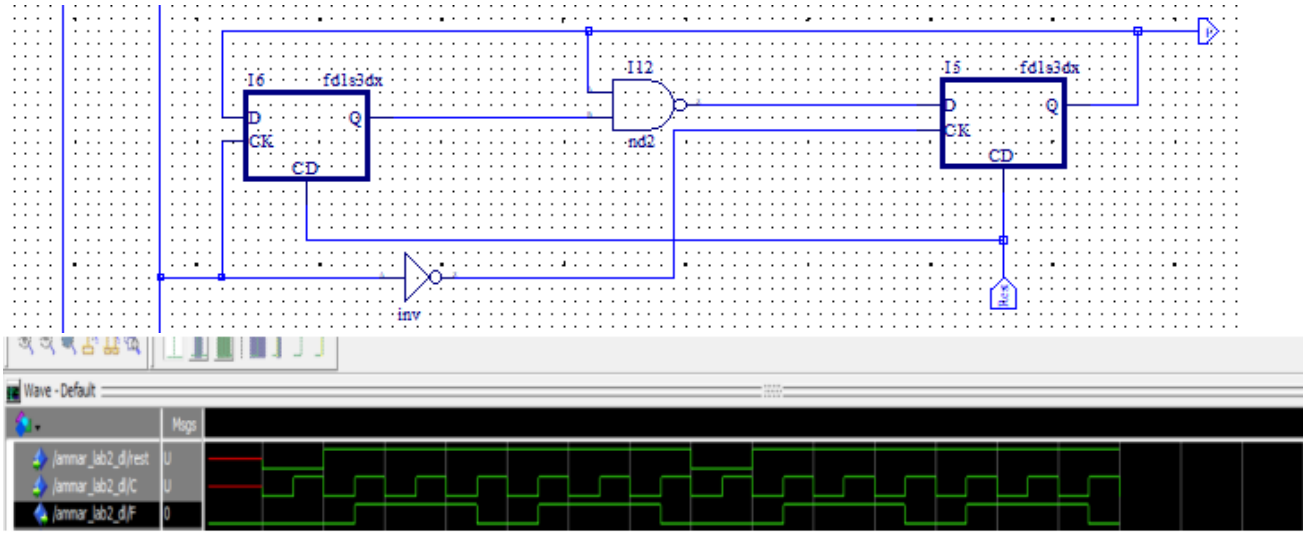


The timing diagrams of the flip flop are presented below:

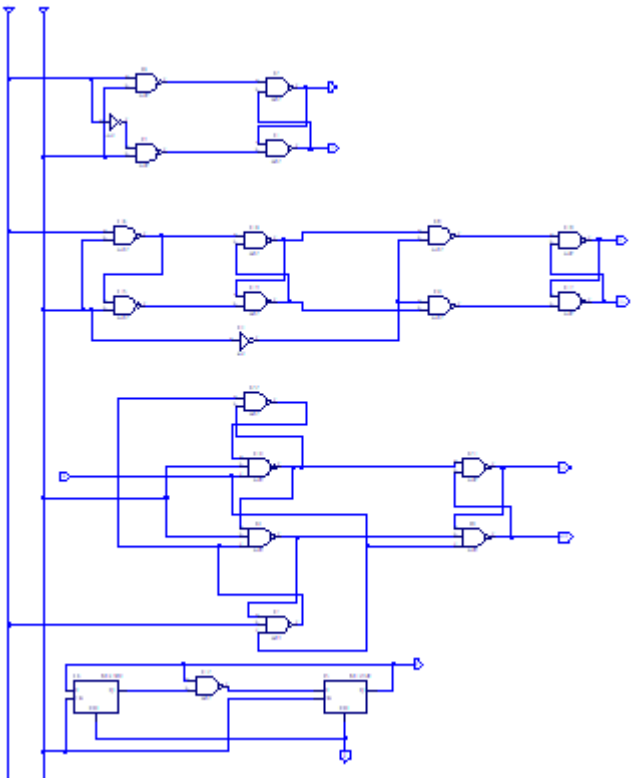


We shall use D type flip-flop from elements library in the next Exercise. The C input of the circuit is connected to a single source.

We also note that the frequency of the clock signal C is thrice the frequency of the output signal F.



Whole Schematic:



Conclusion :

To conclude, in this Laboratory work we designed the schematics of the circuit of an D gated latch, D master-slave gated latch, a D Flip-Flop and a circuit using D flip-flop from elements library (using fd1sdx from Lattice Diamond). Also, by running and analysing the simulation we understand the applications of latches and Flip-Flops and how they are being used as a frequency divider and as a Storage device.