KAUNAS UNIVERSITY OF TECHNOLOGY

THE FIRST PRPICNICPLE OF DIGITAL LOGIC

LAB 4: Counters

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TASK:

Assignment	Initial value	Increment	M1	Initial value	Increment	M2	M3
25	1	4	9	1	4	17	153

OBJECTIVE:

The objective of this laboratory work is to analyze digital counters operations and the way they are executed by designing asynchronous up counter with parallel-load and carry-out. By a specific modulus number which is specified to each student by a given table. Also, to design higher modulus-Nsk counter using two previously designed mod-N counters.

Theory:

_Counters are sequential circuits (devices with memory) that follow the binary sequence upon occurrence of input impulse. Up counters perform operation C := C + 1, in other words increase in its value by 1, Down counters perform C := C − 1 or decreases by 1. An n-bit binary counter consists of n flip-flops and can count in binary form 0 to 2n − 1. To take it other way around, if you design a counter to count up to a number M, the number of flip-flops needed are m ≥ blog2Mc. Often counter have an carry-out signal that show when counter reaches its maximum value. This signal can be used as input pulse for an other counter and enlarge overall counting value. Digital counters come in two categories: ripple counters and synchronous counters. In ripple counters, the flip-flop output transition serves as a source for triggering other flip-flops. In a synchronous counters, the input pulse are applied to clock inputs of all flip-flops. The change of state of a particular flip-flop is dependent on the present state of other flip-flops. A binary ripple counter consists of a series type D flip-flops with the inverted output of each flip-flop connected to the clock input of the next higher-order (more significant) flip-flop. A 3-bit counter is shown in Fig. 5.1, its maximum value is M = 23 . In this schematic an input R(R − reset) sets initial value of zero, an input Cnt(Cnt − count) increases value by 1 on a rising edge.

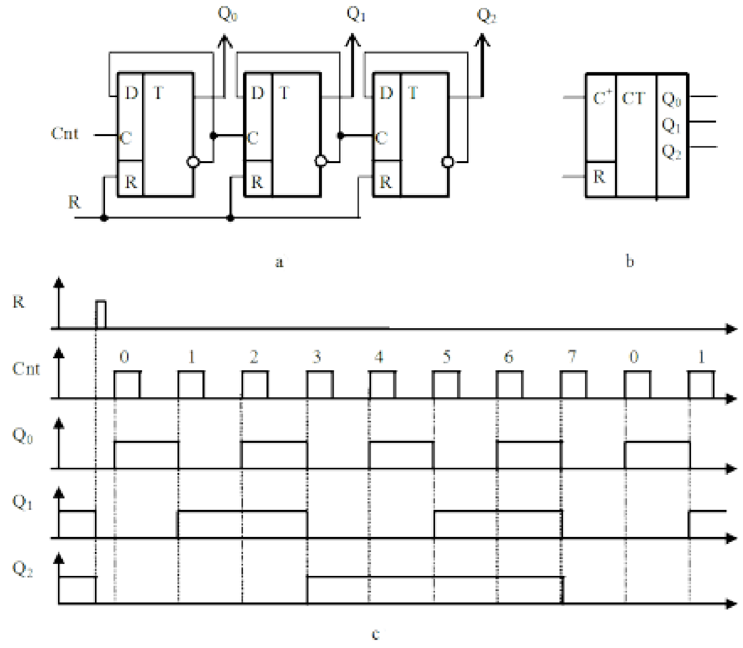


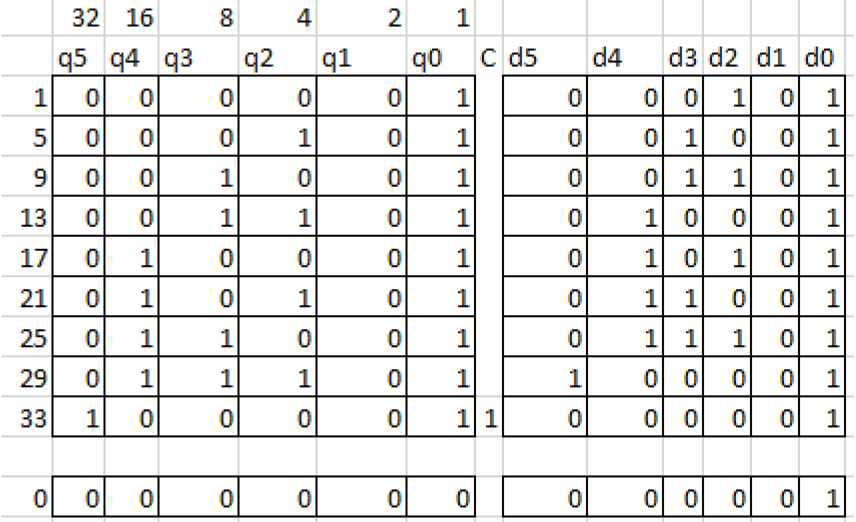
Figure 5.1: A schematic of 3-bit ripple counter (a), a symbol (b), a timing diagram (c)

A modulo-N (abbreviated mod-N) counter is a counter that goes through a repeated sequence of N counts. For example, a 3-bit counter is a mod-8 counter. In some applications, it is desired to have counter where modulus is not in power of 2. In this case a combinational logic to for flip-flop inputs is needed. A mod-N counter is usually implemented as synchronous, using type D flip-flops. For example, we need to design a mod-6 up counter with a carry-out signal (P).

PROCEDURE:

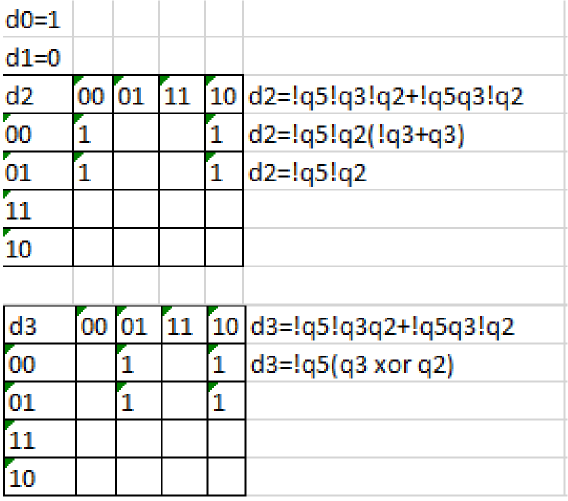
First Counter M1:

According to given formula a truth table for the first counter is presented below:

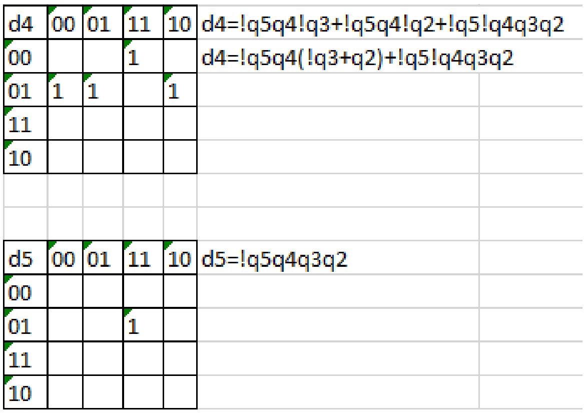


	32	16	8	4	2	1							
	q5	q4	q3	q2	q1	q0	C	d5	d4	d3	d2	d1	d0
1	0	0	0	0	0	1		0	0	0	1	0	1
5	0	0	0	1	0	1		0	0	1	0	0	1
9	0	0	1	0	0	1		0	0	1	1	0	1
13	0	0	1	1	0	1		0	1	0	0	0	1
17	0	1	0	0	0	1		0	1	0	1	0	1
21	0	1	0	1	0	1		0	1	1	0	0	1
25	0	1	1	0	0	1		0	1	1	1	0	1
29	0	1	1	1	0	1		1	0	0	0	0	1
33	1	0	0	0	0	1	1	0	0	0	0	0	1
0	0	0	0	0	0	0		0	0	0	0	0	1

Using the table, we can form functions for each flip-flop data input:



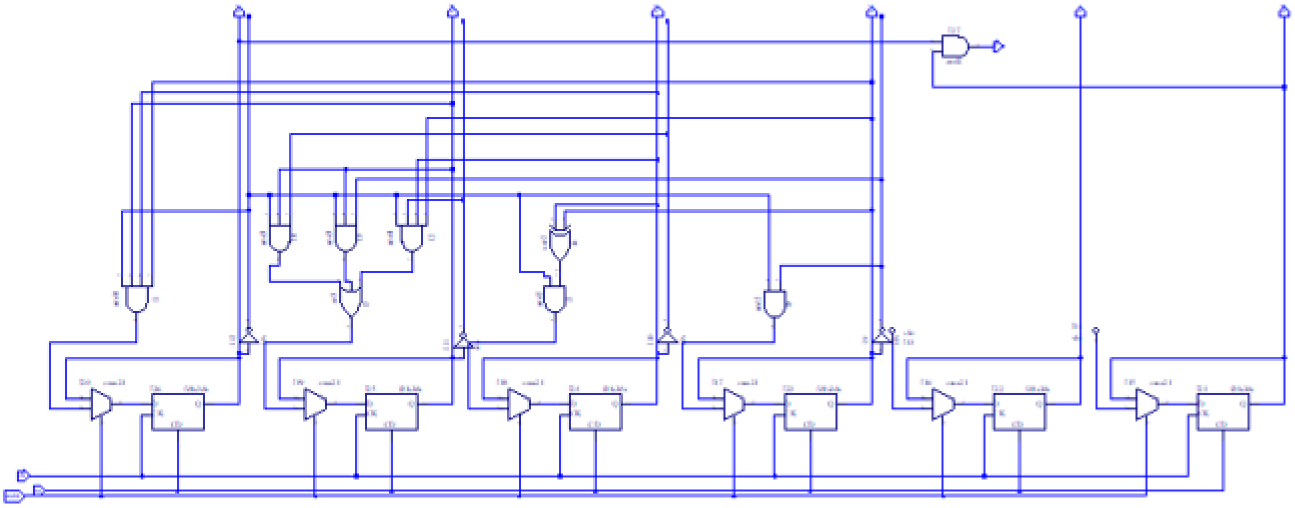
d0=1					
d1=0					
d2	00	01	11	10	d2=!q5!q3!q2+!q5q3!q2
00	1			1	d2=!q5!q2(!q3+q3)
01	1			1	d2=!q5!q2
11					
10					
d3	00	01	11	10	d3=!q5!q3q2+!q5q3!q2
00		1		1	d3=!q5(q3 xor q2)
01		1		1	
11					
10					



d4	00	01	11	10	d4=!q5q4!q3+!q5q4!q2+!q5!q4q3q2
00			1		d4=!q5q4(!q3+q2)+!q5!q4q3q2
01	1	1		1	
11					
10					

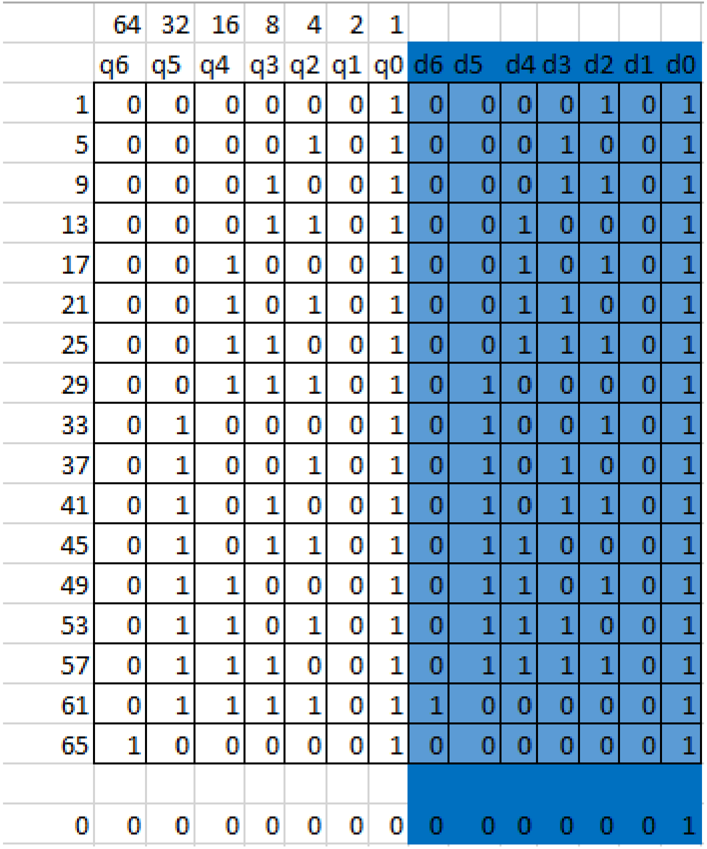
d5	00	01	11	10	d5=!q5q4q3q2
00					
01			1		
11					
10					

A schematic for the counter implemented using these functions is shown below:



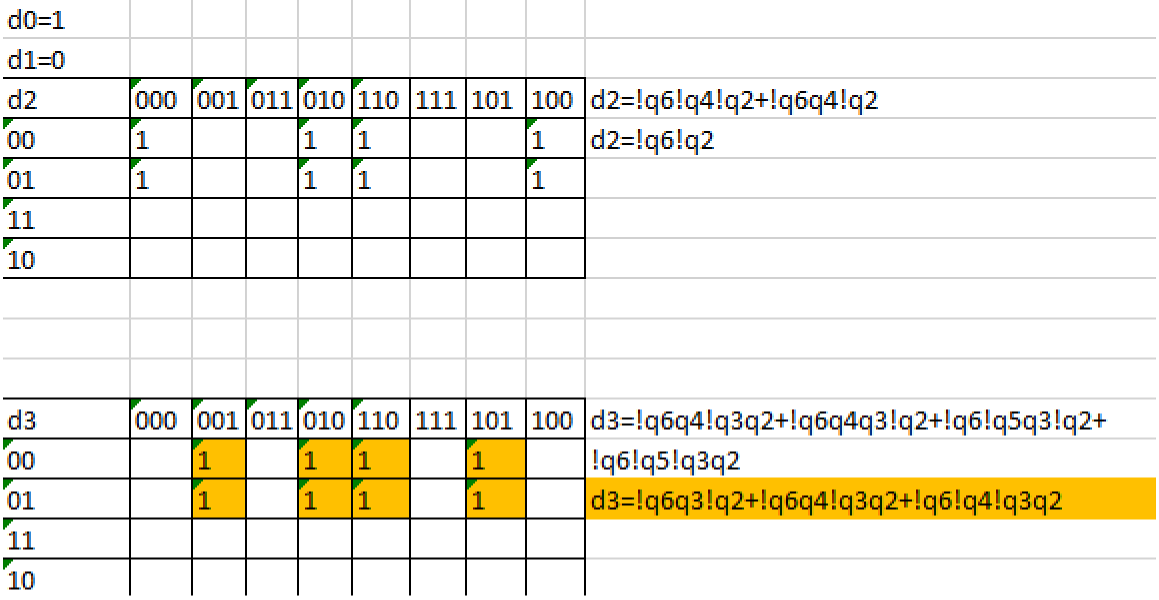
Second counter M2:

A truth table for the first counter is presented below:

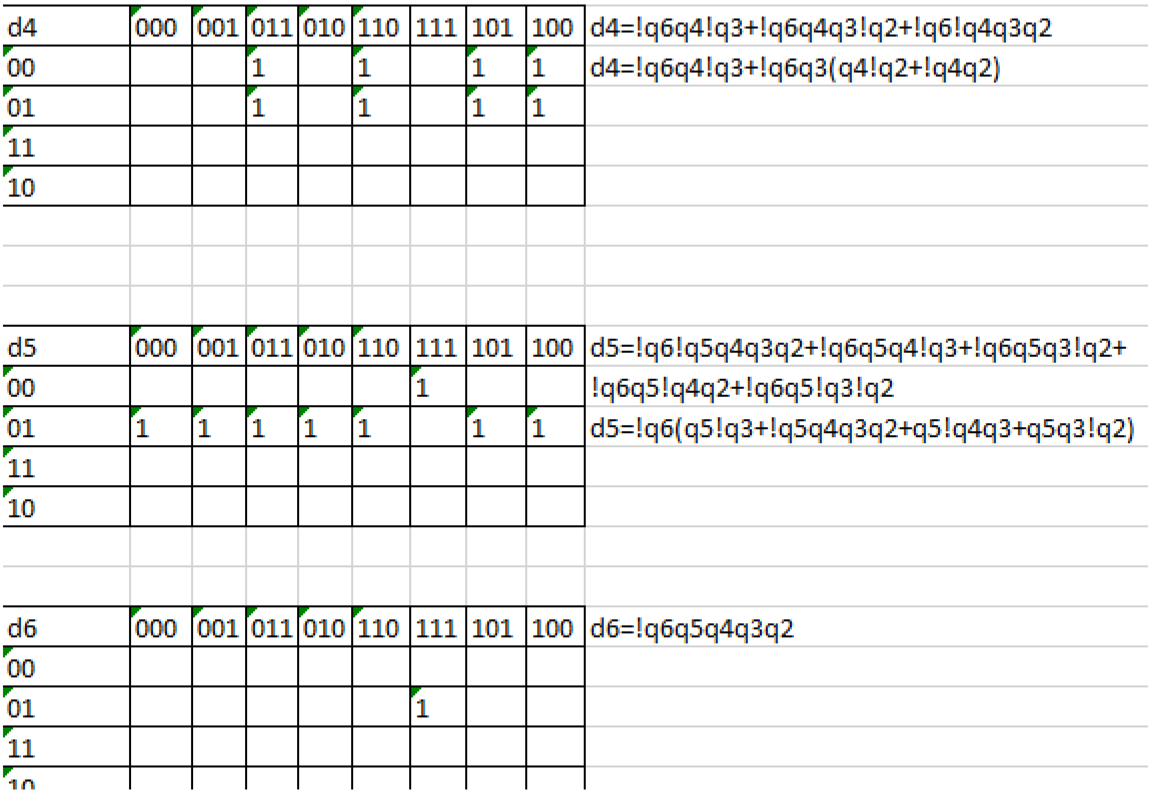


	64	32	16	8	4	2	1							
	q6	q5	q4	q3	q2	q1	q0	d6	d5	d4	d3	d2	d1	d0
1	0	0	0	0	0	0	1	0	0	0	0	1	0	1
5	0	0	0	0	1	0	1	0	0	0	1	0	0	1
9	0	0	0	1	0	0	1	0	0	0	1	1	0	1
13	0	0	0	1	1	0	1	0	0	1	0	0	0	1
17	0	0	1	0	0	0	1	0	0	1	0	1	0	1
21	0	0	1	0	1	0	1	0	0	1	1	0	0	1
25	0	0	1	1	0	0	1	0	0	1	1	1	0	1
29	0	0	1	1	1	0	1	0	1	0	0	0	0	1
33	0	1	0	0	0	0	1	0	1	0	0	1	0	1
37	0	1	0	0	1	0	1	0	1	0	1	0	0	1
41	0	1	0	1	0	0	1	0	1	0	1	1	0	1
45	0	1	0	1	1	0	1	0	1	1	0	0	0	1
49	0	1	1	0	0	0	1	0	1	1	0	1	0	1
53	0	1	1	0	1	0	1	0	1	1	1	0	0	1
57	0	1	1	1	0	0	1	0	1	1	1	1	0	1
61	0	1	1	1	1	0	1	1	0	0	0	0	0	1
65	1	0	0	0	0	0	1	0	0	0	0	0	0	1
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Using the table, we can form functions for each flip-flop data input:



d0=1									
d1=0									
d2	000	001	011	010	110	111	101	100	d2=!q6!q4!q2+!q6q4!q2
00	1			1	1			1	d2=!q6!q2
01	1			1	1			1	
11									
10									
d3	000	001	011	010	110	111	101	100	d3=!q6q4!q3q2+!q6q4q3!q2+!q6!q5q3!q2+
00		1		1	1		1		!q6!q5!q3q2
01		1		1	1		1		d3=!q6q3!q2+!q6q4!q3q2+!q6!q4!q3q2
11									
10									



d4	000	001	011	010	110	111	101	100
00			1		1		1	1
01			1		1		1	1
11								
10								

d4=!q6q4!q3+!q6q4q3!q2+!q6!q4q3q2

d4=!q6q4!q3+!q6q3(q4!q2+!q4q2)

d5	000	001	011	010	110	111	101	100
00						1		
01	1	1	1	1	1		1	1
11								
10								

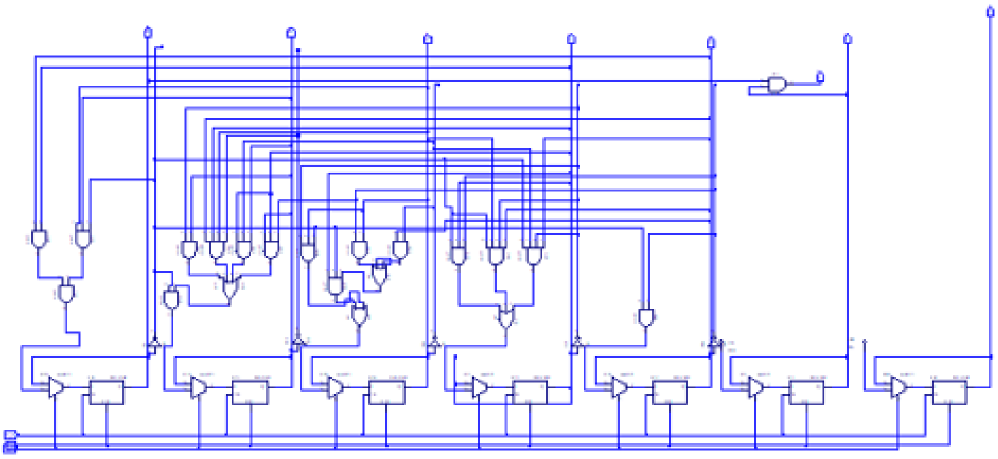
d5=!q6!q5q4q3q2+!q6q5q4!q3+!q6q5q3!q2+
!q6q5!q4q2+!q6q5!q3!q2

d5=!q6(q5!q3+!q5q4q3q2+q5!q4q3+q5q3!q2)

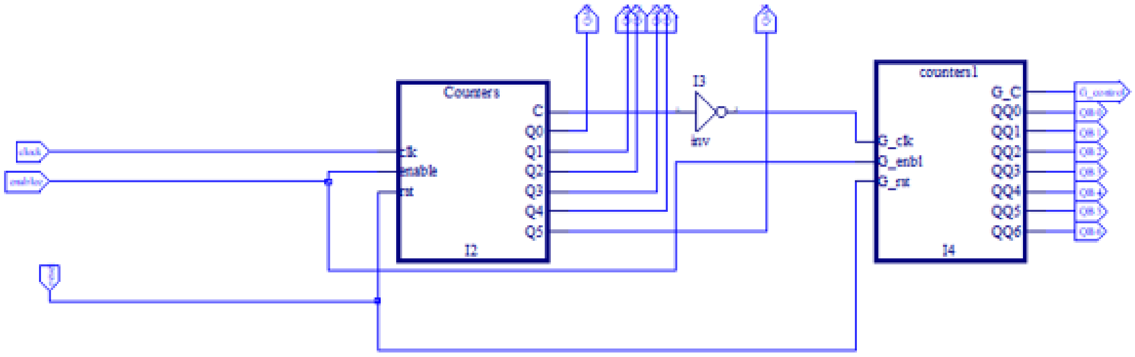
d6	000	001	011	010	110	111	101	100
00								
01						1		
11								
10								

d6=!q6q5q4q3q2

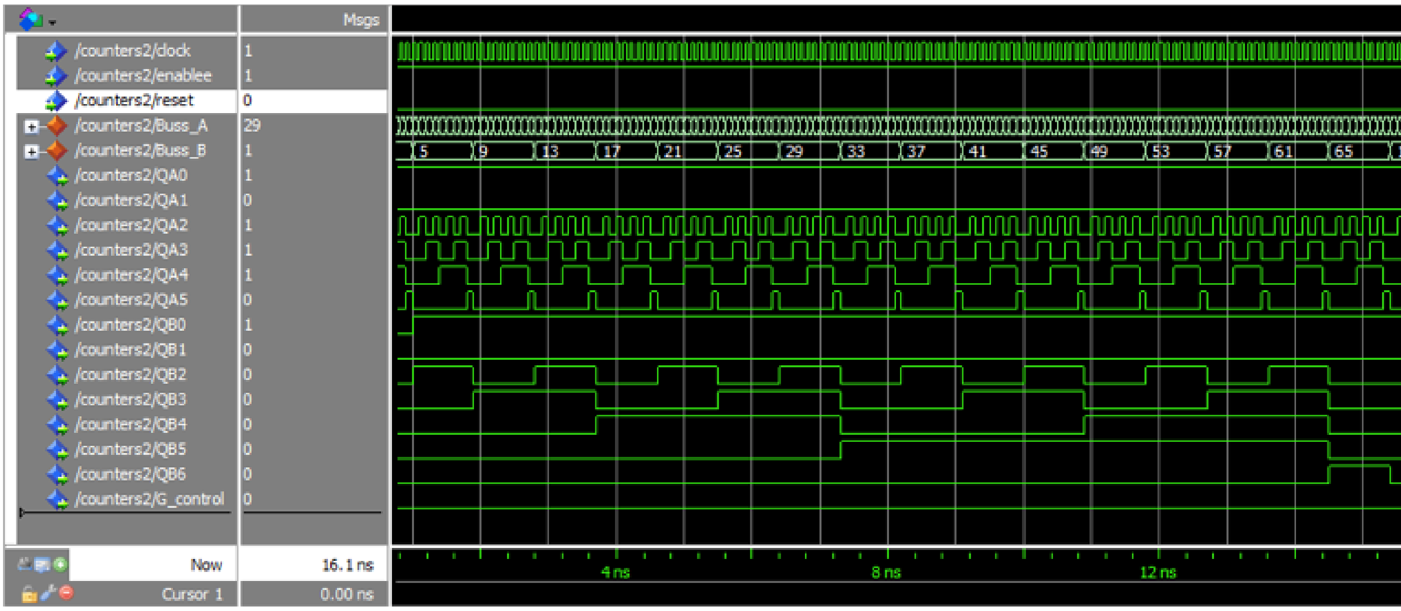
A schematic for the counter implemented using these functions is shown below:



A schematic for combined M1 and M2:



Simulation results is shown below:



```
                              Msgs
/counters2/clock              1
/counters2/enablee            1
/counters2/reset              0
/counters2/Buss_A             29
/counters2/Buss_B             1
/counters2/QA0                1
/counters2/QA1                0
/counters2/QA2                1
/counters2/QA3                1
/counters2/QA4                1
/counters2/QA5                0
/counters2/QB0                1
/counters2/QB1                0
/counters2/QB2                0
/counters2/QB3                0
/counters2/QB4                0
/counters2/QB5                0
/counters2/QB6                0
/counters2/G_control          0

Now                           16.1 ns
Cursor 1                      0.00 ns
```

CONCLUSION:

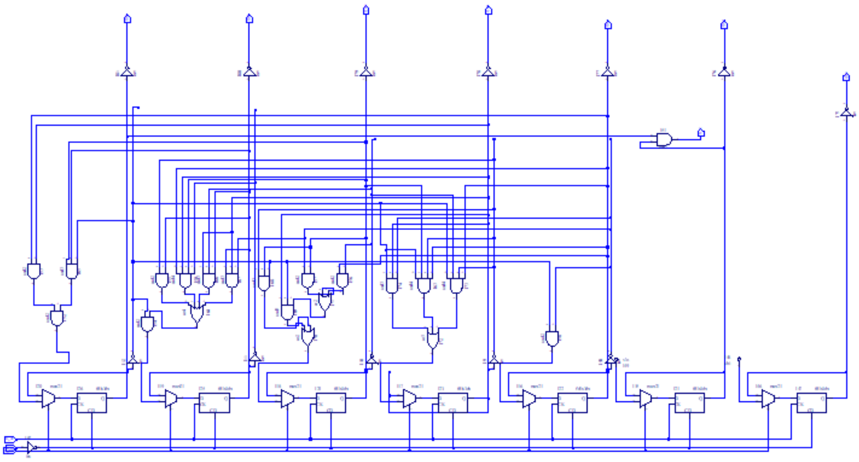
To conclude, in digital logic and computing, a counter is a device which stores (and sometimes displays) the number of times a particular event or process has occurred, often in relationship to a clock. The most common type is a sequential digital logic circuit with an input line called the clock and multiple output lines.

FPGA implementation:

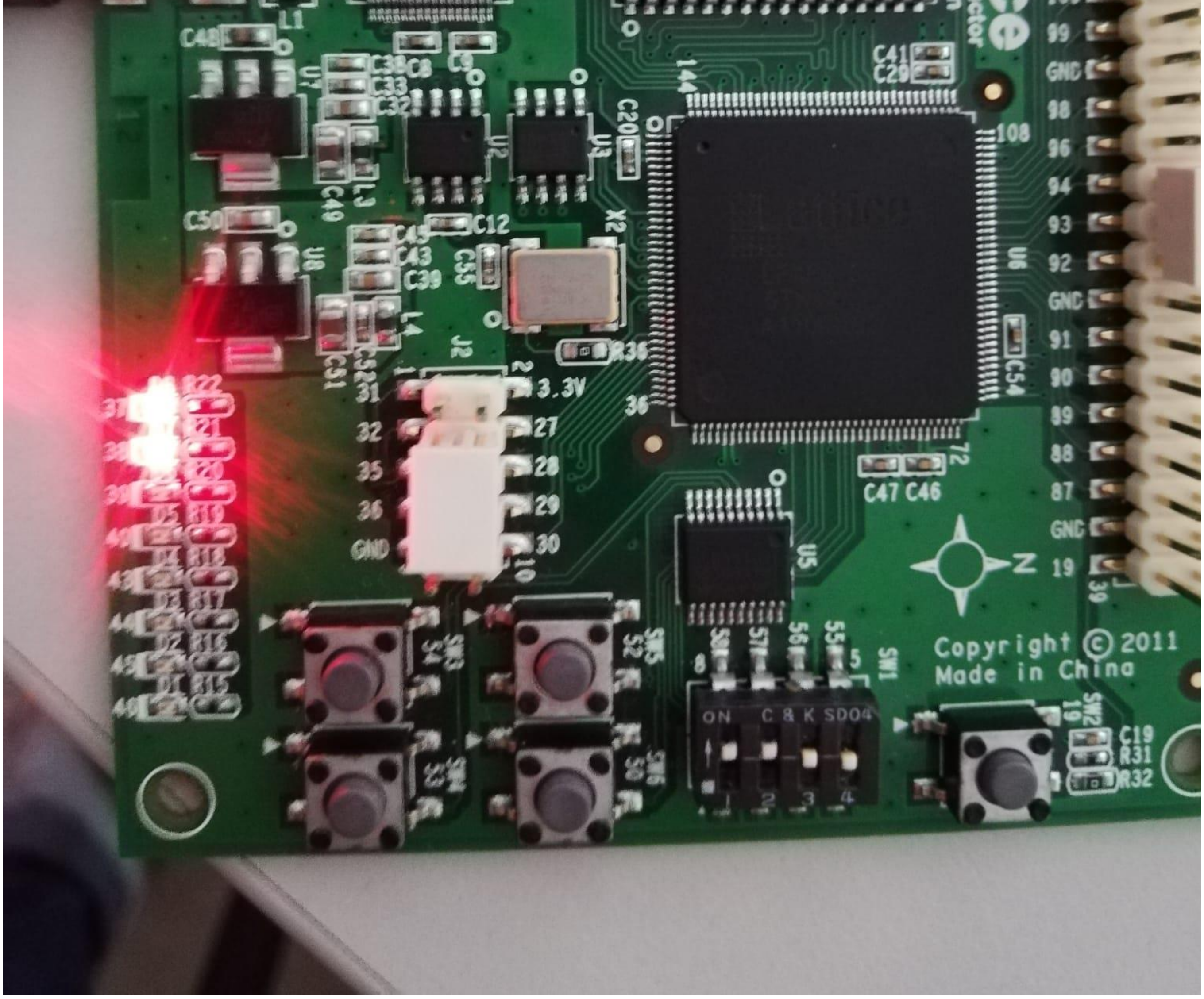
In order for the circuits to function on FPGA board some minor modifications must be performed. The list of modifications is provided below.

1. All outputs must be inverted
2. Asynchronous reset signal must be inverted, synchronous must not be inverted 3.
   All parallel data inputs must be exchange into Vhi or Vlo components

Modified schematics for M1:



Results on FPGA board is shown below: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Evaluation Board REV A
P/N:LFXP2-5E-B2-EVN
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Semiconductor
Corporation
PWR_ON
TCK
GND
TMS
TDI
TDO
3.3V
J1
J2
J4
U1
U2
U3
U4
U5
U6
U7
U8
X1
X2
SW1
SW2
SW3
SW4
SW5
SW6
ON
C & K
SDO4
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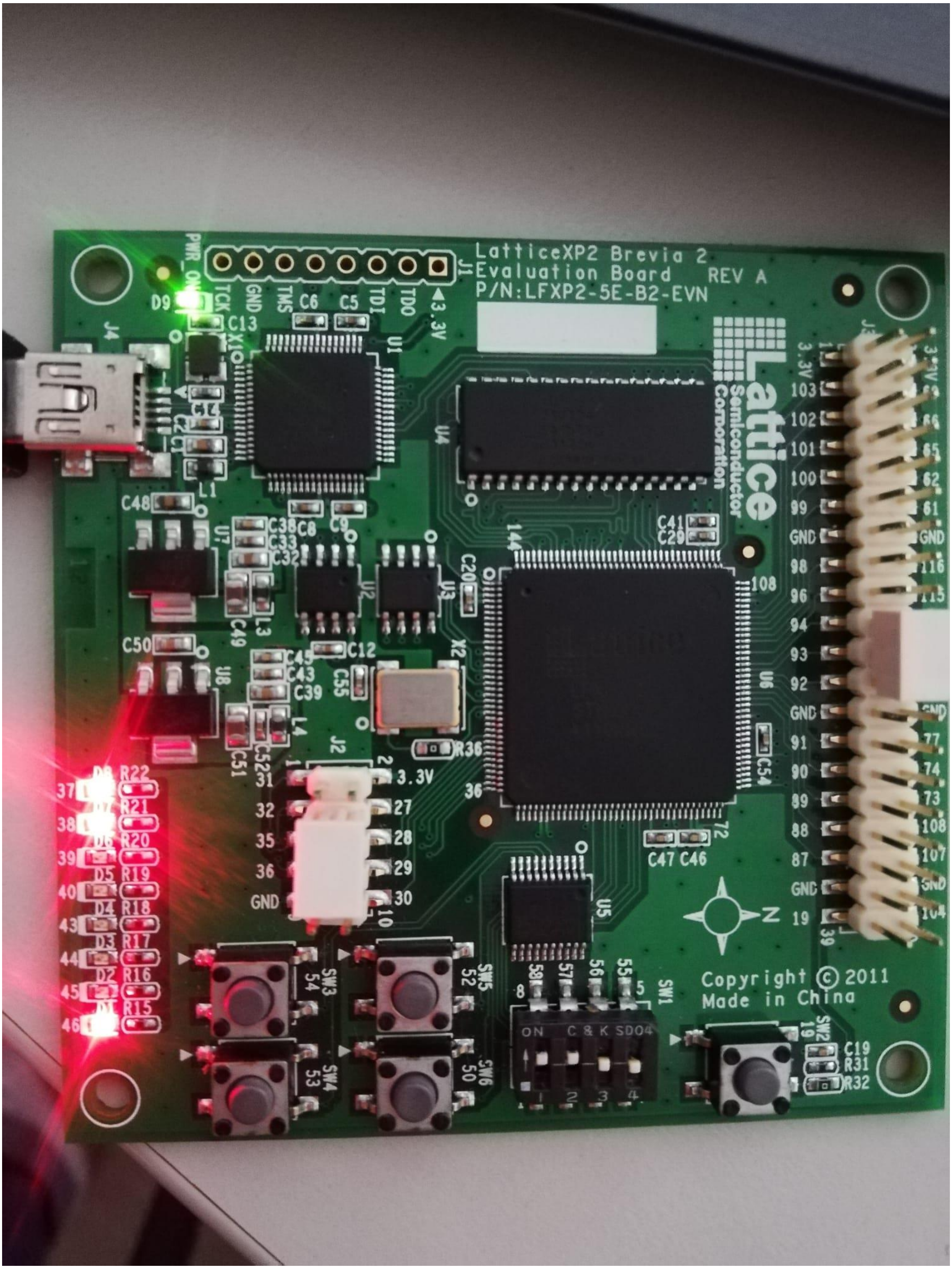
LatticeXP2 Brevia 2
Evaluation Board REV A
P/N:LFXP2-5E-B2-EVN
Lattice
Semiconductor
Corporation
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PWR_ON
TCK
GND
TMS
TDI
TDO
3.3V
J1
J2
J3
J4
U1
U2
U3
U4
U5
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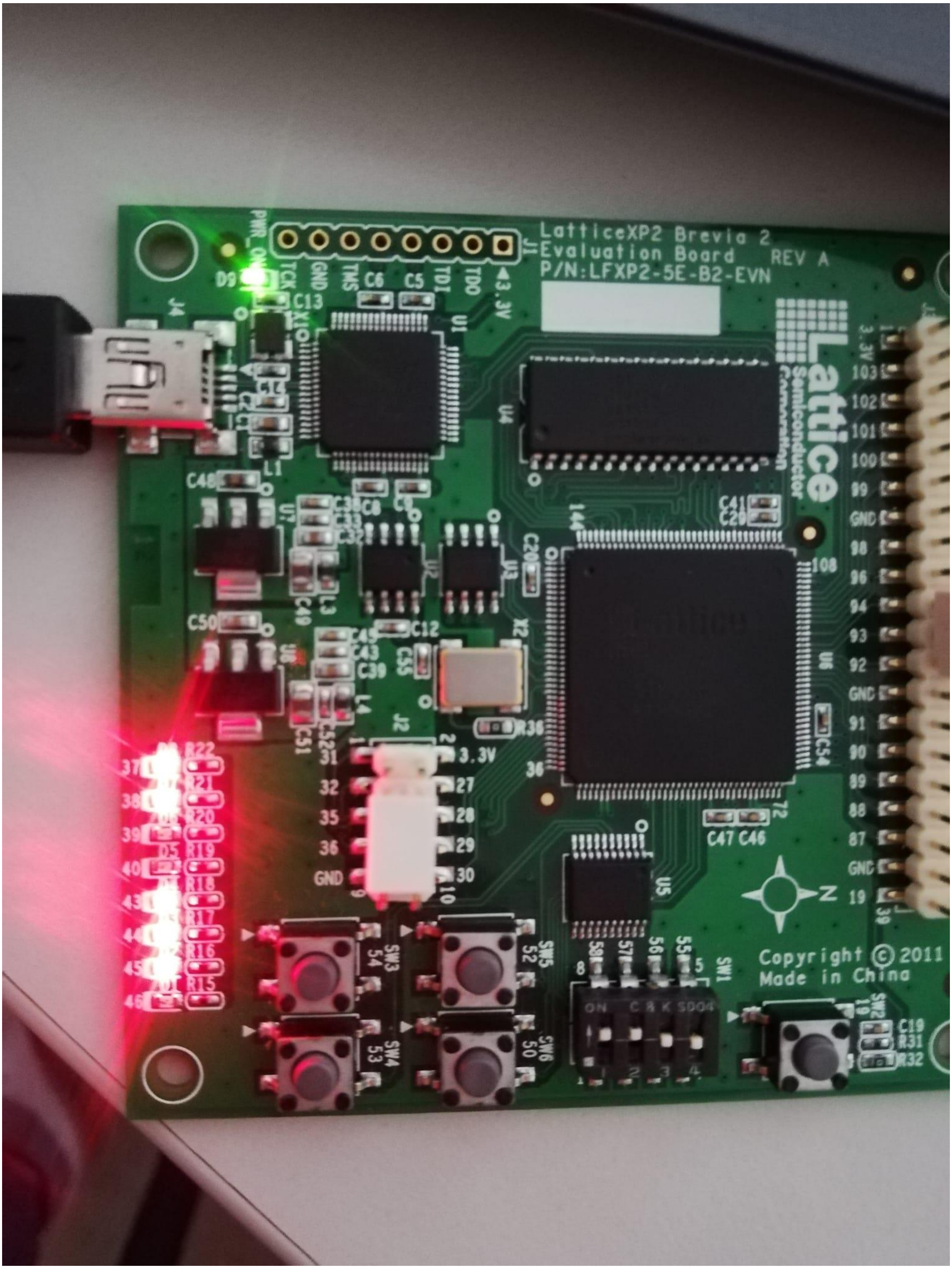
SW6
ON
C & K SDO4
N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Evaluation Board REV A
P/N:LFXP2-5E-B2-EVN
Lattice Semiconductor Corporation
PWR_ON
D9
J1
TCK GND TMS C6 C5 TDI TDO 3.3V
J4
U1
U4
U6
U5
J2
3.3V
GND
SW1
ON
SW2
SW3
SW4
SW5
SW6
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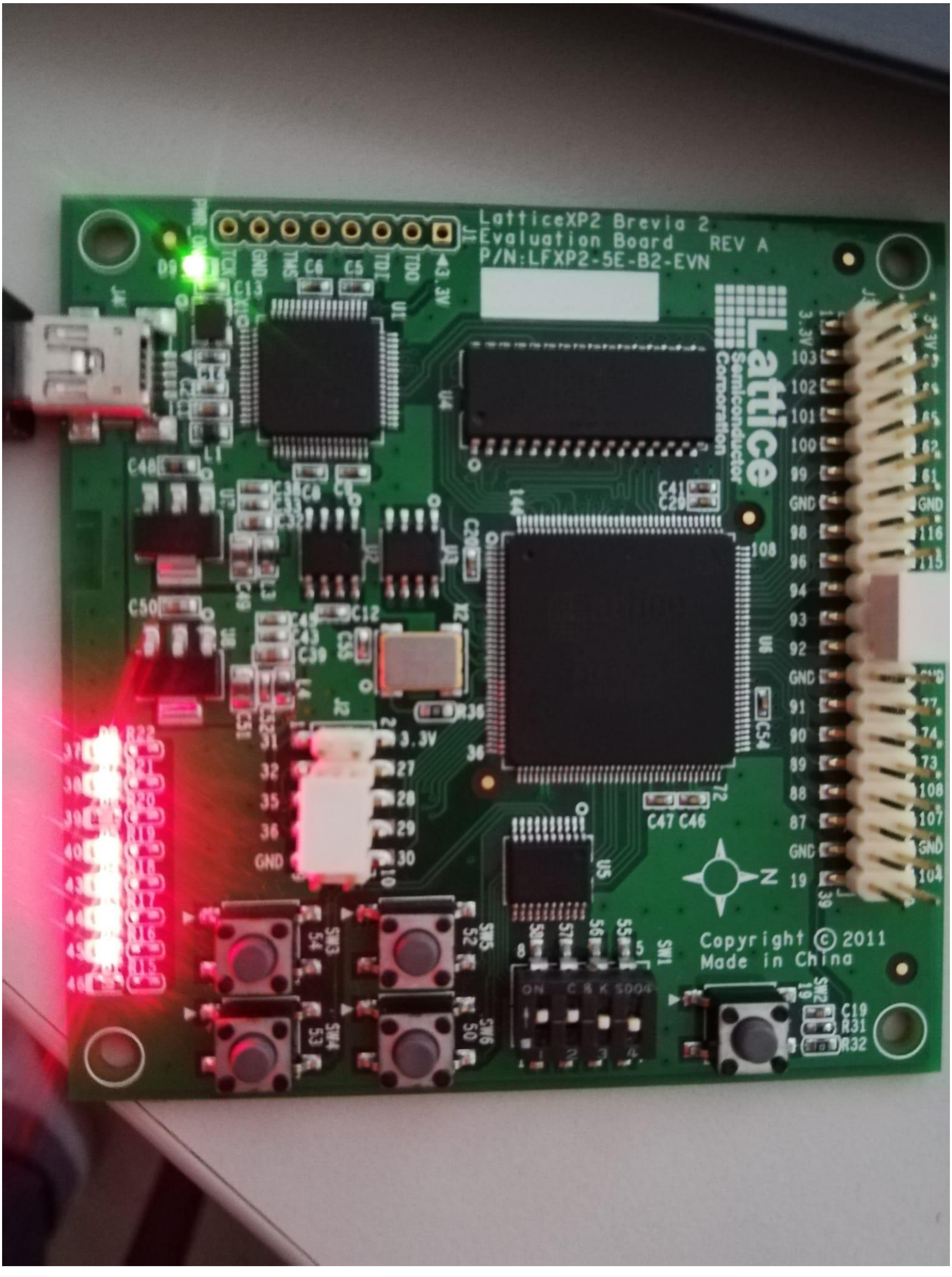
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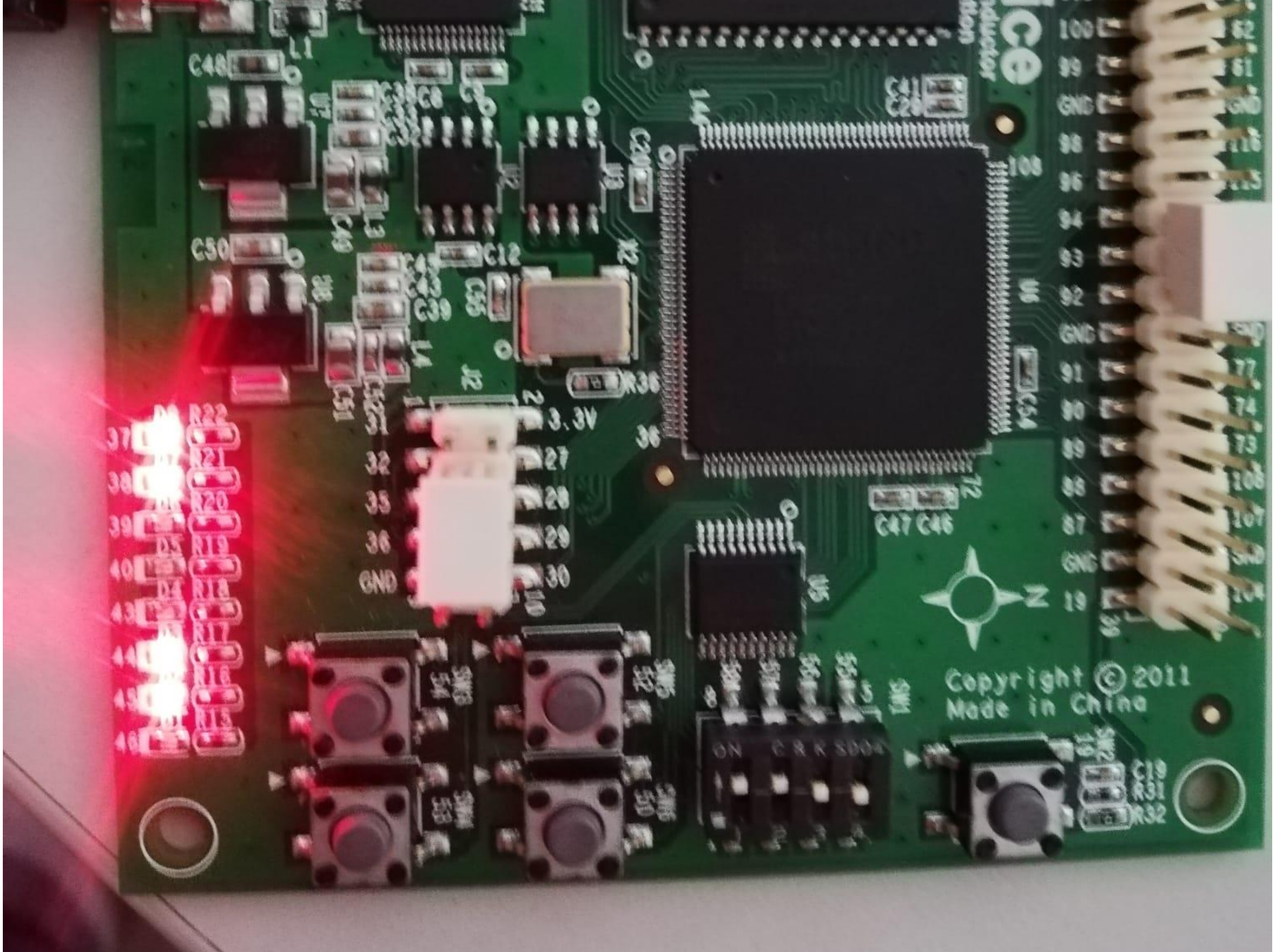
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Lattice Semiconductor Corporation
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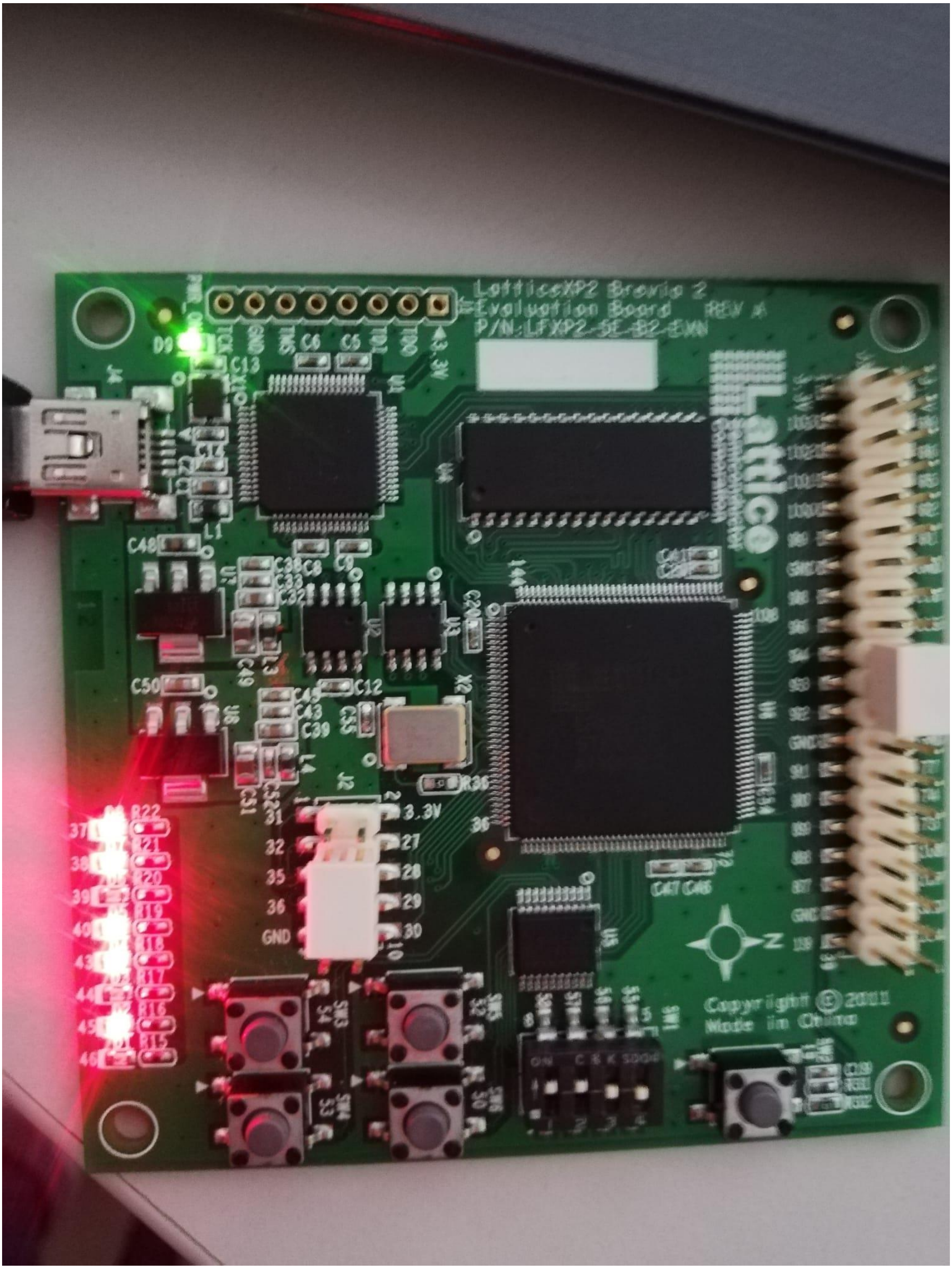
3.3V
GND
N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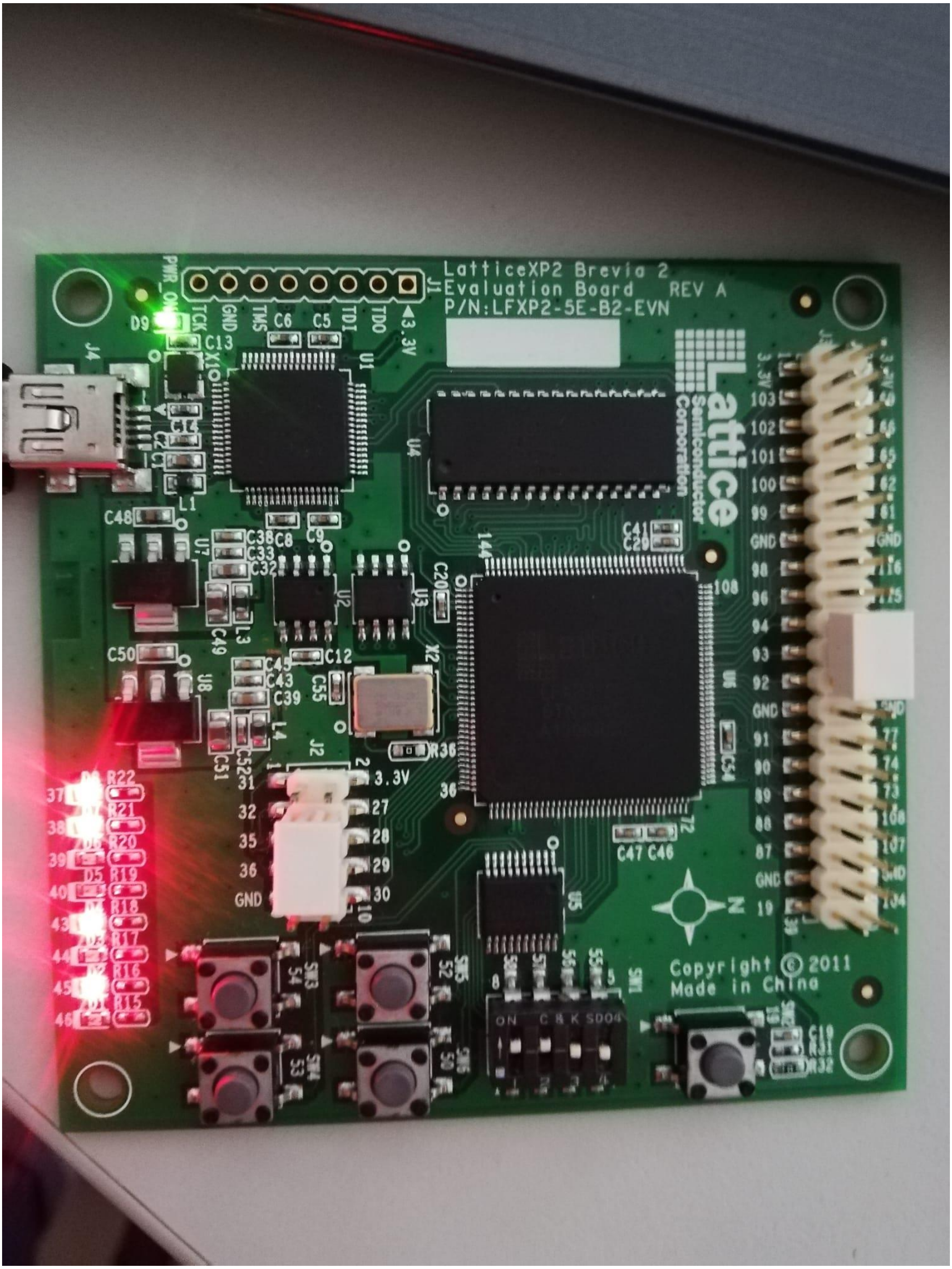
3.3V
GND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Semiconductor
Corporation
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TCK
GND
TMS
TDI
TDO
3.3V
J1
J4
U1
U2
U3
U4
U5
U6
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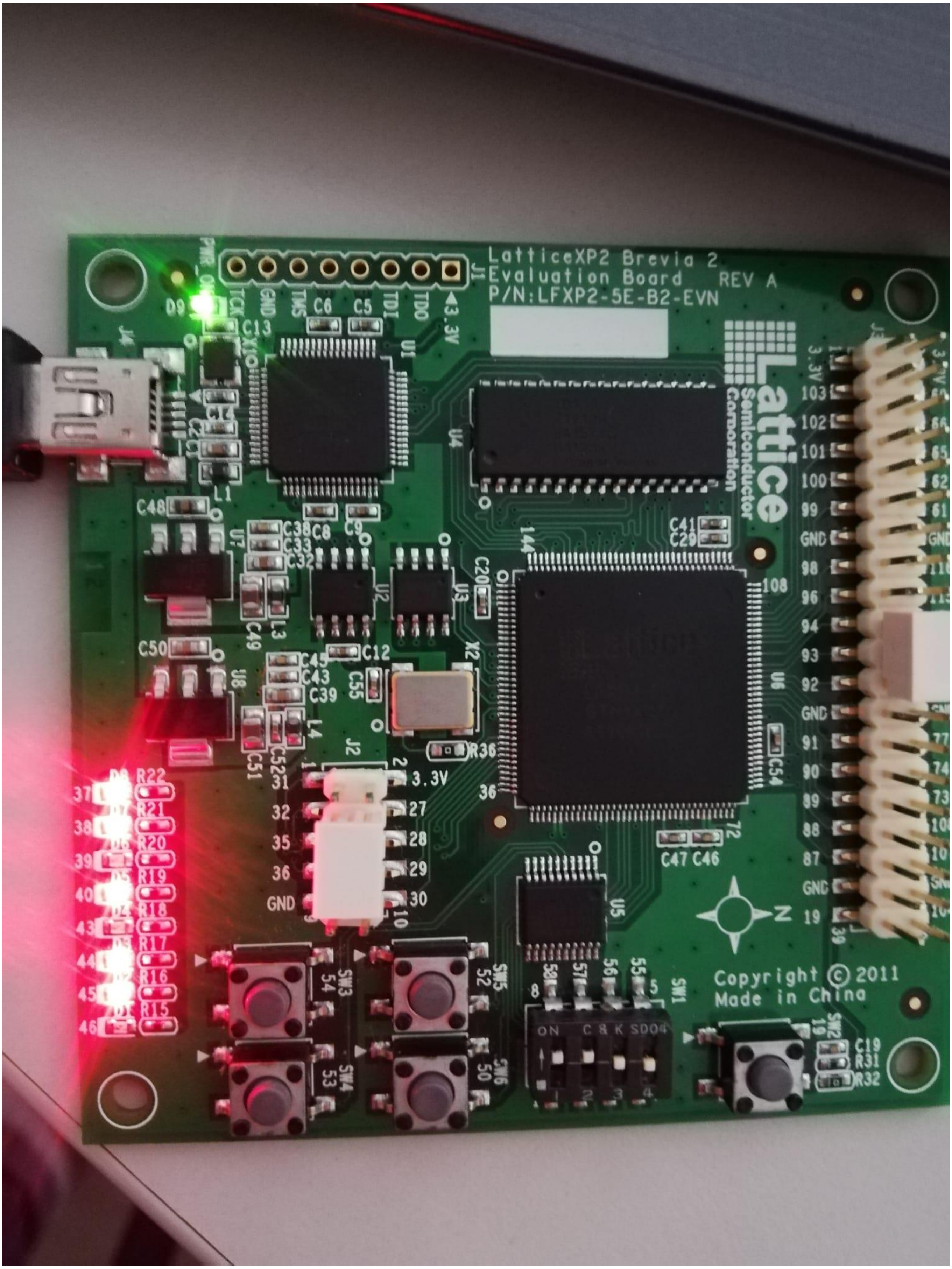
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D9
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TCK
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TMS
C6
C5
TDI
TDO
3.3V
U1
U4
U6
U7
U8
U2
U3
U5
X2
J2
J4
SW1
SW2
SW3
SW4
SW5
SW6
ON
N