Xilinx Tool Flow

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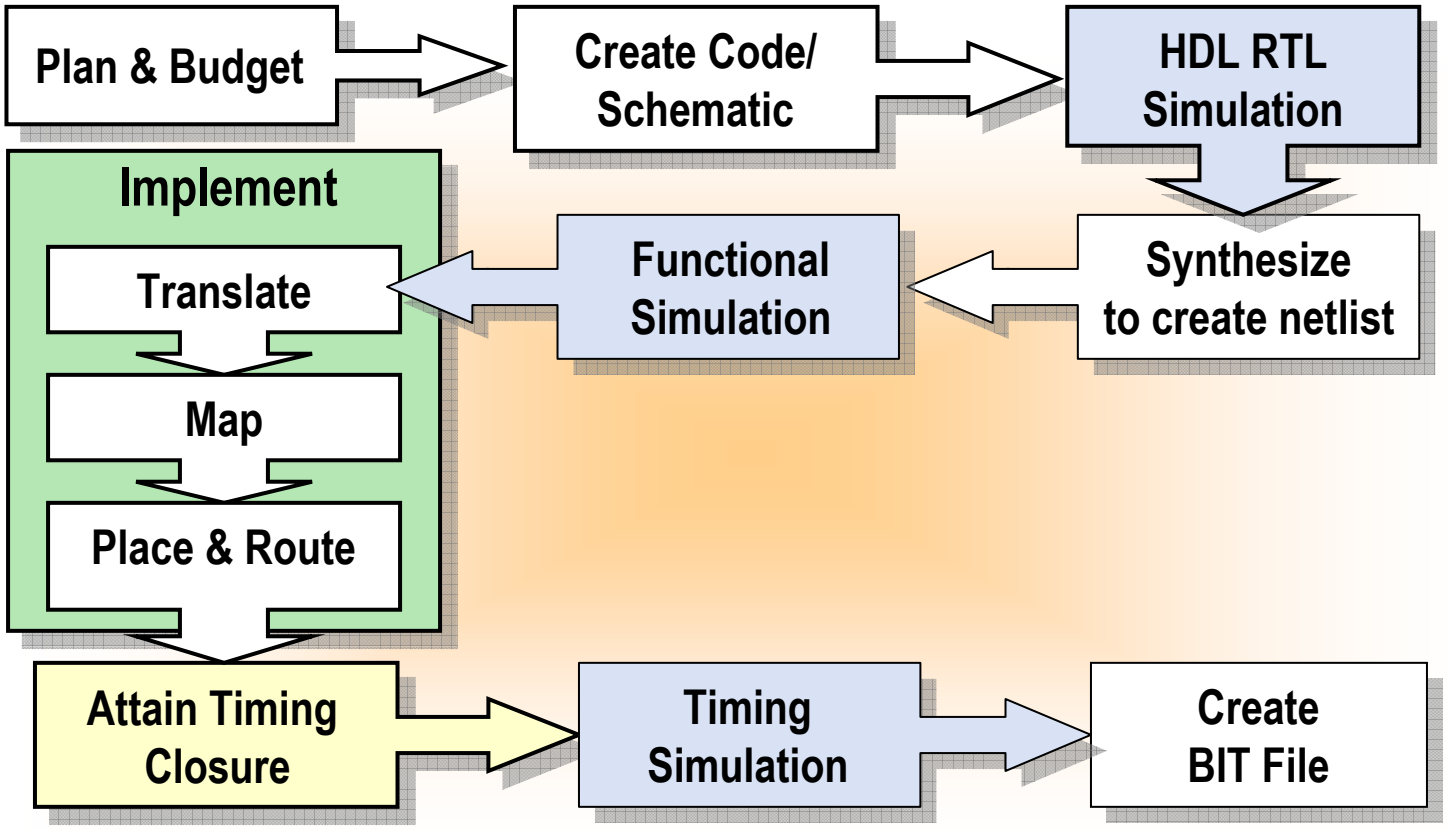
Outline

- **Overview**
- ISE
- Summary
- Lab 1: Xilinx Tool Flow Demo

Xilinx Design Flow



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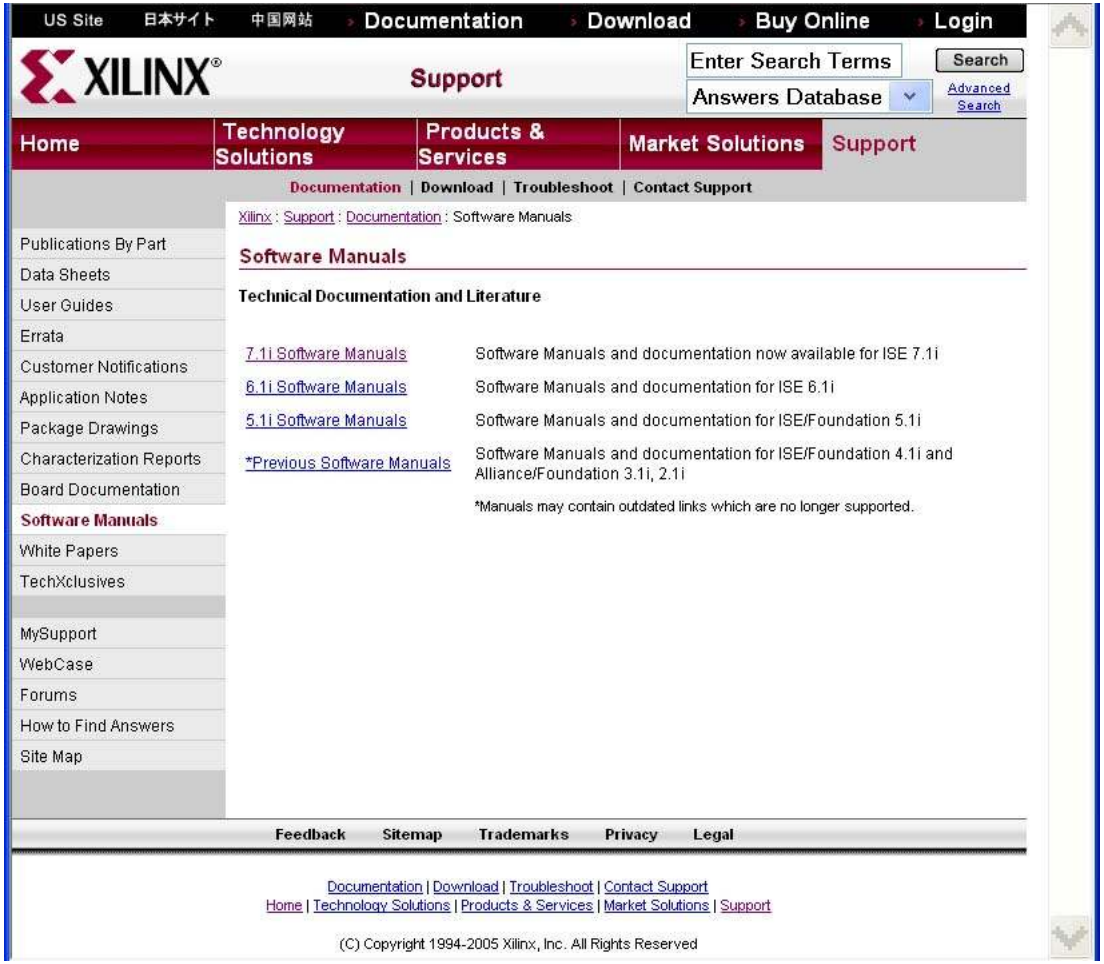
See Development System Reference Guide for Flow Diagrams



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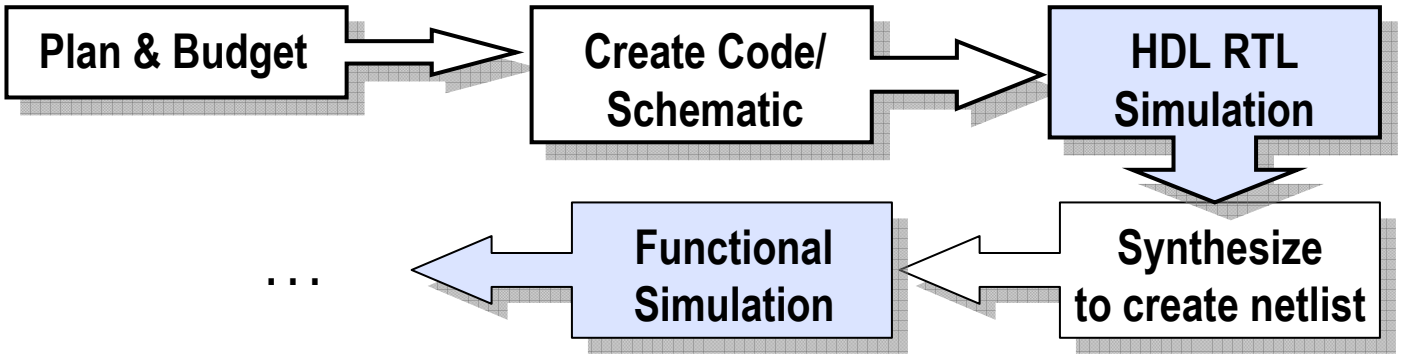
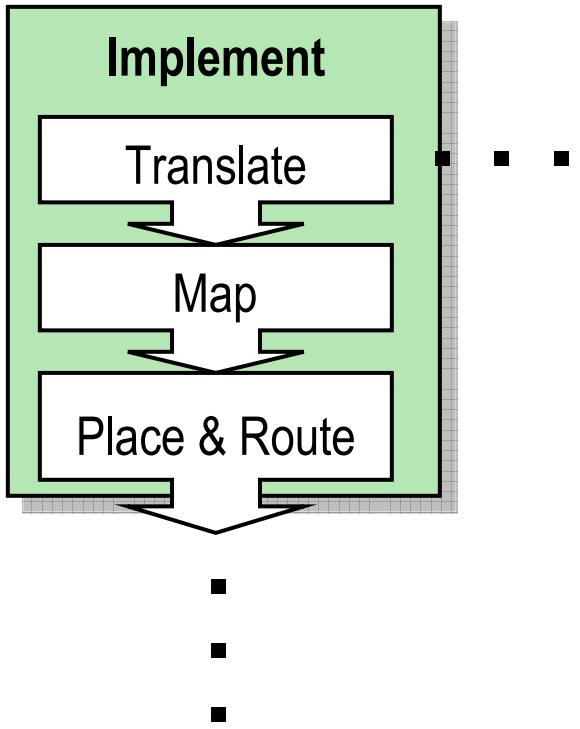
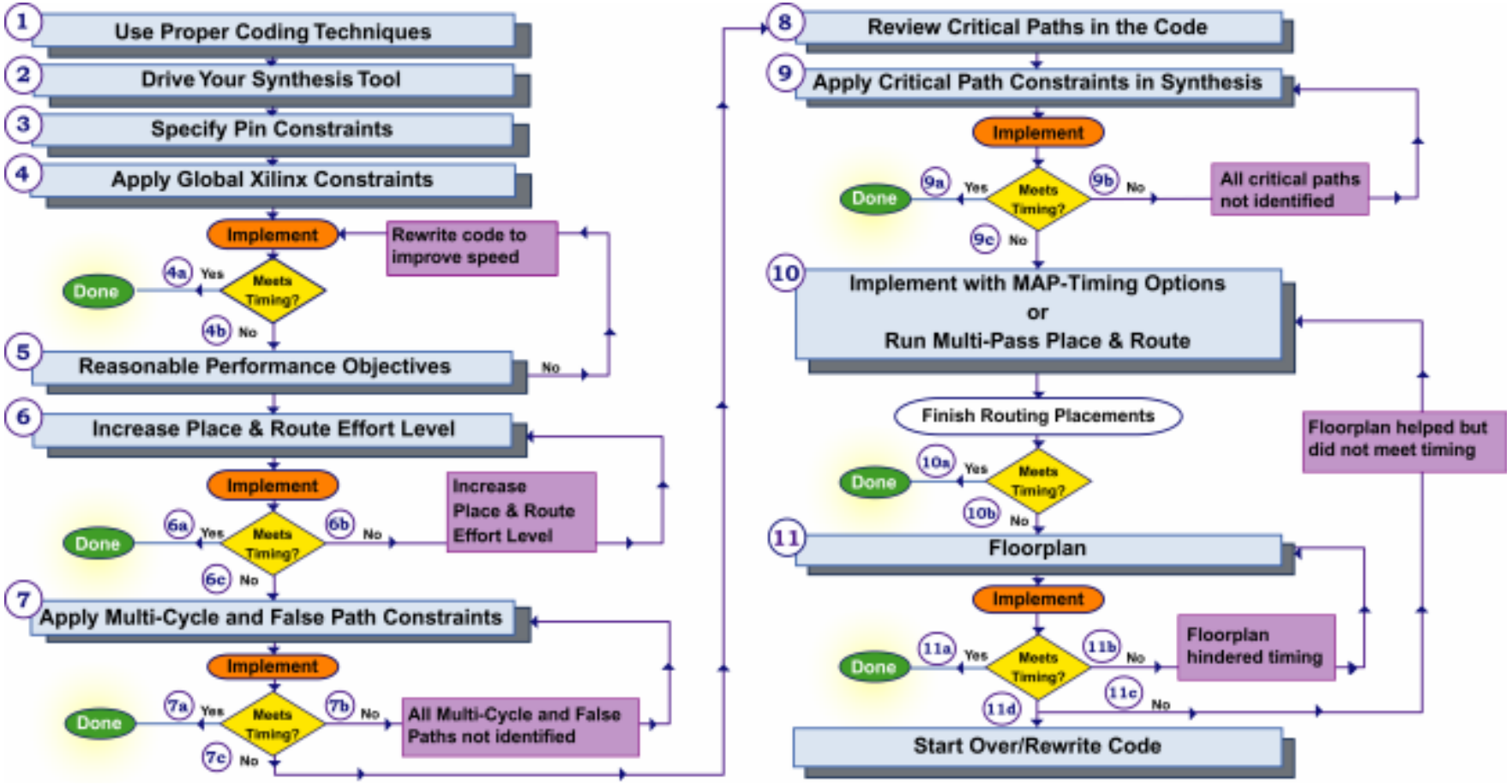
Design Entry Methods: HDL or Schematic



After Generating a Netlist, Implement the Design



Timing Closure



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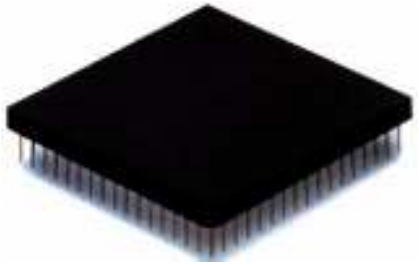
After Implementation, Create a File Called a Bitstream



Knowledge Check

Knowledge Check

- Can you describe the three primary implementation phases?

Answers

- The three primary implementation phases:
  - **Translate:** Merges multiple design files into a single netlist
  - **Map:** Groups logical symbols from the netlist (gates) into physical components (slices and IOBs)
  - **Place & Route:** Places components onto the chip, connect the components, and extracts timing data into reports

Outline

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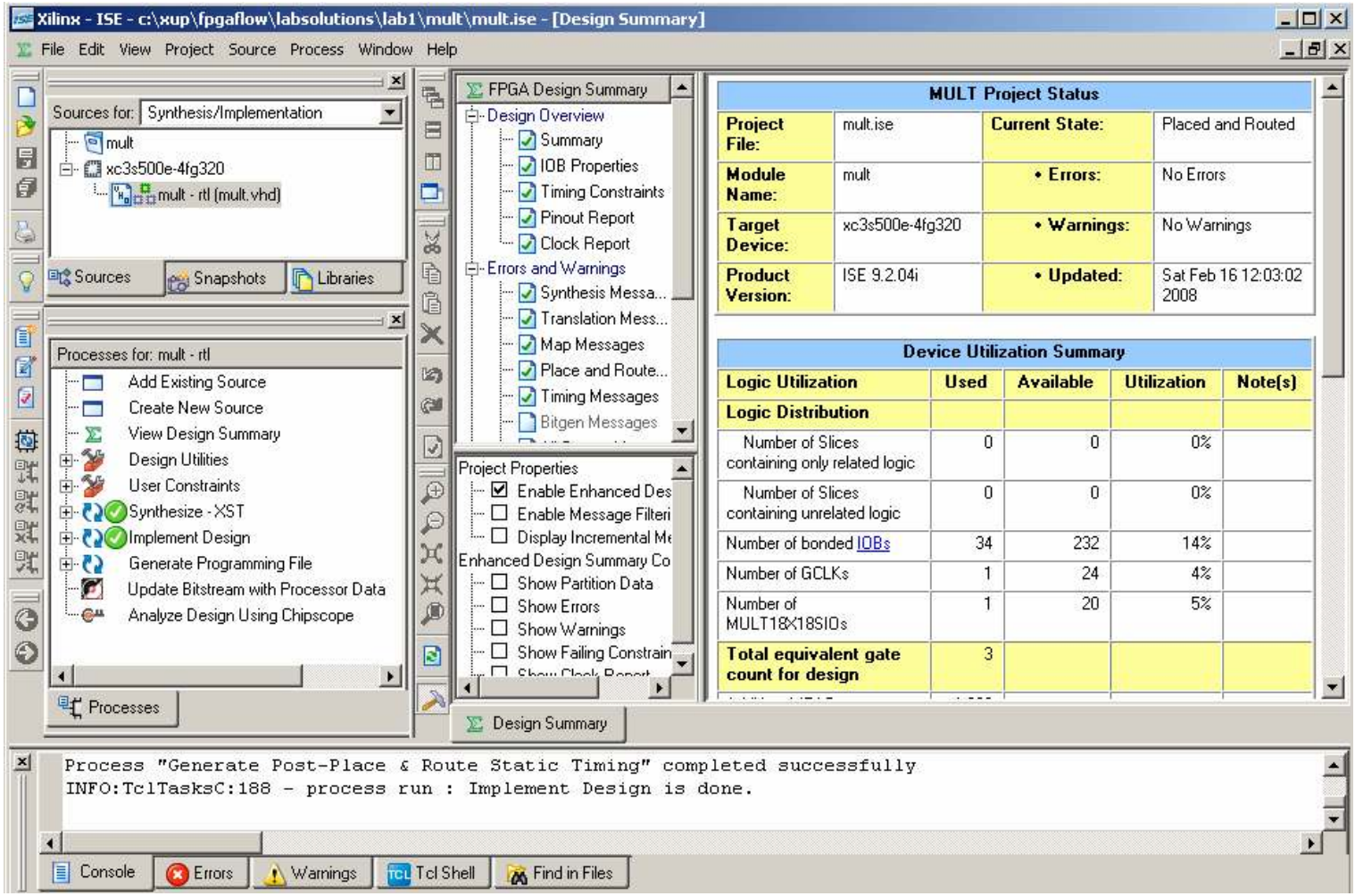
- **ISE**
- Summary
- Lab 1: Xilinx Tool Flow Lab

Project Navigator is the Graphical Interface to the ISE Tool Suite



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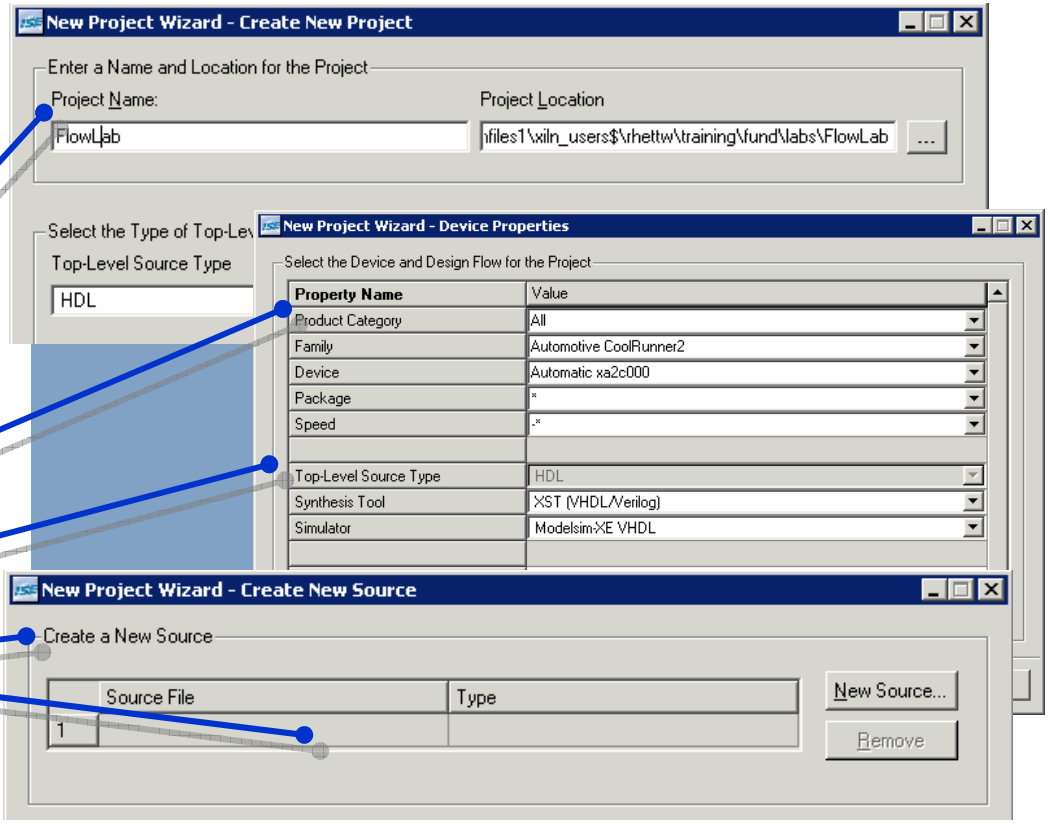
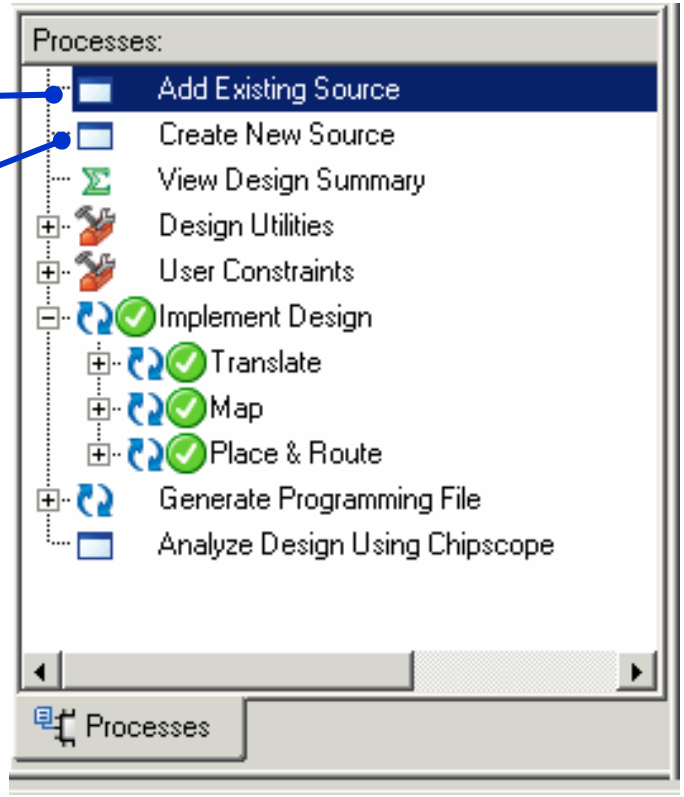
Creating a Project

- Select **File → New Project**
- New Project Wizard guides you through the process
  - Project name and location
  - Target device
  - Software flow
  - Create or add source files



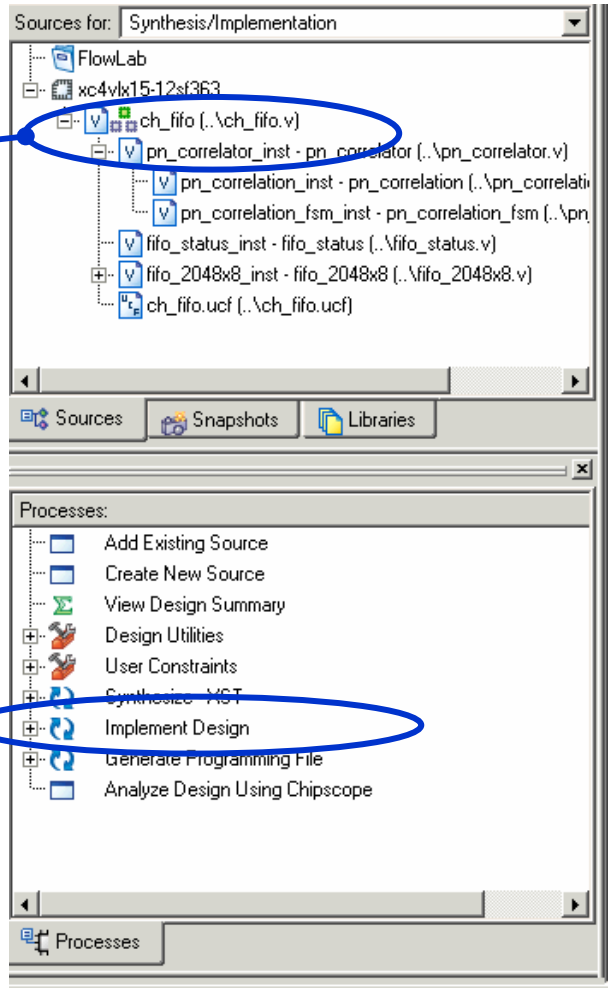
Creating and Adding Source Files

- Double-click **Add Existing Source** to include an existing source file
- Double-click **Create New Source** and choose the type of file to create a new source file
  - HDL
  - IP
  - Schematic
  - State Diagram
  - Testbench
  - Constraints



Implementing a Design

- Implement a design:
  - Select the **top-level source file** in the Sources in Project window
    - HDL, schematic, or EDIF, depending on your design flow
  - Double-click **Implement Design** in the Processes for Source window



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Checking the Implementation Status

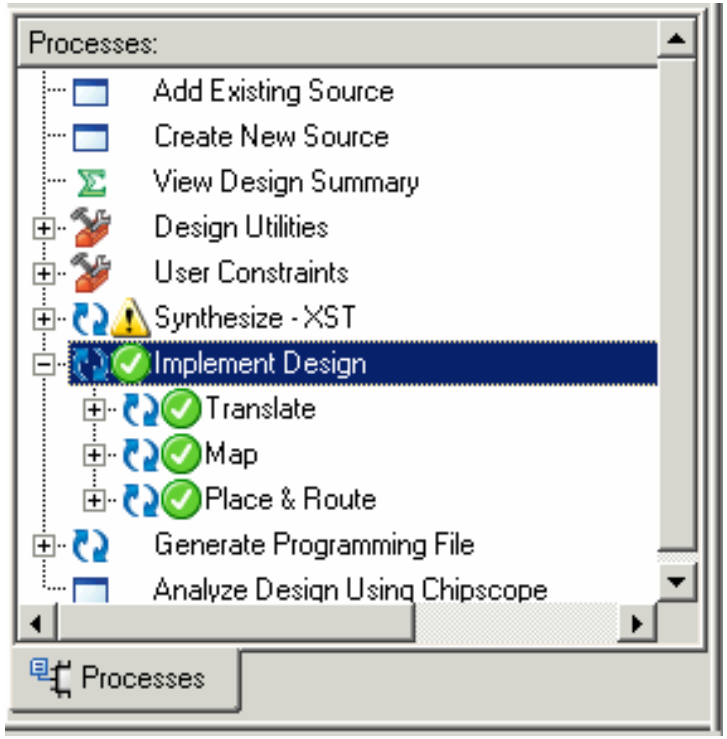
- The ISE™ software will run all of the necessary steps to implement the design
  - Synthesize HDL code
  - Translate
  - Map
  - Place & Route

✓ = process was completed successfully

! = warnings

? = a file that is out of date

X = errors



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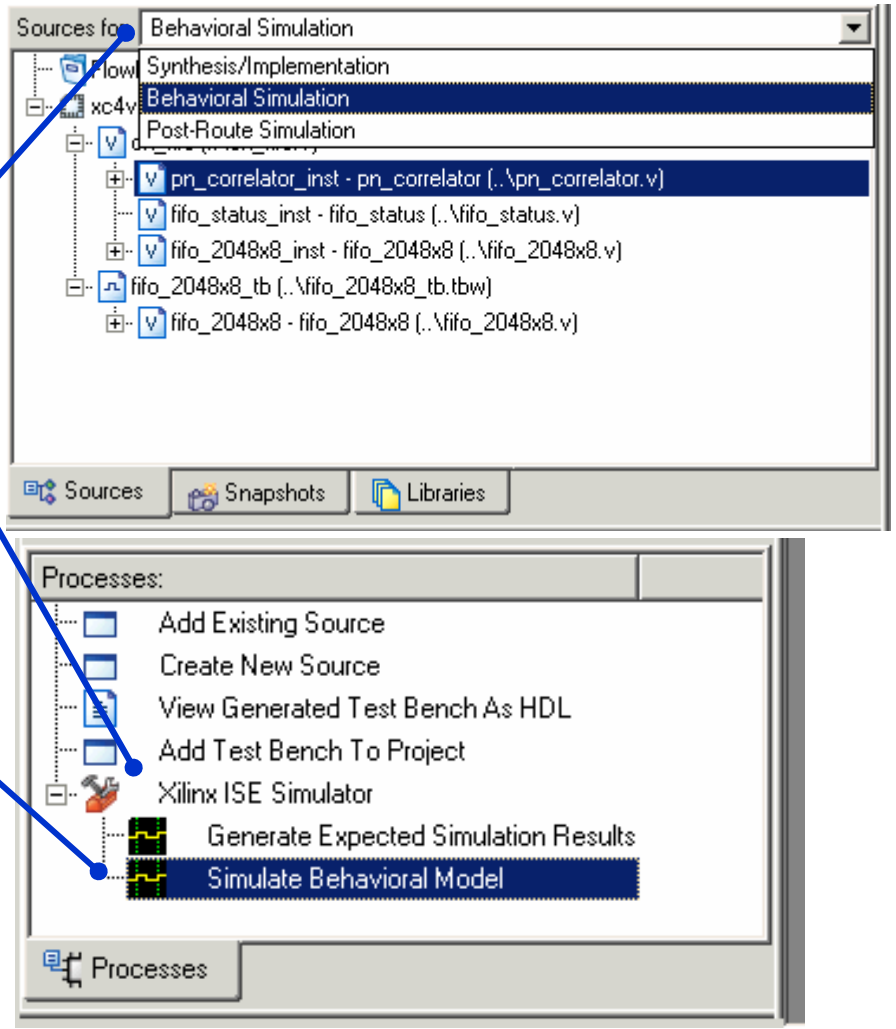
Simulating a Design

- Simulate a design:
  - Select **Sources for: Behavioral Simulation**
  - Expand **Xilinx ISE Simulator** in the Processes for Source window
  - Double-click **Simulate Behavioral Model** or **Simulate Post-Place & Route Model**
    - You can also simulate after Translate or after Map



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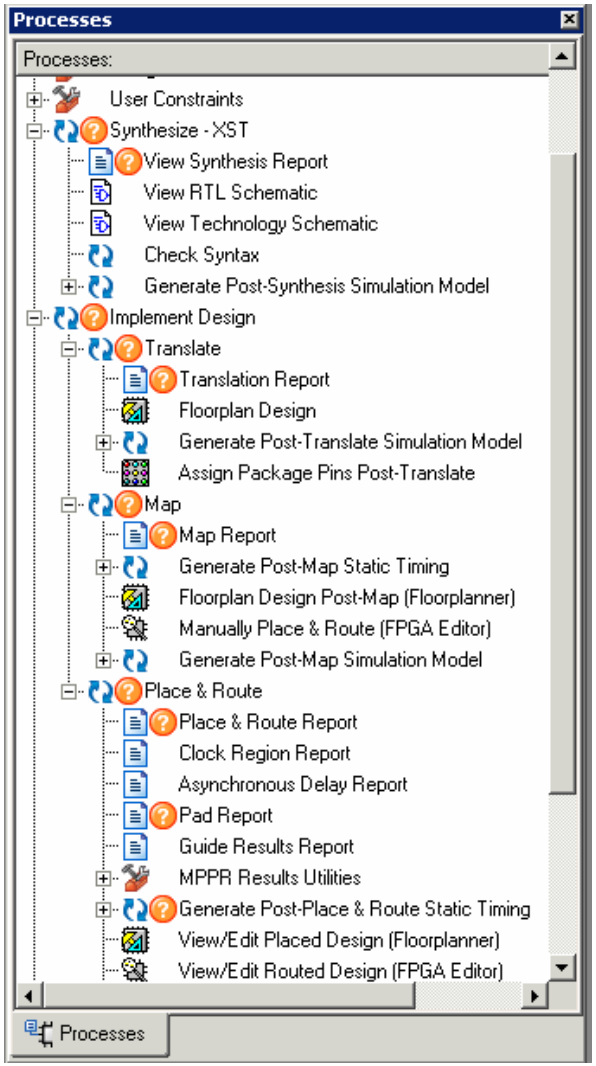
Viewing Subprocesses

- Expand each process to view subtools and subprocesses
  - Translate
    - Floorplan
    - Assign package pins
  - Map
    - Analyze timing
  - Place & Route
    - Analyze timing
    - Floorplan
    - FPGA Editor
    - Analyze power
    - Create simulation model



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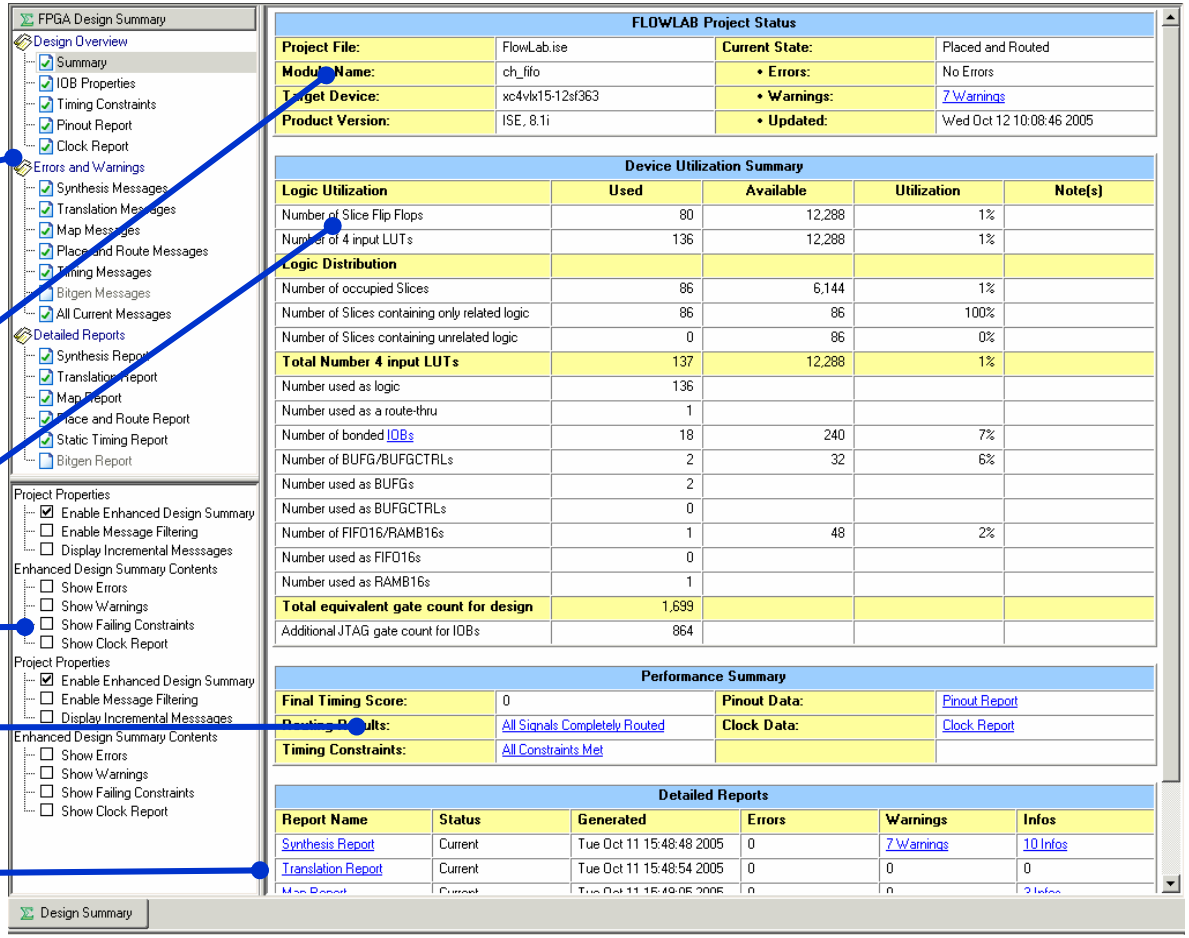
The Design Summary Displays Design Data

- Quick View of Reports, Constraints
- Project Status
- Device Utilization
- Design Summary Options
- Performance and Constraints
- Reports



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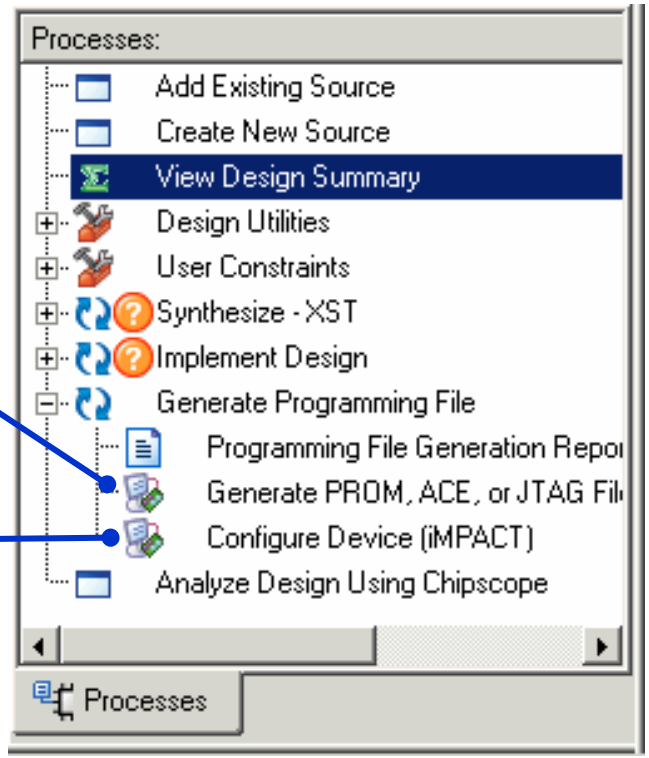
Programming the FPGA

- There are two ways to program an FPGA
  - Through a PROM device
    - You must generate a file that the PROM programmer can understand
  - Directly from the computer
    - Use the iMPACT configuration tool



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Review Questions

- What are the phases of the Xilinx design flow?
- What are the components of implementation, and what happens at each step?
- What are two methods of programming an FPGA?

Answers

- What are the phases of the Xilinx design flow?
  - Plan and budget, create code or schematic, RTL simulation, synthesize, functional simulation, implement, timing closure, timing simulation, and BIT file creation
- What are the components of implementation, and what happens at each step?
  - Translate: merges multiple design files into one netlist
  - Map: groups logical symbols into physical components
  - Place & Route: places components onto the chip and connects them
- What are two methods of programming an FPGA?
  - PROM
  - Xilinx iMPACT configuration tool

Summary

- Implementation means more than Place & Route
- Xilinx provides a simple *pushbutton* tool to guide you through the Xilinx design process

Where Can I Learn More?

- Complete design flow tutorials
  - www.xilinx.com → Documentation → Tutorials
- On implementation: Development System Reference Guide
  - www.xilinx.com → Documentation → Software Manuals
  - Documentation may also be installed on your local computer
- On simulation: ISIM Online Help
- Configuration Problem Solver
  - www.xilinx.com → Support → Problem Solvers → Configuration Problem Solver

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