



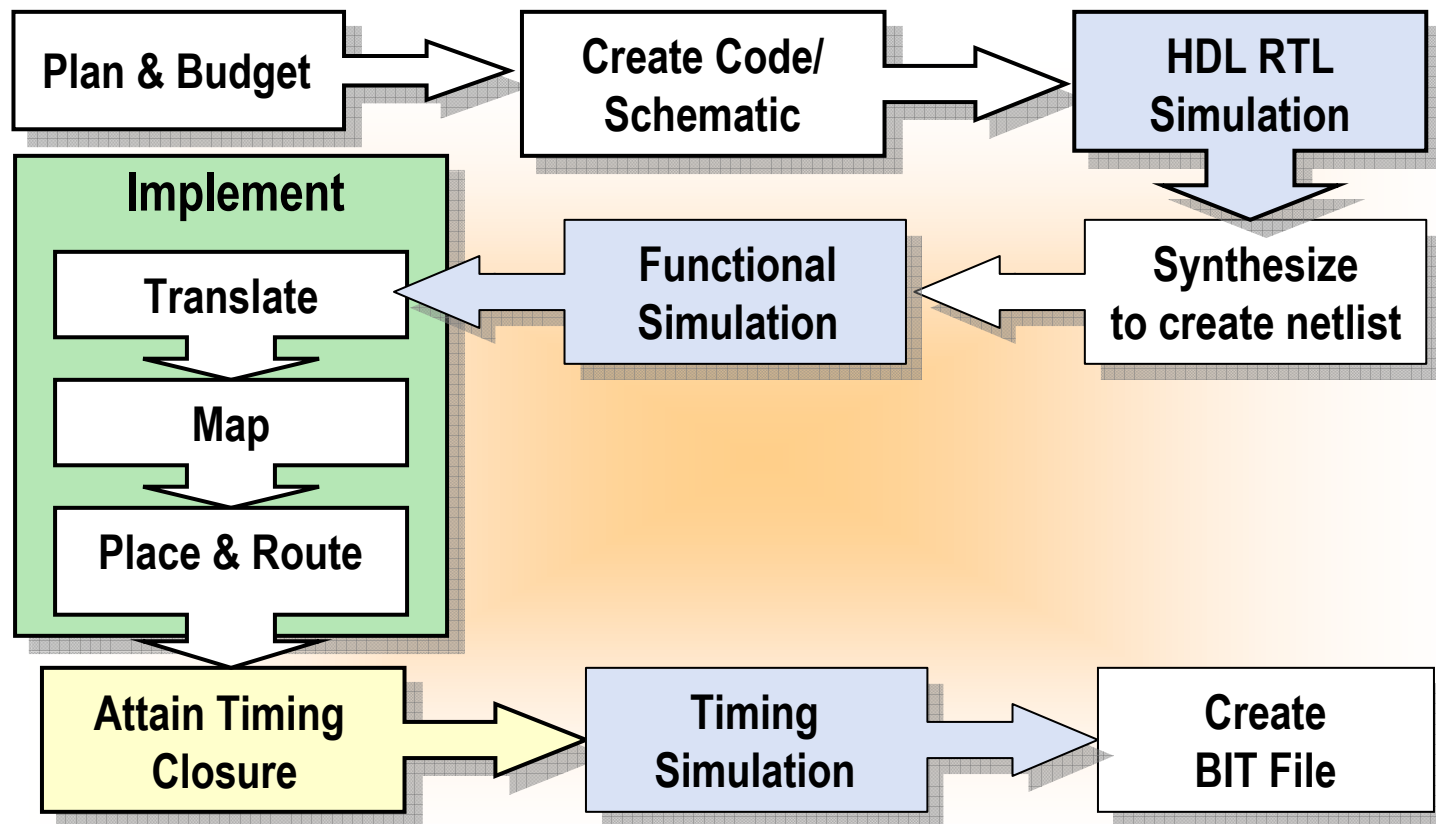
Xilinx Tool Flow

Outline



- Overview
- ISE
- Summary
- Lab 1: Xilinx Tool Flow Demo

Xilinx Design Flow



See Development System Reference Guide for Flow Diagrams

The screenshot displays the Xilinx Support website. At the top, there are navigation links for US Site, 日本サイト, 中国网站, Documentation, Download, Buy Online, and Login. The Xilinx logo and 'Support' text are prominently displayed. A search bar with 'Enter Search Terms' and a 'Search' button is present, along with an 'Answers Database' dropdown and an 'Advanced Search' link. Below this is a main navigation bar with links for Home, Technology Solutions, Products & Services, Market Solutions, and Support. A secondary navigation bar includes Documentation, Download, Troubleshoot, and Contact Support. The left sidebar lists various resources: Publications By Part, Data Sheets, User Guides, Errata, Customer Notifications, Application Notes, Package Drawings, Characterization Reports, Board Documentation, Software Manuals, White Papers, TechXclusives, MySupport, WebCase, Forums, How to Find Answers, and Site Map. The main content area is titled 'Software Manuals' and 'Technical Documentation and Literature'. It lists links for 7.1i, 6.1i, and 5.1i Software Manuals, each with a brief description of the available documentation. A link for '*Previous Software Manuals' is also provided. A disclaimer states: '*Manuals may contain outdated links which are no longer supported.' At the bottom, there are links for Feedback, Sitemap, Trademarks, Privacy, and Legal. The footer contains the copyright notice: '(C) Copyright 1994-2005 Xilinx, Inc. All Rights Reserved'.

US Site 日本サイト 中国网站 Documentation Download Buy Online Login

XILINX® Support

Enter Search Terms Search

Answers Database Advanced Search

Home Technology Solutions Products & Services Market Solutions Support

Documentation Download Troubleshoot Contact Support

Xilinx : Support : Documentation : Software Manuals

Software Manuals

Technical Documentation and Literature

[7.1i Software Manuals](#) Software Manuals and documentation now available for ISE 7.1i

[6.1i Software Manuals](#) Software Manuals and documentation for ISE 6.1i

[5.1i Software Manuals](#) Software Manuals and documentation for ISE/Foundation 5.1i

[*Previous Software Manuals](#) Software Manuals and documentation for ISE/Foundation 4.1i and Alliance/Foundation 3.1i, 2.1i

*Manuals may contain outdated links which are no longer supported.

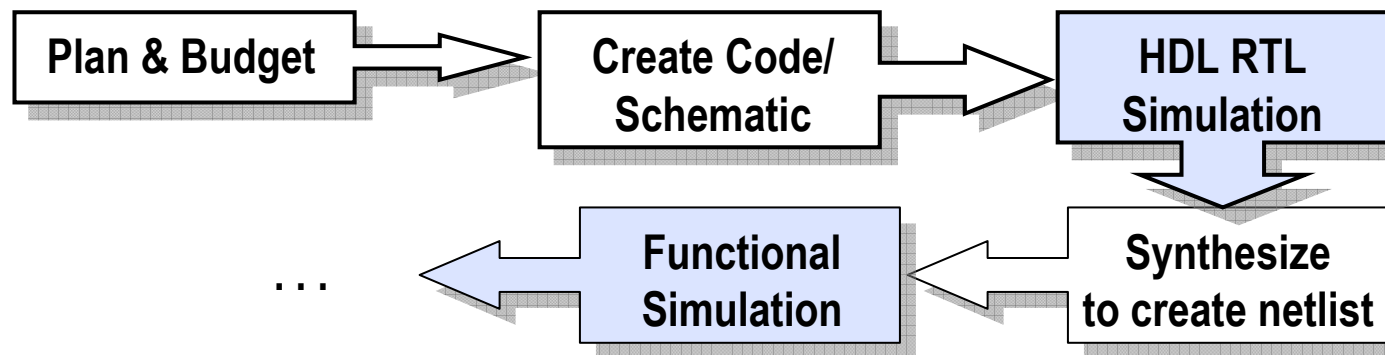
Feedback Sitemap Trademarks Privacy Legal

[Documentation](#) | [Download](#) | [Troubleshoot](#) | [Contact Support](#)

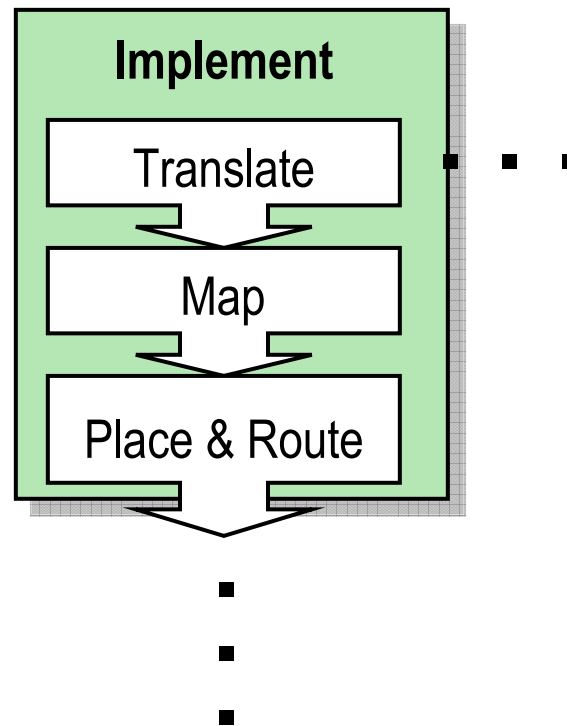
[Home](#) | [Technology Solutions](#) | [Products & Services](#) | [Market Solutions](#) | [Support](#)

(C) Copyright 1994-2005 Xilinx, Inc. All Rights Reserved

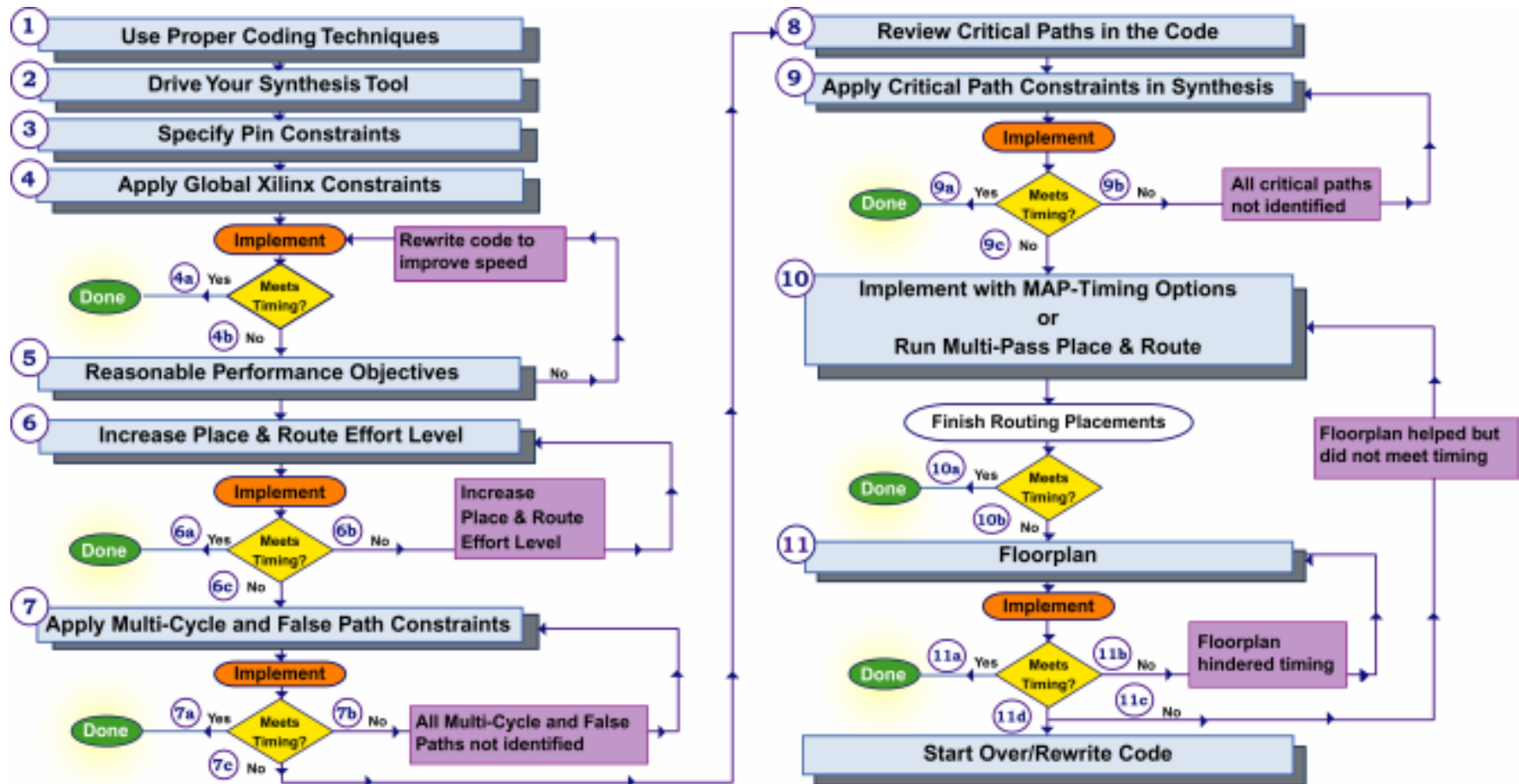
Design Entry Methods: HDL or Schematic



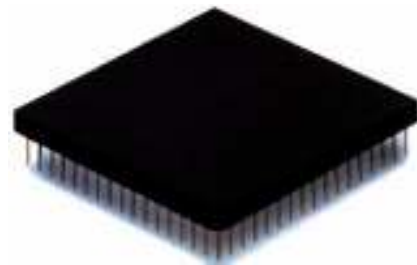
After Generating a Netlist, Implement the Design



Timing Closure



After Implementation, Create a File Called a Bitstream



Knowledge Check

Knowledge Check

- Can you describe the three primary implementation phases?

Answers

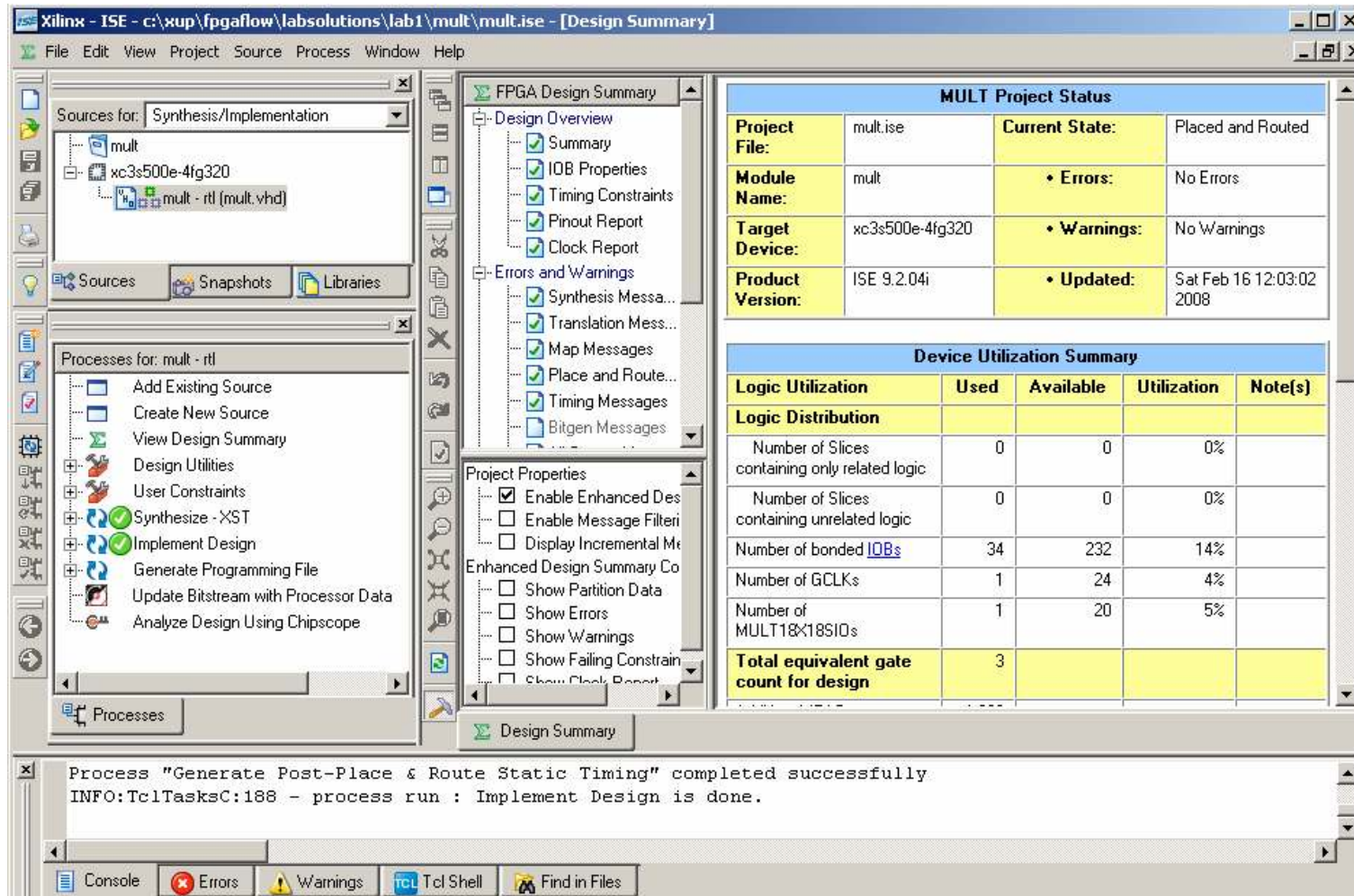
- The three primary implementation phases:
 - **Translate:** Merges multiple design files into a single netlist
 - **Map:** Groups logical symbols from the netlist (gates) into physical components (slices and IOBs)
 - **Place & Route:** Places components onto the chip, connect the components, and extracts timing data into reports

Outline

- Overview
- **ISE**
- Summary
- Lab 1: Xilinx Tool Flow Lab



Project Navigator is the Graphical Interface to the ISE Tool Suite

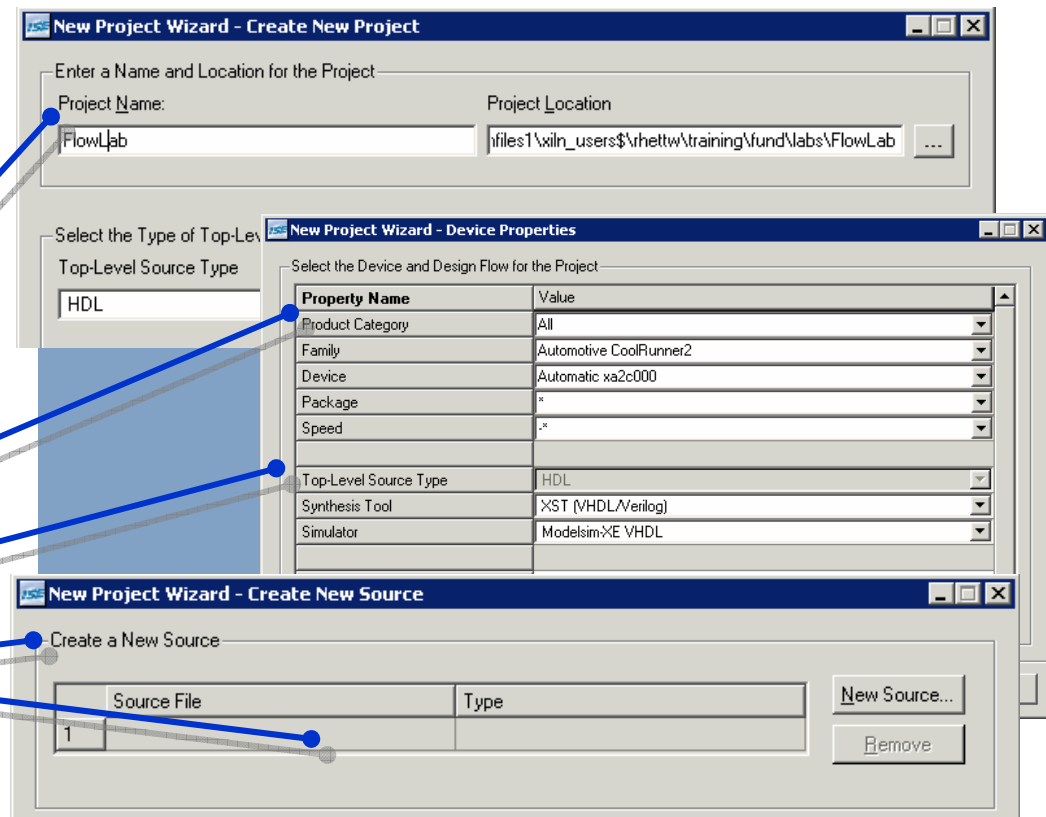


Creating a Project

- Select **File** → **New Project**

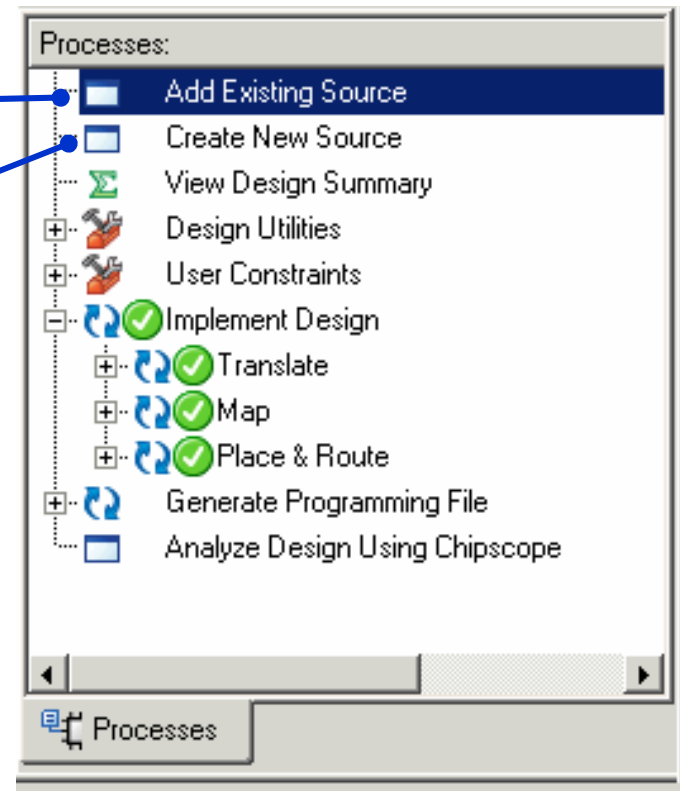
- New Project Wizard guides you through the process

- Project name and location
- Target device
- Software flow
- Create or add source files



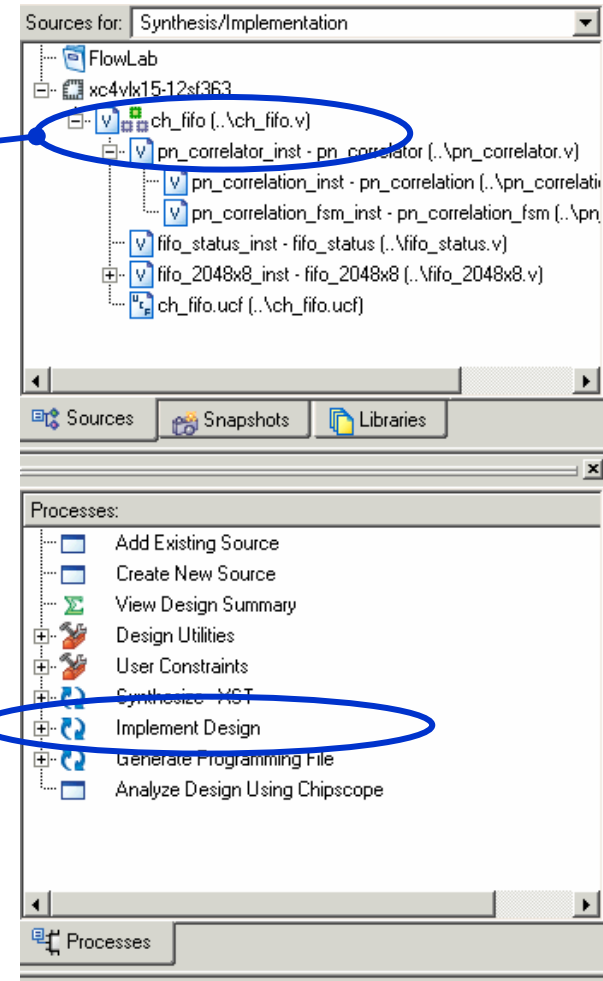
Creating and Adding Source Files

- Double-click **Add Existing Source** to include an existing source file
- Double-click **Create New Source** and choose the type of file to create a new source file
 - HDL
 - IP
 - Schematic
 - State Diagram
 - Testbench
 - Constraints



Implementing a Design

- Implement a design:
 - Select the **top-level source file** in the Sources in Project window
 - HDL, schematic, or EDIF, depending on your design flow
 - Double-click **Implement Design** in the Processes for Source window



Checking the Implementation Status

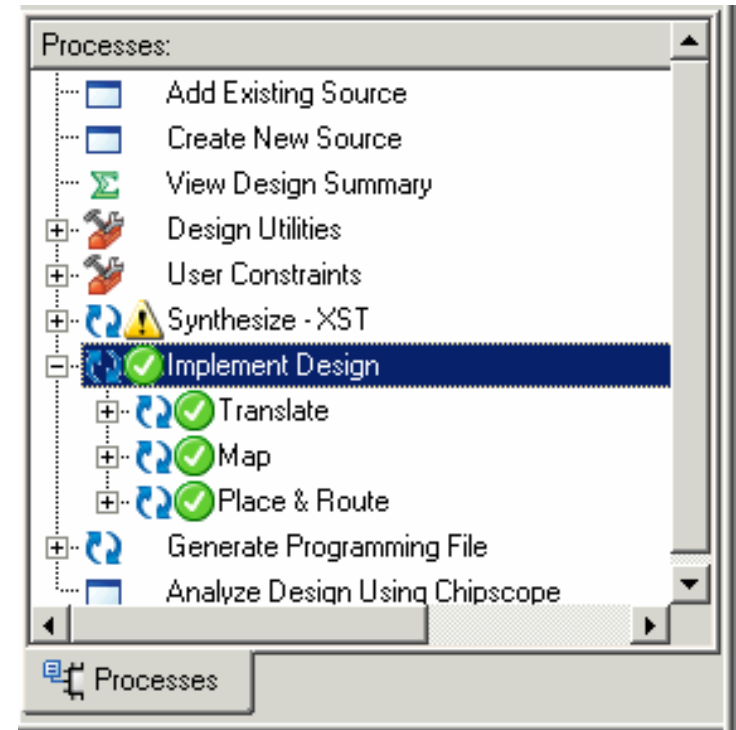
- The ISE™ software will run all of the necessary steps to implement the design
 - Synthesize HDL code
 - Translate
 - Map
 - Place & Route

✓ = process was completed successfully

! = warnings

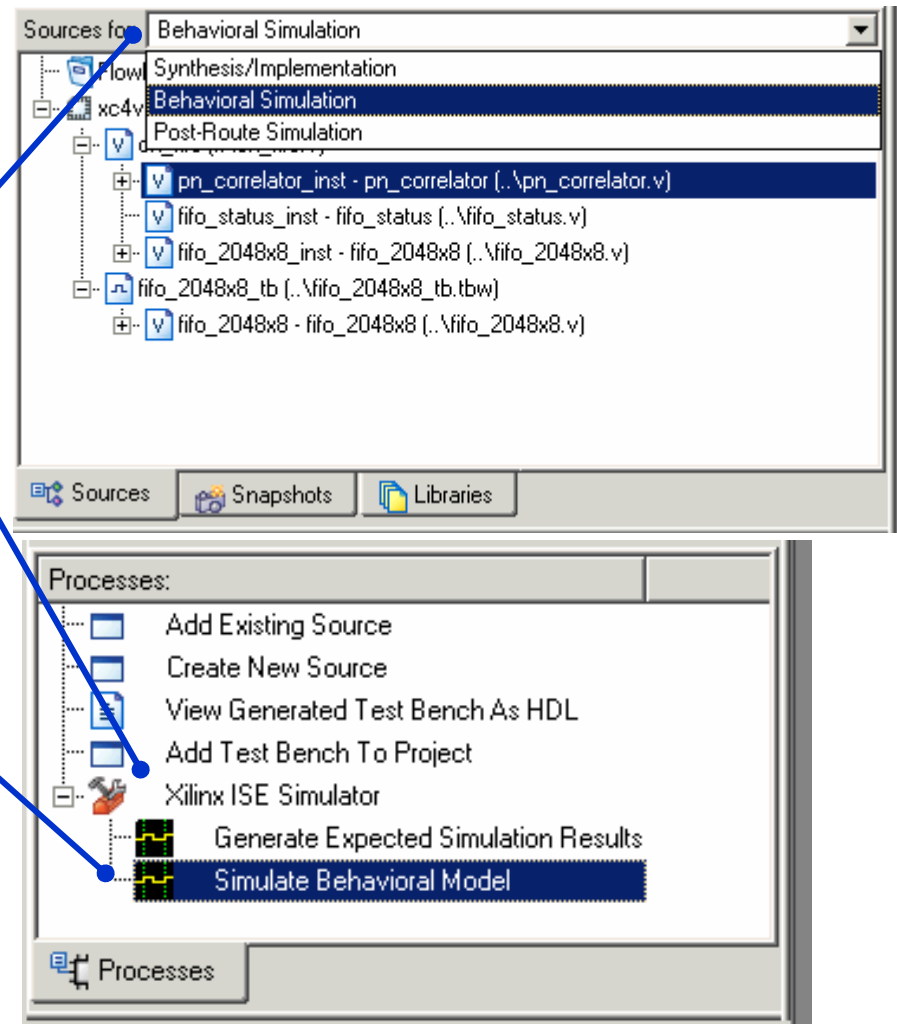
? = a file that is out of date

X = errors



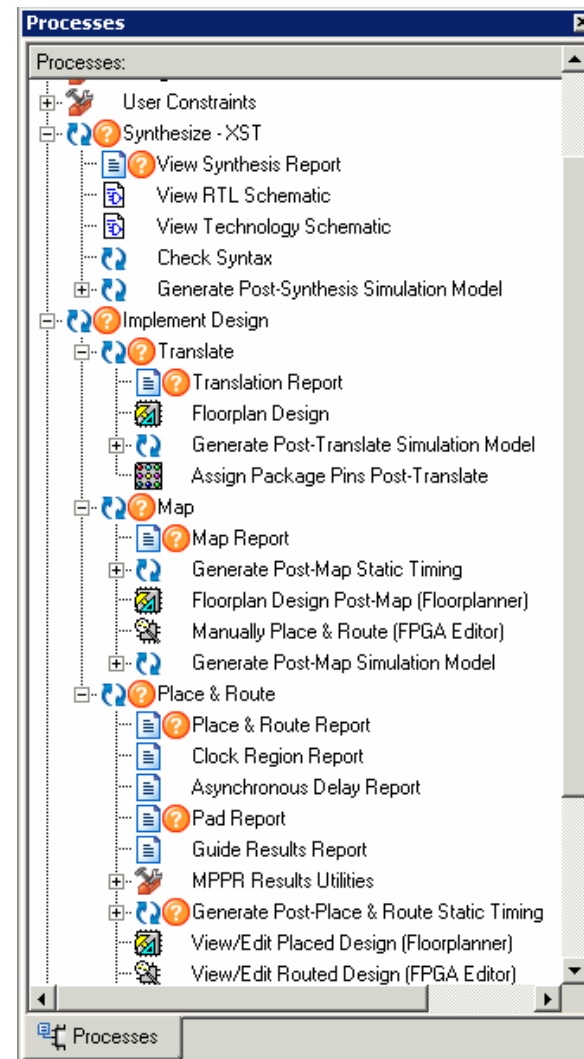
Simulating a Design

- Simulate a design:
 - Select **Sources for: Behavioral Simulation**
 - Expand **Xilinx ISE Simulator** in the Processes for Source window
 - Double-click **Simulate Behavioral Model** or **Simulate Post-Place & Route Model**
 - You can also simulate after Translate or after Map



Viewing Subprocesses

- Expand each process to view subtools and subprocesses
 - Translate
 - Floorplan
 - Assign package pins
 - Map
 - Analyze timing
 - Place & Route
 - Analyze timing
 - Floorplan
 - FPGA Editor
 - Analyze power
 - Create simulation model



The Design Summary Displays Design Data

- Quick View of Reports, Constraints
- Project Status
- Device Utilization
- Design Summary Options
- Performance and Constraints
- Reports

FLOWLAB Project Status

Project File:	FlowLab.isc	Current State:	Placed and Routed
Module Name:	ch_fifo	Errors:	No Errors
Target Device:	xc4vkl15-12sf363	Warnings:	7 Warnings
Product Version:	ISE, 8.1i	Updated:	Wed Oct 12 10:08:46 2005

Device Utilization Summary

Logic Utilization	Used	Available	Utilization	Note(s)
Number of Slice Flip Flops	80	12,288	1%	
Number of 4 input LUTs	136	12,288	1%	
Logic Distribution				
Number of occupied Slices	86	6,144	1%	
Number of Slices containing only related logic	86	86	100%	
Number of Slices containing unrelated logic	0	86	0%	
Total Number 4 input LUTs	137	12,288	1%	
Number used as logic	136			
Number used as a route-thru	1			
Number of bonded I/Os	18	240	7%	
Number of BUFG/BUFGCTRLs	2	32	6%	
Number used as BUFGs	2			
Number used as BUFGCTRLs	0			
Number of FIFO16/RAMB16s	1	48	2%	
Number used as FIFO16s	0			
Number used as RAMB16s	1			
Total equivalent gate count for design	1,699			
Additional JTAG gate count for I/Os	864			

Performance Summary

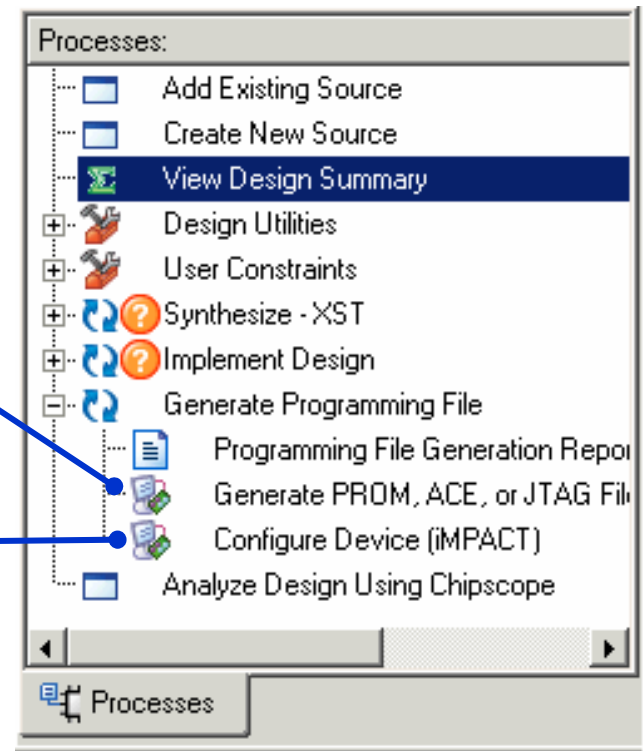
Final Timing Score:	0	Pinout Data:	Pinout Report
Routing Results:	All Signals Completely Routed	Clock Data:	Clock Report
Timing Constraints:	All Constraints Met		

Detailed Reports

Report Name	Status	Generated	Errors	Warnings	Infos
Synthesis Report	Current	Tue Oct 11 15:48:48 2005	0	7 Warnings	10 Infos
Translation Report	Current	Tue Oct 11 15:48:54 2005	0	0	0
Map Report	Current	Tue Oct 11 15:49:05 2005	0	0	2 Infos

Programming the FPGA

- There are two ways to program an FPGA
 - Through a PROM device
 - You must generate a file that the PROM programmer can understand
 - Directly from the computer
 - Use the iMPACT configuration tool



Outline

- Overview
- ISE
- **Summary**
- Lab 1: Xilinx Tool Flow



Review Questions

- What are the phases of the Xilinx design flow?
- What are the components of implementation, and what happens at each step?
- What are two methods of programming an FPGA?

Answers

- What are the phases of the Xilinx design flow?
 - Plan and budget, create code or schematic, RTL simulation, synthesize, functional simulation, implement, timing closure, timing simulation, and BIT file creation
- What are the components of implementation, and what happens at each step?
 - Translate: merges multiple design files into one netlist
 - Map: groups logical symbols into physical components
 - Place & Route: places components onto the chip and connects them
- What are two methods of programming an FPGA?
 - PROM
 - Xilinx iMPACT configuration tool

Summary

- Implementation means more than Place & Route
- Xilinx provides a simple *pushbutton* tool to guide you through the Xilinx design process

Where Can I Learn More?

- Complete design flow tutorials
 - www.xilinx.com → Documentation → Tutorials
- On implementation: Development System Reference Guide
 - www.xilinx.com → Documentation → Software Manuals
 - Documentation may also be installed on your local computer
- On simulation: ISIM Online Help
- Configuration Problem Solver
 - www.xilinx.com → Support → Problem Solvers → Configuration Problem Solver

Outline

- Overview
- ISE
- Summary
- **Lab 1: Xilinx Tool Flow**

