Lab 1: Xilinx Tool Flow Lab

Targeting Spartan-3E Starter Kit

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Xilinx Tool Flow Lab

Introduction

This lab demonstrates the tool flow of Xilinx ISE

Objectives

After completing this lab, you will be able to:

- Create a new project in the ISE Project Navigator
- Add design files to a project
- Use the ISE Simulator to simulate a design
- Use default software options to implement a design

Procedure

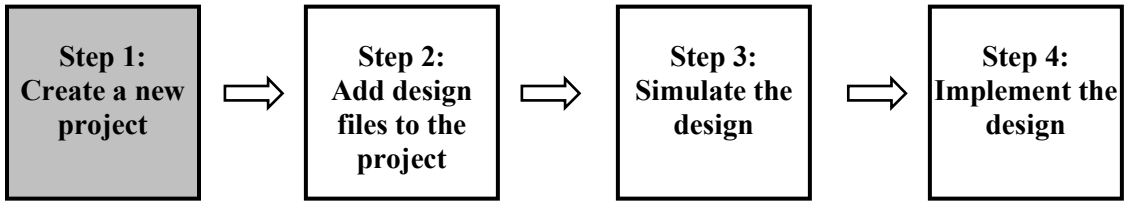
This lab comprises four primary steps:

1. Create a new project
2. Add design files to the project
3. Simulate the design
4. Implement the design

Below each general instruction for a given procedure, you will find accompanying step-by-step directions and illustrated figures that provide more detail for performing the general instruction. If you feel confident about a specific instruction, feel free to skip the step-by-step directions and move on to the next general instruction in the procedure.

Create a new project Step 1

General Flow for this lab:



Launch the ISE Project Navigator and create a new design project.

❶ Select **Start → Programs → Xilinx ISE 9.2i → Project Navigator**

❷ In the Project Navigator, select **File → New Project**

The New Project Wizard opens (**Figure 1.1**)

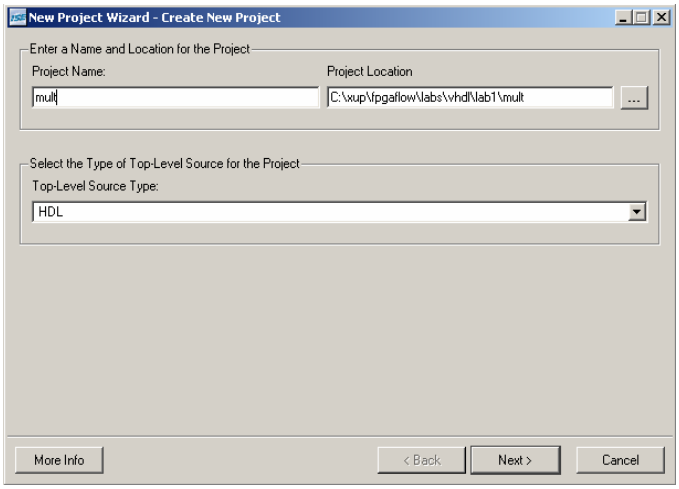


Figure 1.1 - New Project Wizard

❸ For Project Location, use the "**…**" button to browse to one of the following directories, and then click <OK>
- **Verilog users: c:\xup\fpgaflow\labs\verilog\lab1**
- **VHDL users: c:\xup\fpgaflow\labs\vhdl\lab1**

❹ For Project Name, type **mult**

❺ Click **Next**

The Device and Design Flow dialog will appear (**Figure 1.2**)

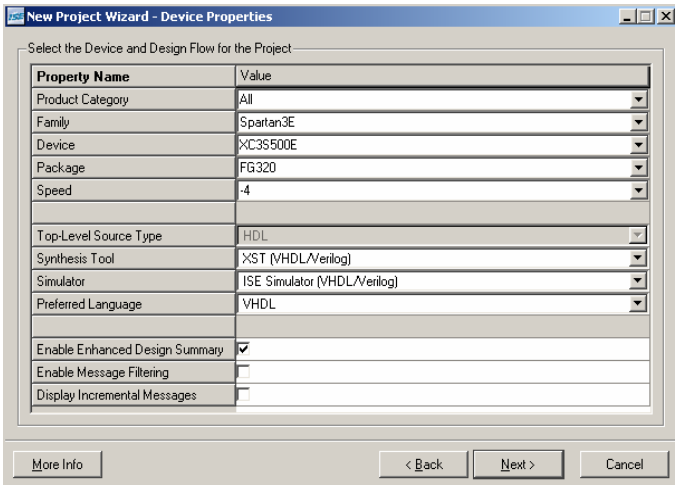


Figure 1.2 - Device and Design Flow Dialog

❻ Select the following options and click **Next**:

Device Family	:	**Spartan3E**
Device	:	**XC3S500E**
Package	:	**FG320**
Speed Grade	:	**–4**
Synthesis Tool	:	**XST (VHDL/Verilog)**
Simulator	:	**ISE Simulator (VHDL/Verilog)**
Preferred Language	:	**Verilog** or **VHDL** *(select your preference)*

The Create New Source dialog will appear (Figure 1.3). You can use this dialog to create a new HDL source file by defining the module name and ports. All of the source files have been created for you in this project.

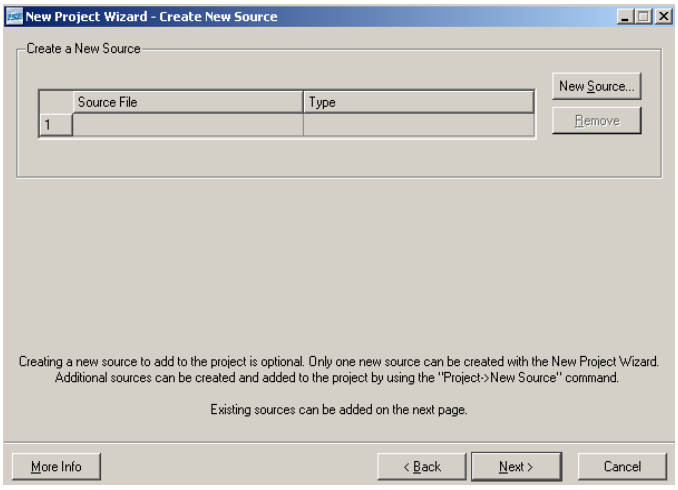


Figure 1.3 - Create New Source Dialog

❼ Click **Next**

The Add Existing Sources dialog appears (**Figure 1.4**).

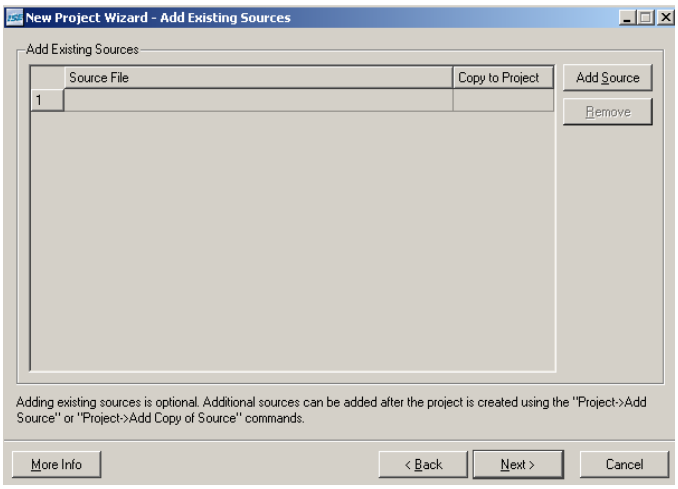
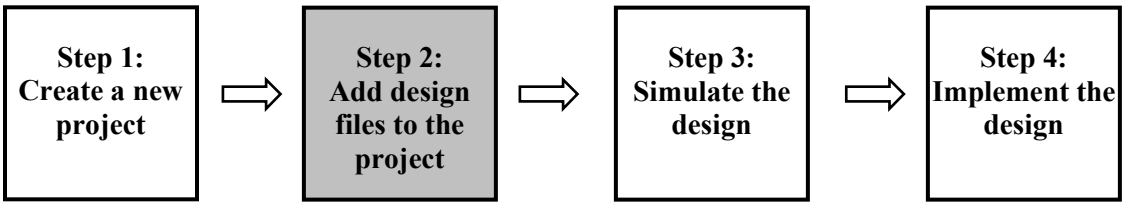


Figure 1.4 - Add Existing Sources Dialog

Add Design Files for the Project — Step 2

General Flow for this lab:



Add HDL source files into the project.

❶ Click **Add Source** and browse to the **c:\xup\fpgaflow\sources\vhdl** *or* **c:\xup\fpgaflow\sources\Verilog** folder

❷ Select the VHDL/Verilog files **mult** and **tb_mult** files and click **Open**.

❸ Click **<Next>** leaving a check mark in each box for the copy to project option. Click **Finish**.

The dialogue below should appear which allows you to select a flow associated with each source file.

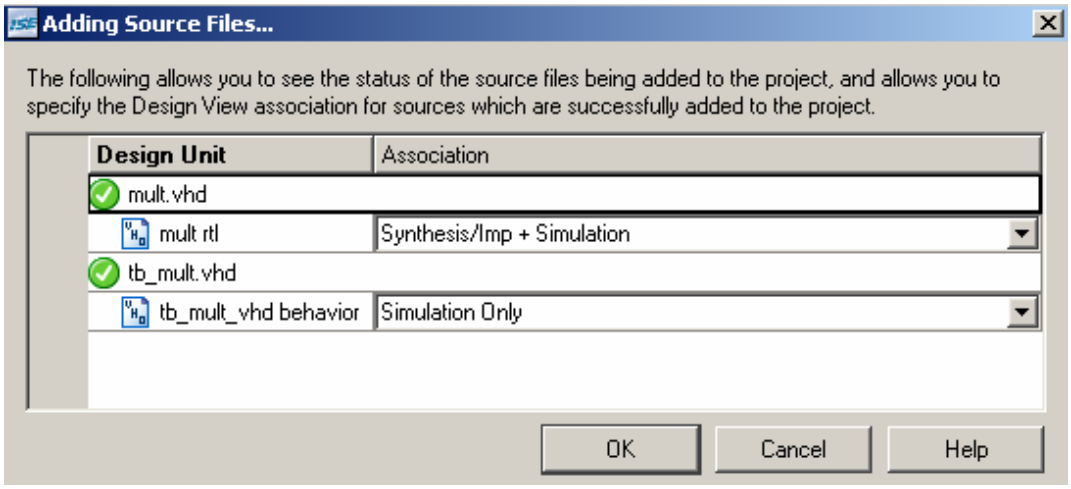


Figure 2.1 - Choose Source Type

❹ Click **<OK>** accepting the default settings.

❺ ISE copies the source file and creates a project. Note that in the "**Sources for**" window of ISE Project Navigator only **mult** is present since the flow is **"Synthesis/Implementation"**.

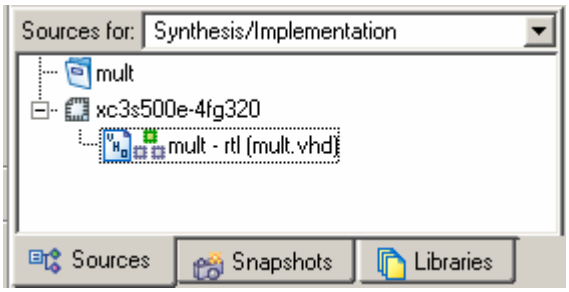


Figure 2.2 – Sources window

1. What Information can you gather from Sources Window?

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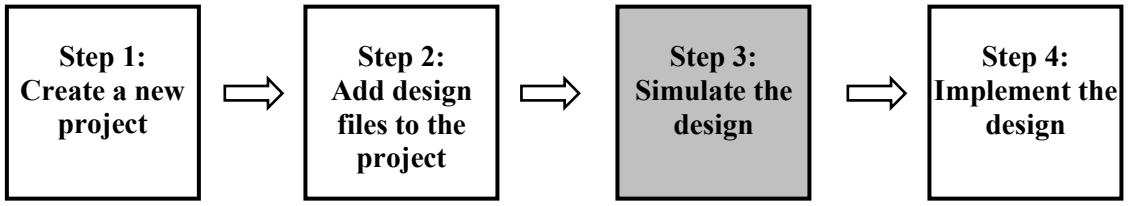
Simulate the design Step 3

General Flow for this lab:



Run a Behavioral Simulation of the design using ISE simulator and examine the results.

❶ In the **Sources for** window, select **"Behavioral Simulation"** from the drop-down list.

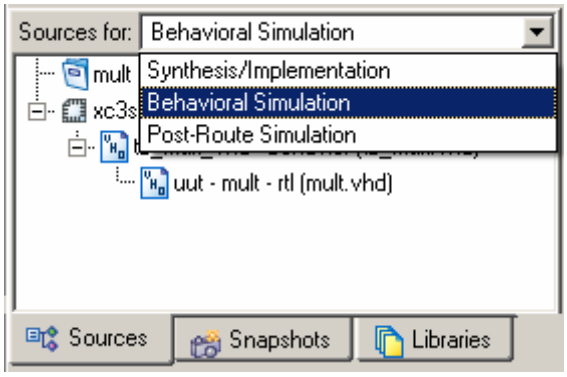


Figure 3.1 – Sources for – Behavioral Simulation

❷ In the Sources For window, double click on **tb_mult** (_vhd or _v) to open the Testbench. Browse this simple Testbench. If you have any questions ask the instructor.

❸ With the testbench – **tb_mult** selected in the sources window, expand **Xilinx ISE Simulator** in the **Processes** window and double click on **Simulate Behavioral Model.**

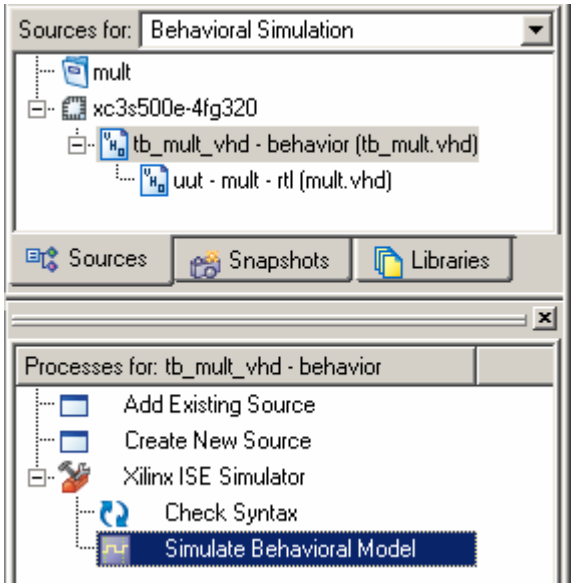


Figure 3.2 – Simulate the design

❹ ISE simulator runs the simulation for 1000 ns (default value). When the simulation completes, waveform window will appear displaying the Simulation results.

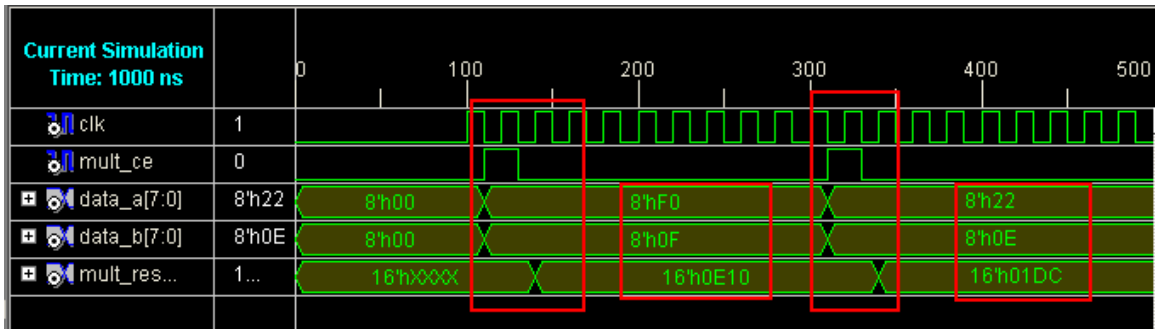


Figure 3.3 - Simulation Result

❺ Examine the simulation results and confirm that that **mult_result** appears two clock cycles after the **mult_ce** is applied.

❻ Close the **simulator Waveform window** to end the simulation.

2. Why did we include running a simple simulation in this lab?

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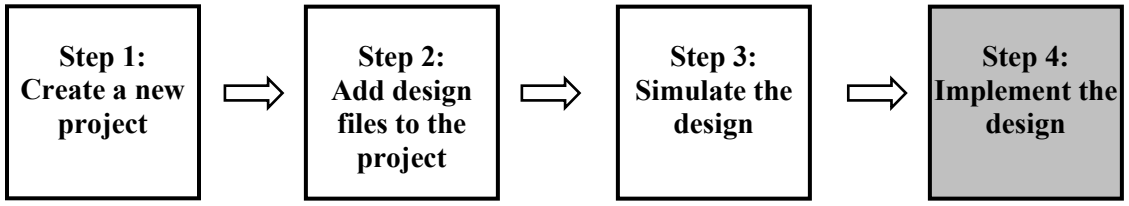
Implement the design Step 4

General Flow for this lab:



Implement the design. During implementation, some reports will be created. You will look more closely at some of these reports in the next module.

❶ In the Sources For window, select **Synthesis/Implementation** from the drop-down list and select the **mult.vhd or mult.v** top level module.

❷ In the Processes for Source window, double-click **Implement Design** (**Figure 4.1**)

Notice that the tools run all of the processes required to implement the design. In this case, the tools run Synthesis before going into Implementation.

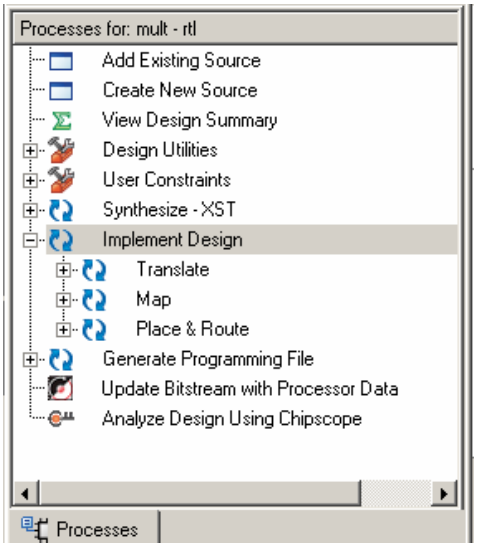


Figure 4.1 - Processes for Source Window

❸ While the implementation is running, click the + next to **Implement Design** to expand the implementation step and view the progress. We refer to this as *expanding* a process

After each stage is completed, a symbol will appear next to each stage:

- => Process completed successfully
- => Warnings
- => Errors
- => A file that is out of date

❹ Read some of the messages in the message window located across the bottom of the Project Navigator window.

❺ When implementation is complete, double click on View Design Summary in the processes window(Figure 4.2).

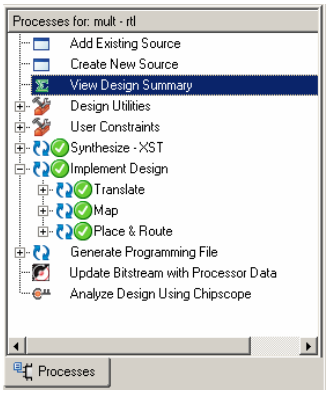


Figure 4.2 – View Design Summary

MULT Project Status			
Project File:	mult.ise	**Current State:**	Placed and Routed
Module Name:	mult	**• Errors:**	No Errors
Target Device:	xc3s500e-4fg320	**• Warnings:**	No Warnings
Product Version:	ISE 9.2.04i	**• Updated:**	Wed Feb 27 18:10:45 2008

Device Utilization Summary				
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Logic Distribution				
Number of Slices containing only related logic	0	0	0%	
Number of Slices containing unrelated logic	0	0	0%	
Number of bonded IOBs	34	232	14%	
Number of GCLKs	1	24	4%	
Number of MULT18X18SIOs	1	20	5%	
Total equivalent gate count for design	3			
Additional JTAG gate count for IOBs	1,632			

Performance Summary			
Final Timing Score:	0	**Pinout Data:**	Pinout Report
Routing Results:	All Signals Completely Routed	**Clock Data:**	Clock Report
Timing Constraints:	All Constraints Met		

Detailed Reports					
Report Name	**Status**	**Generated**	**Errors**	**Warnings**	**Infos**
Synthesis Report	Current	Wed Feb 27 18:07:26 2008	0	0	0
Translation Report	Current	Wed Feb 27 18:07:31 2008	0	0	0
Map Report	Current	Wed Feb 27 18:07:37 2008	0	0	3 Infos
Place and Route Report	Current	Wed Feb 27 18:07:49 2008	0	0	1 Info
Static Timing Report	Current	Wed Feb 27 18:07:53 2008	0	0	3 Infos
Bitgen Report					

Figure 4.3 - Design Summary

Conclusion

In this lab, you completed the major stages of the ISE™ design flow: creating a project, adding source files, simulating the design, and implementing the design.

In the next module, you will examine some of the software reports, determine how the design was implemented, and determine whether or not design goals for area and performance were met.