Digital Current-Mode Control of DC-DC Converters

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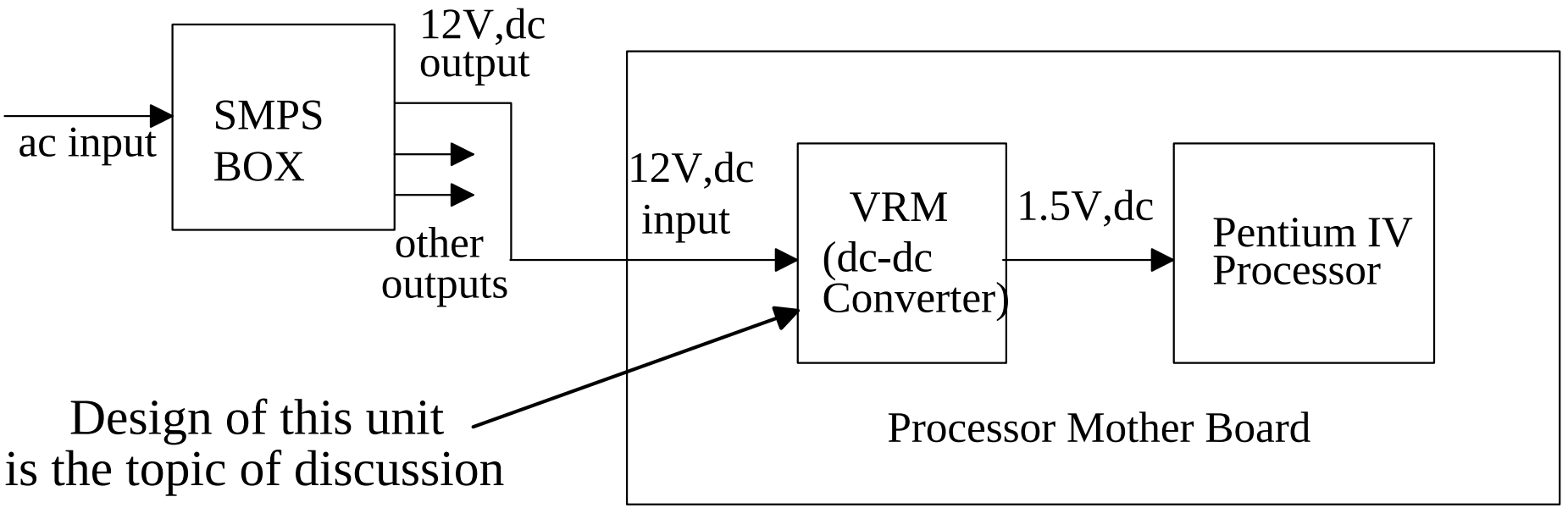
Objectives /Scope

Presents the application areas that require digital control of DC-DC converters

Answers the question why Digital Current-Mode Control is preferable over Digital Voltage-Mode Control.

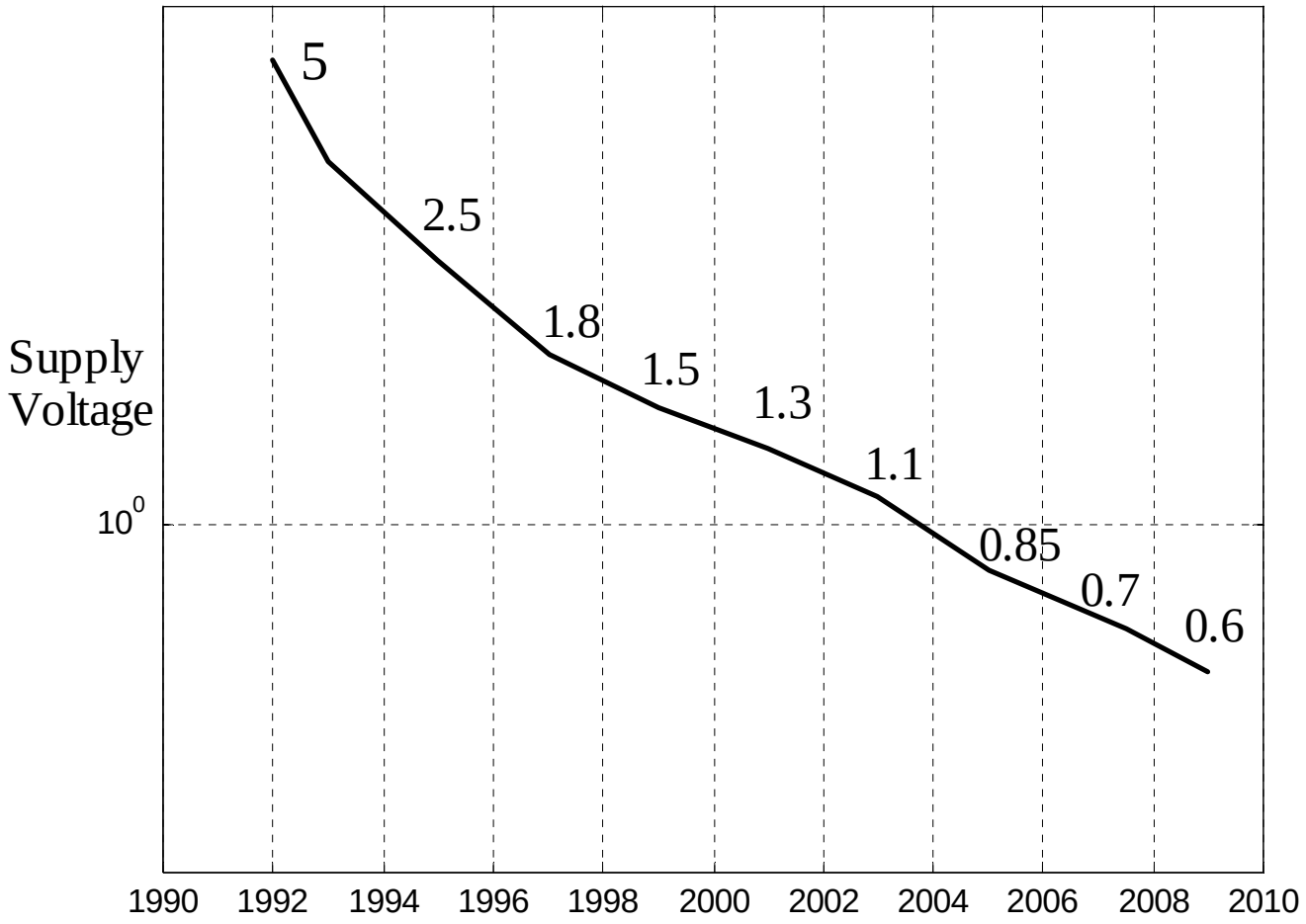
Presents analysis and implementation of the proposed Digital Current-Mode Control.

VRM : Connection Configuration



A Typical Connection Configuration of Voltage Regulator Module (VRM)

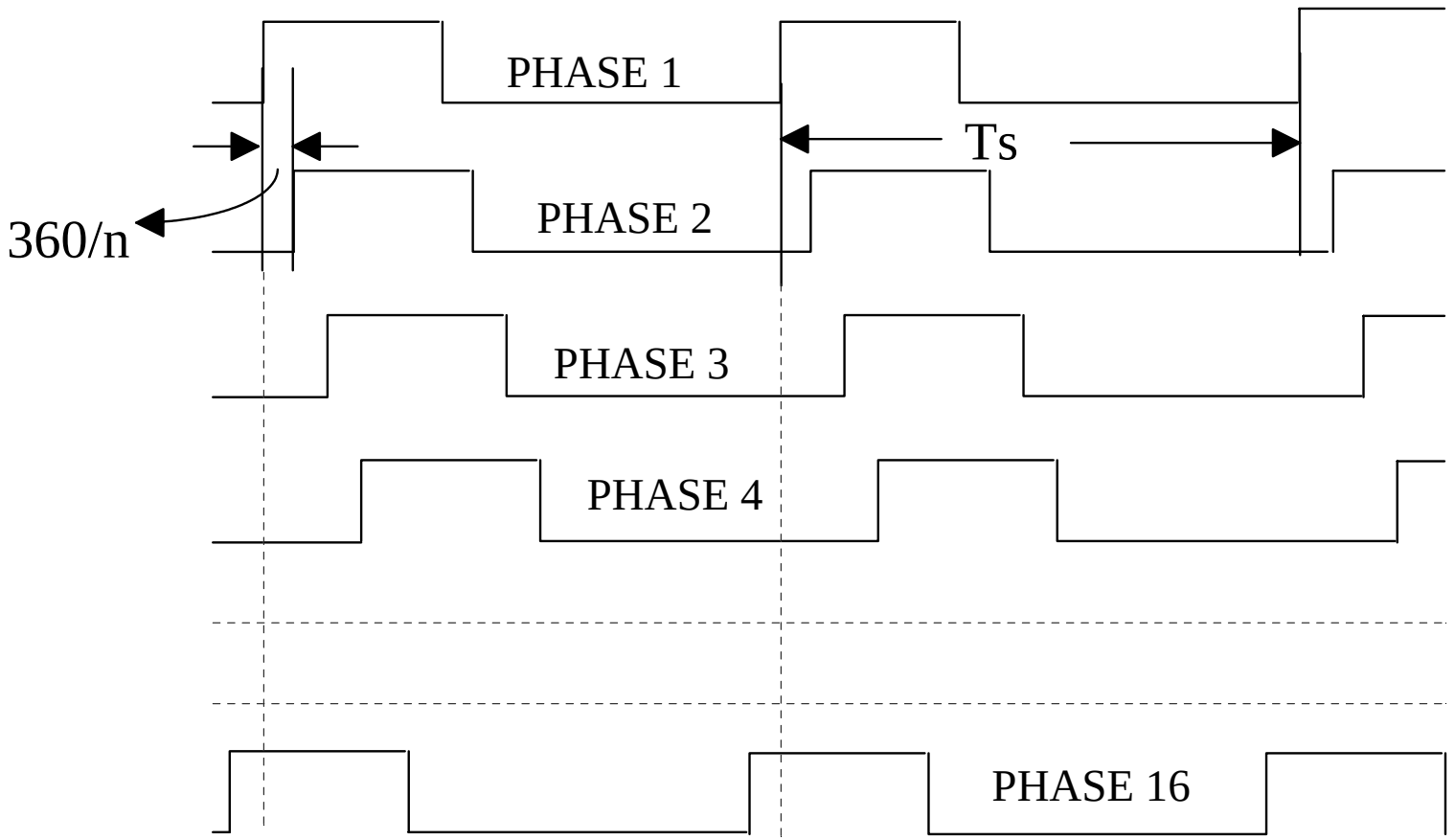
VRM : Voltage Roadmap for Intel's Microprocessors



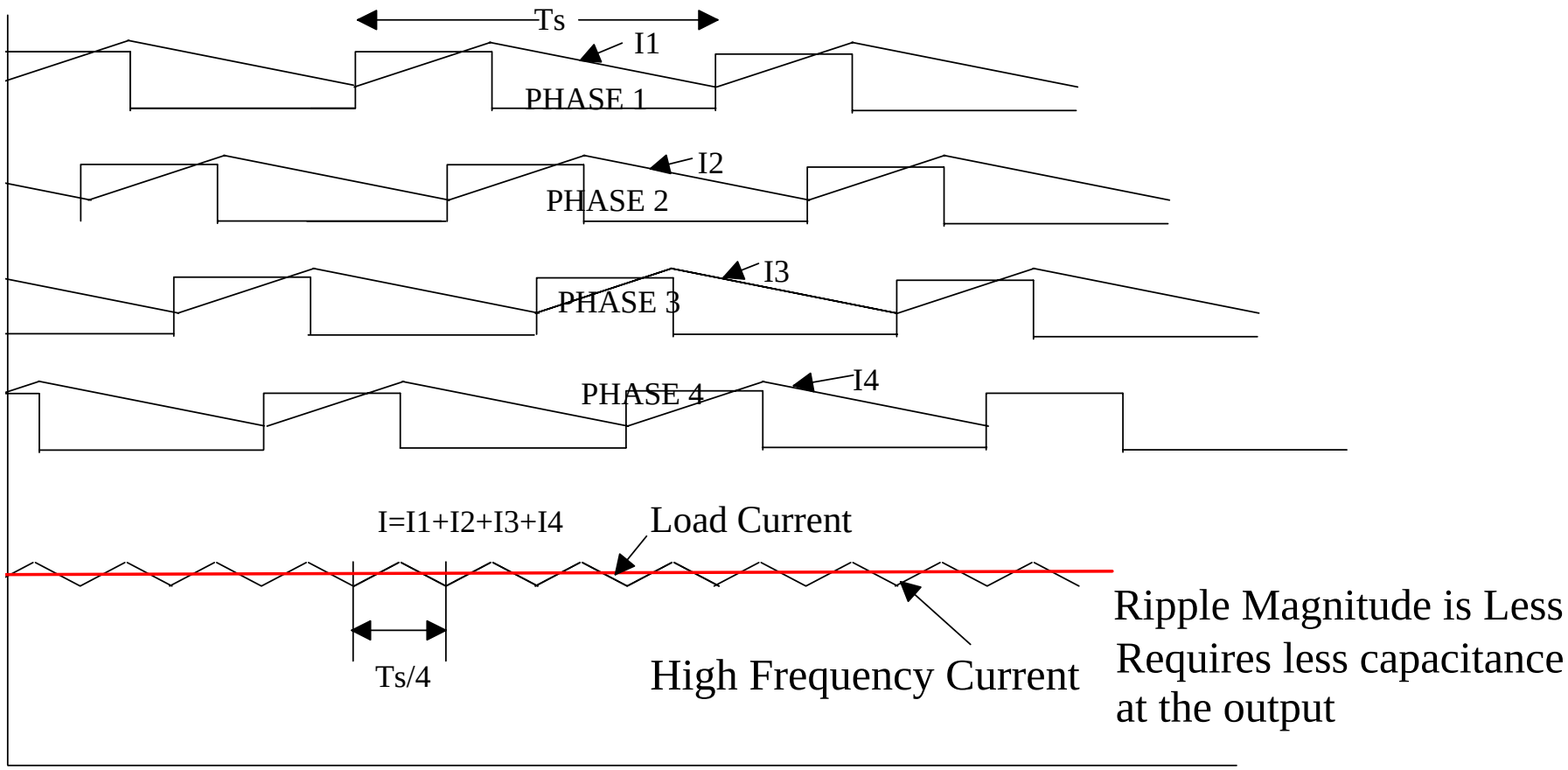
VRM : Next Generation Microprocessor VRM Specifications

V_{in}	input voltage	>12 V
V_{ref}	reference voltage	<1 V
$\Delta V_{o,\max}$	regulation tolerance	< 50 mV
$I_{o,\max}$	load current	> 100 A
$\frac{dI_o}{dt}$	current slew rate	> 350A/μSec
T_d	regulator response time	<200 ns

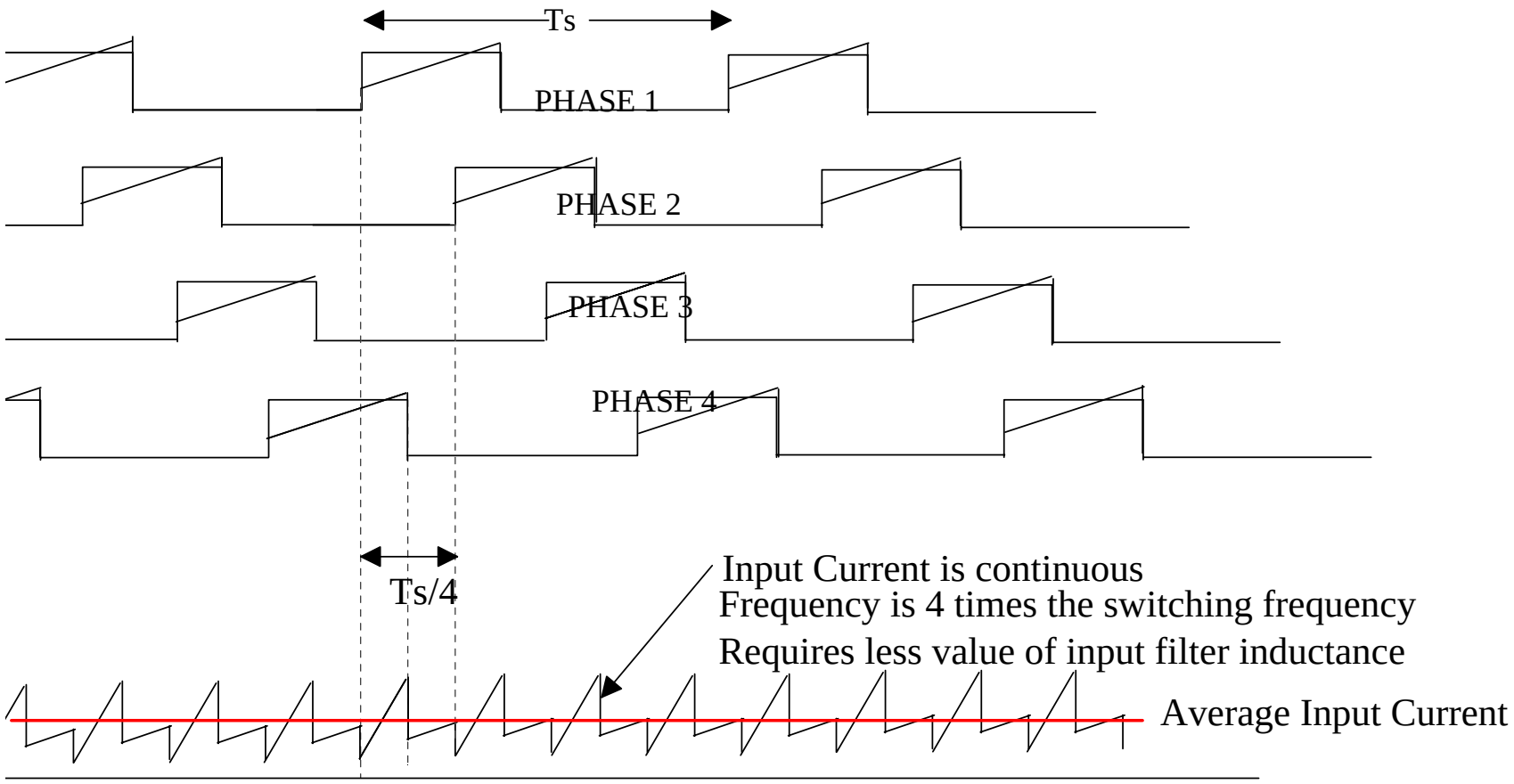
Driving Signals of Multiphase Converter



Other Advantage: Less Output Capacitance



Other Advantage: Less Input Filter Inductance



VRM : Advantages of multiphase

(1) Reduce the output voltage ripple (as the effective frequency is $n * f_s$)
(2) Redule the input current ripple (as the effective frequency is $n * f_s$)
(3) Better transient response

VRM : Disadvantages of miltiphase

Phase current mismatch due to
(1) Duty ratio and frequency mismatch between phases
(2) Power train resistance mismatch
(3) MOSFET switching parameter mismatch

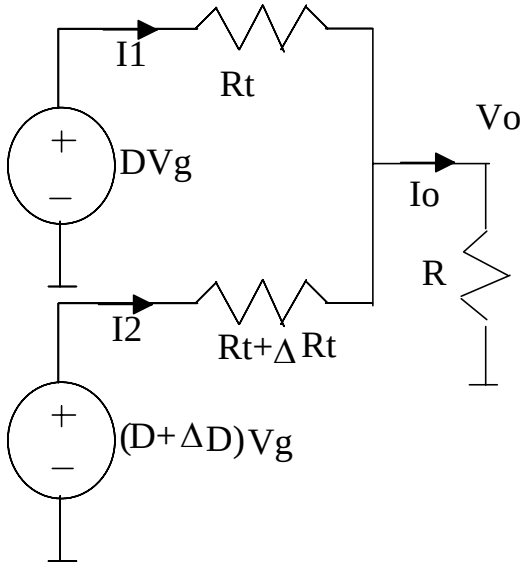
VRM : Preferred Control Method

Digital
(1) Immunity to analog component variations
(2) Can implement sophisticated control - precise matching of duty ratio
(3) Ease of integration with other digital system

Multiphase Converter: Design Problems

- Current in each phase of the converter need not be equal due to unbalance in circuit components and duty ratios.

- Typically 1% difference in the duty ratio would cause about 47% unbalance in the current.



Steady State Equivalent Circuit of Unbalance

If R>>Rt and ΔRt=0 then

Current Unbalance is given by

$$\frac{\Delta D}{D}\ \frac{R}{Rt}$$

Multiphase Converter: Reasons for Current Unbalance

- PCB trace layout of each phase need not be exactly identical
- The dc resistances of the inductors need not be exactly same
- The Rds(on) of the MOSFETs of the same part number may also be slightly different.
- The switching characteristics of the power semiconductor devices and the threshold voltages of the gate need not be exactly same and this will result into unequal effective duty ratios in the phases
- The duty ratio signals generated by the analog PWM controller need not exactly match in all the phases. => Most Important

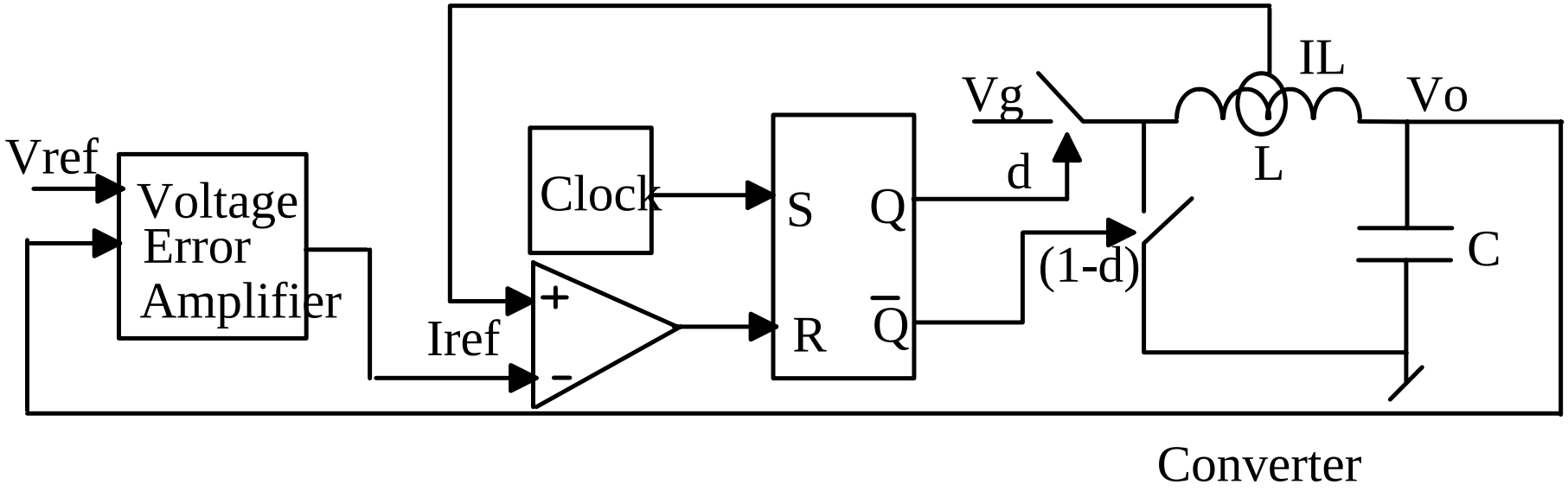
Multiphase Converter: Solutions to Current Unbalance

Try Passive Current Equalization Techniques:

- ✓ Symmetrical low resistance layout of each phase of the converter.
- ✓ Selection of very low Rds(on) MOSFETs
- ✓ Implement the control algorithm in a high performance digital hardware such as FPGA (Field Programmable Gate Array).
- ✓ => Most Important : Introduce a current loop per phase.

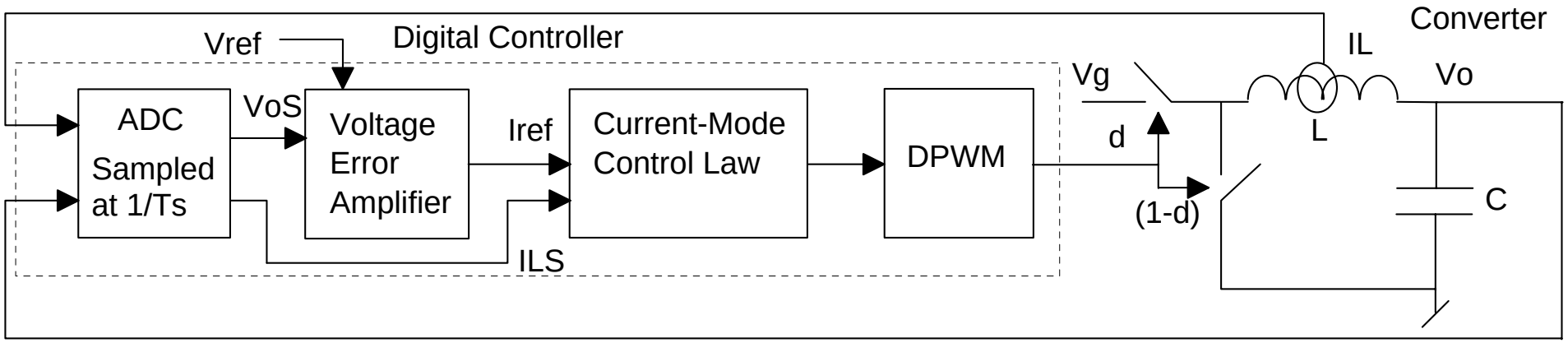
=> Solution : DIGITAL CURRENT-MODE CONTROL

Analog Current Mode Control: Schematic Diagram



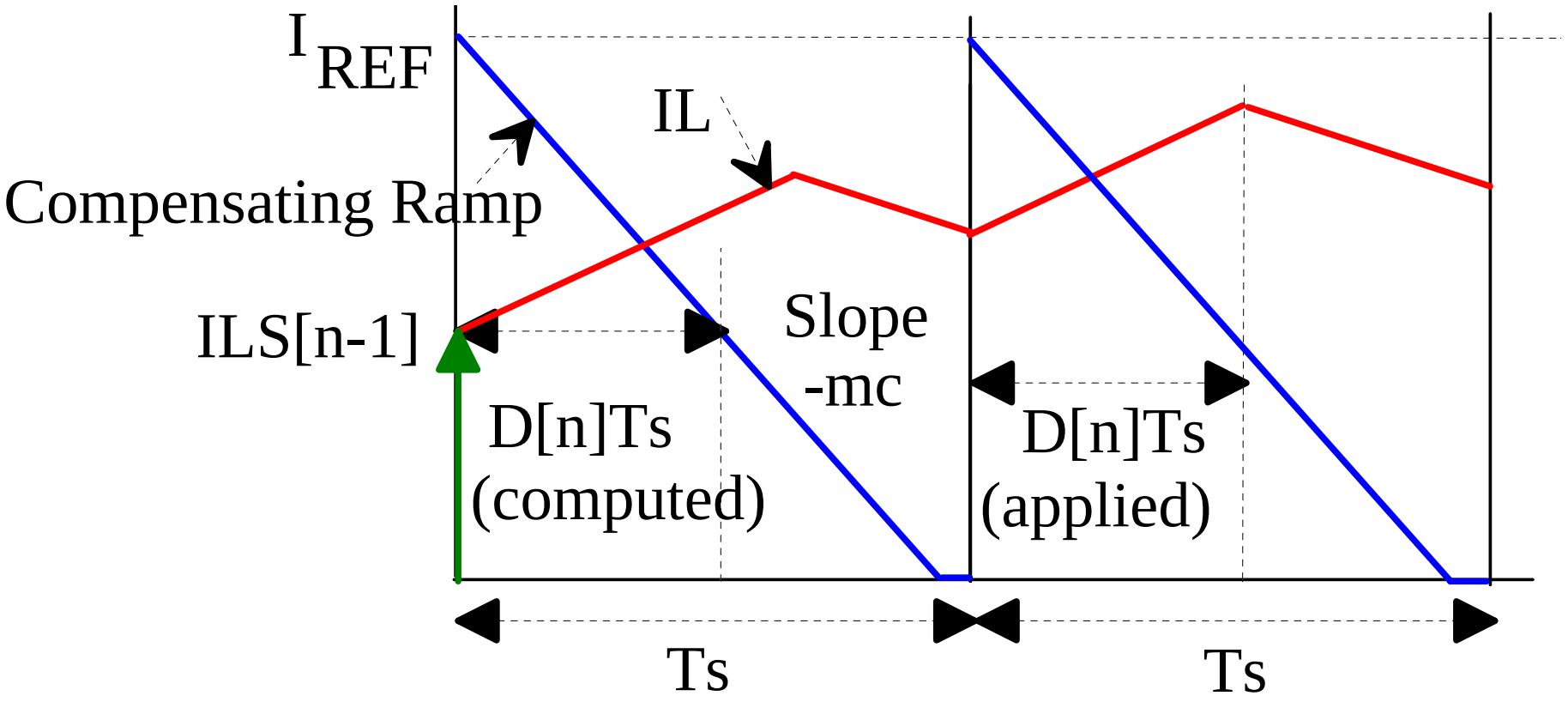
Note: During ON-time inductor current IL is continuously sensed

Digital Current Mode Control: Circuit Schematic



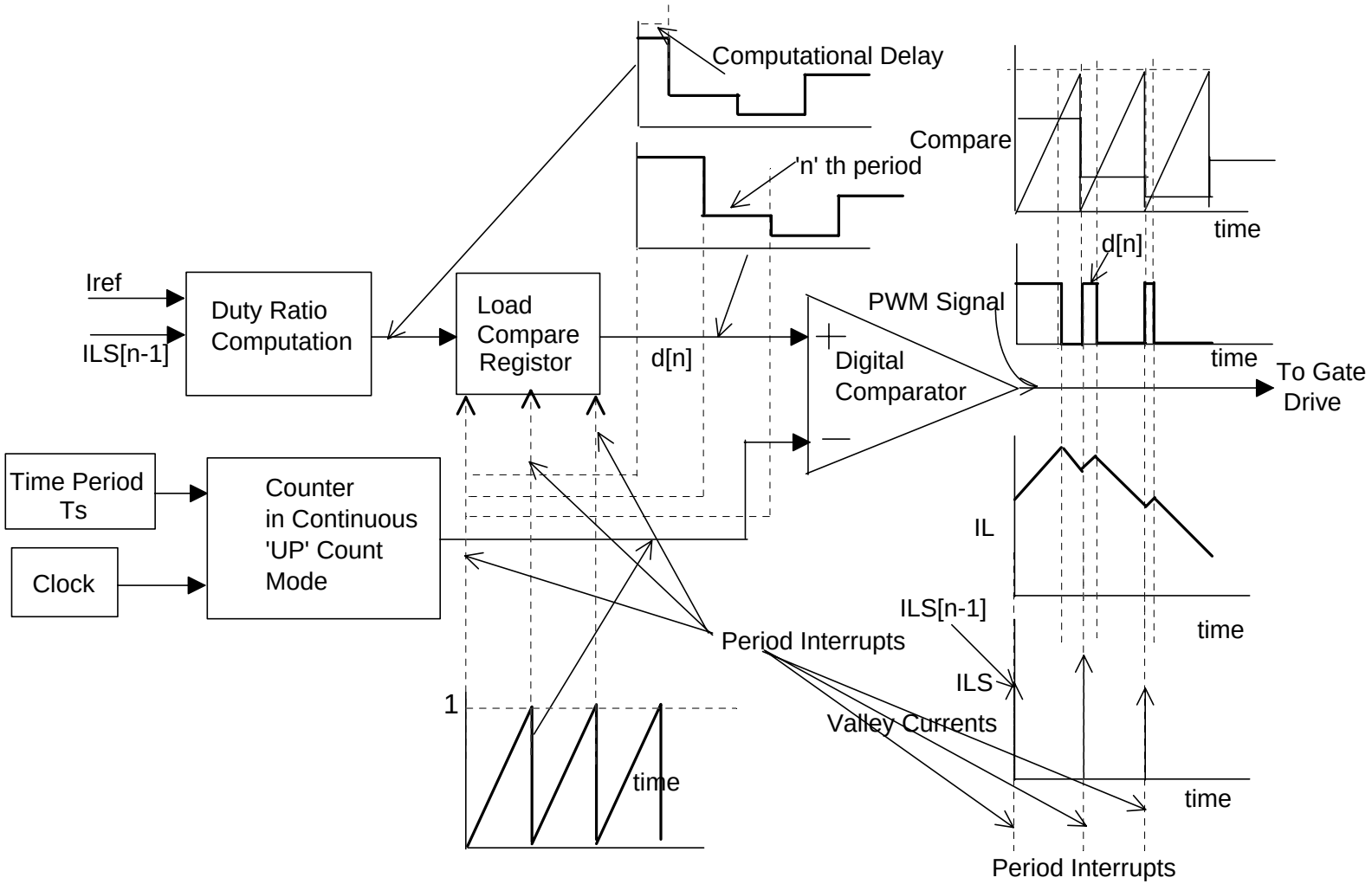
Note: The Current is sampled only once in a switching period (Ts)

Proposed Control Law: Duty Ratio Generation

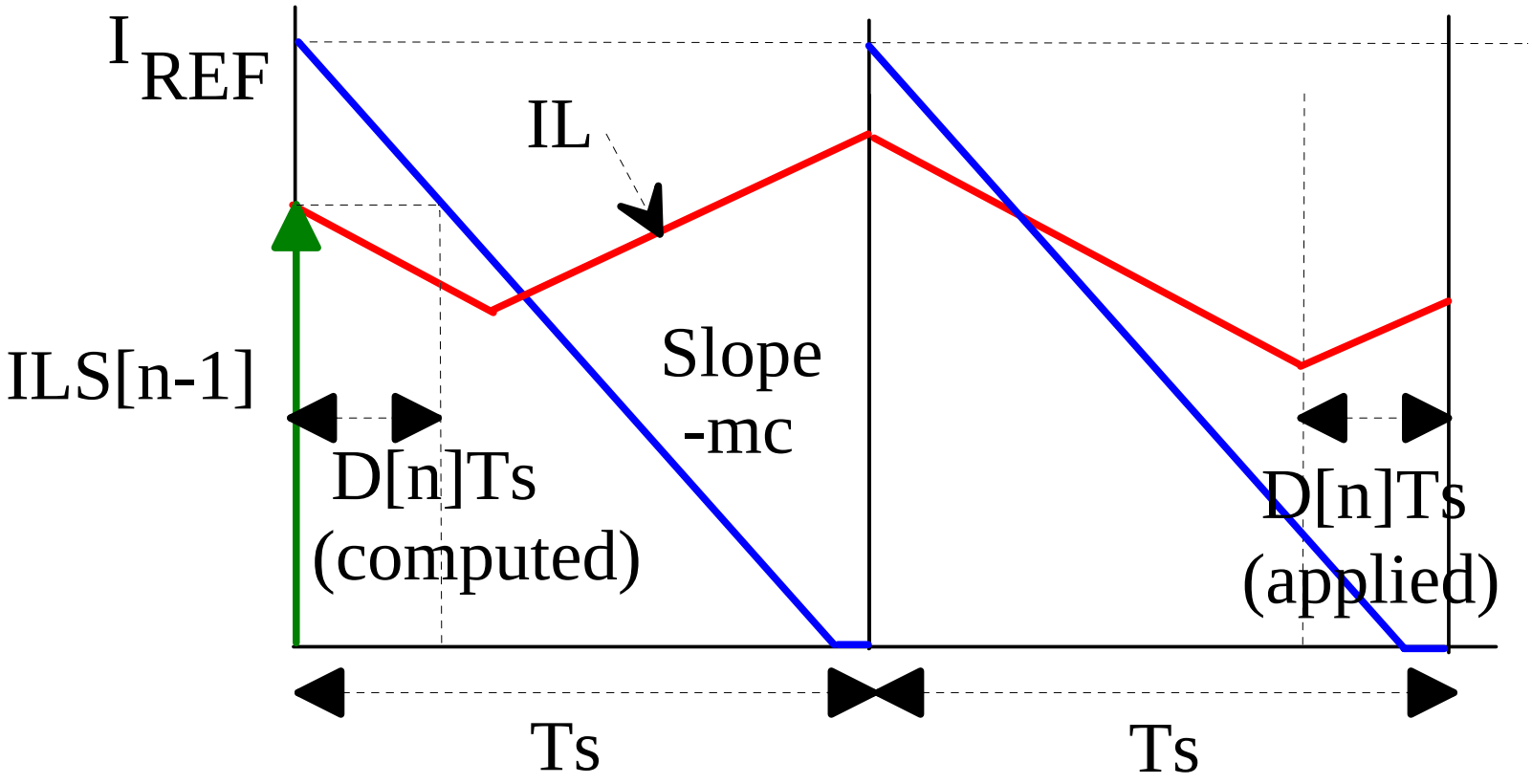


Note: Use of Compensating Ramp
One Cycle Delay in Effective Duty Ratio
Valley Current Mode Control

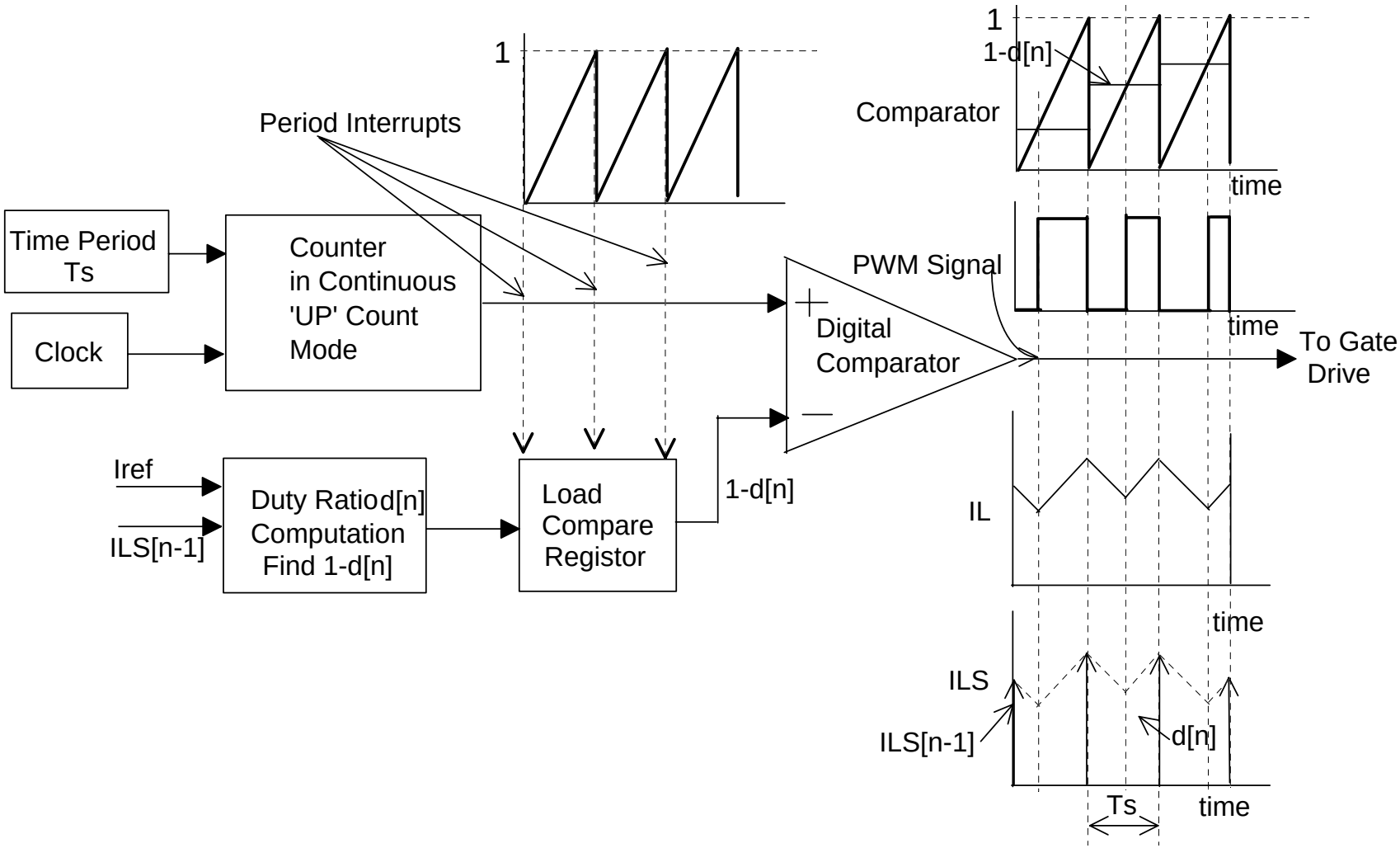
Digital Pulse Width Modulator: Valley Current Mode Control



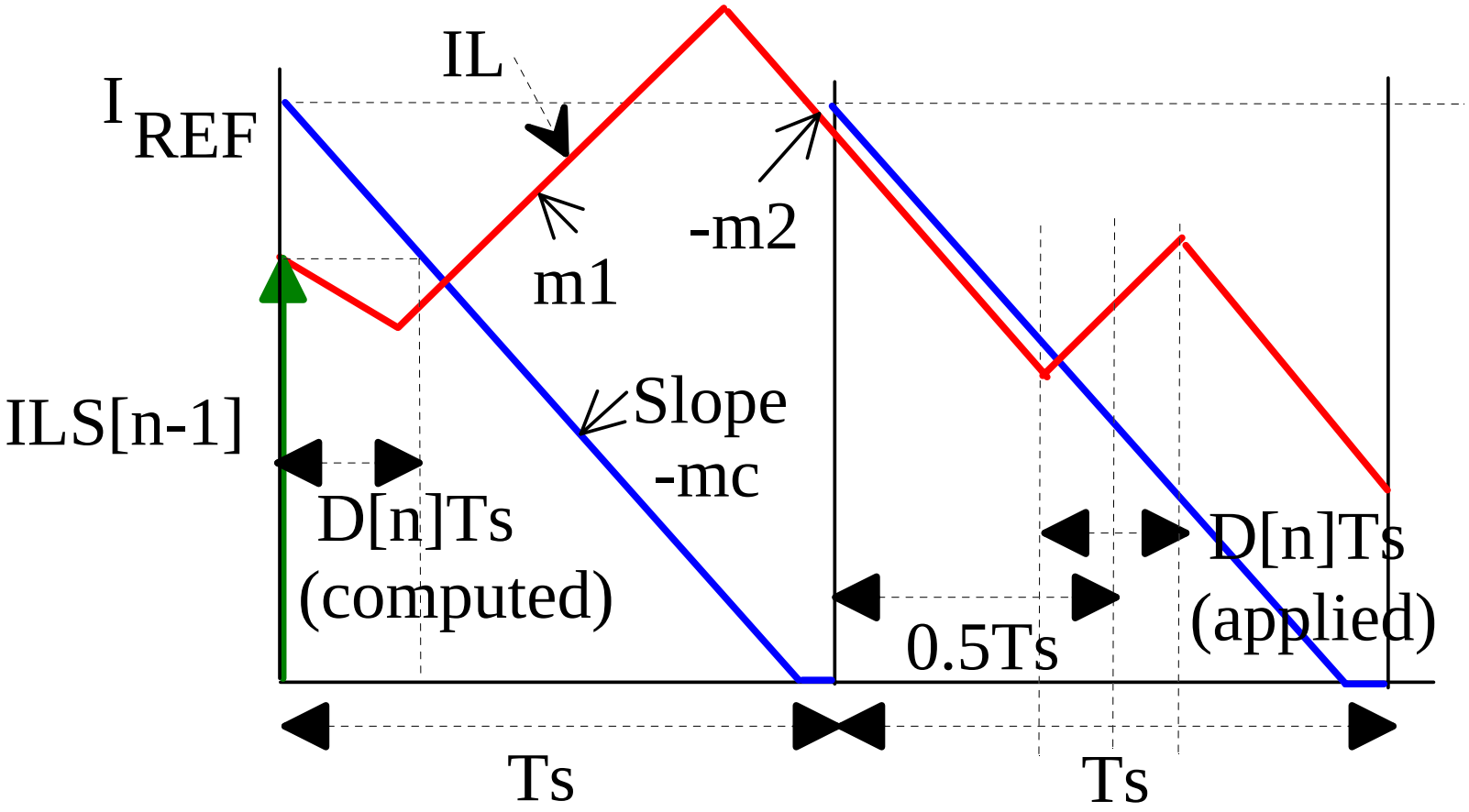
Peak Current Mode Control



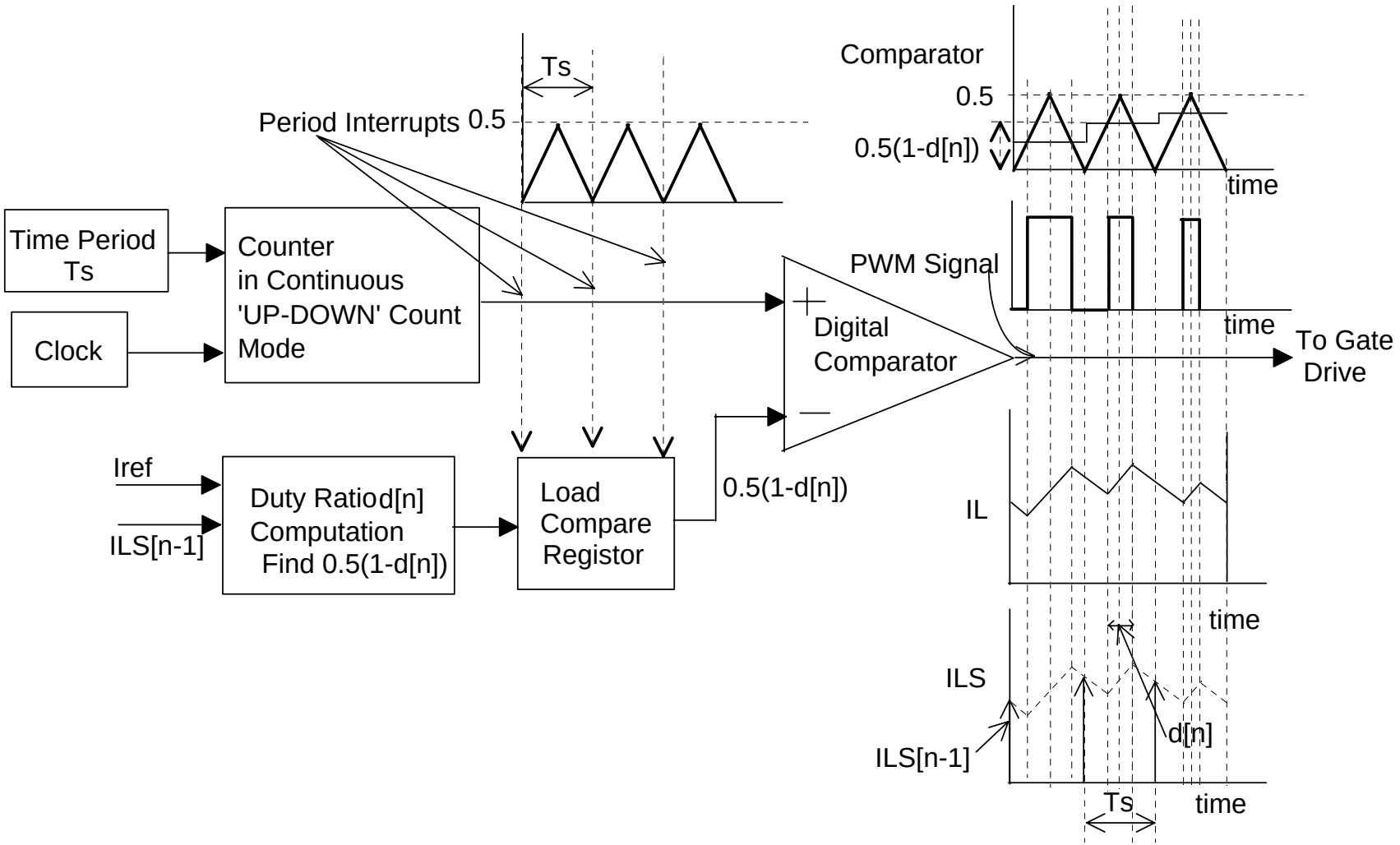
Digital Pulse Width Modulator: Peak Current Mode Control



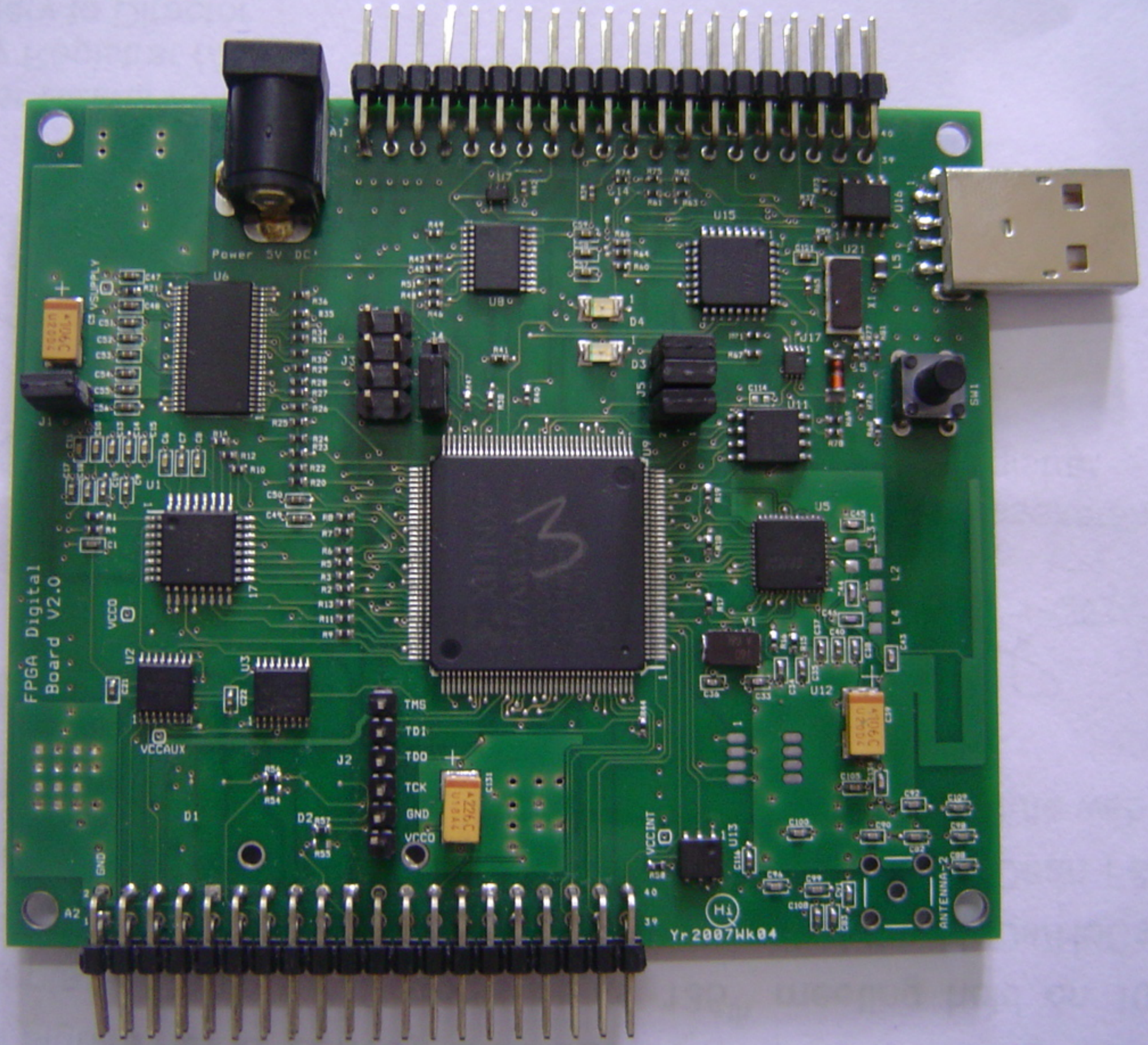
Average Current Mode Control



Digital Pulse Width Modulator: Average Current Mode Control



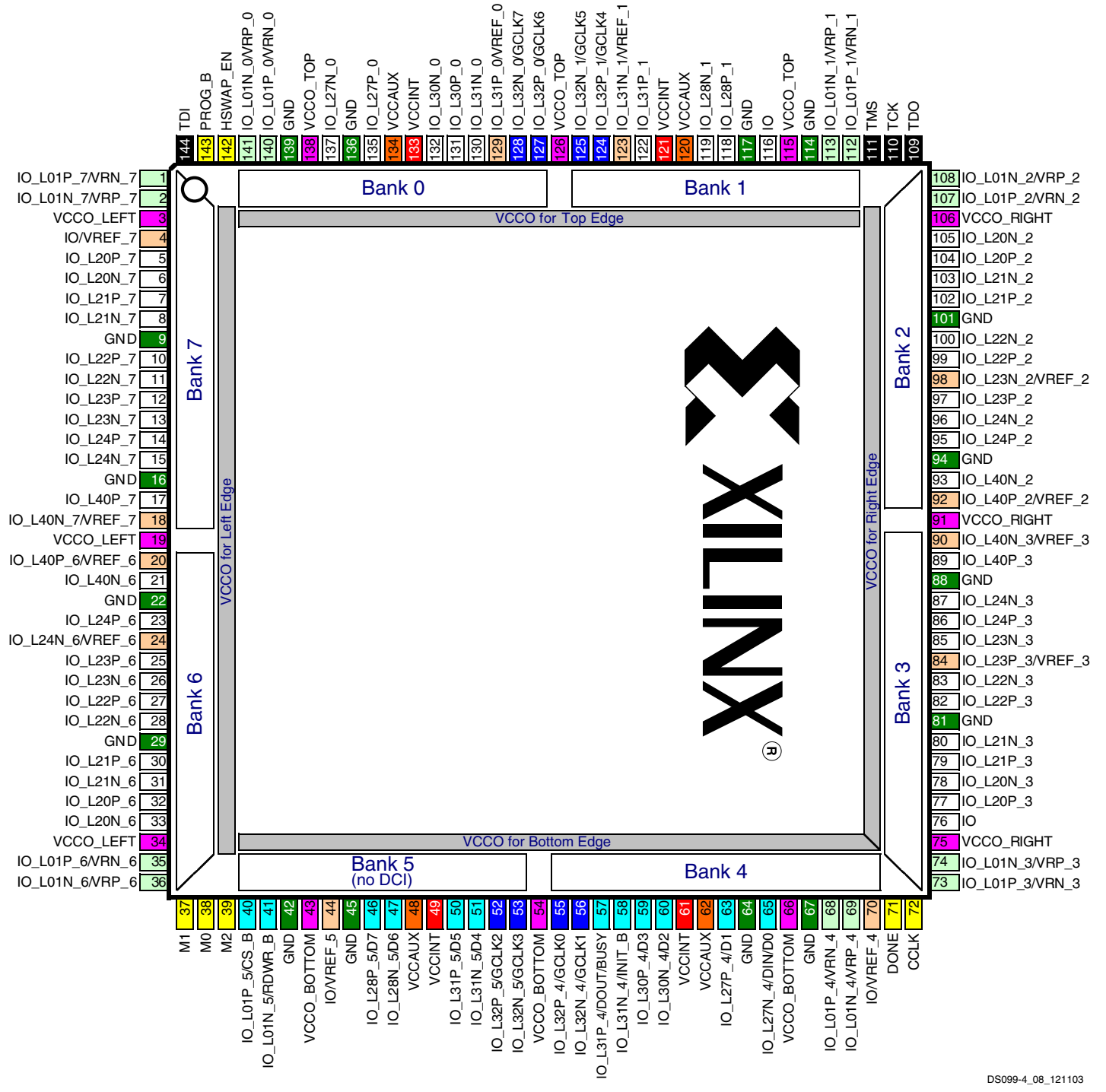
Multiphase Converter: Digital Control Board (Version I)


FPGA Digital
Board V2.0
Power 5V DC
VSUPPLY
VCCO
VCCAUX
VCCINT
GND
TMS
TDI
TDO
TCK
GND
VCCO
J1
J2
J3
J4
J5
D1
D2
D3
D4
U1
U2
U3
U5
U6
U8
U11
U12
U13
U15
U17
U21
Y1
SW1
ANTENNA-2
Yr2007Wk04

Digital Hardware : Advantage of FPGA Over DSP in VRM Application

- The desirable bandwidth of VRM >100 KHz
- Switching frequency required > 500 kHz.
- Control loop execution time < 2 μsec
- TI's DSP TMS320F2407 Clock Frequency: 40 MHz
- Spartan-III FPGA Clock Frequency: 250 MHz
- Advantage of FPGA : Concurrency => faster execution
- In this project digital current mode control algorithm has been implemented in Spartan III FPGA devices

TQ144 Footprint



DS099-4_08_121103

Figure 7: **TQ144 Package Footprint (top view). Note pin 1 indicator in top-left corner and logo orientation.**

51 **I/O:** Unrestricted, general-purpose user I/O	12 **DUAL:** Configuration pin, then possible user I/O	12 **VREF:** User I/O or input voltage reference for bank
14 **DCI:** User I/O or reference resistor input for bank	8 **GCLK:** User I/O or global clock buffer input	12 **VCCO:** Output voltage supply for bank
7 **CONFIG:** Dedicated configuration pins	4 **JTAG:** Dedicated JTAG port pins	4 **VCCINT:** Internal core voltage supply (+1.2V)
0 **N.C.:** No unconnected pins in this package	16 **GND:** Ground	4 **VCCAUX:** Auxiliary voltage supply (+2.5V)

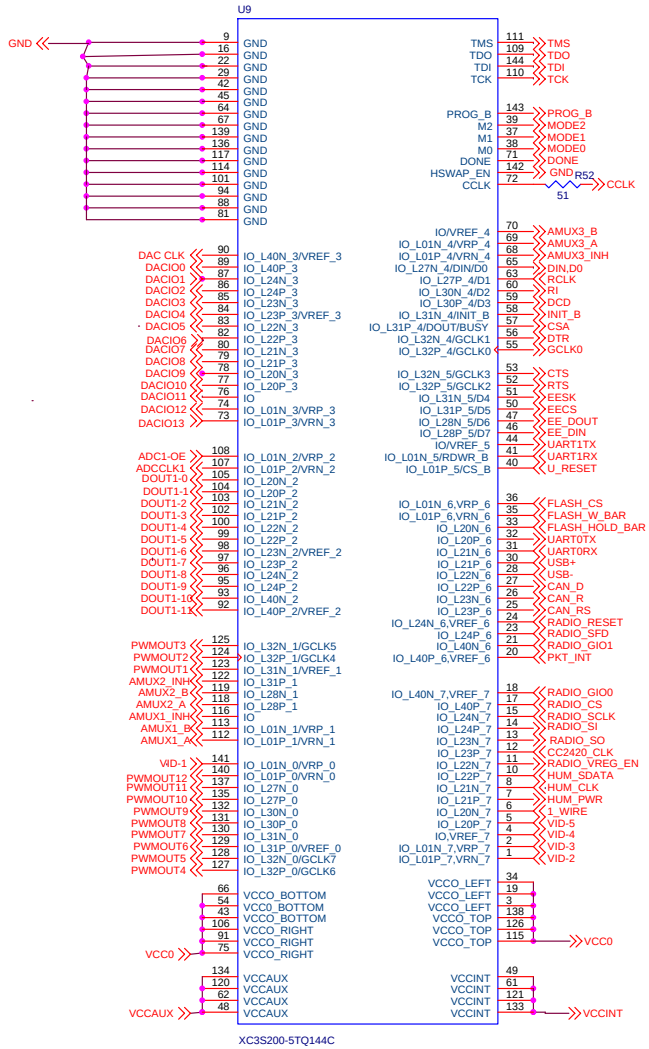
Spartan III Specification

- 200K System Gates
- 4320 Equivalent Logic Cells (1 Logic Cell = 4 Input Look-Up Table + 1 D Flop/Flop) with shift register capability
- 30K Distributed RAM Bits and 120K Block RAM Bits
- 12 Dedicated (18*18) Fast Multipliers
- JTAG Logic Compatible with IEEE 1149.1/1532 standard
- 4 DCM (Digital Clock Manager) Modules
- 8 Global Clock lines with abundant routing
- MicroBlaze processor, PCI and other cores
- 622 Mb/s data transfer rates per I/O
- 18 single-ended signal standards
- 8 differential I/O standards including LVDS, RSDS
- Signal swing ranging from 1.14V to 3.45V
- Double Data Rate (DDR) support
- Well supported by development tools for synthesis, mapping, placement and routing

FPGA Board Specification

- High Speed (15 Mega Samples/Sec) 12 bit Analog to Digital Converter -2 Numbers
- High Speed (150 Mega Samples/Sec) 14 bit Digital to Analog Converters
- Xilinx XC3S200TQ144 FPGA Device
- 2 Mb FPGA Configuration Flash Memory
- 8 Mbit Serial Flash Memory with 40 MHz SPI Interface
- JTAG Interface with PC for FPGA Configuration
- LDO Voltage Regulators 3.3V, 2.5V, 1.2V
- 78 User IOs
- 64K*16 external SRAM

FPGA Connections



National Semiconductor

April 2003

ADC12010
12-Bit, 10 MSPS, 160 mW A/D Converter with Internal Sample-and-Hold

General Description

The ADC12010 is a monolithic CMOS analog-to-digital converter capable of converting analog input signals into 12-bit digital words at 10 Megasamples per second (MSPS), minimum. This converter uses a differential, pipeline architecture with digital error correction and an on-chip sample-and-hold circuit to minimize die size and power consumption while providing excellent dynamic performance. Operating on a single 5V power supply, this device consumes just 160 mW at 10 MSPS, including the reference current. The Power Down feature reduces power consumption to 25 mW.

The differential inputs provide a full scale input swing equal to $2V_{REF}$ with the possibility of a single-ended input. Full use of the differential input is recommended for optimum performance. For ease of use, the buffered, high impedance, single-ended reference input is converted on-chip to a differential reference for use by the processing circuitry. Output data format is 12-bit offset binary.

This device is available in the 32-lead LQFP package and will operate over the industrial temperature range of –40˚C to +85˚C.

Features

- Internal sample-and-hold
- Outputs 2.4V to 5V compatible
- TTL/CMOS compatible input/outputs
- Power down mode
- On-chip reference buffer

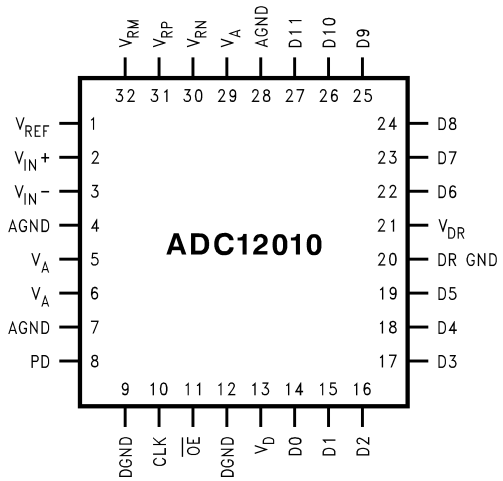
Key Specifications

■ Resolution	12 Bits
■ Conversion Rate	10 MSPS (min)
■ DNL	±0.3 LSB (typ)
■ INL	±0.5 LSB (typ)
■ SNR (f_{IN} = 10.1 MHz)	70 dB (typ)
■ ENOB (f_{IN} = 10.1 MHz)	11.3 bits (typ)
■ Data Latency	6 Clock Cycles
■ Supply Voltage	+5V ±5%
■ Power Consumption, 10 MHz	160 mW (typ)

Applications

- Image Processing Front End
- Instrumentation
- PC-Based Data Acquisition
- Fax Machines
- Wireless Local Loops/Cable Modems
- Waveform Digitizers
- DSP Front Ends

Connection Diagram



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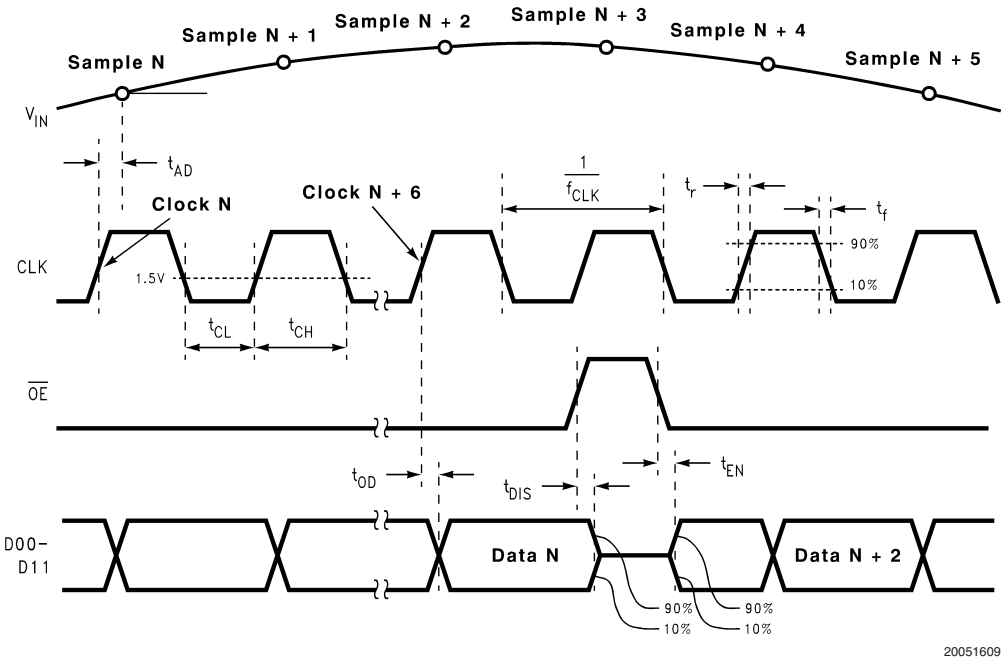
Timing Diagram



Output Timing

Transfer Characteristic

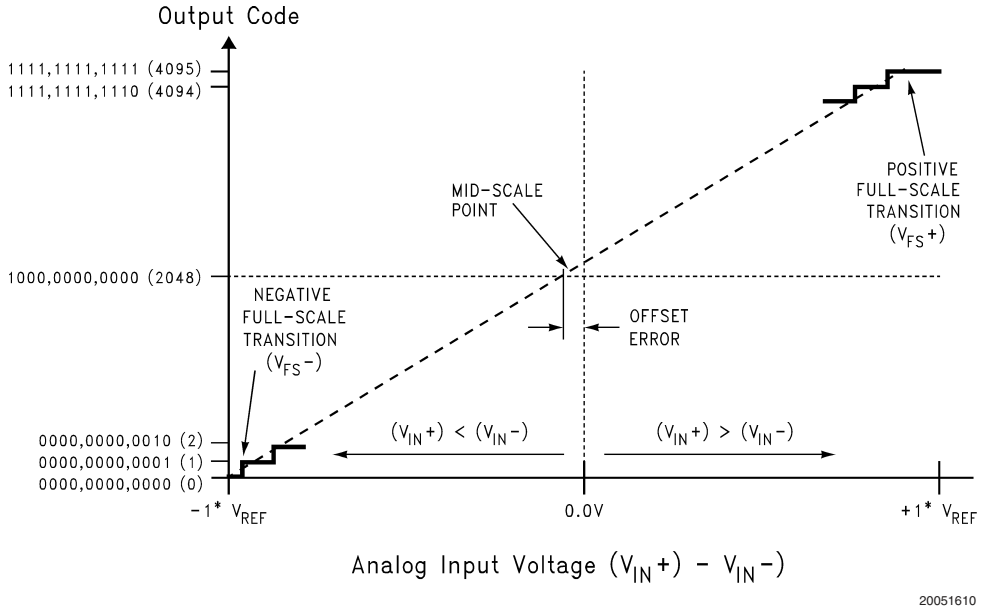


FIGURE 1. Transfer Characteristic

Functional Description

Operating on a single +5V supply, the ADC12010 uses a pipeline architecture with error correction circuitry to help ensure maximum performance. The differential analog input signal is digitized to 12 bits.

The reference input is buffered to ease the task of driving that pin.

The output word rate is the same as the clock frequency, which can be between 100 kSPS and 15 MSPS (typical). The analog input voltage is acquired at the rising edge of the clock and the digital data for a given sample is delayed by the pipeline for 6 clock cycles.

A logic high on the power down (PD) pin reduces the converter power consumption to 40 mW.

Applications Information

1.0 OPERATING CONDITIONS

We recommend that the following conditions be observed for operation of the ADC12010:

$4.75V \le V_A \le 5.25V$

$V_D = V_A$

$2.35V \le V_{DR} \le V_D$

$100\ kHz \le f_{CLK} \le 15\ MHz$

$1.0V \le V_{REF} \le 2.4V$

1.1 Analog Inputs

The ADC12010 has two analog signal inputs, $V_{IN}+$ and $V_{IN}-$. These two pins form a differential input pair. There is one reference input pin, V_{REF}.

1.2 Reference Pins

The ADC12010 is designed to operate with a 2.0V reference, but performs well with reference voltages in the range of 1.0V to 2.4V. Lower reference voltages will decrease the signal-to-noise ratio (SNR) of the ADC12010. Increasing the reference voltage (and the input signal swing) beyond 2.4V will degrade THD for a full-scale input. It is very important that all grounds associated with the reference voltage and the input signal make connection to the analog ground plane at a single point to minimize the effects of noise currents in the ground path.

The three Reference Bypass Pins (V_{RP}, V_{RM} and V_{RN}) are made available for bypass purposes. These pins should each be bypassed to ground with a 0.1 µF capacitor. Smaller capacitor values will allow faster recovery from the power down mode, but may result in degraded noise performance. DO NOT LOAD these pins.

1.3 Signal Inputs

The signal inputs are $V_{IN}+$ and $V_{IN}-$. The input signal, V_{IN}, is defined as

$$V_{IN} = (V_{IN}+) - (V_{IN}-)$$

Figure 2 shows the expected input signal range.

Note that the common mode input voltage range is 1V to 3V with a nominal value of $V_A/2$. The input signals should remain between ground and 4V.

The Peaks of the individual input signals ($V_{IN}+$ and $V_{IN}-$) should each never exceed the voltage described as

$$V_{IN}+,\ V_{IN}- = V_{REF} + V_{CM}$$

to maintain THD and SINAD performance.

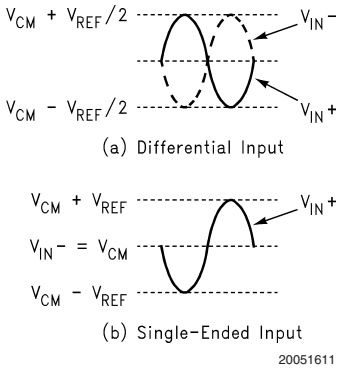


FIGURE 2. Expected Input Signal Range

The ADC12010 performs best with a differential input with each input centered around V_{CM}. The peak-to-peak voltage swing at both $V_{IN}+$ and $V_{IN}-$ each should not exceed the value of the reference voltage or the output data will be clipped. The two input signals should be exactly 180˚ out of phase from each other and of the same amplitude. For single frequency inputs, angular errors result in a reduction of the effective full scale input. For a complex waveform, however, angular errors will result in distortion.

For angular deviations of up to 10 degrees from these two signals being 180 out of phase, the full scale error in LSB can be described as approximately

$$E_{FS} = dev^{1.79}$$

Where dev is the angular difference, in degrees, between the two signals having a 180˚ relative phase relationship to each other (see *Figure 3*). Drive the analog inputs with a source impedance less than 100Ω.

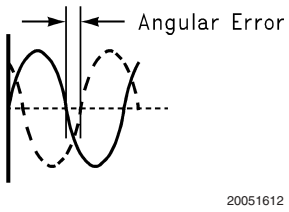


FIGURE 3. Angular Errors Between the Two Input Signals Will Reduce the Output Level

For differential operation, each analog input signal should have a peak-to-peak voltage equal to the input reference voltage, V_{REF}, and be centered around a common mode voltage, V_{CM}.

TABLE 1. Input to Output Relationship— Differential Input

$V_{IN}+$	$V_{IN}-$	Output
$V_{CM} - V_{REF}/2$	$V_{CM} + V_{REF}/2$	0000 0000 0000
$V_{CM} - V_{REF}/4$	$V_{CM} + V_{REF}/4$	0100 0000 0000
V_{CM}	V_{CM}	1000 0000 0000
$V_{CM} + V_{REF}/4$	$V_{CM} - V_{REF}/4$	1100 0000 0000
$V_{CM} + V_{REF}/2$	$V_{CM} - V_{REF}/2$	1111 1111 1111

Applications Information (Continued)

TABLE 2. Input to Output Relationship— Single-Ended Input

$V_{IN}+$	$V_{IN}-$	Output
$V_{CM} - V_{REF}$	V_{CM}	0000 0000 0000
$V_{CM} - V_{REF}/2$	V_{CM}	0100 0000 0000
V_{CM}	V_{CM}	1000 0000 0000
$V_{CM} + V_{REF}/2$	V_{CM}	1100 0000 0000
$V_{CM} + V_{REF}$	V_{CM}	1111 1111 1111

1.3.1 Single-Ended Operation

Single-ended performance is lower than with differential input signals. For this reason, single-ended operation is not recommended. However, if single ended-operation is required, one of the analog inputs should be connected to the d.c. common mode voltage of the driven input. The peak-to-peak differential input signal should be twice the reference voltage to maximize SNR and SINAD performance (*Figure 2*b).

For example, set V_{REF} to 1.0V, bias $V_{IN}-$ to 1.0V and drive $V_{IN}+$ with a signal range of 0V to 2.0V. Because very large input signal swings can degrade distortion performance, better performance with a single-ended input can be obtained by reducing the reference voltage when maintaining a full-range output. *Table 1* and *Table 2* indicate the input to output relationship of the ADC12010.

1.3.2 Driving the Analog Input

The $V_{IN}+$ and the $V_{IN}-$ inputs of the ADC12010 consist of an analog switch followed by a switched-capacitor amplifier. The capacitance seen at the analog input pins changes with the clock level, appearing as 8 pF when the clock is low, and 7 pF when the clock is high. Although this difference is small, a dynamic capacitance is more difficult to drive than is a fixed capacitance, so choose the driving amplifier carefully. The LMH6702 and the LMH6628 are good amplifiers for driving the ADC12010.

The internal switching action at the analog inputs causes energy to be output from the input pins. As the driving source tries to compensate for this, it adds noise to the signal. To prevent this, use 100Ω series resistors at each of the signal inputs with a 150 pF at each of the inputs, as can be seen in *Figure 5* and *Figure 6*. These components should be placed close to the ADC because the input pins of the ADC is the most sensitive part of the system and this is the last opportunity to filter the input. *Table 3* gives component values for *Figure 5* to convert individual input signals to a range of 2.5V ±2.0V at each of the input pins of the ADC12010.

TABLE 3. Resistor Values for Circuit of *Figure 5*

SIGNAL RANGE	R1	R2	R3	R4	R5, R6
0 - 0.5V	392Ω	1540Ω	102Ω	115Ω	1000Ω
0 - 1.0V	634Ω	1470Ω	2490Ω	1050Ω	499Ω
±0.25V	499Ω	499Ω	499Ω	499Ω	1000Ω
±0.5V	100Ω	200Ω	100Ω	200Ω	499Ω

1.3.3 Input Common Mode Voltage

The input common mode voltage, V_{CM}, should be in the range of 0.5V to 4.0V and be of a value such that the peak excursions of the analog signal does not go more negative than ground or more positive than 0.5 Volts below the V_A supply voltage. The nominal V_{CM} should generally be equal to $V_{REF}/2$, but V_{RM} can be used as a V_{CM} source as long as V_{CM} need not supply more than 10 µA of current.

2.0 DIGITAL INPUTS

The digital TTL/CMOS compatible inputs consist of CLK, $\overline{OE}$ and PD.

2.1 CLK

The **CLK** signal controls the timing of the sampling process. Drive the clock input with a stable, low jitter clock signal in the range of 100 kHz to 15 MHz with rise and fall times of less than 3ns. The trace carrying the clock signal should be as short as possible and should not cross any other signal line, analog or digital, not even at 90˚.

If the **CLK** is interrupted, or its frequency too low, the charge on internal capacitors can dissipate to the point where the accuracy of the output data will degrade. This is what limits the lowest sample rate to 100 kSPS.

The duty cycle of the clock signal can affect the performance of the A/D Converter. Because achieving a precise duty cycle is difficult, the ADC12010 is designed to maintain performance over a range of duty cycles. While it is specified and performance is guaranteed with a 50% clock duty cycle, performance is typically maintained over a clock duty cycle range of 20% to 80%.

The clock line should be series terminated at the source end in the characteristic impedance of that line if the clock line is longer than

$$\frac{t_r}{6 \times t_{PR}}$$

where t_r is the rise time of the clock signal and t_{PR} is the propagation rate along the line. For a Board of FR-4 material, t_{PR} is typically about 150 ps/inch, or 60 ps/cm. This resistor should be as close to the source as possible.

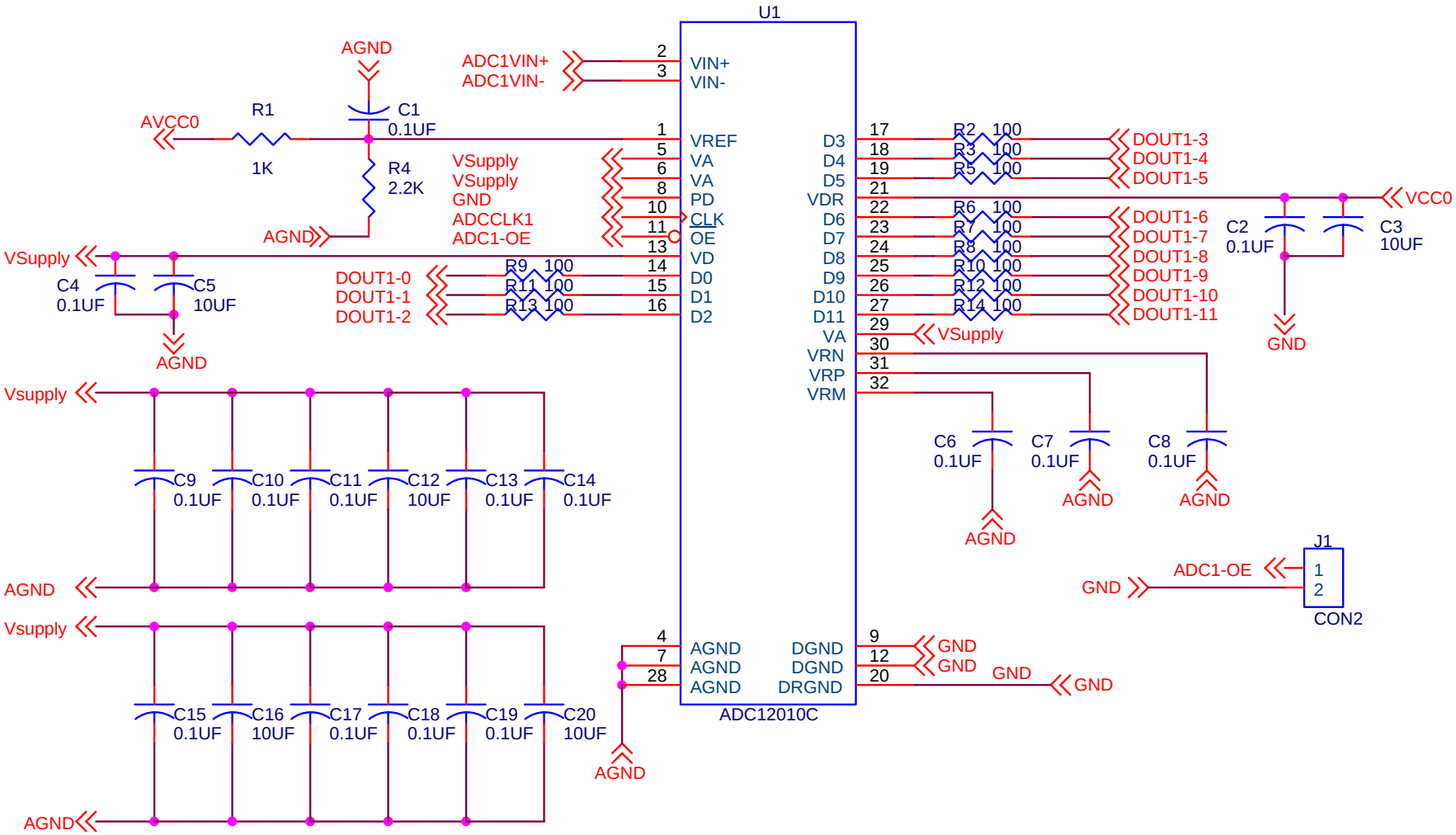
It might also be necessary to AC terminate the ADC end of the clock line with a series RC to ground such that the resistor value equals the characteristic impedance of the clock line and the capacitor value is

$$C \geq \frac{4 \times t_{PR} \times L}{Z_0}$$

where t_{PR} is again the propagation rate down the clock line, L is the length of the line in inches and Z_O is the characteristic impedance of the clock line. A.C. termination should be near the ADC clock pin but beyond that pin as seen from the clock source.

Take care to maintain a constant clock line impedance throughout the length of the line. Refer to Application Note AN-905 or AN-1113 for information on setting and determining characteristic impedance.

ADC Interface



National Semiconductor

DAC14135
14-bit, 135MSPS D/A Converter

General Description

The DAC14135 is a monolithic 14-bit, 135MSPS digital-to-analog converter. The device has been optimized for use in cellular base stations and other applications where high resolution, high sampling rate, wide dynamic range, and compact size are required. The DAC14135 has many integrated features including a proprietary segmented DAC core, differential current outputs, a band-gap voltage reference, and TTL/CMOS compatible inputs. The converter features an 85dBc spurious free dynamic range (SFDR) at low frequencies and a 70dBc SFDR with 20MHz output signals. The 48-pin TSSOP package provides an extremely small footprint for applications where space is a critical consideration. The DAC14135 operates from a single +5V power supply. The digital power supply can also operate from +3.3V for lower power consumption and compatibility with +3.3V data inputs. The DAC14135 is fabricated in a 0.5µm CMOS process and is specified over the industrial temperature range of -40°C to +85°C. National Semiconductor thoroughly tests each part to verify full compliance with the guaranteed specifications.

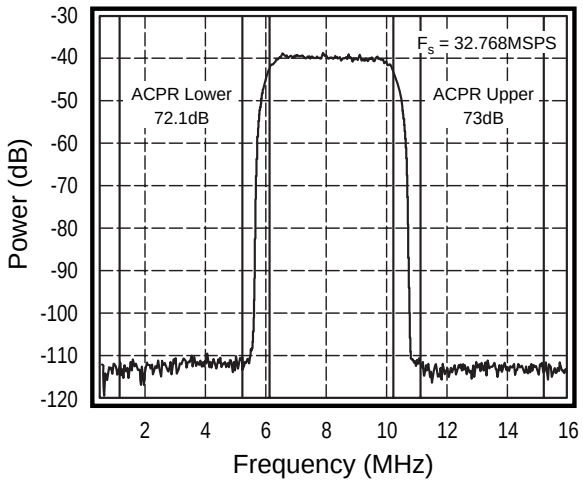
Features

- 135 MSPS
- Wide dynamic range
  - SFDR @ 1MHz f_{out}: 85dBc
  - SFDR @ 5MHz f_{out}: 79dBc
  - SFDR @ 20MHz f_{out}: 70dBc
- Differential Current Outputs
- Low power consumption: 185mW
- Very small package: 48-pin TSSOP
- TTL/CMOS (+3.3V or +5V) inputs

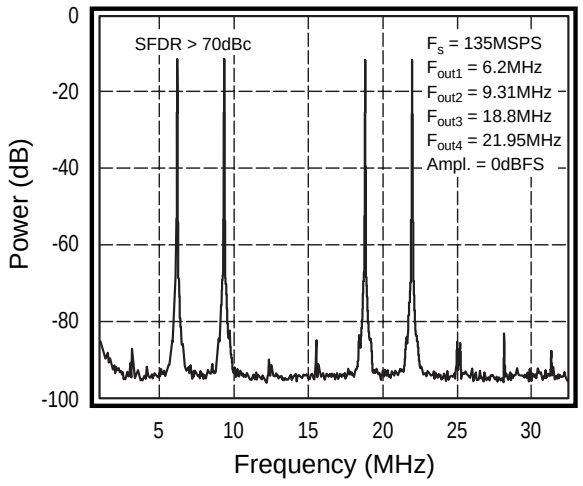
Applications

- Cellular Basestations:
  - GSM, WCDMA, DAMPS, etc.
- Multi-carrier Basestations
- Multi-standard Basestations
- Direct digital synthesis (DDS)
- ADSL modems
- HFC modems

W-CDMA ACPR



Four-Tone SFDR



DAC14135 Electrical Characteristics

(sample rate = 135MSPS, T_{min} = -40°C, T_{max} = +85°C, AV_{DD} = +5V, DV_{DD} = +5V, CV_{DD} = +5V, full scale current = 20mA, differential 50Ω doubly terminated output, unless specified otherwise)

PARAMETERS	CONDITIONS	TEMP	RATINGS			UNITS	NOTES
			MIN	TYP	MAX		
POWER REQUIREMENTS							
analog supply current		+25°C		28	35	mA	1
digital supply current	135MSPS, DV_{DD} = +5V	+25°C		9	15	mA	1
digital supply current	100MSPS, DV_{DD} = +3.3V	+25°C		4.5		mA	
power consumption	135MSPS, DV_{DD} = +5V	+25°C		185		mW	
power consumption	100MSPS, DV_{DD} = +3.3V	+25°C		150		mW	
AV_{DD} power supply rejection ratio	at mid-scale	+25°C		1.0		%FS/V	

Min/max ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

Notes

1) These parameters are 100% tested at 25°C.
2) These parameters are sample tested at -40°C, +25°C and +85°C.
3) Defined as the net area of undesired output transients in pV-s at a major transition.

Absolute Maximum Ratings

positive supply voltage (V_{DD})	-0.5V to +6V
analog output voltage range	-0.7V to +V_{DD}
digital input voltage range	-0.5V to +V_{DD}
output short circuit duration	infinite
junction temperature	175°C
storage temperature range	-65°C to 150°C
lead solder duration (+300°C)	10sec

Note: Absolute maximum ratings are limiting values, to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied. Exposure to maximum ratings for extended periods may affect device reliability.

Recommended Operating Conditions

positive analog supply voltage	+5V ±5%
positive digital supply voltage	+3.3V or +5V ±5%
positive clock supply voltage	+5V ±5%
operating temperature range	-40°C to +85°C

Package Thermal Resistance

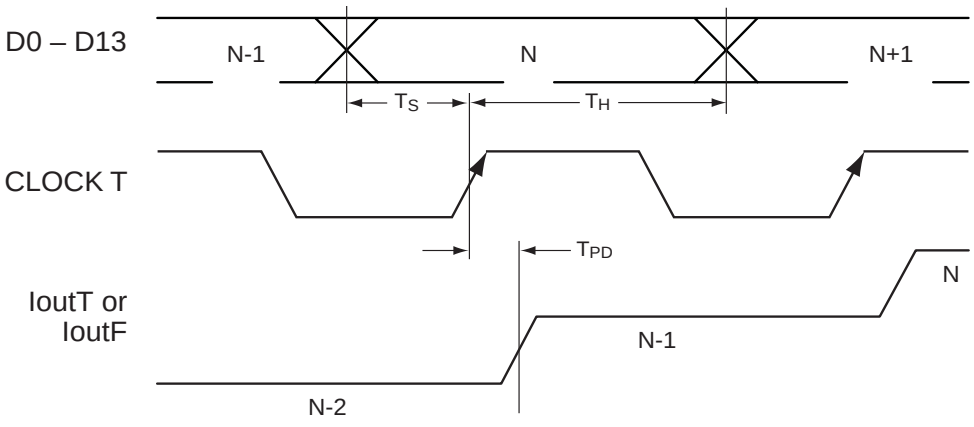
Package	θ_{JA}	θ_{JC}
48-pin TSSOP	56°C/W	16°C/W

Package Transistor Count

Transistor count	8,600

Ordering Information

Model	Temperature Range	Description
DAC14135MT	-40°C to +85°C	48-pin TSSOP (industrial temperature range)
DAC14135MTX	-40°C to +85°C	48-pin TSSOP (TNR 1000 pc reel)
DAC14135PCASM		Fully loaded evaluation board with DAC14135 … ready for test.



NOTE: 1 clock cycle latency

DAC14135 Timing Diagram

ridden by an external bandgap reference voltage. The reference ground (REFLO) should always be tied to analog ground. The REFIO pin should be bypassed to REFLO using a 0.1µF capacitor. For reduced noise, an external compensation capacitor (0.1µF) should also be used to bypass the internal reference loop from pin REFCOMP to AGND. Figure 3 shows the internal voltage reference loop functional schematic.

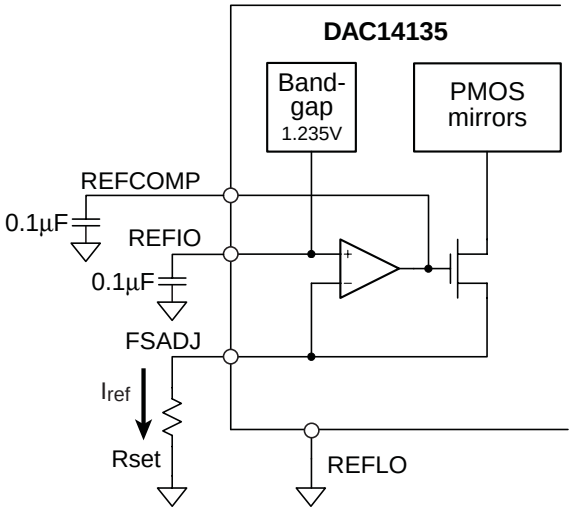


Figure 3: Internal Voltage Loop Functional Schematic

A reference current source (Iref) from pin FSADJ to ground may be used to set the full scale output current (Ifs) of the DAC14135. The full scale current is given by,

$$Ifs = 42.67 \times Iref$$

Alternatively, a resistor (Rset) from FSADJ to AGND may be used to set the full scale output current of the DAC.

$$Ifs\ (mA) = 42.67 \times REFIO/Rset$$

The voltage at REFIO is nominally set by the internal bandgap at 1.235V. For a full scale output current of 20mA, the value of Rset is 2.635kΩ.

Analog Outputs

The differential analog outputs, I_{OUTT} and I_{OUTF}, are high impedance current source outputs. These outputs, if terminated into 50Ω at 20mA full scale current, will generate a differential voltage output at $2V_{pp}$. The output compliance of each of the current outputs of the DAC14135 is -0.5V to +1.25V. The differential outputs can be converted to a single-ended output using an RF center-tapped transformer or a differential to single-ended amplifier. The I_{OUTT} and I_{OUTF} traces on the printed circuit board should be short and matched with adequate analog grounding nearby. One example of an AC coupled differential to single-ended topology is shown in Figure 4.

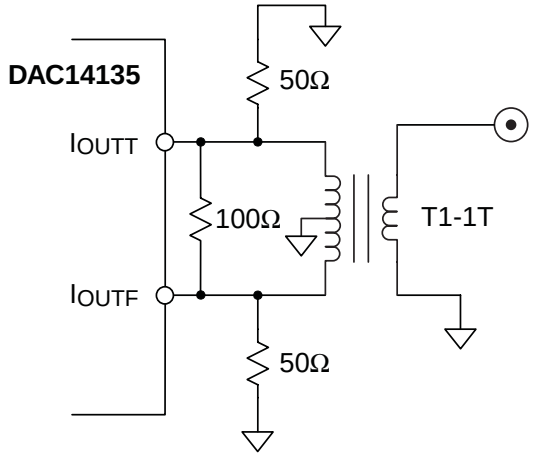
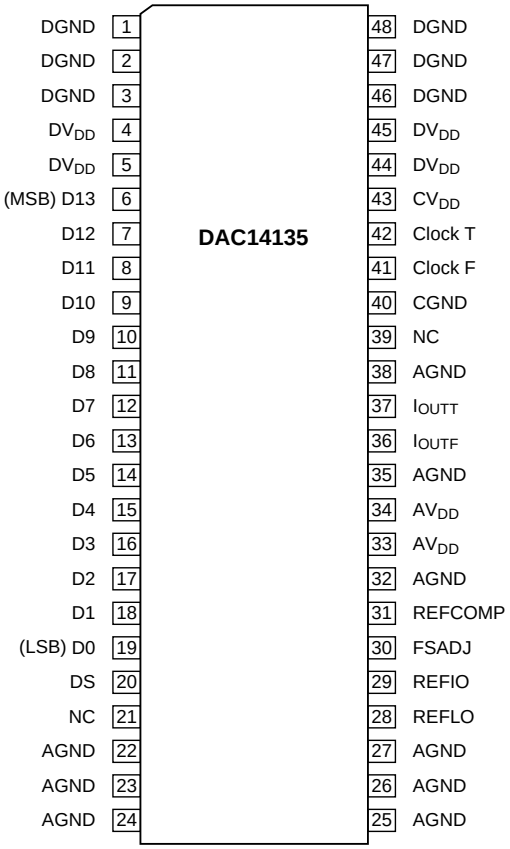


Figure 4: AC Coupled Differential to Single-ended Topology

DAC14135 Grounding Information

In the DAC14135, all the grounds AGND, REFLO, DGND and CGND are shorted together inside the package. The purpose of having separate grounds on the printed circuit board is to prevent digital data currents from returning through the analog or reference grounds, and corrupting the analog outputs. Refer to the evaluation board layout.

DAC14135 Pin Definitions



I_{OUTT}
I_{OUTF} (Pins 37, 36) Differential current outputs. Output compliance range is -0.5V to +1.25V.

Clock T
Clock F (Pins 42, 41) Differential clock inputs. Bypass CLOCKF with a 0.1µF capacitor to CGND if using single-ended clock on CLOCKT. Both inputs have internal self-bias at approximately 1.5V.

D0 - D13 (Pins 6 - 19) Digital data inputs. CMOS (+3.3V and +5V) and TTL (with +3.3V DV_{DD}) compatible. **D13** is the MSB.

DS (Pin 20) Data scramble input. If not used, either connect to ground or leave unconnected.

AGND (Pins 22 - 27, 32, 35, 38) Analog ground.

DGND (Pins 1 - 3, 46 - 48) Digital ground.

CGND (Pin 40) Clock ground. Connect to AGND.

AV_{DD} (Pins 33, 34) +5V power supply for the analog section. Bypass to analog ground with a 0.1µF capacitor.

DV_{DD} (Pins 4, 5, 44, 45) +5V or +3.3V power supply for the digital section. Bypass to digital ground with a 0.1µF capacitor.

CV_{DD} (Pin 43) Internal clock buffer power supply. Bypass to clock ground with 0.1µF capacitor.

REFIO (Pin 29) Internal voltage reference output (Vref) or voltage reference input. Nominally +1.235V. Can be overdriven with an external reference. Bypass to AGND with 0.1µF capacitor.

REFLO (Pin 28) Ground for reference circuitry. Should be connected to AGND.

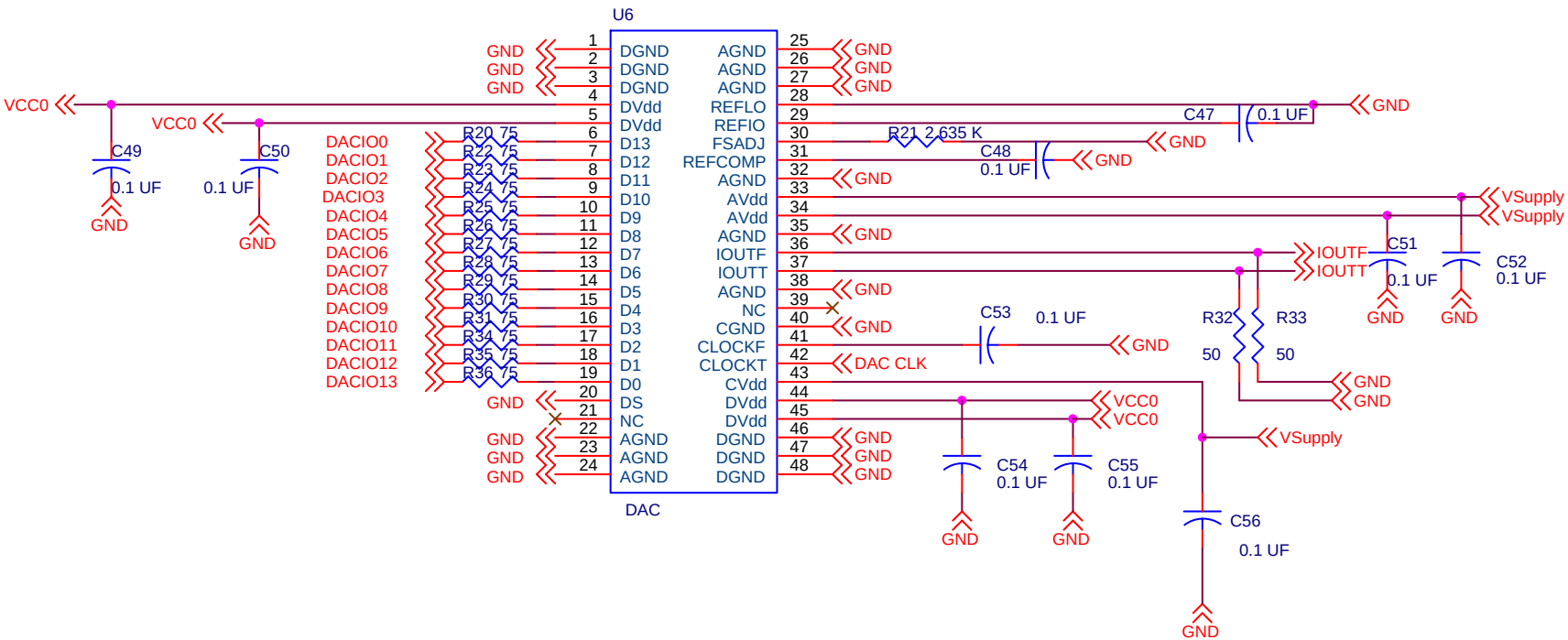
FSADJ (Pin 30) Full scale current adjust. Must be connected with an external resistor (Rset) or an external current source (Iref) to analog ground.

Ifullscale (mA) = 42.67 x Iref = 42.67 x REFIO/Rset

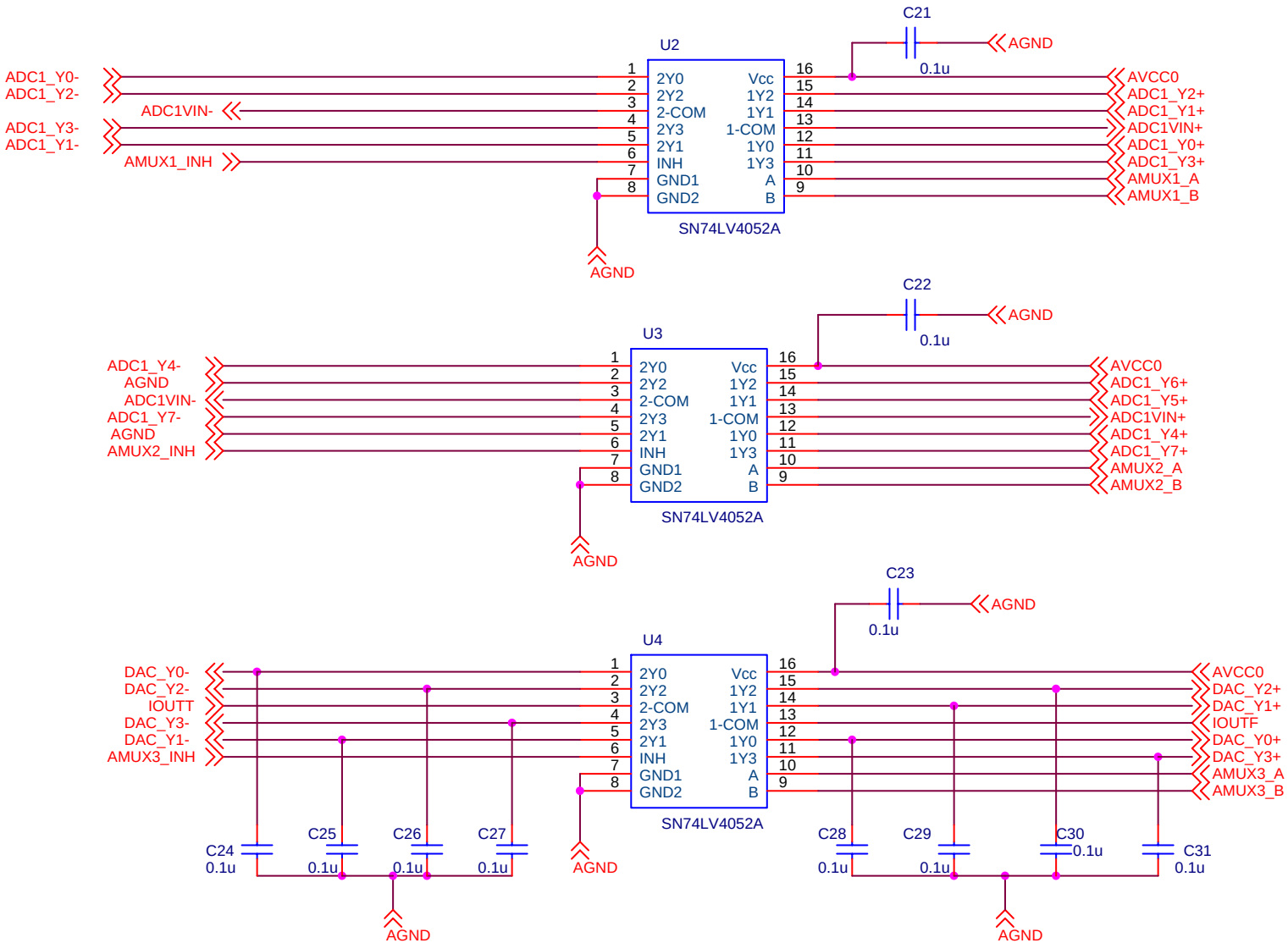
REFCOMP (Pin 31) Compensation pin for the internal reference circuitry. Bypass to analog ground with a 0.1µF capacitor.

NC (Pins 21, 39) No connect.

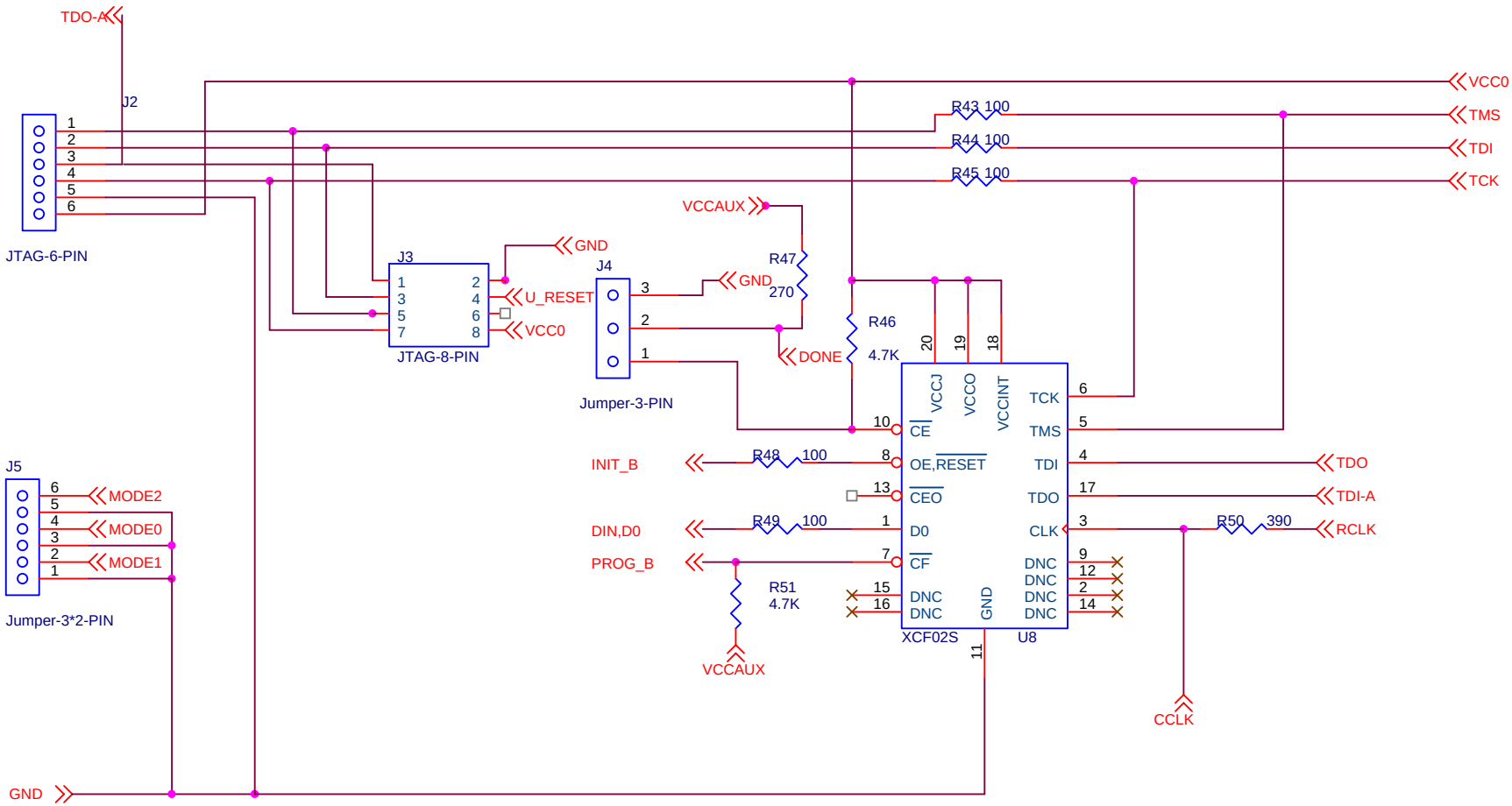
DAC Interface



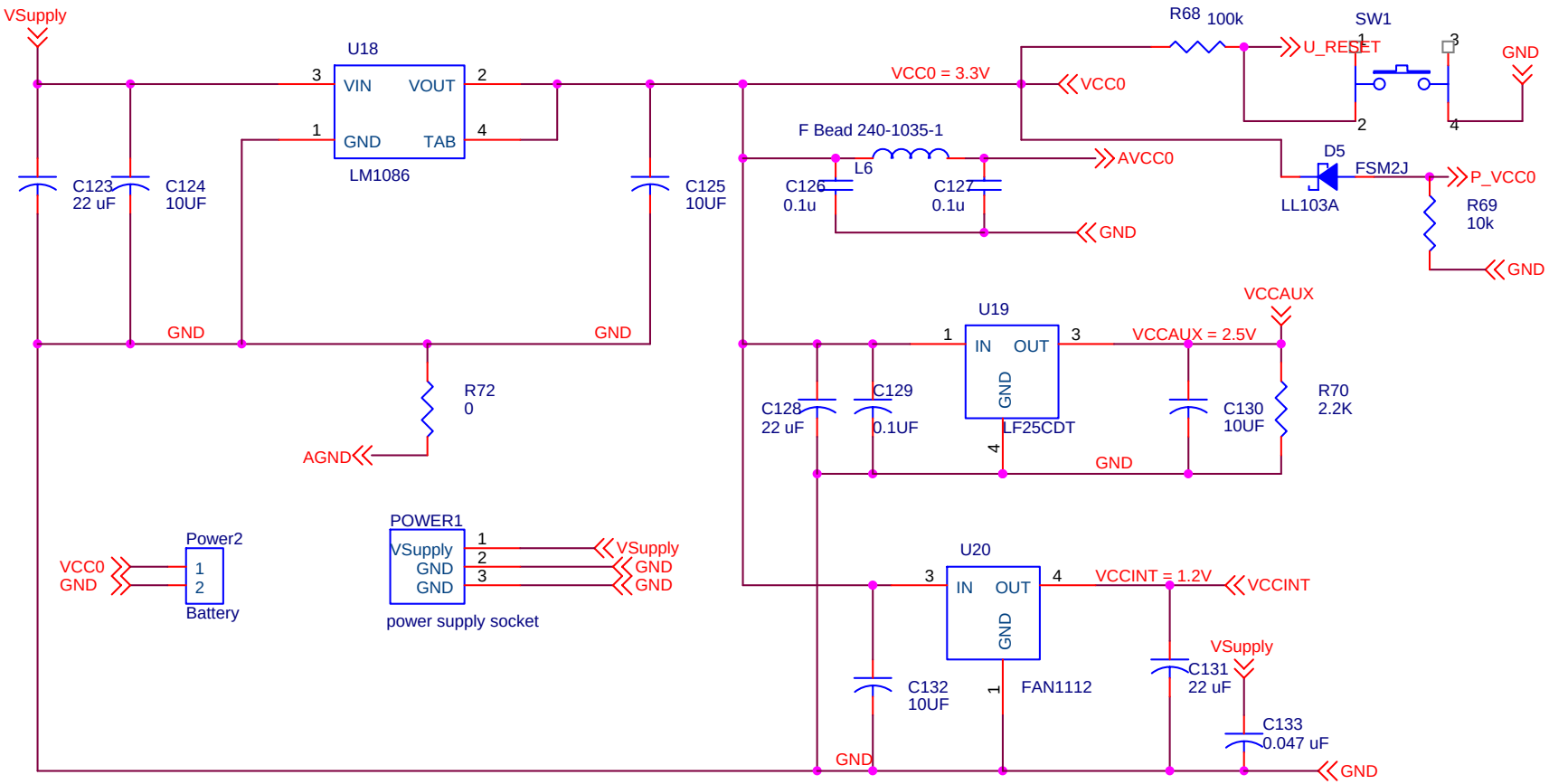
Analog Multiplexer



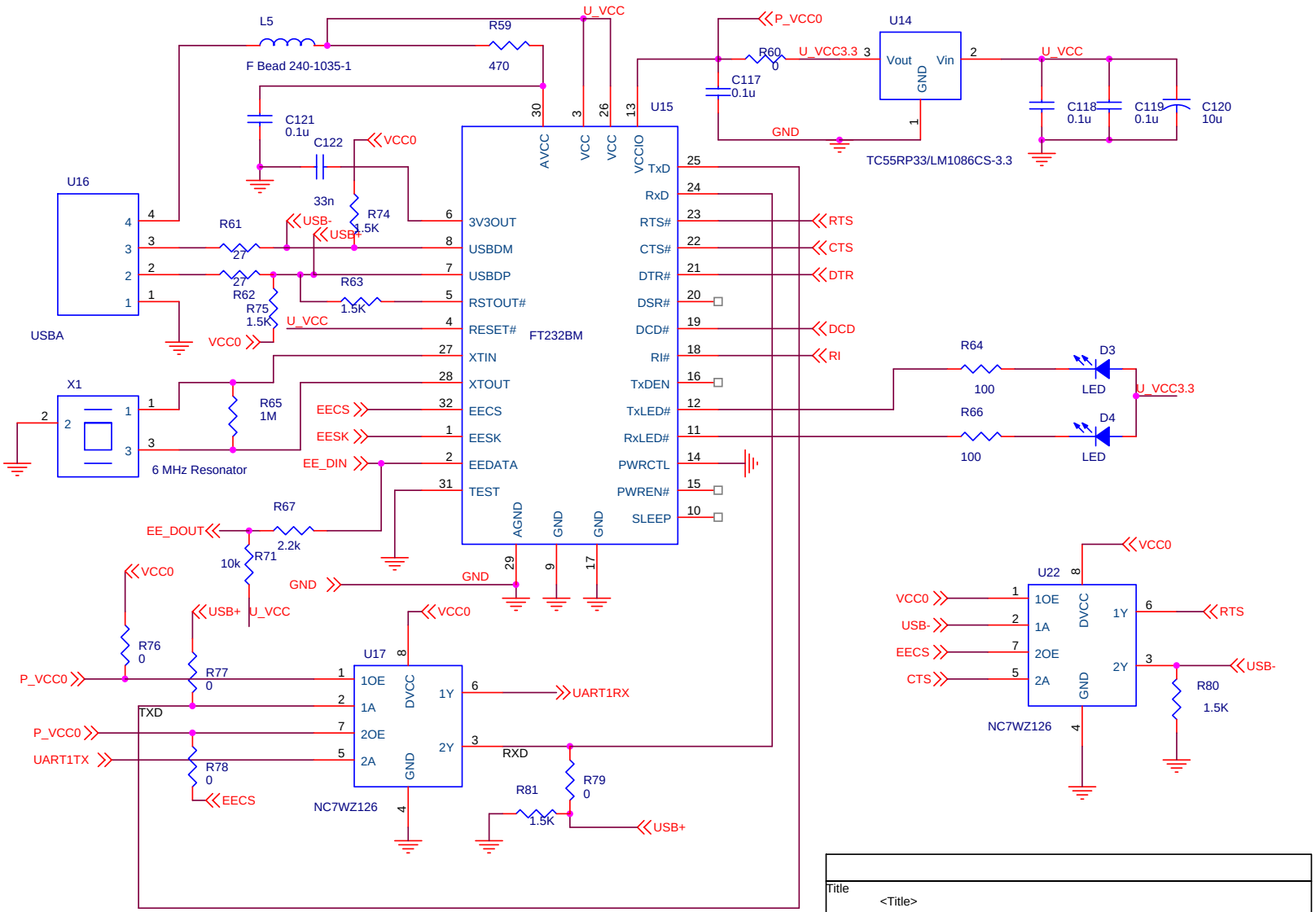
JTAG and PROM Interface



Voltage Regulators

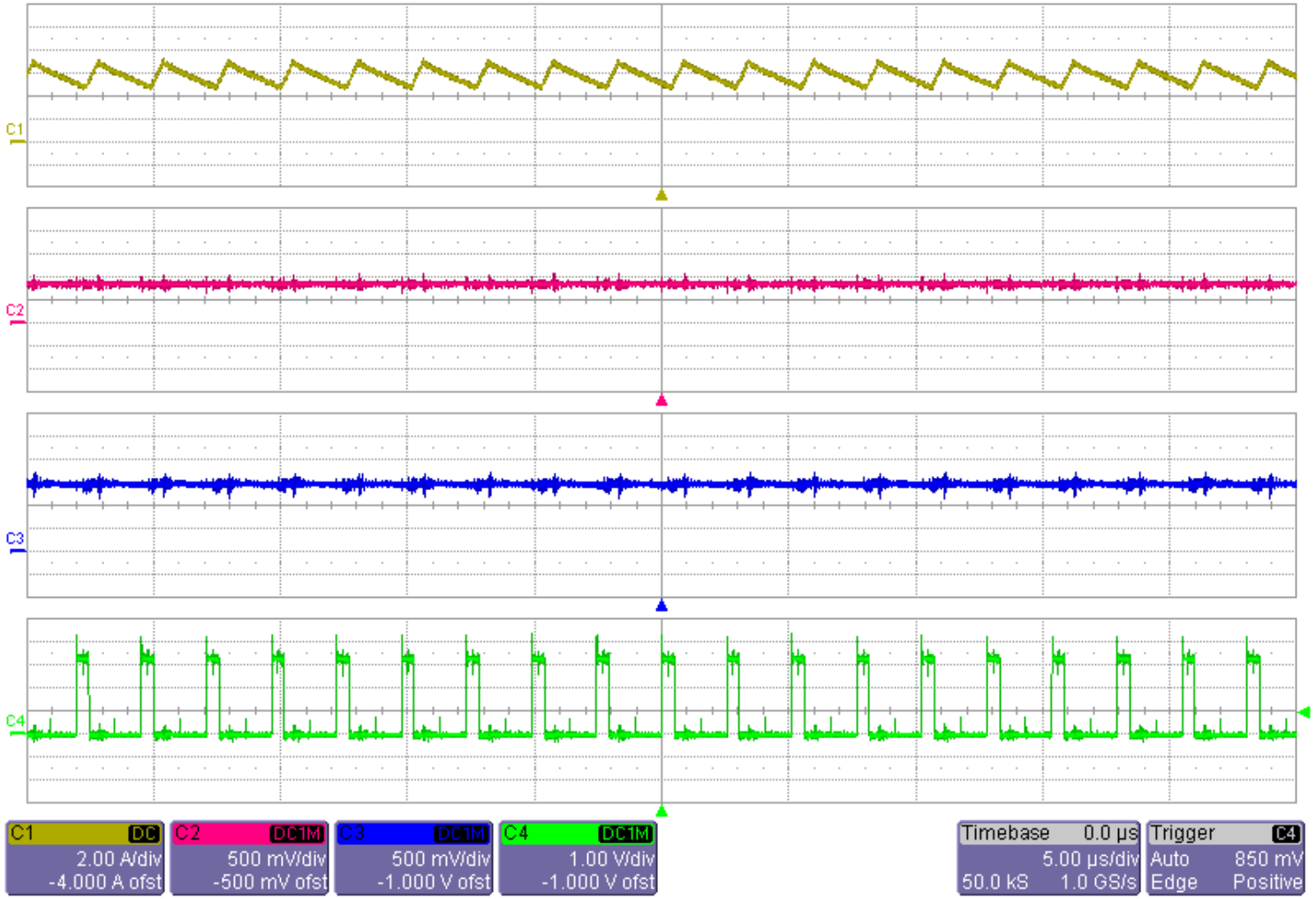


USB Interface

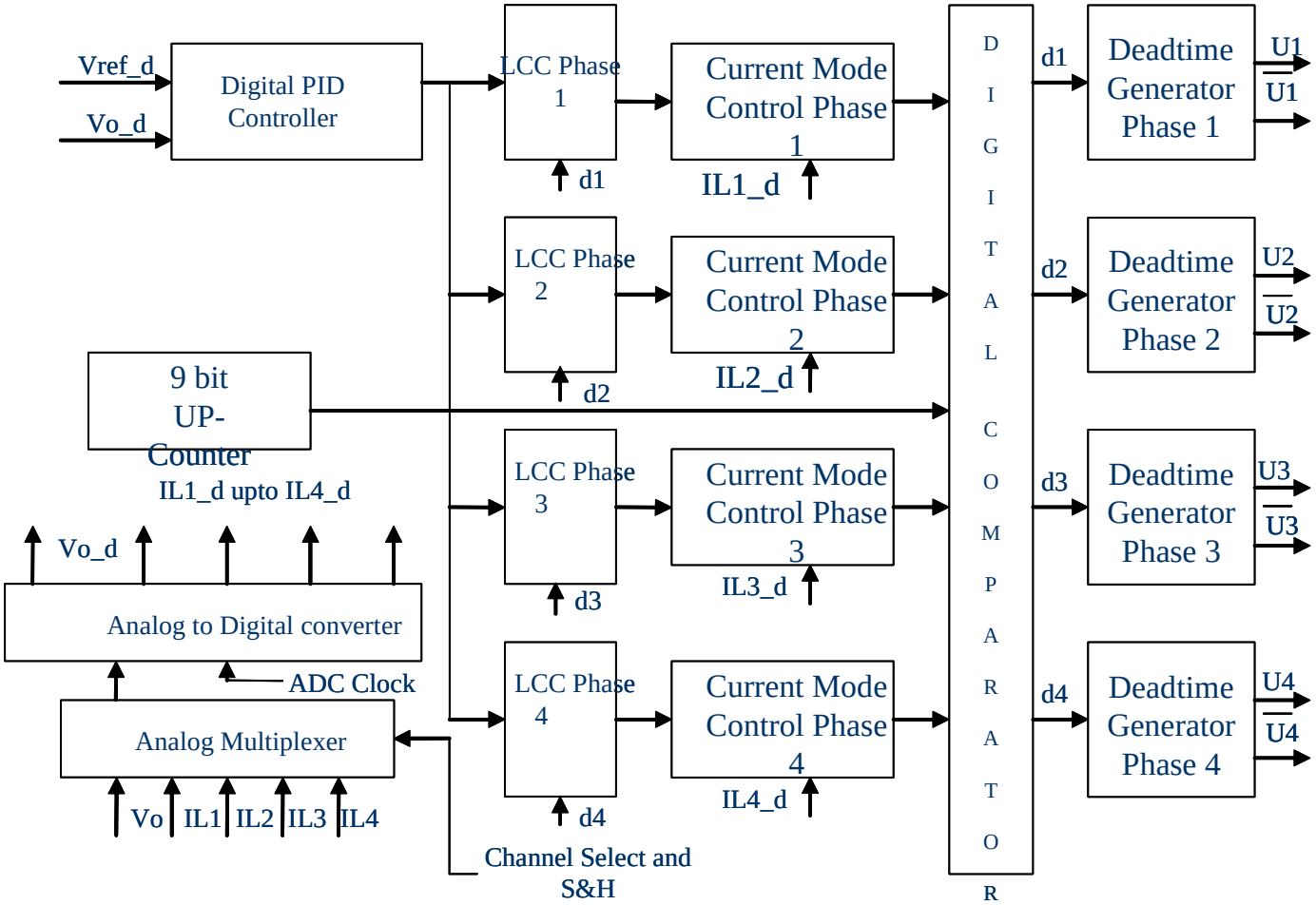


Title	<Title>

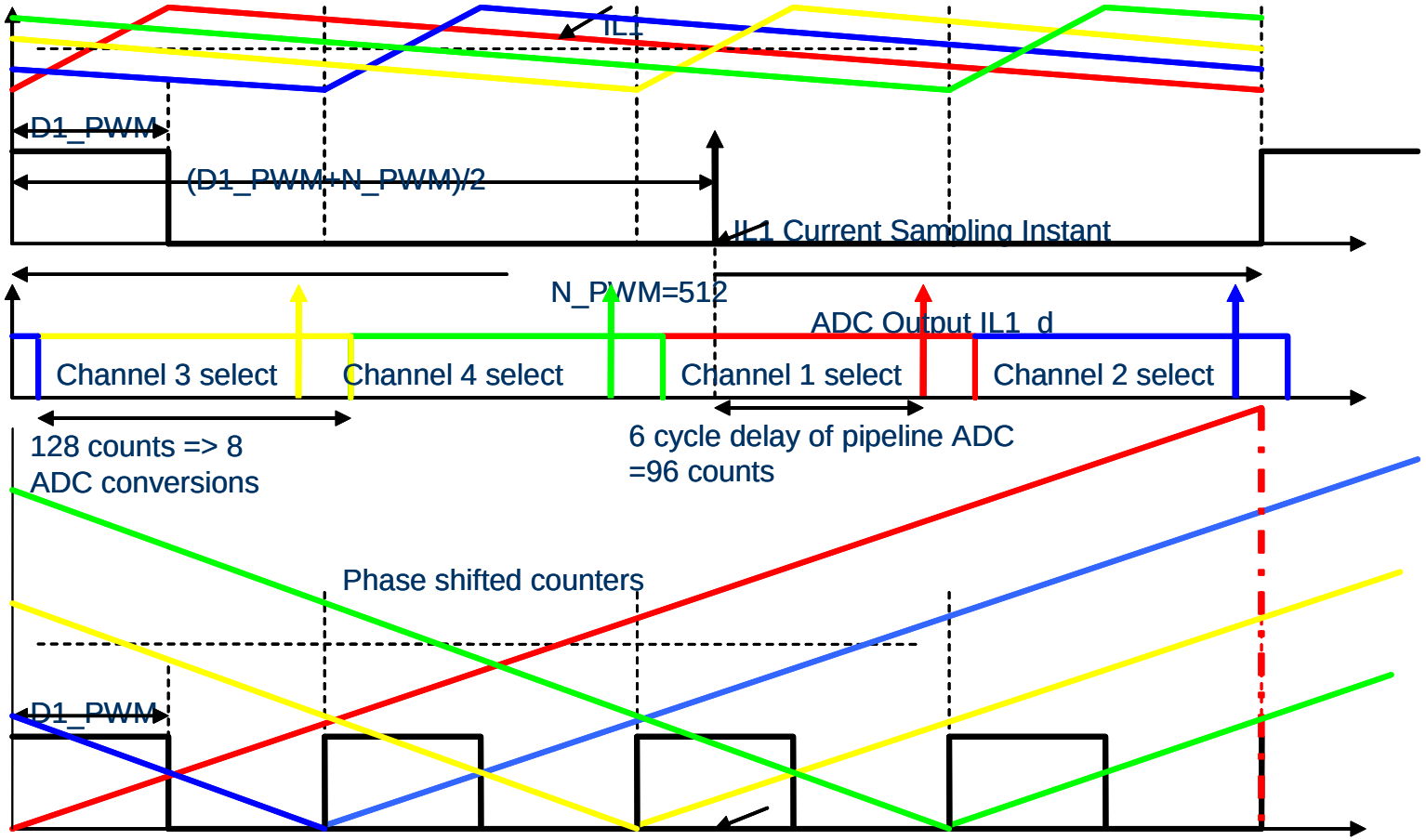
Digital Current-Mode Control: FPGA Implementation



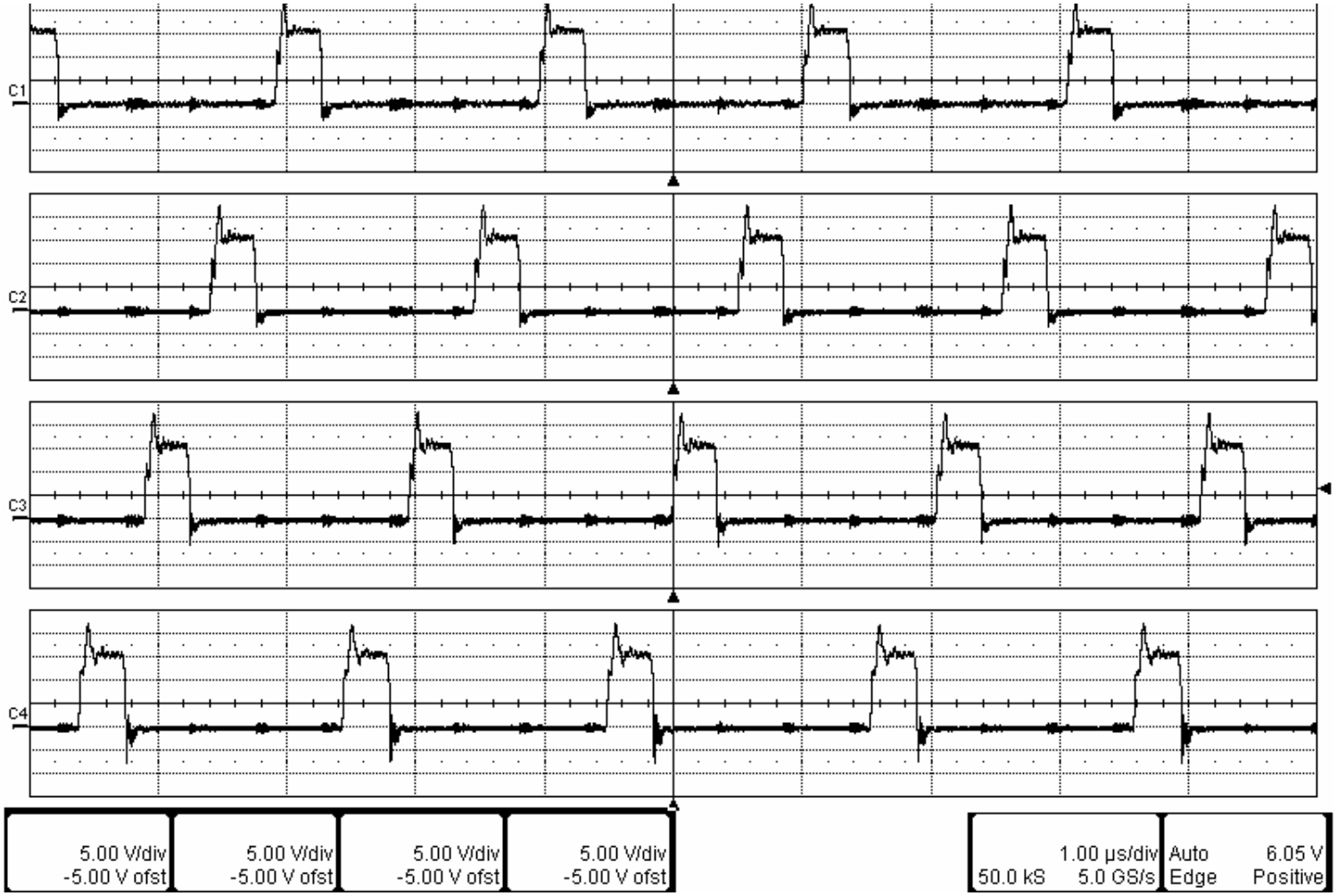
Multiphase Converter Current-Mode Control : Block Diagram



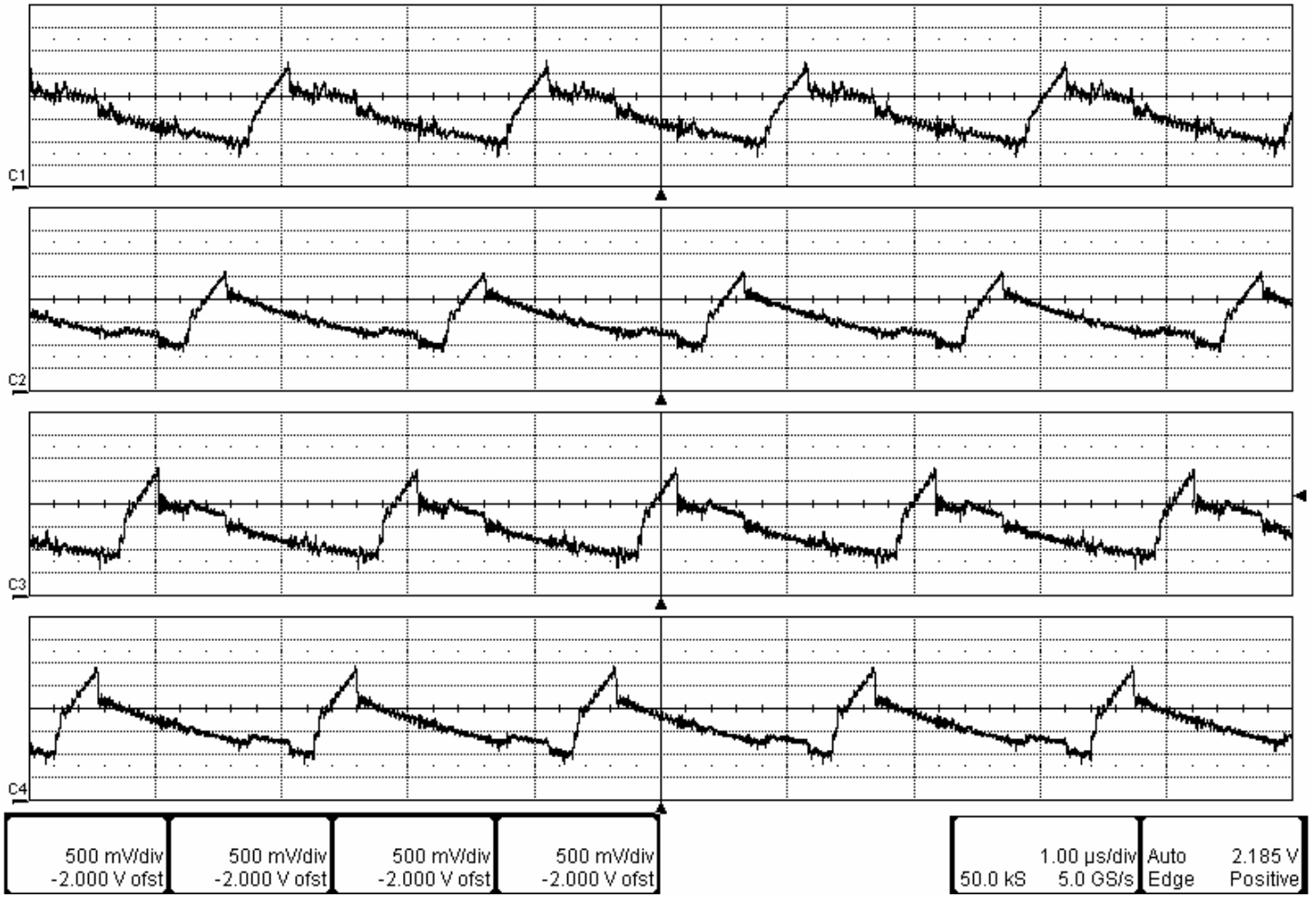
Sampling Strategy in 4 Phase Average Current-Mode Control



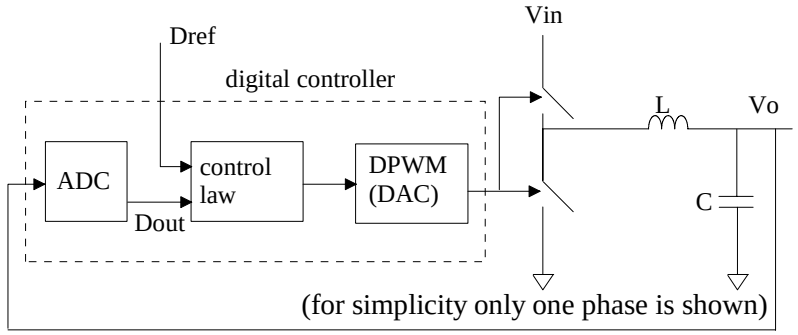
Gate Pulses of 4 Phase Buck Converter



Inductor Currents of 4 Phase Buck Converter



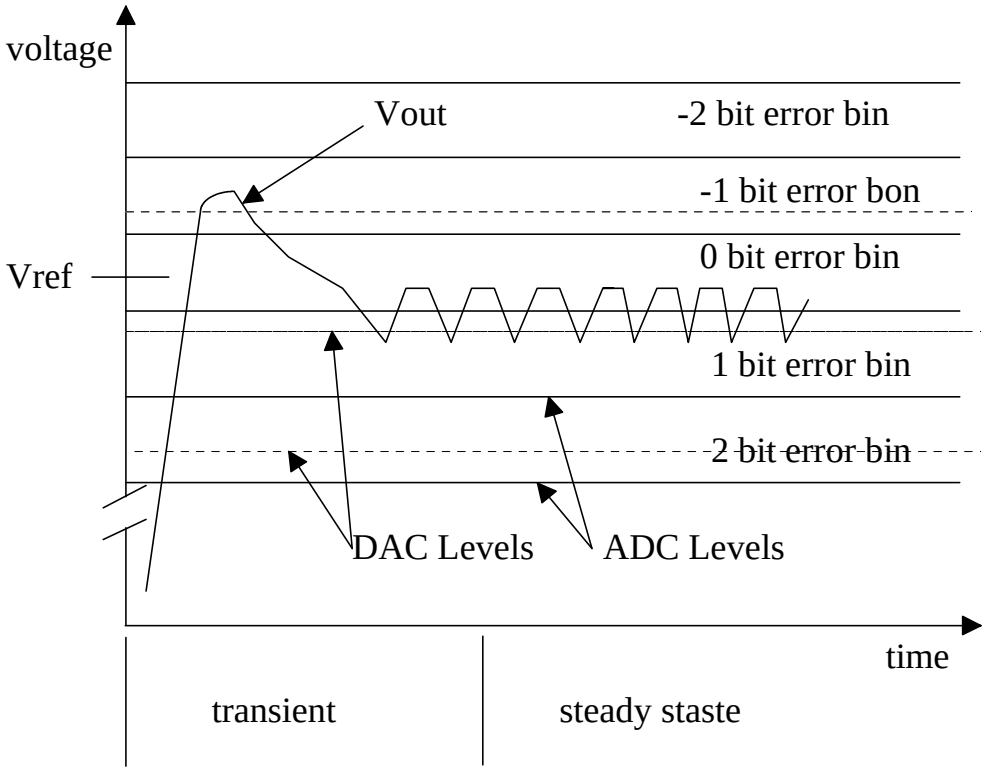
VRM : Elimination of Limit Cycles in Digitally Controlled VRM



Limit Cycles

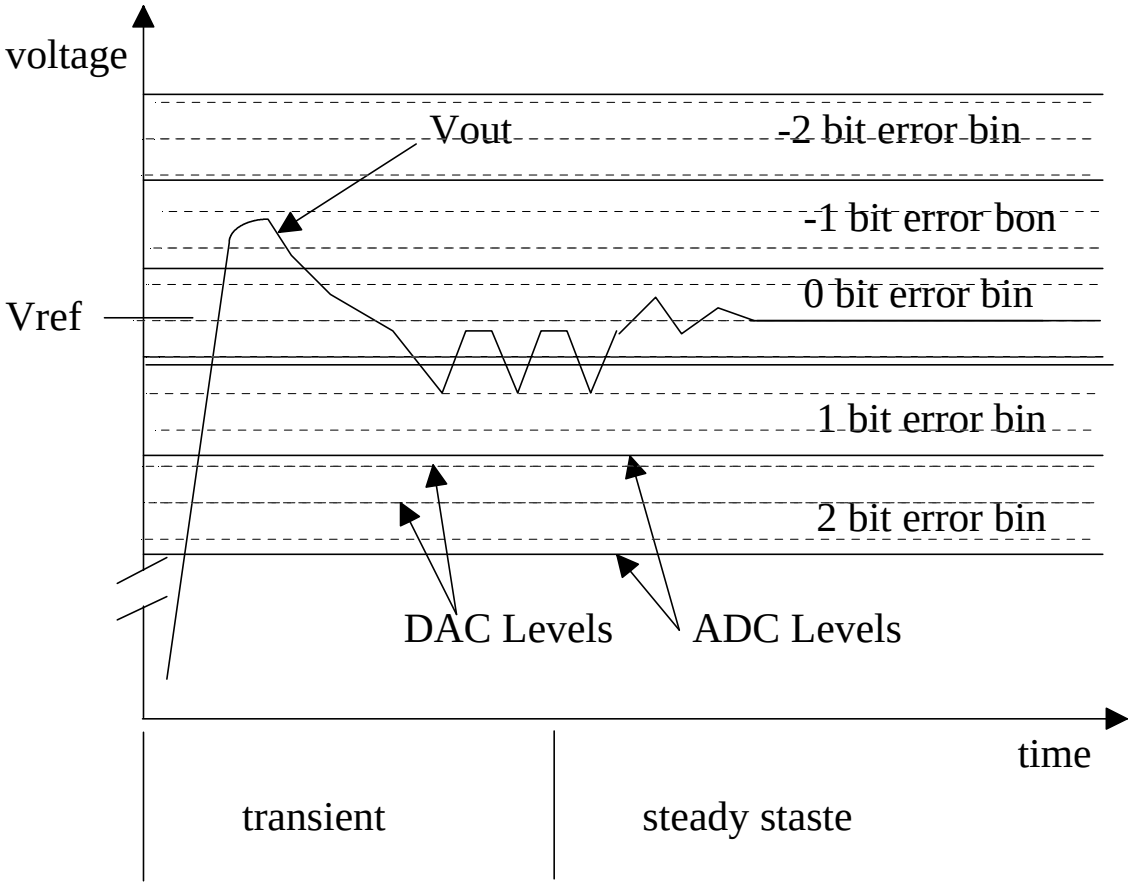
Oscillations of V_o at frequencies lower than f_{sw} - Cause EMI problem

Reason
Presence of quantizers such as ADC and DPWM in the controller



Limit Cycle Oscillations of V_o

VRM : Elimination of Limit Cycles in Digitally Controlled VRM



No limit cycle condition #1
resolution(DPWM) > resolution(ADC)

No limit cycle condition #2
$0 < K_I < 1$, K_I: integral gain

No limit cycle condition #3
$1 + N(A)L(j\omega) \neq 0$ (Nyquist Criterion)

Solution
Increase DPWM resolution

Digital Current Mode Control : Operating Parameters

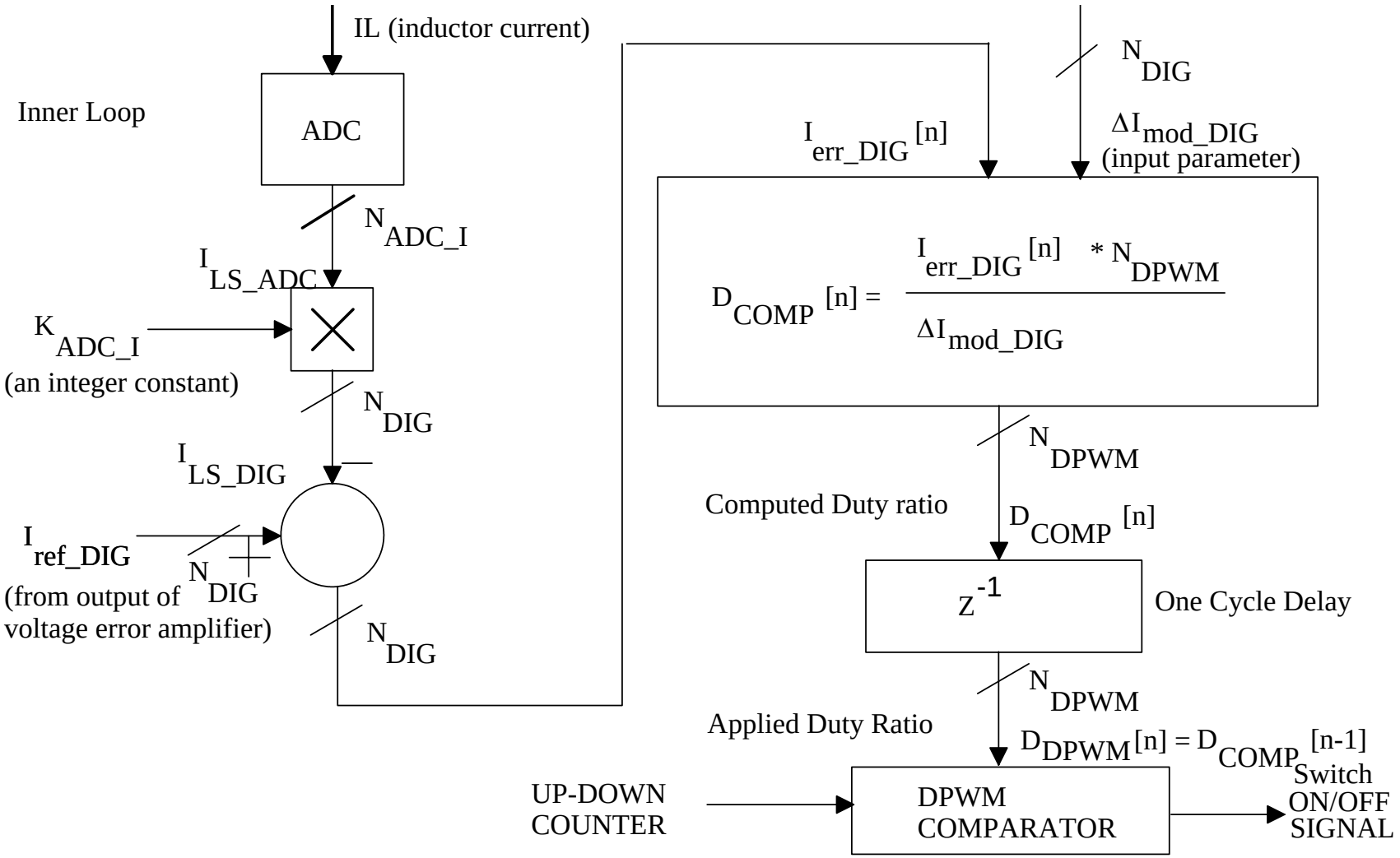
BUCK CONVERTER PARAMETERS

V_g	L	C	T_S	R	$M_c(\min)$	I_{ref}
$12\,V$	$12\,\mu H$	$100\,\mu F$	$10\,\mu Sec$	$0.2\,\Omega$	$2\,A/\mu Sec$	$10.25\,A$

SPECIFICATION OF DIGITAL CONTROLLER

N_{DIG}	T_{clk}	$N_{ADC}(hardware)$	N_{ADC_I}	N_{DPWM}	N_{ADC_V}	I_{LM}	V_{OM}
2^{16}	$50\,nSec$	2^{10}	2^4	200	2^5	$15\,A$	$3.3\,V$

Digital Current-Mode Control: Quantization Analysis of Algorithm



Digital Current-Mode Control: Parameters for Graphical Analysis

PARAMETERS FOR ANALYSIS OF LIMIT CYCLE OSCILLATIONS

K_{ADC_I}	$I_{ref\ DIG}$	$\Delta I_{\mathrm{mod}\ DIG}$	ΔI_{con_DIG}	$\Delta I_{adc\ DIG}$
512	5597	54	163	512

Definitions:

$$K_{ADC\_I} = floor(\frac{N_{DIG}}{P} * \frac{1}{N_{ADC\_I}})$$

$$\Delta I_{\mathrm{mod}\_DIG} = floor(\frac{M_c T_S}{I_{LM}} \frac{1}{N_{DPWM}} \frac{N_{DIG}}{P})$$

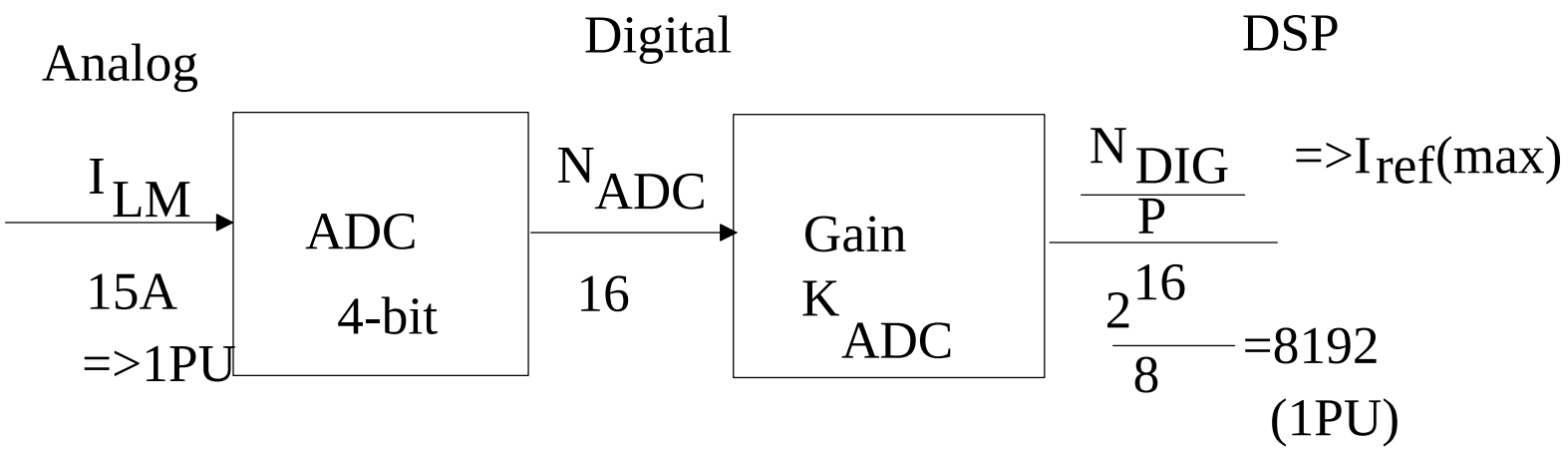
$$I_{ref\_DIG} = floor(\frac{I_{ref}}{I_{LM}} \frac{N_{DIG}}{P})$$

$$\Delta I_{con\_DIG} = floor(\frac{V_g}{R * N_{DPWM}} \frac{N_{DIG}}{I_{LM} * P})$$

$$\Delta I_{adc\_DIG} = K_{ADC\_I}$$

$$P = \frac{I_{ref}(\max)}{I_{LM}}$$

Digital Current-Mode Control: Quantization Analysis of Algorithm

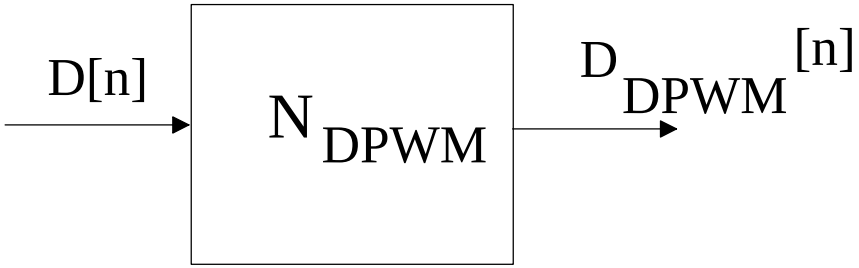


$$K_{ADC\_I} = floor(\frac{N_{DIG}}{P} * \frac{1}{N_{ADC\_I}})$$

$$\Delta I_{adc\_DIG} = K_{ADC\_I}$$

$$I_{ref\_DIG} = floor(\frac{I_{ref}}{I_{LM}}\frac{N_{DIG}}{P})$$

Digital Current-Mode Control: Quantization Analysis of Algorithm



D[n]=1=>$D_{DPWM}[n] = 200$

Analog Equation:

$$D[n] = \left(\frac{I_{ref}[n-1] - I_{LS}[n-1]}{M_C T_S}\right)$$

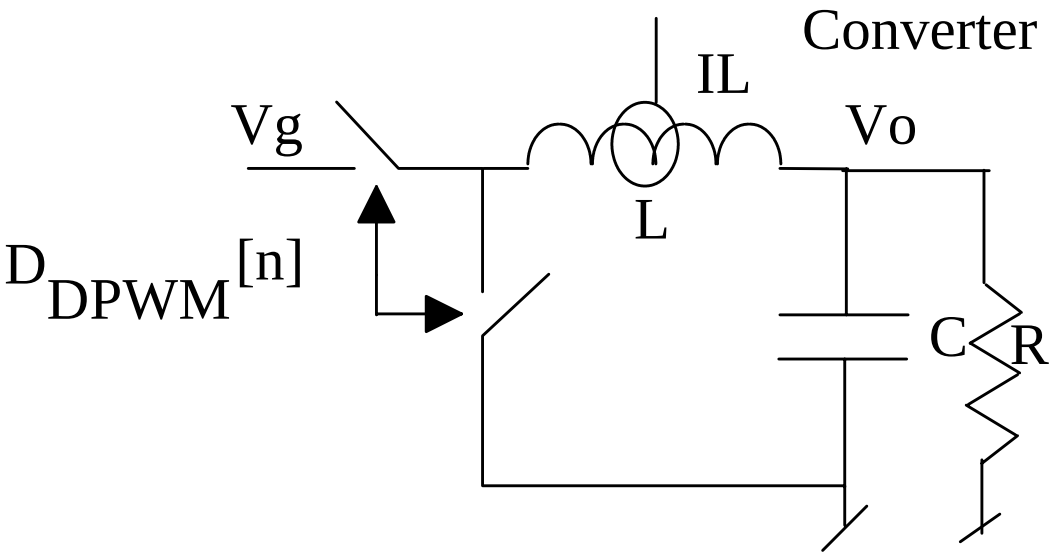
Digital Equivalent:

$$D_{DPWM}[n] = floor\left(\frac{I_{ref\_DIG}[n-1] - I_{LS\_DIG}[n-1]}{\Delta I_{\mathrm{mod}\_DIG}}\right)$$

Therefore

$$\Delta I_{\mathrm{mod}\_DIG} = floor\left(\frac{M_c T_S}{I_{LM}} \frac{1}{N_{DPWM}} \frac{N_{DIG}}{P}\right)$$

Digital Current-Mode Control: Quantization Analysis of Algorithm



Steady state:
IL(av)=Vo/R

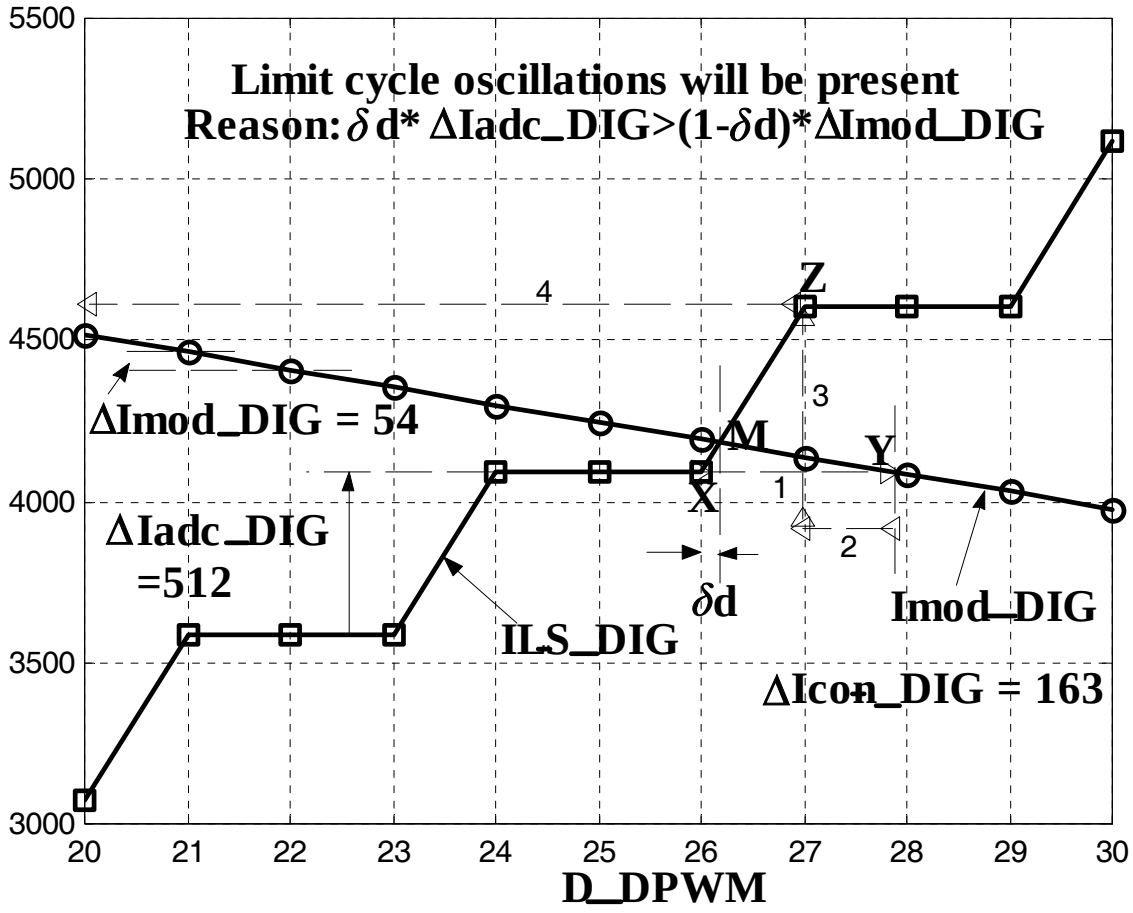
Note that if D_{DPWM} changes by 1the output current (also the inductor current) changes by $\frac{V_g}{R*N_{DPWM}}$

Therefore

$$\Delta I_{con\_DIG} = floor(\frac{V_g}{R*N_{DPWM}}\frac{N_{DIG}}{I_{LM}*P})$$

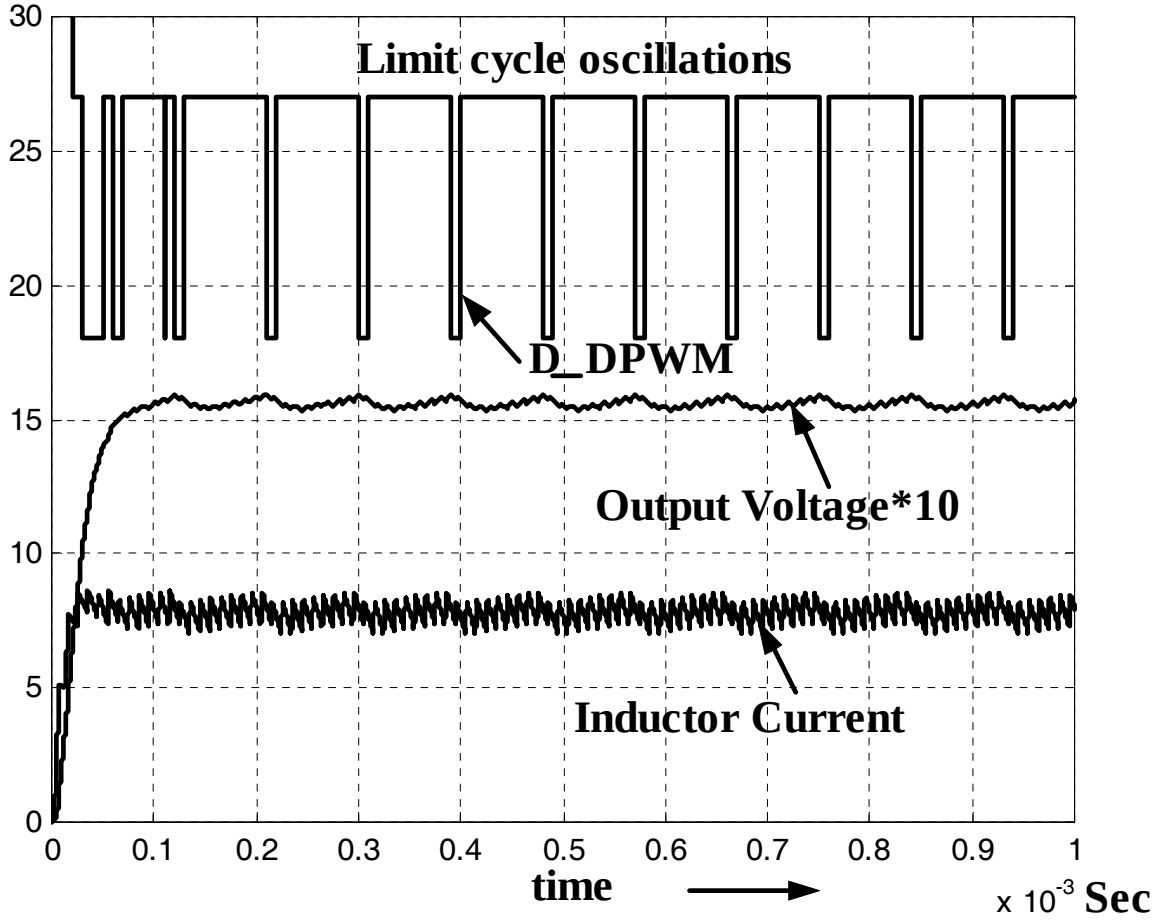
Digital Current-Mode Control: Graphical Analysis

Condition : *Iref_DIG* = 5597 , Current Conversion ADC 4 bit



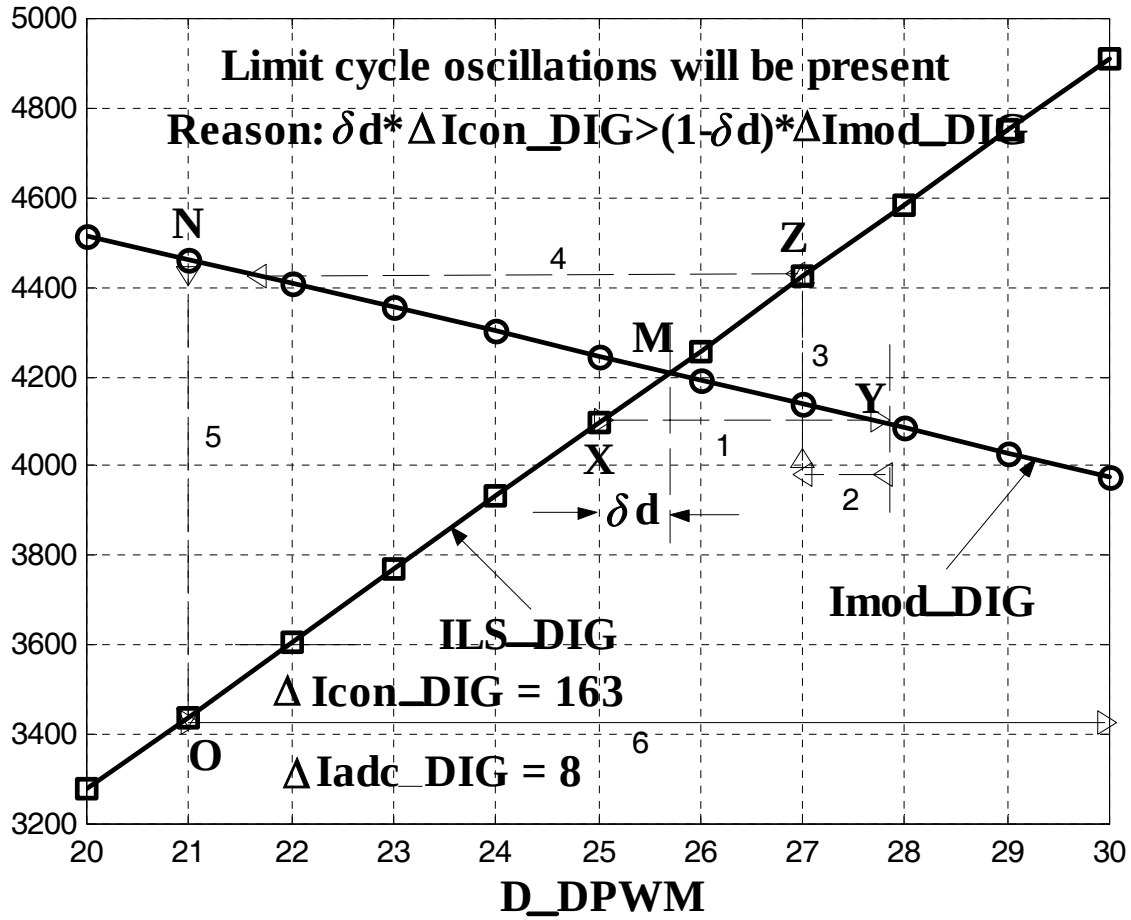
Limit Cycling in Inductor Current : Simulation Results

Condition : *Iref_DIG* = 5597 , Current Conversion ADC 4 bit



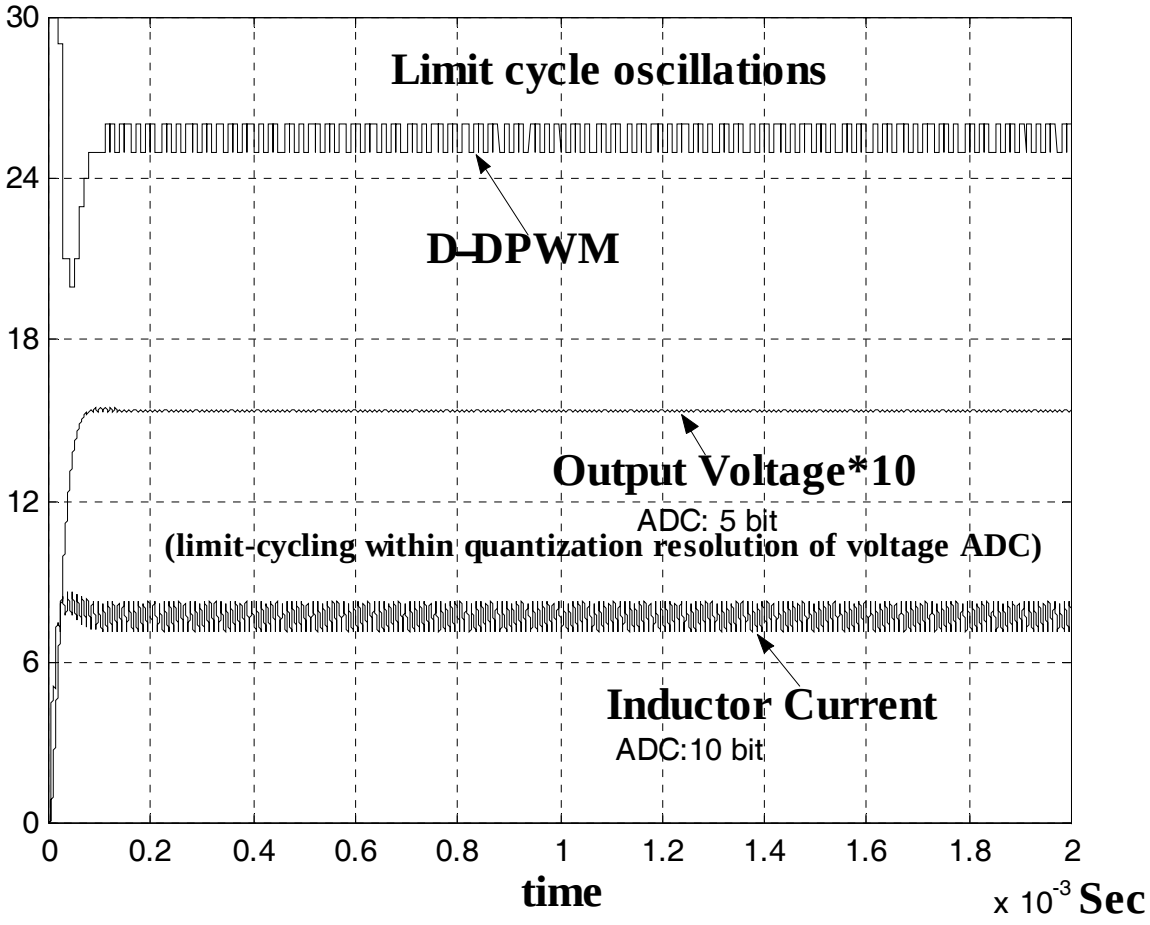
Limit Cycle Oscillations : Prediction by Analysis

Condition : *Iref_DIG* = 5597 , Current Conversion ADC 10 bit

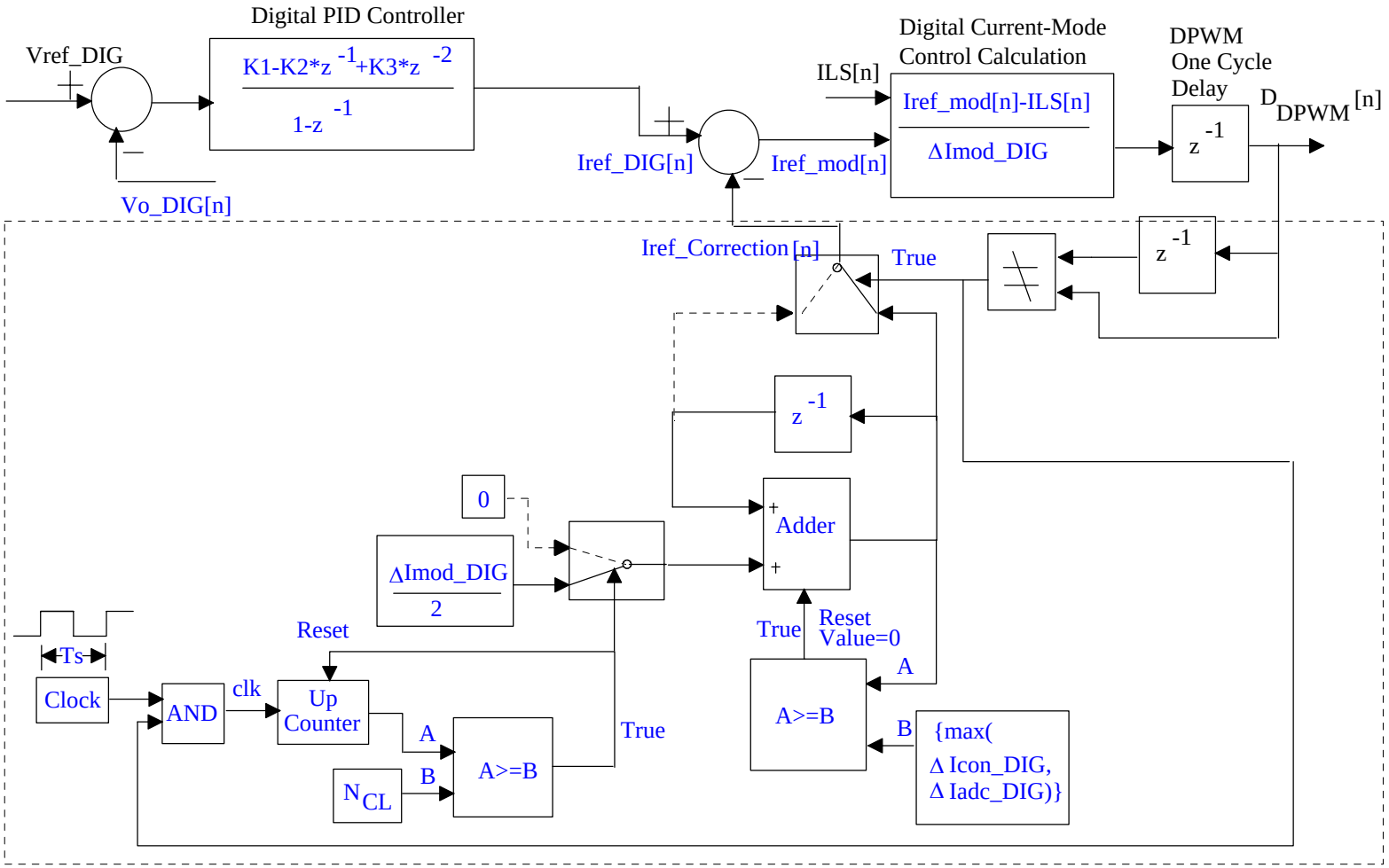


Simulation Results : Verification of the Prediction

Condition : *Iref DIG* = 5597 , Current Conversion ADC 10 bit



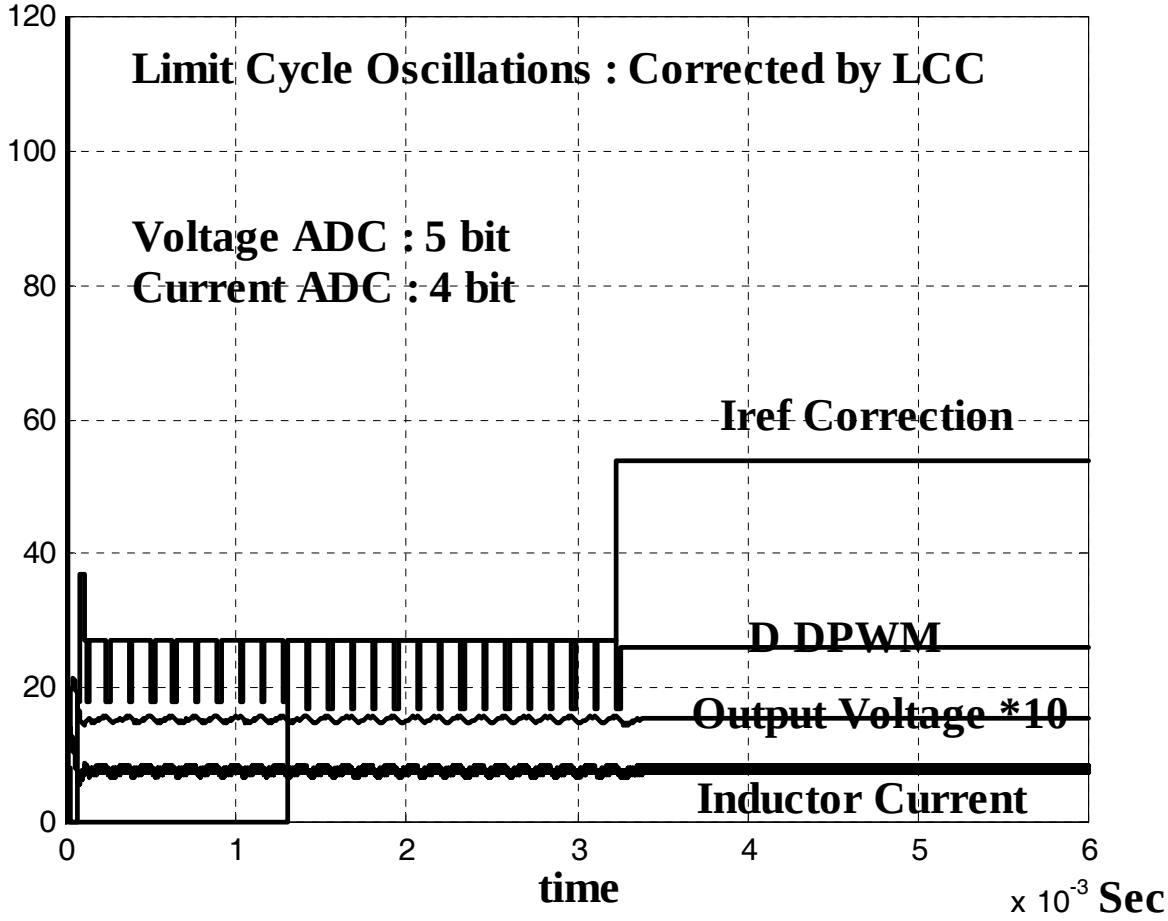
Limit Cycle Corrector (LCC): Block Diagram



Limit Cycle Corrector

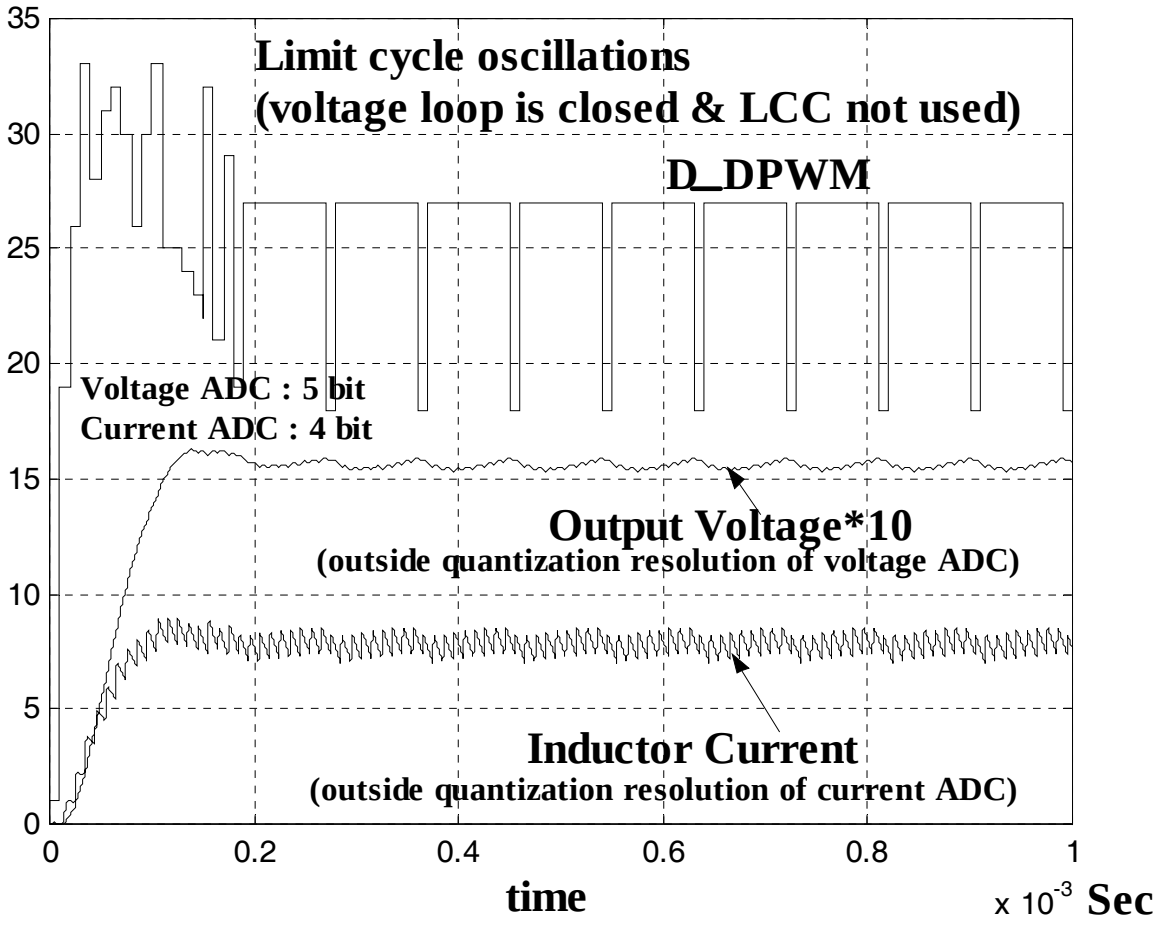
Limit Cycle Oscillations : Corrected by LCC

Condition : **Outer Voltage Loop Open**, *Iref_DIG* = 5597



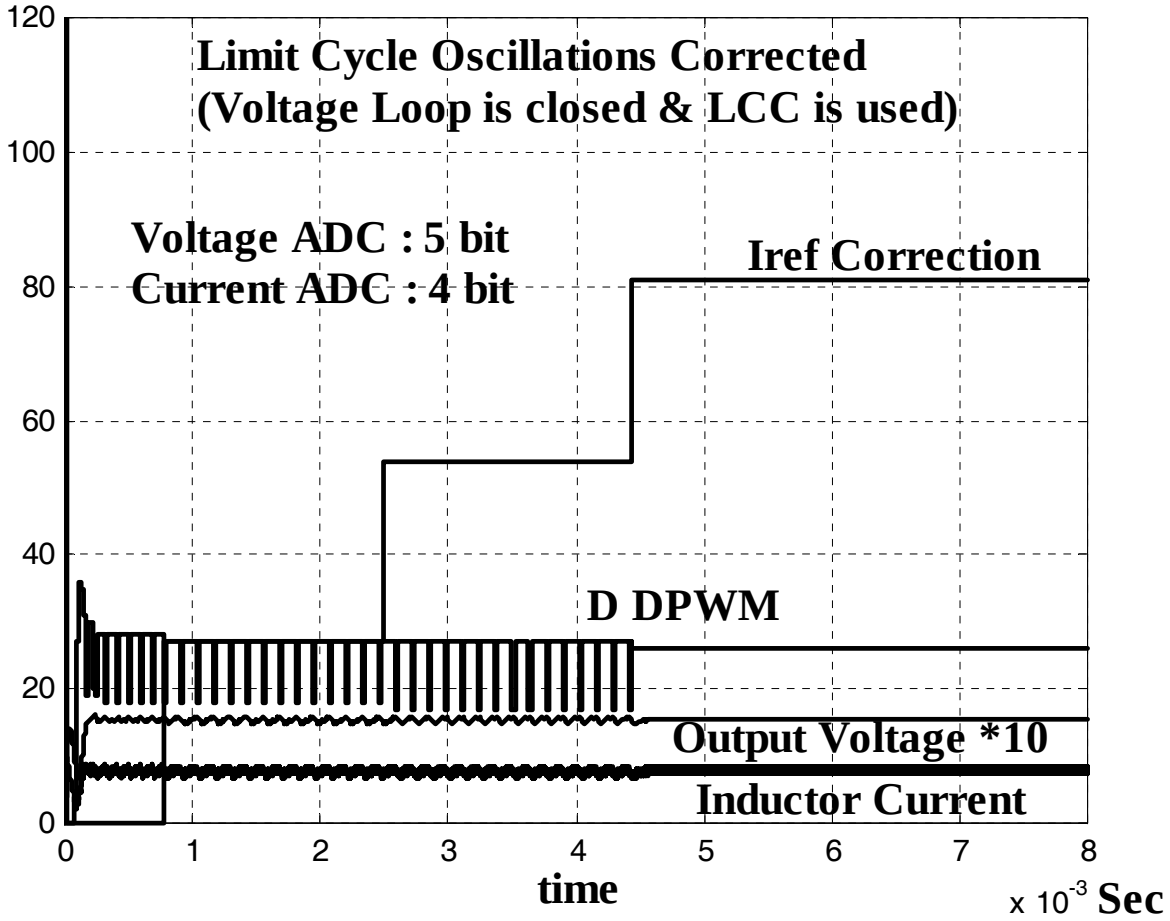
Limit Cycle Oscillations : Without LCC

Condition : **Outer Voltage Loop Closed**, $V_{ref\_DIG} = 3840$ (Equivalent to 1.5 V)



Correction of Limit Cycle Oscillations : With LCC

Condition : **Outer Voltage Loop Closed**, $V_{ref\_DIG} = 3840$ (Equivalent to 1.5 V)

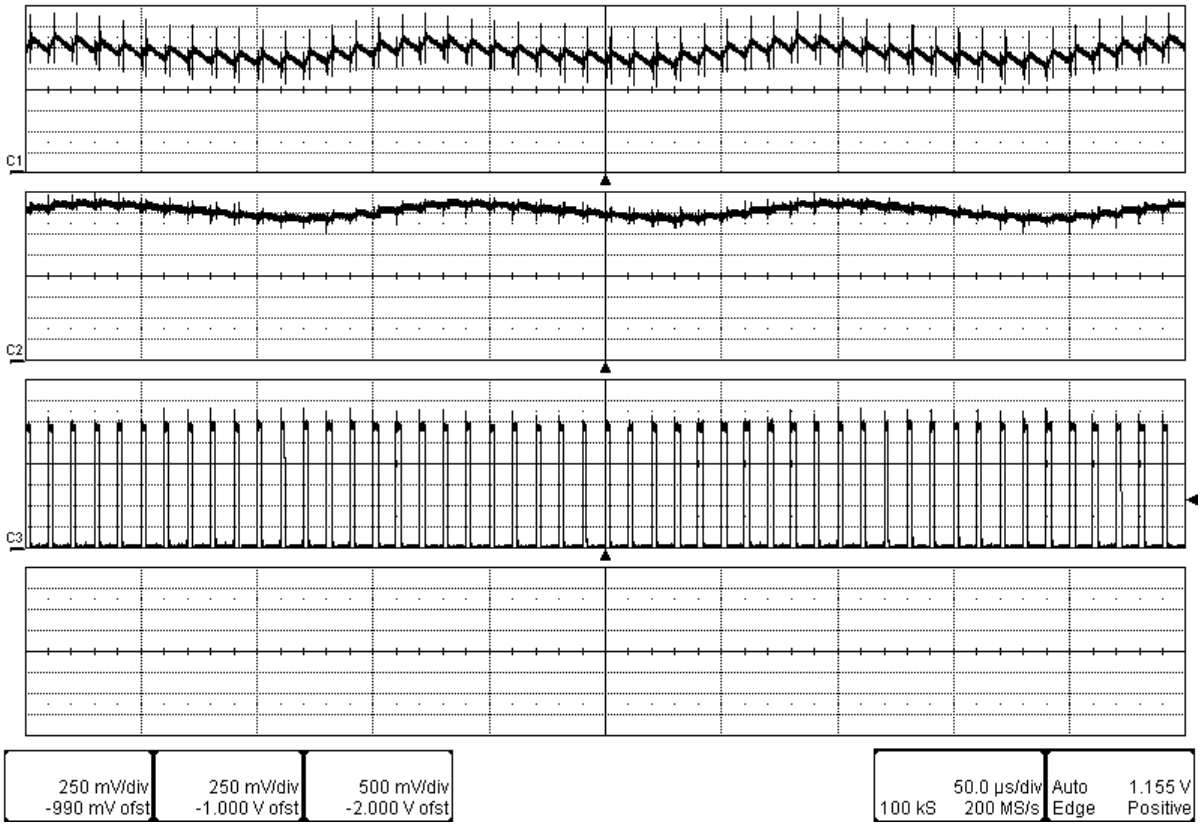


Experimental Results: Limit Cycle Oscillations Without LCC

Buck Converter Parameters: $V_g = 12\,V,\ V_{o\_ref} = 1.5\,V,\ L = 27\,\mu H, C = 100\,\mu F,$

$R = 0.2\,\Omega, T_S = 10\,\mu Sec$

Condition : **Outer Voltage Loop Open**, $Iref\_DIG = 5597$

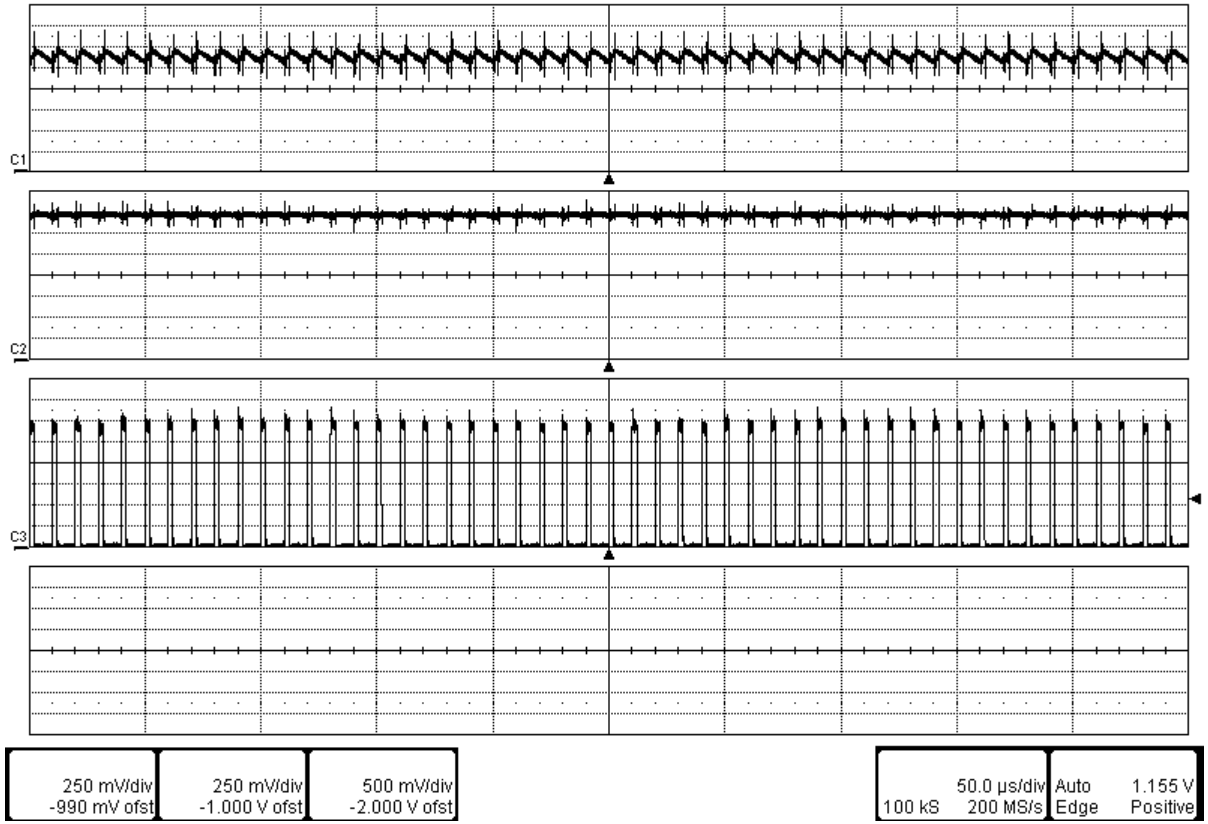


Experimental Results: Limit Cycle Oscillations Corrected by LCC

Buck Converter Parameters: $V_g = 12\,V,\ V_{o\_ref} = 1.5\,V,\ L = 27\,\mu H, C = 100\,\mu F,$

$R = 0.2\,\Omega, T_S = 10\,\mu Sec$

Condition : **Outer Voltage Loop Open**, $Iref\_DIG = 5597$



Experimental Results: Limit Cycle Oscillations Without LCC

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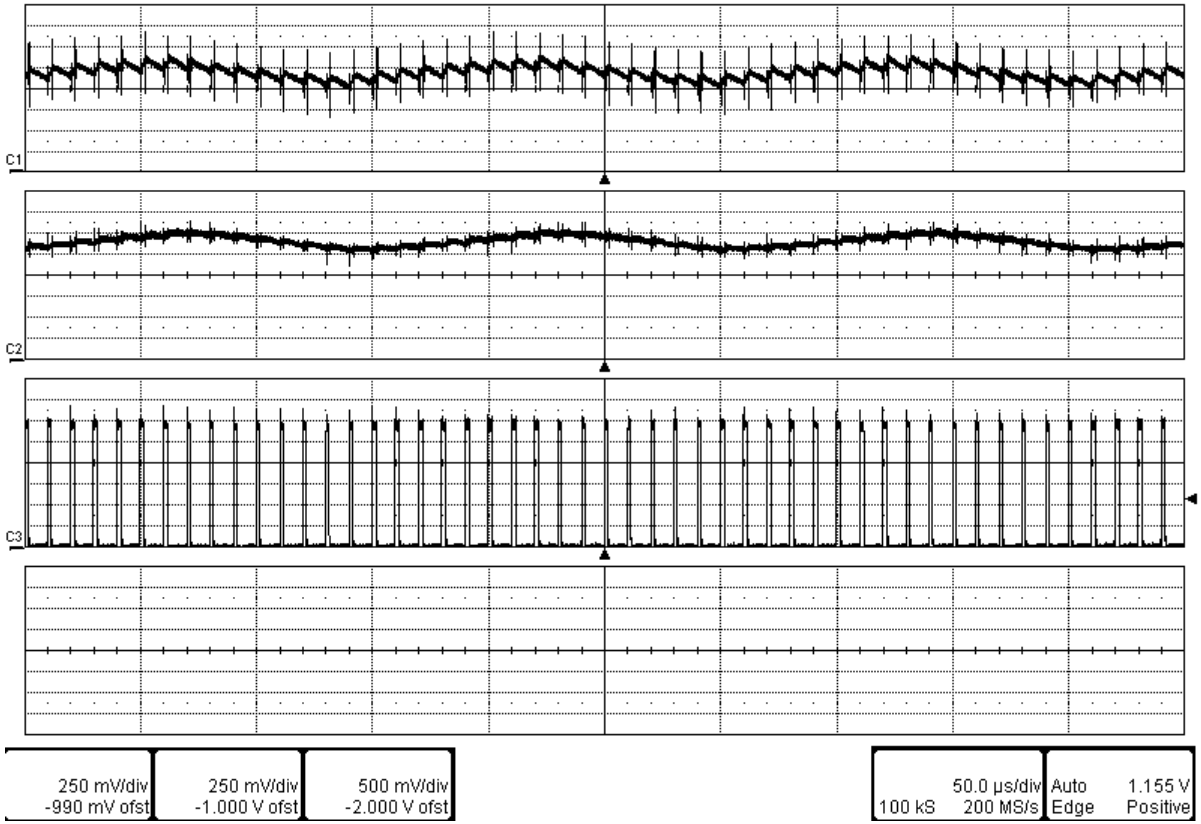

Experimental Results: Limit Cycle Oscillations Corrected by LCC

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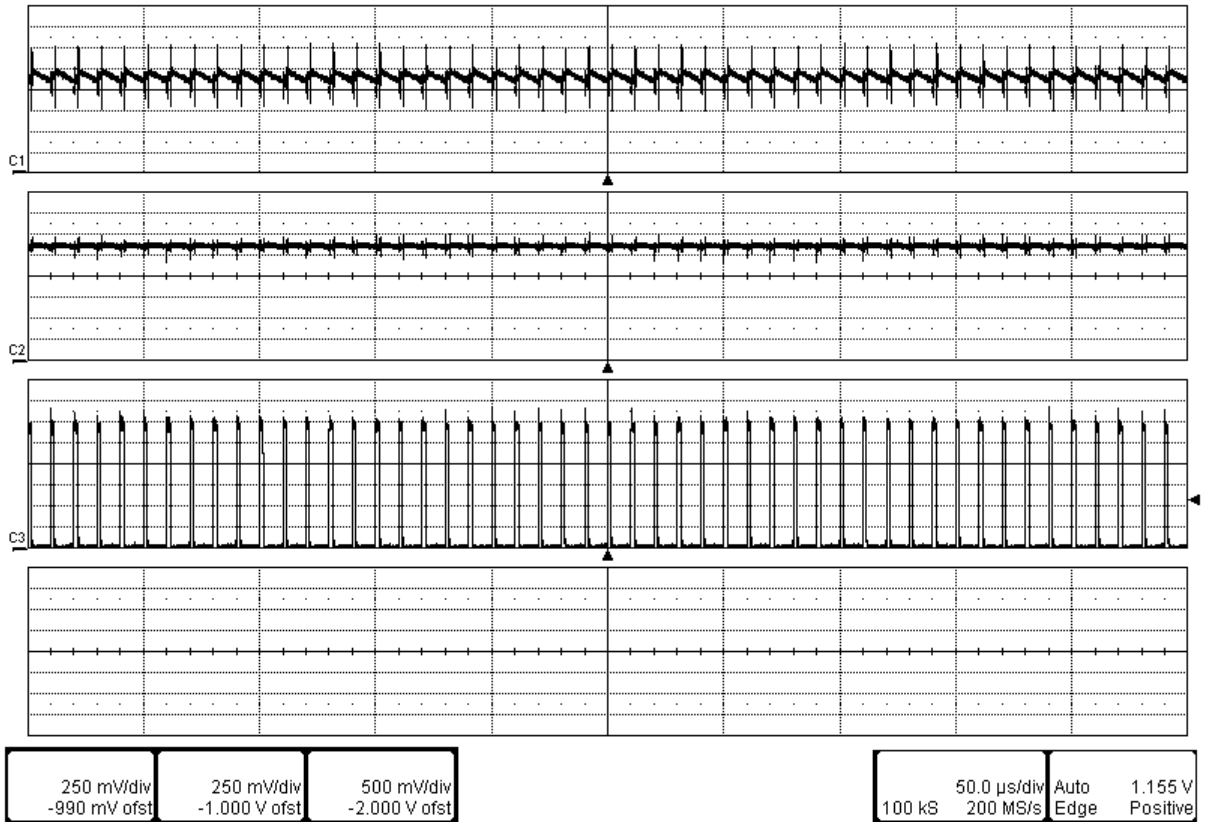

Digital Current-Mode Control: Conclusions

- Digital Current-Mode Control method is simple to implement in digital hardware => Higher Switching Frequency
- Digital architecture for Peak, Valley and Average Current-Mode Controls are described
- Experimental results of a 400 kHz digital implementation is presented. It could achieve 1 MHz with improved digital architecture.
- FPGA is more suitable as digital hardware for high switching frequency applications compared to DSP.
- Digital control is yet to become economical but matching the analog performances and exceeding it on many cases.

Analysis of Limit Cycle Oscillations : Conclusions

- ✓ The talk has shown that when a dc-dc converter employs digital current mode control steady-state limit cycling may occur due to quantization of the inductor current.
- ✓ It has been shown that unlike digital voltage-mode control this problem may appear irrespective of whether the quantization resolution of the ADC is more or less compared to the DPWM.
- ✓ This talk has presented a method of graphical analysis to accurately predict limit cycle oscillations in inductor current.
- ✓ Finally it has also proposed a closed-loop solution to the limit cycling problem by adjustment of the current reference.
- ✓ Simulations and experimental results have been presented to validate the analysis.