Basic FPGA Architecture

XILINX®

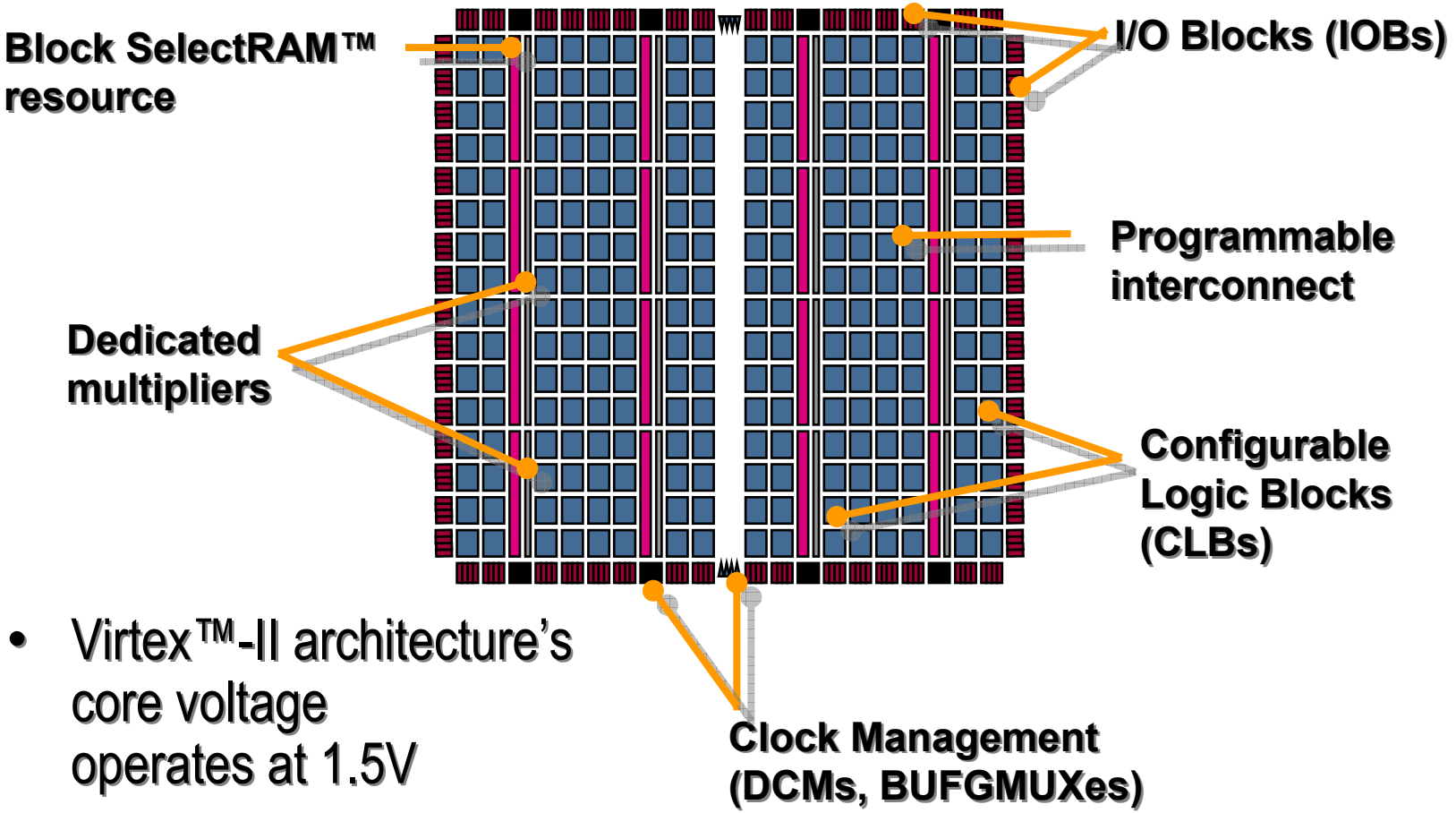
Outline

- **Overview**
- Slice Resources
- I/O Resources
- Memory and Clocking
- Spartan-3, Spartan-3E, and Virtex-II Pro Features
- Virtex-4 Features
- Summary
- Appendix

Overview

- All Xilinx FPGAs contain the same basic resources
  - Slices (grouped into CLBs)
  - IOBs
  - Programmable interconnect
  - Other resources
    - Memory
    - Multipliers
    - Global clock buffers
    - Boundary scan logic

Virtex-II Architecture



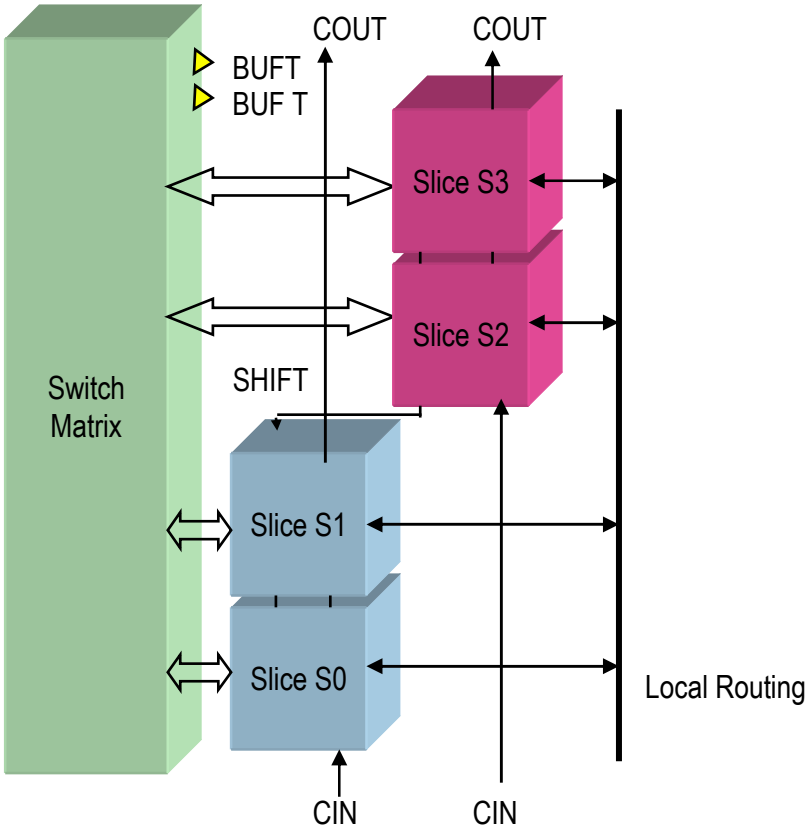
- Virtex™-II architecture's core voltage operates at 1.5V

XILINX®

Outline

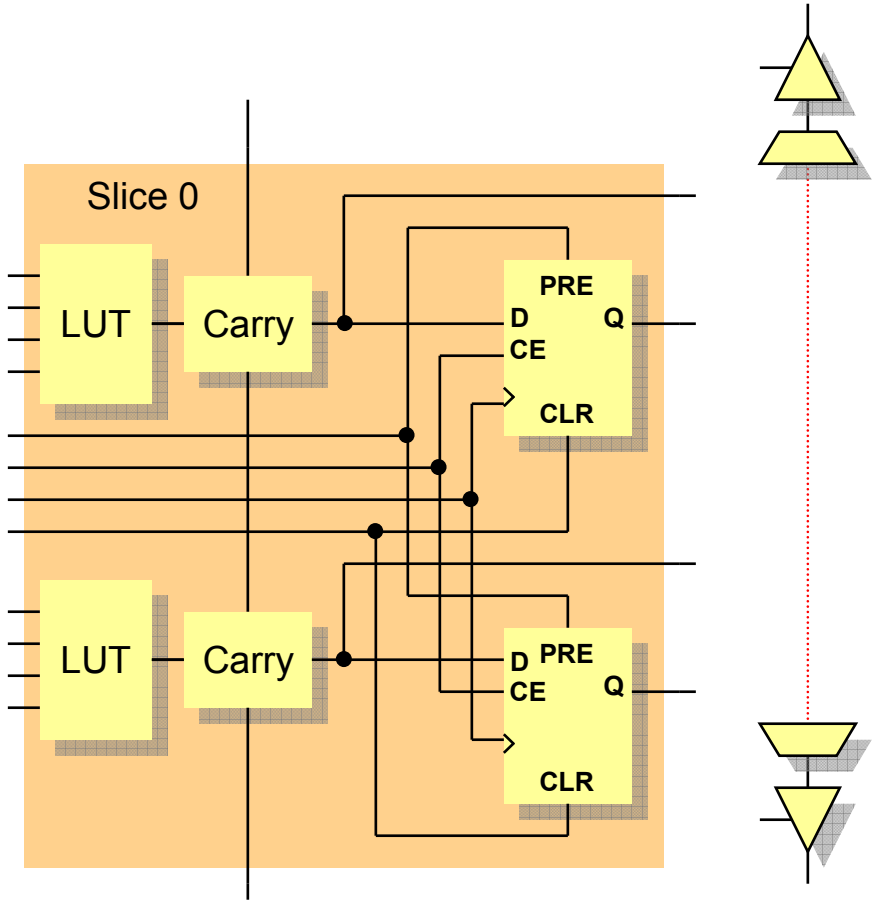
- Overview
- **Slice Resources**
- I/O Resources
- Memory and Clocking
- Spartan-3, Spartan-3E, and Virtex-II Pro Features
- Virtex-4 Features
- Summary
- Appendix

Slices and CLBs

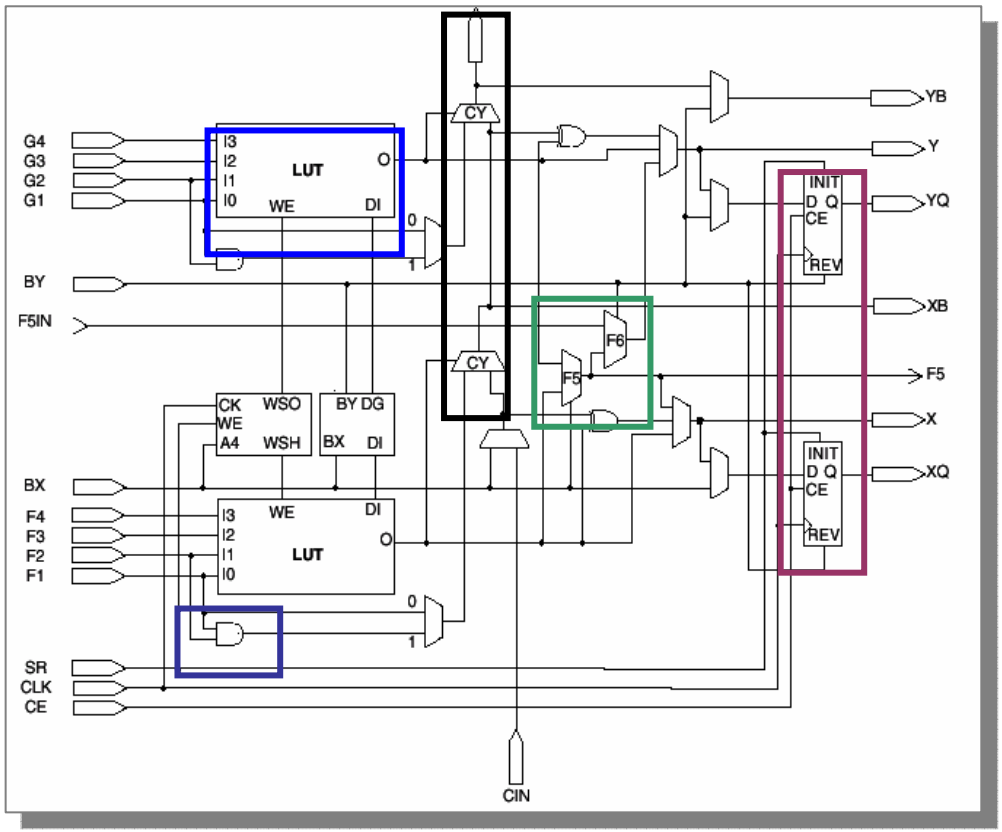


XILINX®

Simplified Slice Structure

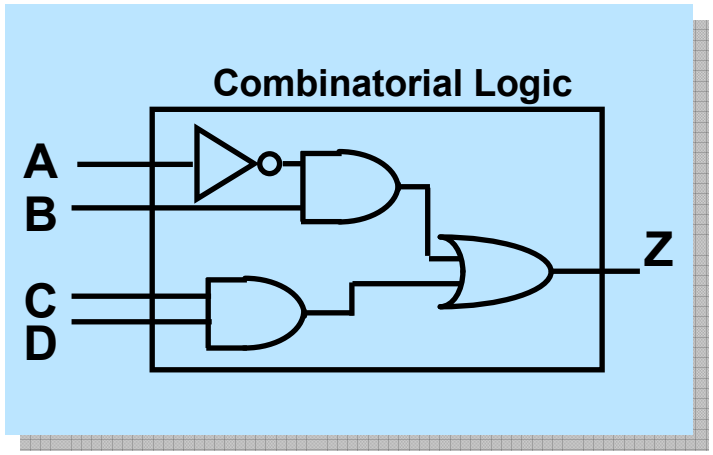


Detailed Slice Structure



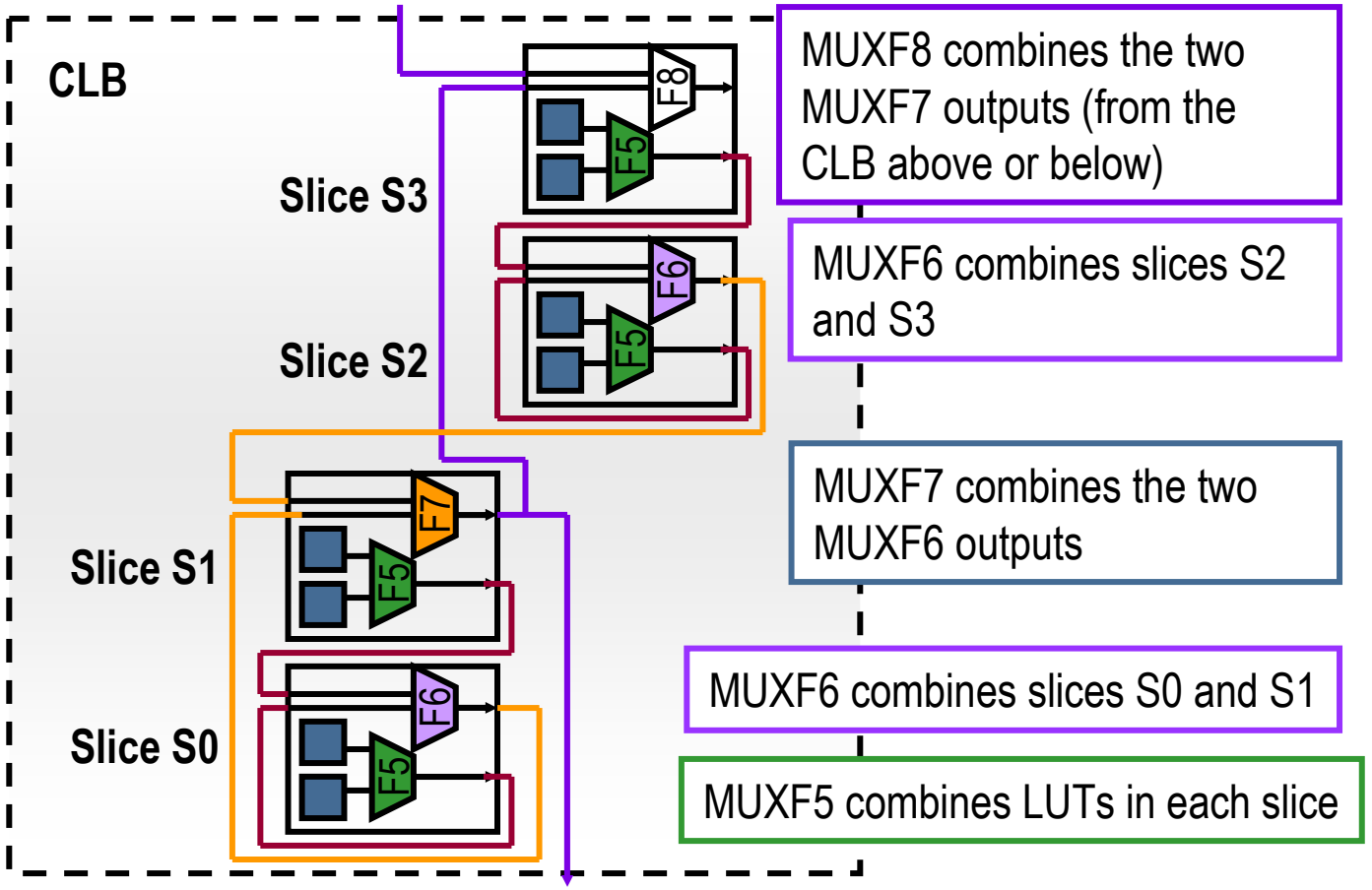
XILINX®

Look-Up Tables



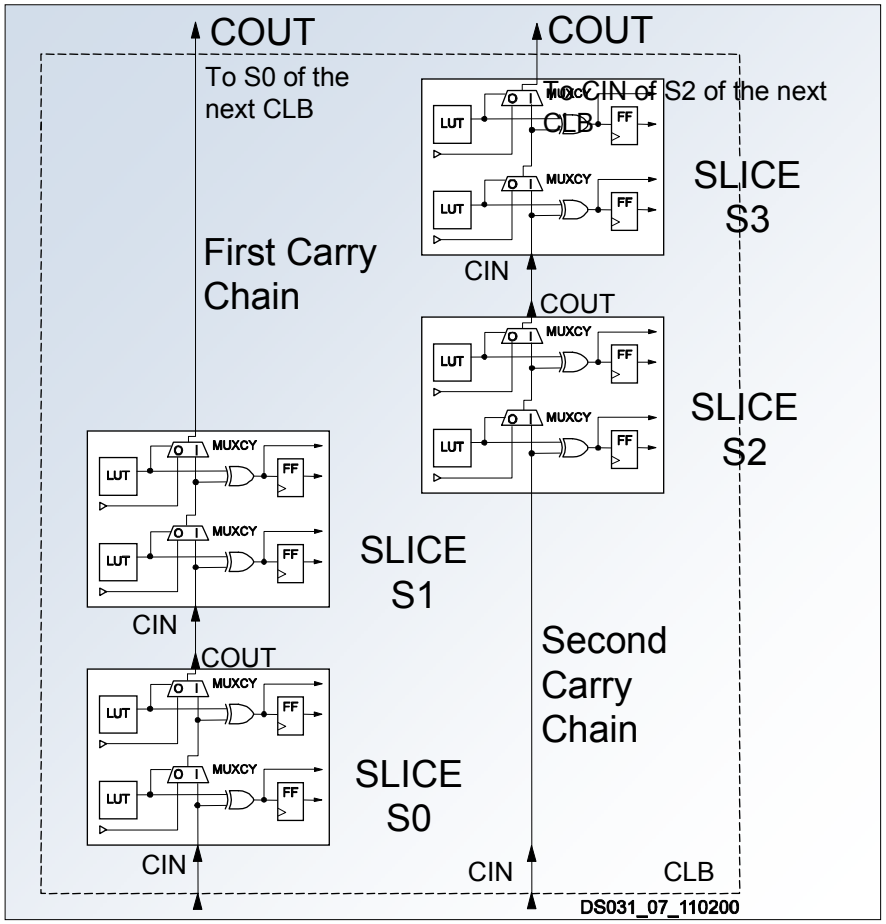
A	B	C	D	Z
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
	.	.	.	
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

Connecting Look-Up Tables

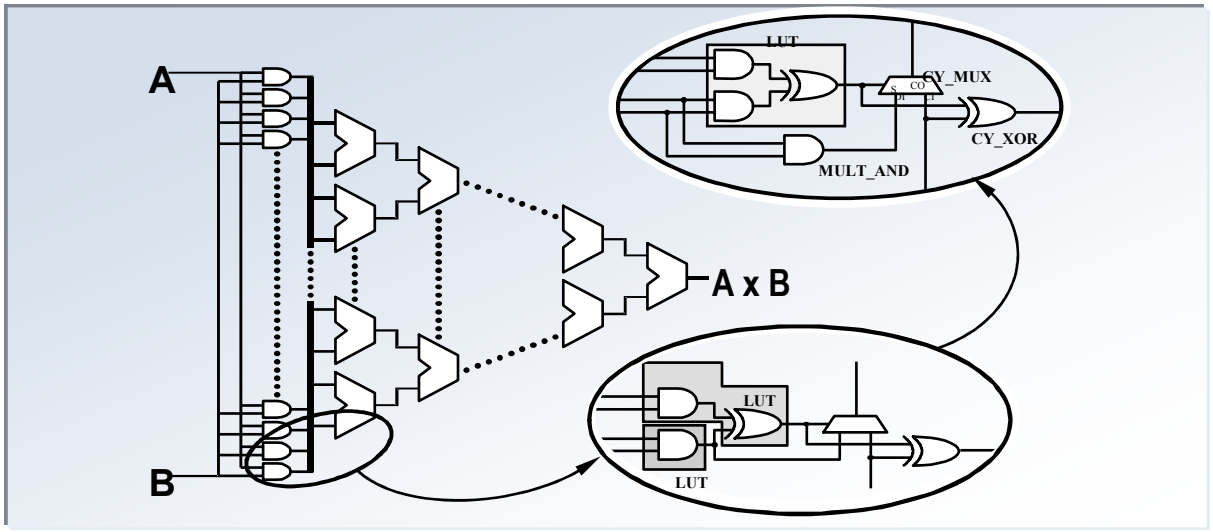


XILINX®

Fast Carry Logic

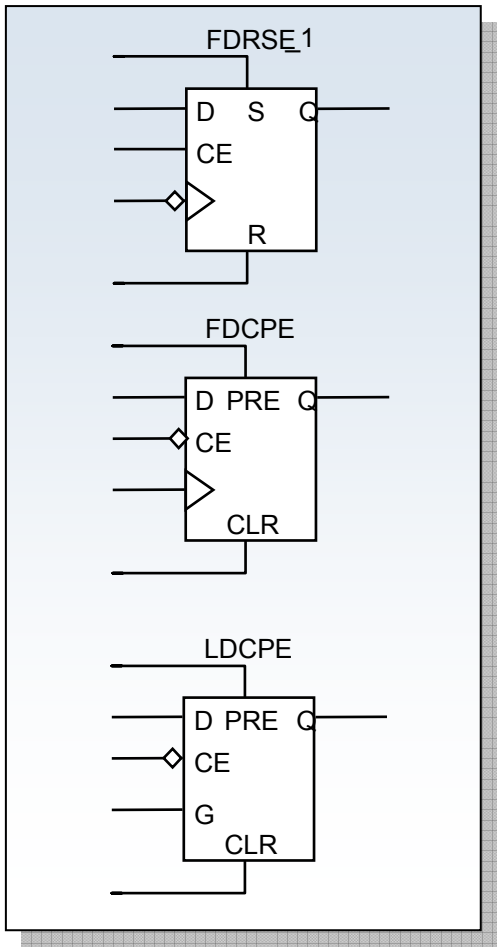


MULT_AND Gate Improves Performance



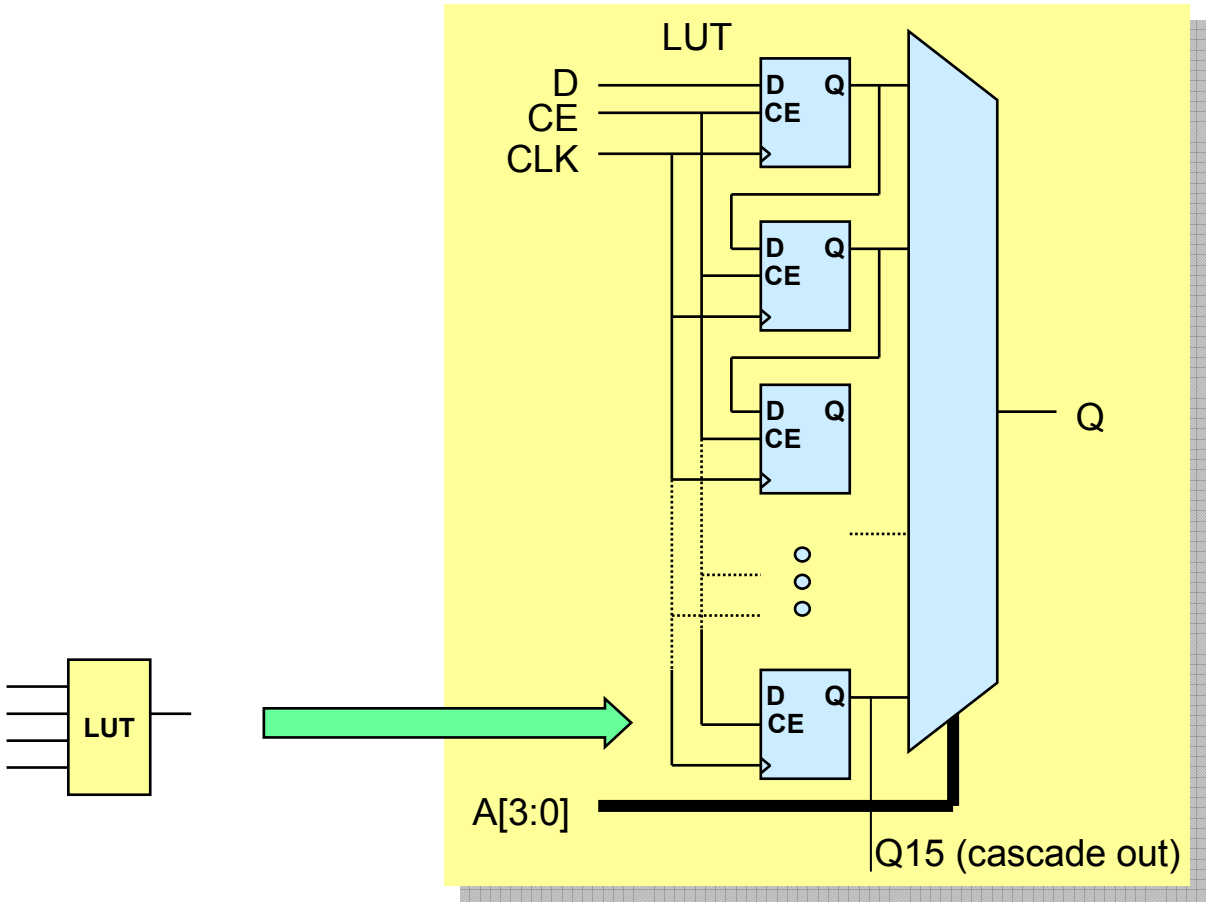
XILINX®

Flexible Sequential Elements



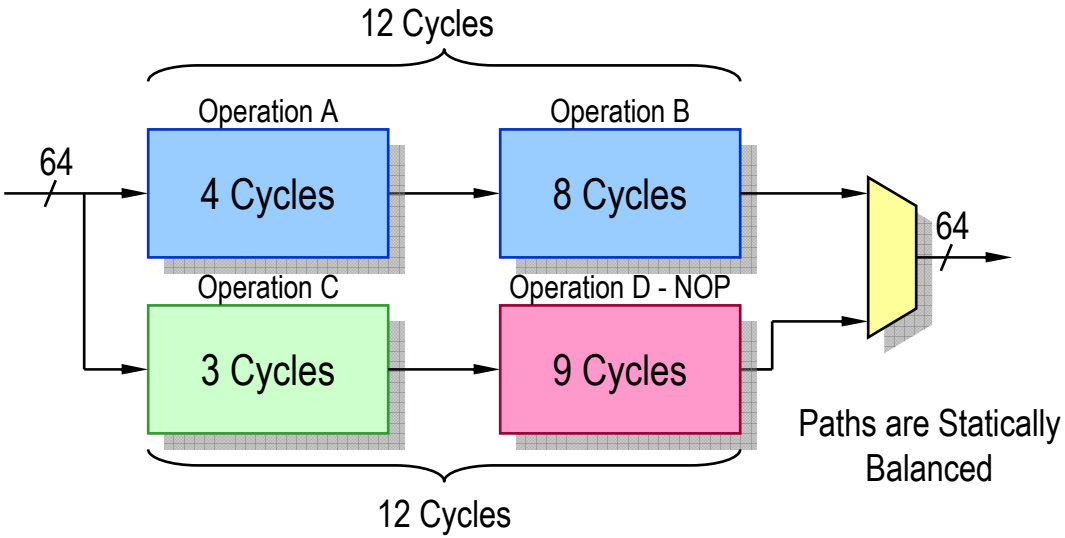
XILINX®

Shift Register LUT (SRL16CE)



XILINX®

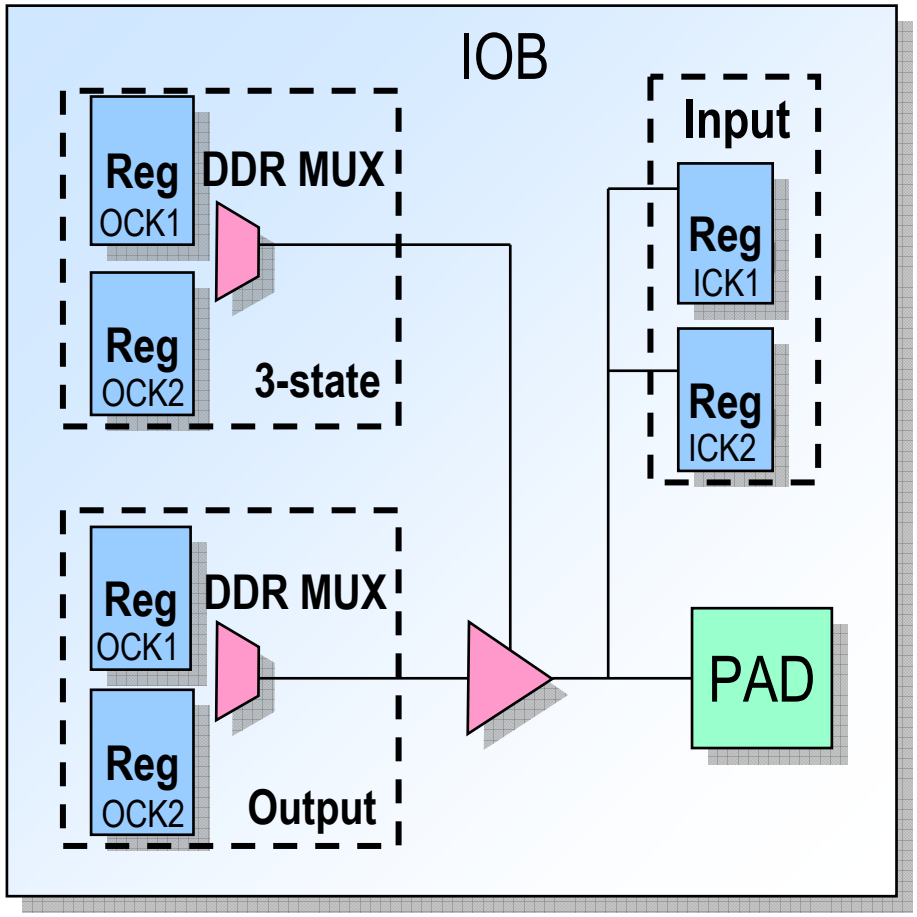
Shift Register LUT Example



Outline

- Overview
- Slice Resources
- **I/O Resources**
- Memory and Clocking
- Spartan-3, Spartan-3E, and Virtex-II Pro Features
- Virtex-4 Features
- Summary
- Appendix

IOB Element



SelectIO Standard

- Differential signaling standards
  - LVDS, BLVDS, ULVDS
  - LDT
  - LVPECL
- Single-ended I/O standards
  - LVTTL, LVCMOS (3.3V, 2.5V, 1.8V, and 1.5V)
  - PCI-X at 133 MHz, PCI (3.3V at 33 MHz and 66 MHz)
  - GTL, GTLP
  - and more!

Easier and More Flexible I/O Design!

Digital Controlled Impedance (DCI)

- DCI provides
  - Output drivers that match the impedance of the traces
  - On-chip termination for receivers and transmitters
- DCI advantages
  - Improves signal integrity by eliminating stub reflections
  - Reduces board routing complexity and component count by eliminating external resistors
  - Eliminates the effects of temperature, voltage, and process variations by using an internal feedback circuit

Outline

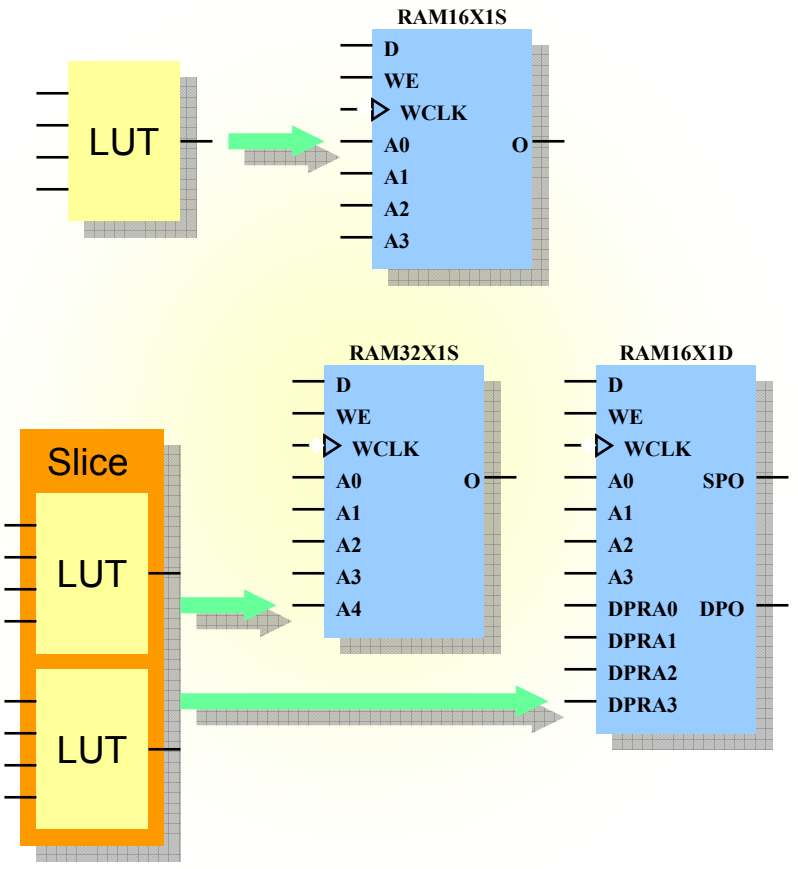
- Overview
- Slice Resources
- I/O Resources
- **Memory and Clocking**
- Spartan-3, Spartan-3E, and Virtex-II Pro Features
- Virtex-4 Features
- Summary
- Appendix

Other Virtex-II Features

- Distributed RAM and block RAM
  - Distributed RAM uses the CLB resources (1 LUT = 16 RAM bits)
  - Block RAM is a dedicated resources on the device (18-kb blocks)
- Dedicated 18 x 18 multipliers next to block RAMs
- Clock management resources
  - Sixteen dedicated global clock multiplexers
  - Digital Clock Managers (DCMs)

Distributed SelectRAM Resources

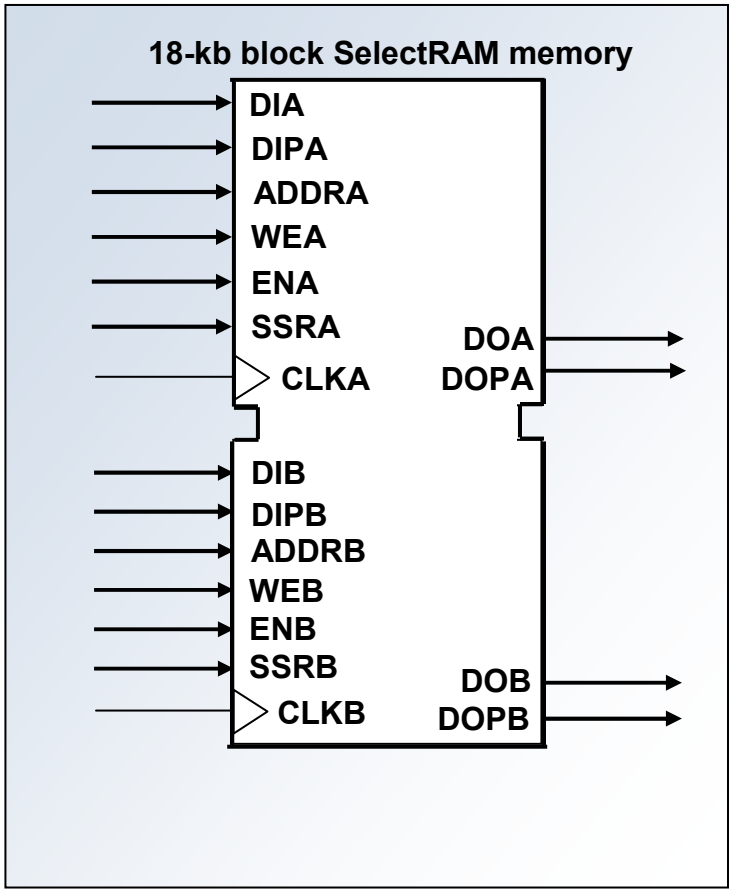
- Uses a LUT in a slice as memory
- Synchronous write
- Asynchronous read
- RAM and ROM are initialized during configuration
- Emulated dual-port RAM
  - One read/write port
  - One read-only port



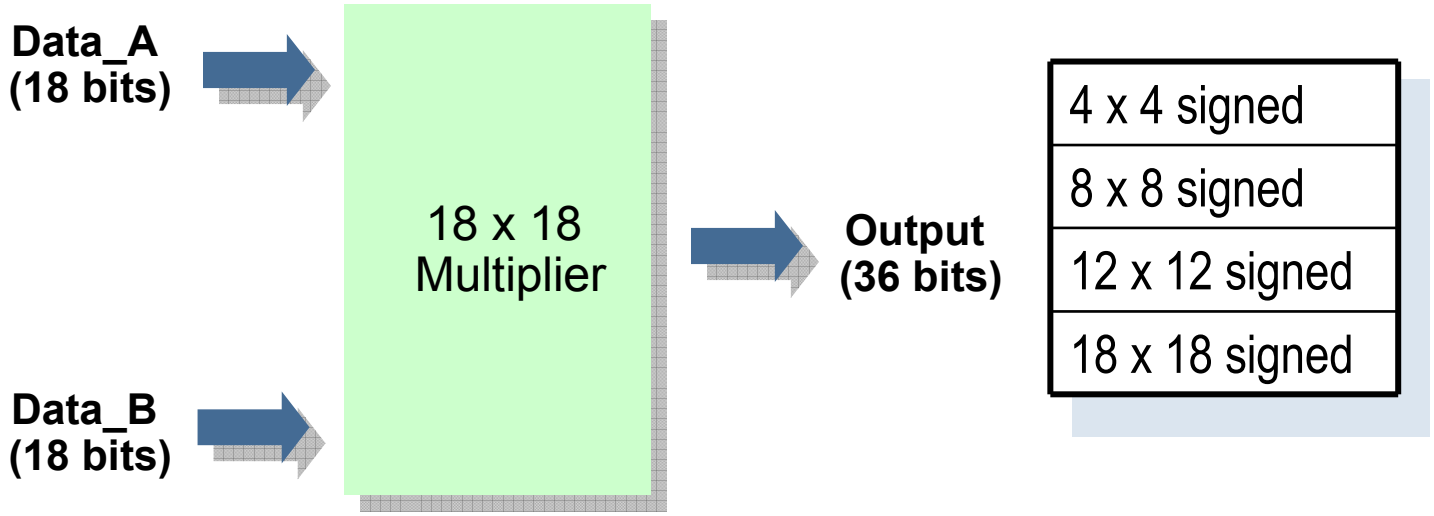
XILINX®

Block SelectRAM Resources

- Up to 3.5 Mb of RAM in 18-kb blocks
  - Synchronous read and write
- True dual-port memory
  - Each port has synchronous read and write capability
  - Different clocks for each port
- Supports initial values
- Synchronous reset on output latches
- Supports parity bits
  - One parity bit per eight data bits



Dedicated Multiplier Blocks

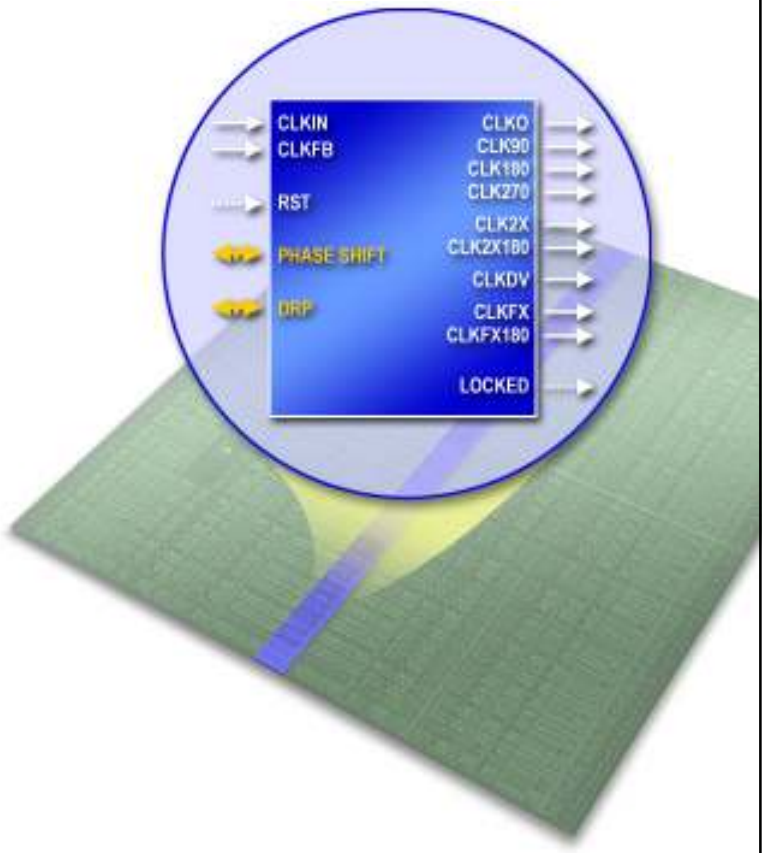


Global Clock Routing Resources

- Sixteen dedicated global clock multiplexers
  - Eight on the top-center of the die, eight on the bottom-center
  - Driven by a clock input pad, a DCM, or local routing
- Global clock multiplexers provide the following:
  - Traditional clock buffer (BUFG) function
  - Global clock enable capability (BUFGCE)
  - Glitch-free switching between clock signals (BUFGMUX)
- Up to eight clock nets can be used in each clock region of the device
  - Each device contains four or more clock regions

Digital Clock Manager (DCM)

- DCMs provide the following:
  - Delay-Locked Loop (DLL)
  - Digital Frequency Synthesizer (DFS)
  - Digital Phase Shifter (DPS)
- Up to four outputs of each DCM can drive onto global clock buffers
  - All DCM outputs can drive general routing



XILINX®

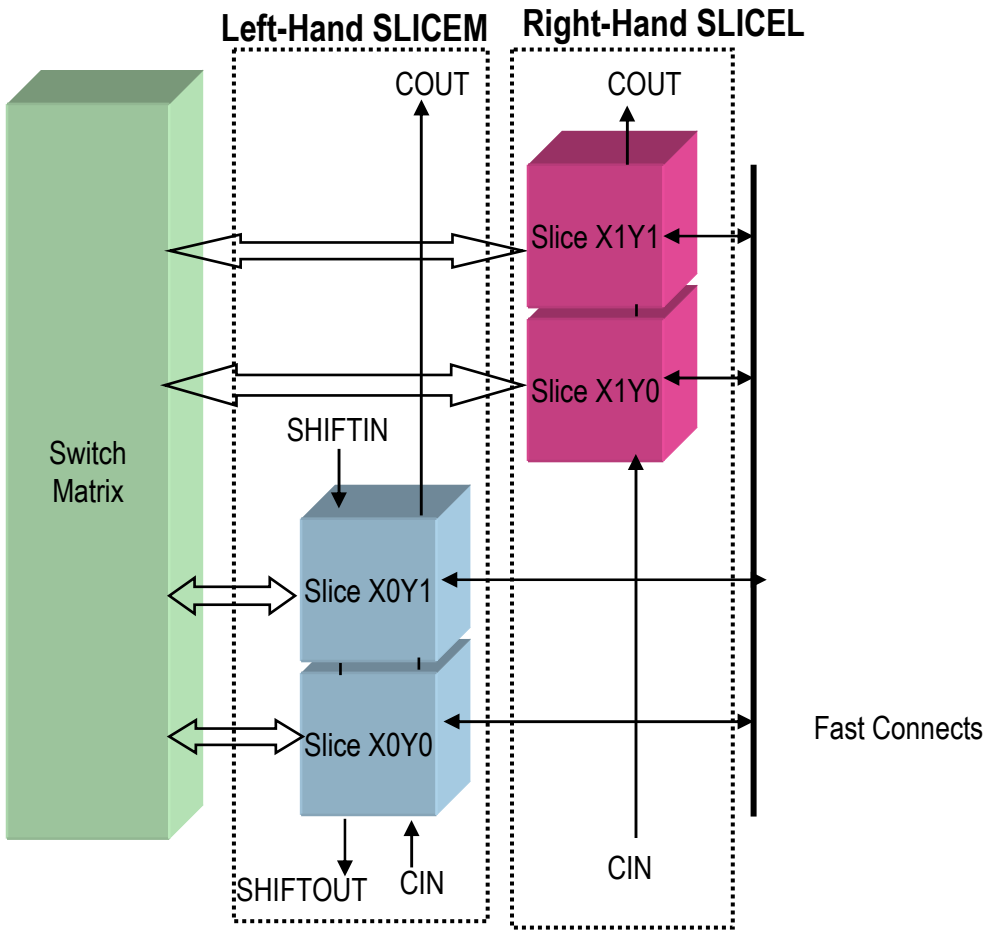
Outline

- Overview
- Slice Resources
- I/O Resources
- Memory and Clocking
- **Spartan-3, Spartan-3E, and Virtex-II Pro Features**
- Virtex-4 Features
- Summary
- Appendix

Spartan-3 versus Virtex-II

- Lower cost
- Smaller process = lower core voltage
  - .09 micron versus .15 micron
  - Vccint = 1.2V versus 1.5V
- Different I/O standard support
  - New standards: 1.2V LVCMOS, 1.8V HSTL, and SSTL
  - Default is LVCMOS, versus LVTTL
- More I/O pins per package
- Only one-half of the slices support RAM or SRL16s (SLICEM)
- Fewer block RAMs and multiplier blocks
  - Same size and functionality
- Eight global clock multiplexers
- Two or four DCM blocks
- No internal 3-state buffers
  - 3-state buffers are in the I/O

SLICEM and SLICEL



XILINX®

Spartan-3E Features

- More gates per I/O than Spartan-3
- Removed some I/O standards
  - Higher-drive LVCMOS
  - GTL, GTLP
  - SSTL2_II
  - HSTL_II_18, HSTL_I, HSTL_III
  - LVDS_EXT, ULVDS
- DDR Cascade
  - Internal data is presented on a single clock edge
- 16 BUFGMUXes on left and right sides
  - Drive half the chip only
  - In addition to eight global clocks
- Pipelined multipliers
- Additional configuration modes
  - SPI, BPI
  - Multi-Boot mode

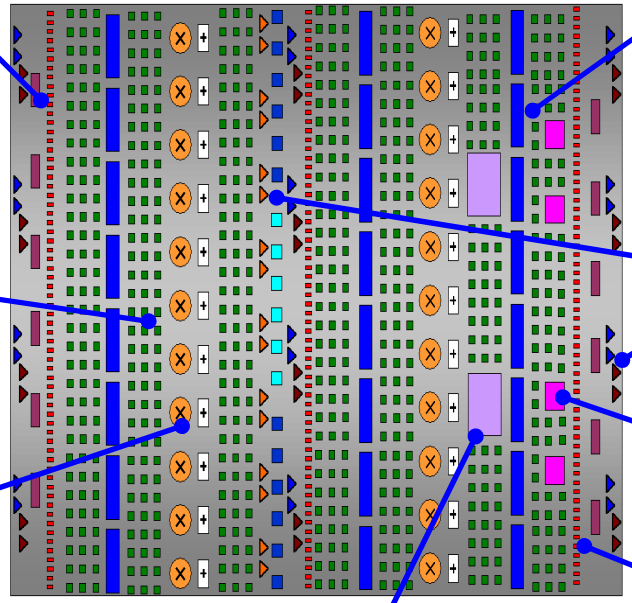
Virtex-II Pro Features

- 0.13 micron process
- Up to 24 RocketIO™ Multi-Gigabit Transceiver (MGT) blocks
  - Serializer and deserializer (SERDES)
  - Fibre Channel, Gigabit Ethernet, XAUI, Infiniband compliant transceivers, and others
  - 8-, 16-, and 32-bit selectable FPGA interface
  - 8B/10B encoder and decoder
- PowerPC™ RISC processor blocks
  - Thirty-two 32-bit General Purpose Registers (GPRs)
  - Low power consumption: 0.9mW/MHz
  - IBM CoreConnect bus architecture support

Outline

- Overview
- Slice Resources
- I/O Resources
- Memory and Clocking
- Spartan-3, Spartan-3E, and Virtex-II Pro Features
- **Virtex-4 Features**
- Summary
- Appendix

Virtex-4 Architecture Has the Most Advanced Feature Set



RocketIO™ Multi-Gigabit Transceivers
622 Mbps–10.3 Gbps

Advanced CLBs
200K Logic Cells

XtremeDSP™ Technology Slices
256 18x18 GMACs

PowerPC™ 405 with APU Interface
450 MHz, 680 DMIPS

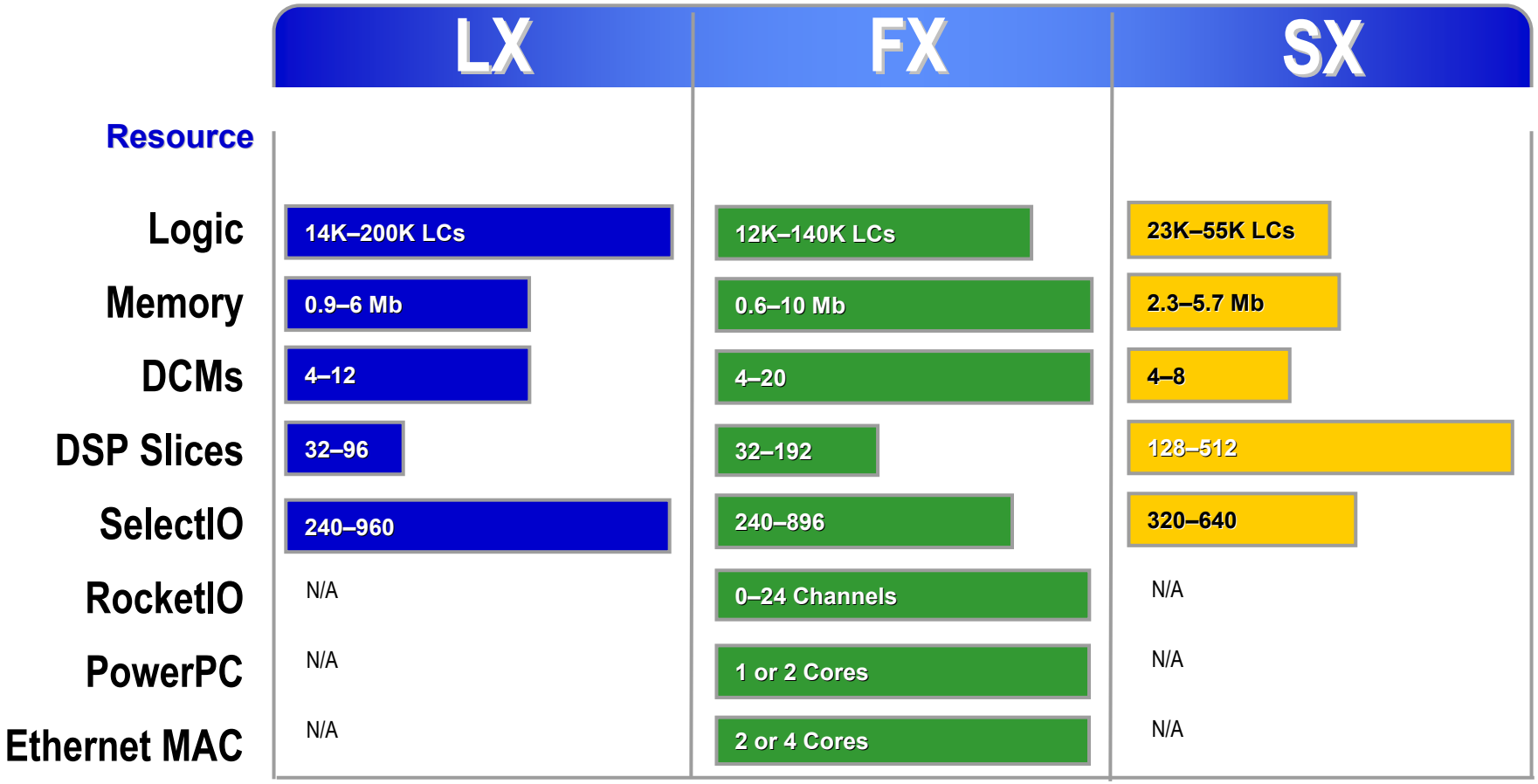
Smart RAM
New block RAM/FIFO

Xesium Clocking Technology
500 MHz

Tri-Mode Ethernet MAC
10/100/1000 Mbps

1 Gbps SelectIO™
ChipSync™ Source synch, XCITE Active Termination

Choose the Platform that Best Fits the Application



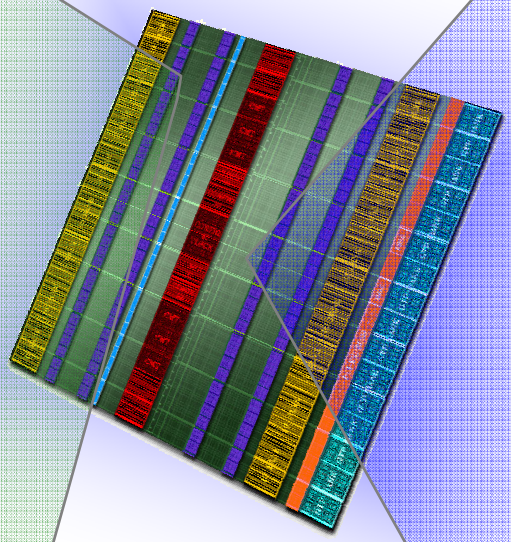
XILINX®

Virtex™-5 Family : First 65nm FPGAs

Continuing the Drive for Innovation

Enhanced

- 36Kbit Dual-Port Block RAM / FIFO with Integrated ECC
- 550 MHz Clock Management Tile with DCM and PLL
- SelectIO with ChipSync Technology and XCITE DCI
- Advanced Configuration Options
- 25x18 DSP Slice with Integrated ALU
- Tri-Mode 10/100/1000 Mbps Ethernet MACs



New

- Most Advanced High-Performance Real 6LUT Logic Fabric
- PCI Express® Endpoint Block
- System Monitor Function with Built-in ADC
- Next Generation PowerPC® Embedded Processor
- RocketIO™ Transceiver Options
  - Low-Power GTP: Up to 3.75 Gbps
  - High-Performance GTX: Up to 6.5 Gbps

Outline

- Overview
- Slice Resources
- I/O Resources
- Memory and Clocking
- Spartan-3, Spartan-3E, and Virtex-II Pro Features
- Virtex-4 Features
- **Summary**
- Appendix

Review Questions

- List the primary slice features
- List the three ways a LUT can be configured

Answers

- List the primary slice features
  - Look-up tables and function generators (two per slice, eight per CLB)
  - Registers (two per slice, eight per CLB)
  - Dedicated multiplexers (MUXF5, MUXF6, MUXF7, MUXF8)
  - Carry logic
  - MULT_AND gate
- List the three ways a LUT can be configured
  - Combinatorial logic
  - Shift register (SRL16CE)
  - Distributed memory

Summary

- Slices contain LUTs, registers, and carry logic
  - LUTs are connected with dedicated multiplexers and carry logic
  - LUTs can be configured as shift registers or memory
- IOBs contain DDR registers
- SelectIO™ standards and DCI enable direct connection to multiple I/O standards while reducing component count
- Virtex™-II memory resources include the following:
  - Distributed SelectRAM™ resources and distributed SelectROM (uses CLB LUTs)
  - 18-kb block SelectRAM resources

Summary

- The Virtex™-II devices contain dedicated 18x18 multipliers next to each block SelectRAM™ resource
- Digital clock managers provide the following:
  - Delay-Locked Loop (DLL)
  - Digital Frequency Synthesizer (DFS)
  - Digital Phase Shifter (DPS)

Where Can I Learn More?

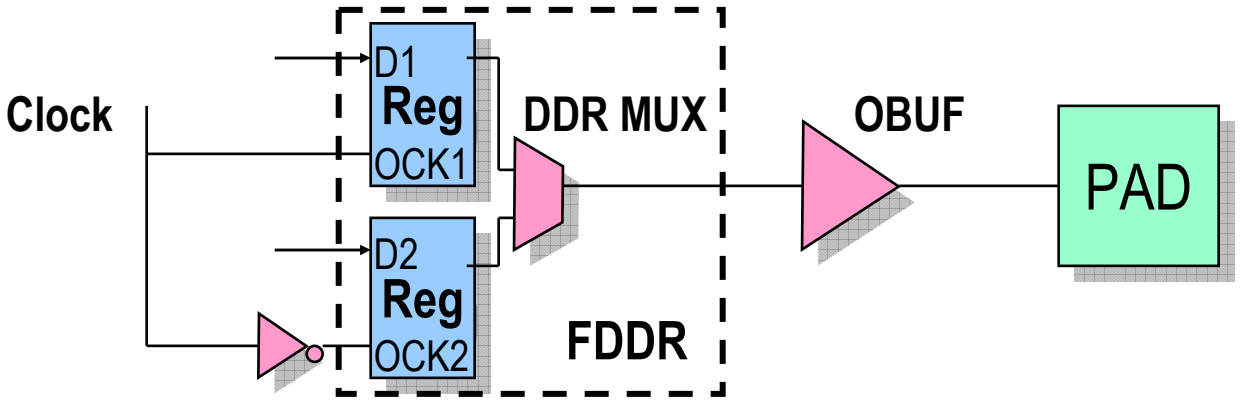
- User Guides
  - www.xilinx.com → Documentation → User Guides
- Application Notes
  - www.xilinx.com → Documentation → Application Notes
- Education resources
  - *Designing with the Virtex-4 Family* course
  - *Spartan-3E Architecture* free Recorded e-Learning

Outline

- Overview
- Slice Resources
- I/O Resources
- Memory and Clocking
- Spartan-3, Spartan-3E, and Virtex-II Pro Features
- Virtex-4 Features
- Summary
- **Appendix**

Double Data Rate Registers

- DDR registers can be clocked
  - By Clock and NOT(Clock) if the duty cycle is 50/50
  - By the CLK0 and CLK180 outputs of a DCM



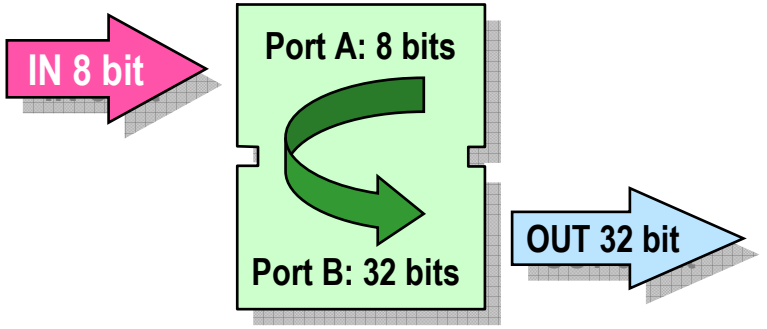
- If D1 = “1” and D2 = “0”, the output is a copy of Clock
  - Use this technique to generate a clock output that is synchronized to DDR output data

Dual-Port Block RAM Configurations

- Configurations available on each port

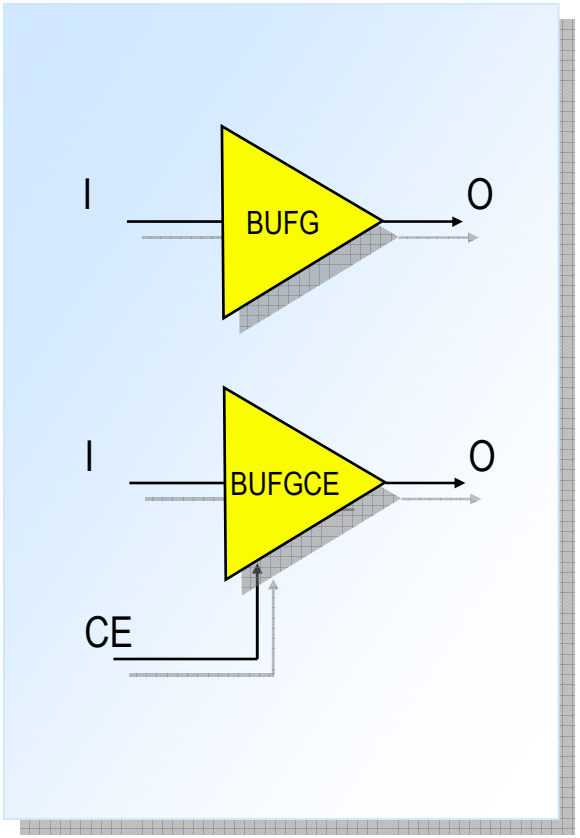
Configuration	Depth	Data Bits	Parity Bits
16k x 1	16 kb	1	0
8k x 2	8 kb	2	0
4k x 4	4 kb	4	0
2k x 9	2 kb	8	1
1k x 18	1 kb	16	2
512 x 36	512	32	4

- Independent configurations on ports A and B
  - Supports data-width conversion, including parity bits



Clock Buffer Configurations

- Clock buffer (BUFG)
  - Low-skew clock distribution
- Clock enable buffer (BUFGCE)
  - Holds the clock output Low when Clock Enable (CE) is inactive
  - CE can be active-High or active-Low
  - Changes in CE are only recognized when the clock input is Low to avoid glitches and short clock pulses



Clock Buffer Configurations

- Clock multiplexer (BUFGMUX)
  - Switches from one clock to another, glitch-free
  - After a change on S, the BUFGMUX waits for the currently selected clock input to go Low
  - The output is held Low until the newly selected clock goes Low, then switches