ChipScope Pro Analyzer

XILINX®

Objectives

After completing this module, you will be able to:

- Describe the value of the ChipScope™ Pro analyzer
- Describe how the ChipScope Pro analyzer works
- List what cores are available
- Use the Core Generator and Core Inserter software
- Plan for and perform debugging with the ChipScope Pro analyzer

Outline

- **Importance of Debug**
- ChipScope Pro Analyzer Cores
- Design Flows
- Summary

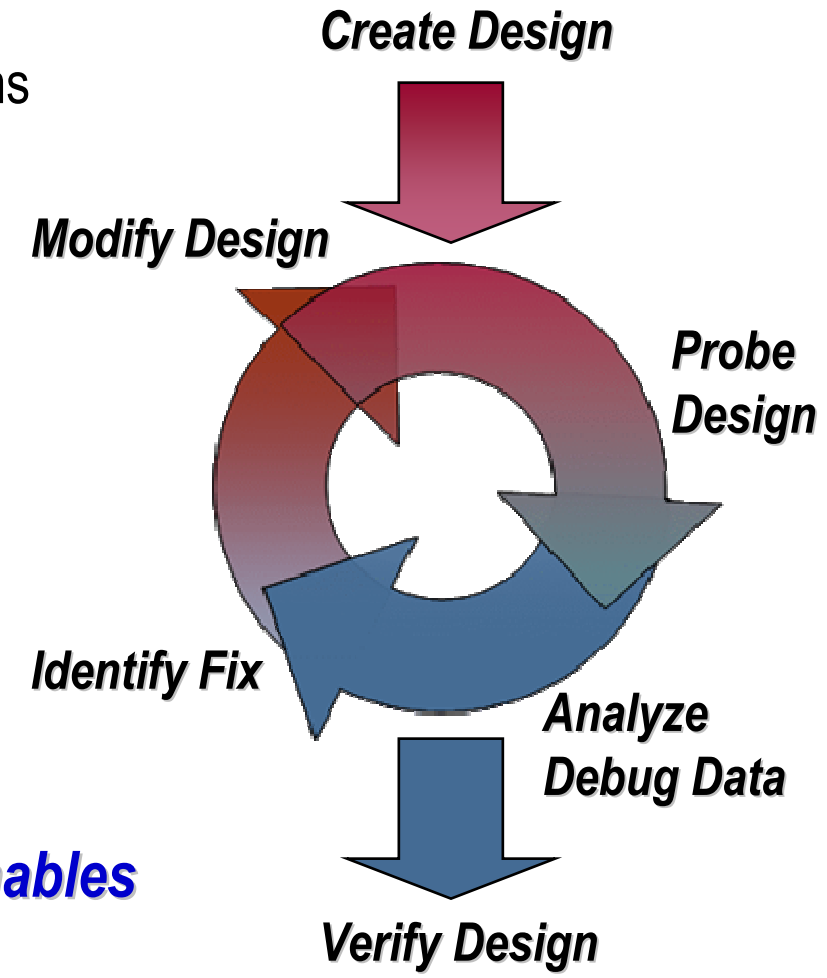
What Engineers are Saying

- FPGA designs are getting more complex
  - Designs are getting faster
  - Design times are getting shorter
- Debug and verification is more challenging
  - Debug and verification consume a significant portion* of FPGA design time
  - Debug and verification need to be easier and integrated into the FPGA design flow

*An FPGA design survey conducted by Xilinx indicates that FPGA debug and verification accounts for nearly half of FPGA design time

Logic of Debug

- Engineers are trained to solve problems
- Debug is problem solving
  - Break a problem into basic parts
  - Remove or reduce variables and variation
  - Predict and verify
- Debug is an iterative process
- Verification is a component of debug
  - Confirming no problems remain

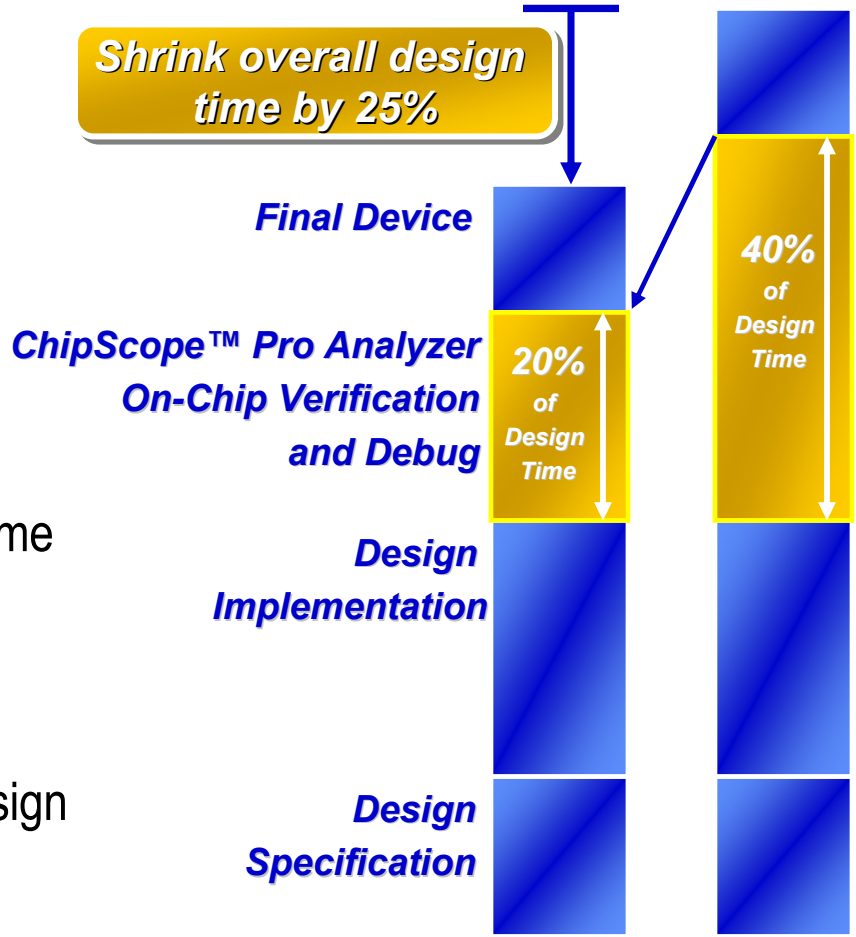


Reconfigurable nature of FPGAs enables an iterative debug process

Xilinx ChipScope Pro Analyzer

Dramatically Shortens Debug and Verification

- Works the way you solve problems
  - Breaks a problem into basic parts
  - Removes variation introduced by external debug solutions
  - Enables a very fast, iterative process of prediction and verification
- Provides what you have requested
  - Reduction of debug and verification time
  - A powerful tool that is easy to use
  - Focus on solving the problem, not on learning the tool
  - Integrated part of the Xilinx FPGA design flow



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- **ChipScope Pro Analyzer Cores**
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What is the ChipScope Pro Analyzer?

- Tailored debug and verification cores
- Efficient core generation and insertion tools
- Total control via JTAG

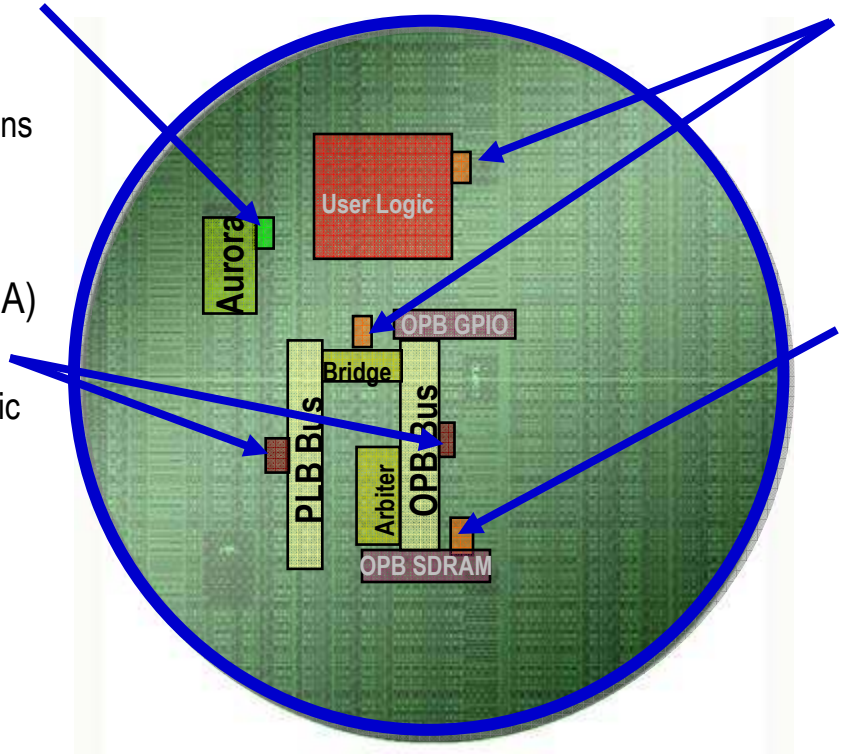
Multiple Debug Cores to Address Different Debug Challenges

Virtual Input/Output (VIO) Core

- Virtual inputs and outputs
- Stimulate logic with pulse trains

Integrated Bus Analysis (IBA) Core

- PLB-specific and OPB-specific bus analysis cores
- Protocol detection
- Debug and verify control, address, and data buses



Integrated Logic Analysis (ILA) Core

- Access internal nodes and signals
- Debug and verify signal behavior
- Define detailed trigger conditions

Agilent Trace Core 2 (ATC2)

- Agilent-created core enabling on-chip debug of Xilinx FPGAs via Agilent FPGA Dynamic Probing

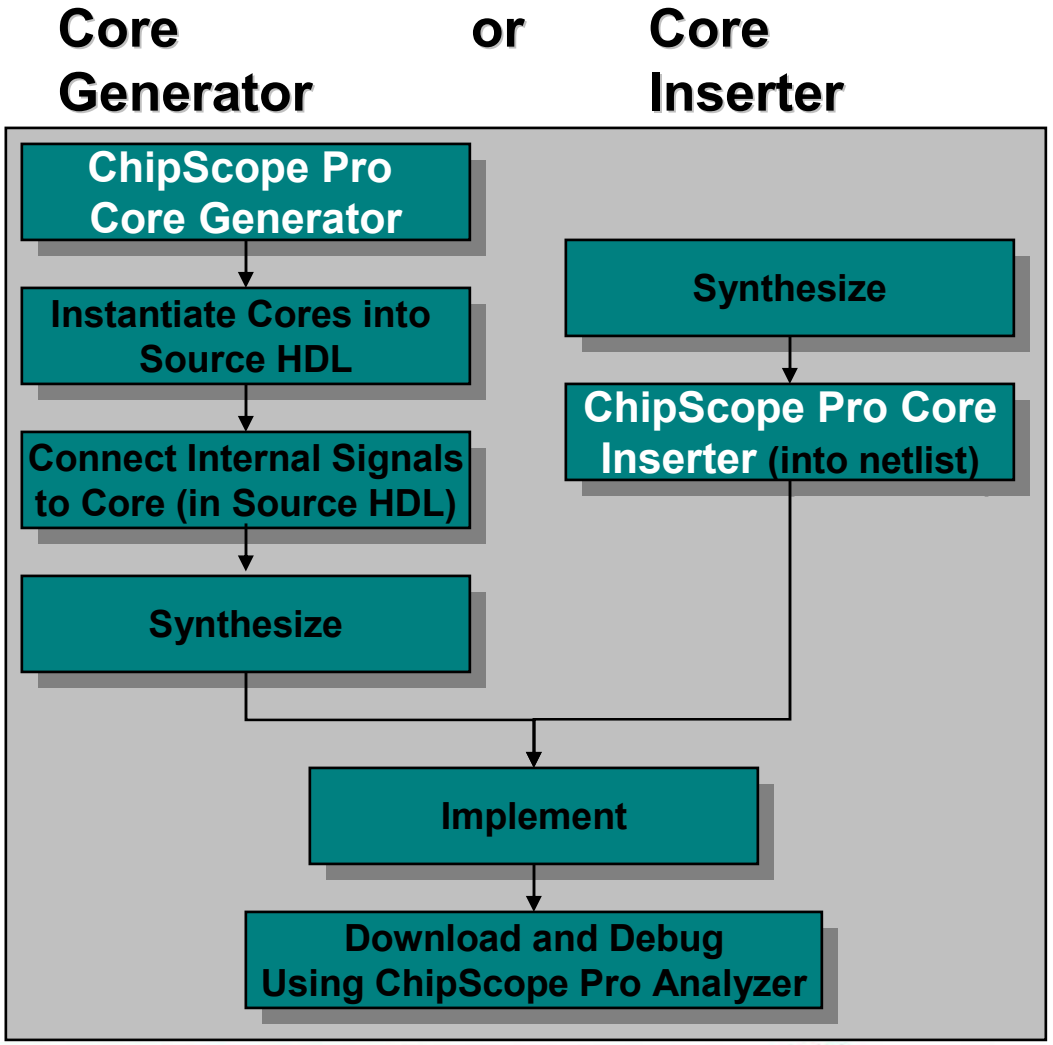
View cores as “virtual test headers” placed anywhere in the design

Core Resources

- ChipScope™ Pro analyzer cores utilize FPGA resources
  - For what?
    - Block RAM: trigger and data storage
    - Slice logic: trigger comparisons
- You must leave room for the ChipScope Pro analyzer cores in the FPGA
  - This may require using a larger part in the same package as you will use in production
- ChipScope Pro analyzer 9.2i includes a built-in resource estimator

Using ChipScope Pro Analyzer

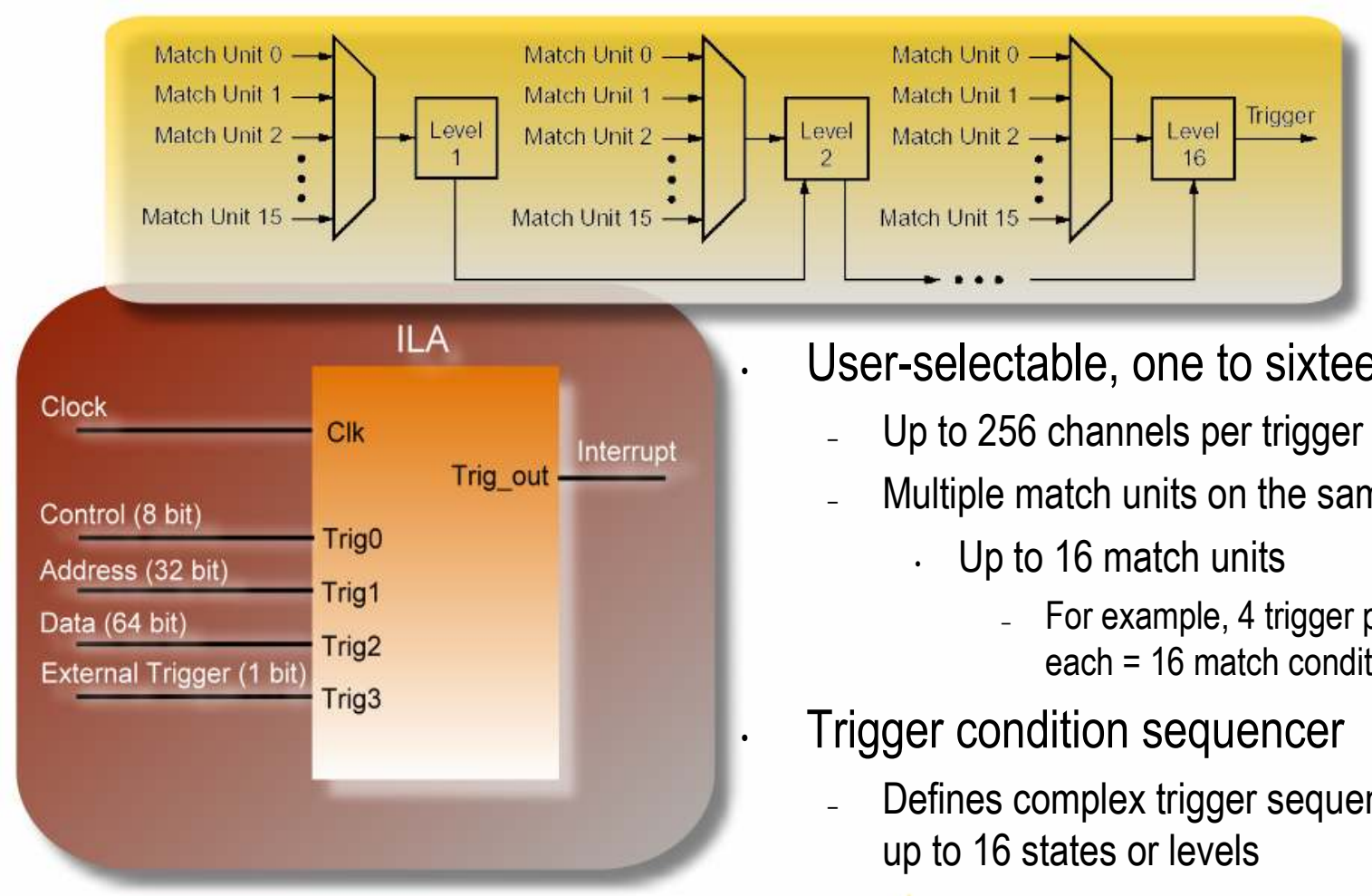
- Place ChipScope™ Pro analyzer cores into the design
  - Attach internal nodes for viewing to the ChipScope Pro analyzer core
  - Generate the ChipScope Pro analyzer cores by using the ChipScope Pro analyzer Core Generator or Core Inserter tools
- Place and route the design with the Xilinx ISE™ implementation software tools
- Download the bitstream to the device under test and analyze the design with the ChipScope Pro analyzer software



ChipScope Pro Analyzer ICON Core

- ICON (Integrated Control) core: This core controls up to 15 capture cores
  - The ICON core interfaces between the JTAG interface and the capture cores
- Capture cores: customizable cores for creating triggers and data storage
  - Customizable number, width, and storage of trigger ports
    - ILA (Integrated Logic Analyzer) core: capture core for HDL designs
    - ILA/ATC (Integrated Logic Analyzer with Agilent Trace) core: similar to the ILA core, except data is captured off-chip by the Agilent Trace Port Analyzer
    - IBA/OPB (Integrated Bus Analyzer for CoreConnect On-Chip Peripheral Bus) core: capture core for debugging CoreConnect OPB buses
    - IBA/PLB (Integrated Bus Analyzer for CoreConnect Processor Local Bus) core: similar to the IBA/OPB core, except for the PLB bus
    - VIO (Virtual Input/Output) core: define and generate virtual I/O ports

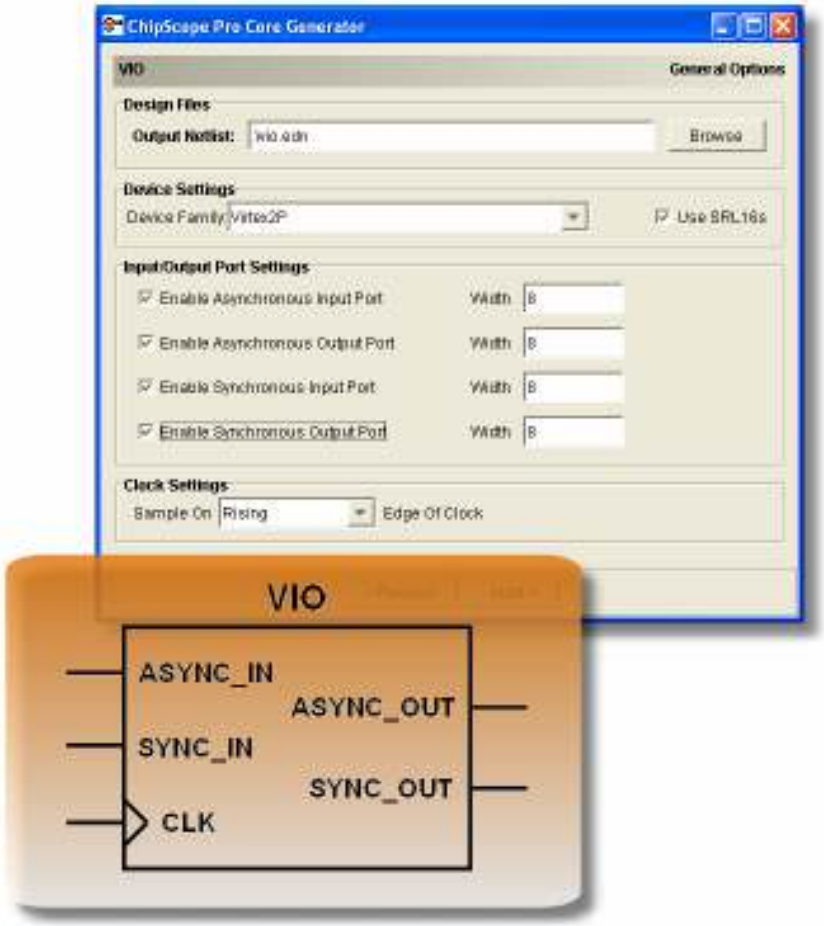
ChipScope Pro Analyzer ILA Core



- User-selectable, one to sixteen trigger ports
  - Up to 256 channels per trigger port
  - Multiple match units on the same trigger port
    - Up to 16 match units
      - For example, 4 trigger ports, 4 match units each = 16 match conditions
- Trigger condition sequencer
  - Defines complex trigger sequences that include up to 16 states or levels

ChipScope Pro Analyzer VIO Core

- Insert virtual pins into your design
  - Input or output
  - Synchronous or asynchronous
    - System clock or JTAG clock
  - Up to 256 bits each
- Inputs are virtual LEDs
  - Different refresh rates are available
- Outputs are virtual DIP switches
  - Force value or pulse train into the FPGA



Things to Know About VIO Cores

- Can only be added with the ChipScope™ Pro analyzer Core Generator tool
- Uses no block RAM, only logic
- Inputs are like LEDs, for examining signals
- Outputs are switches or pushbuttons, for driving signals

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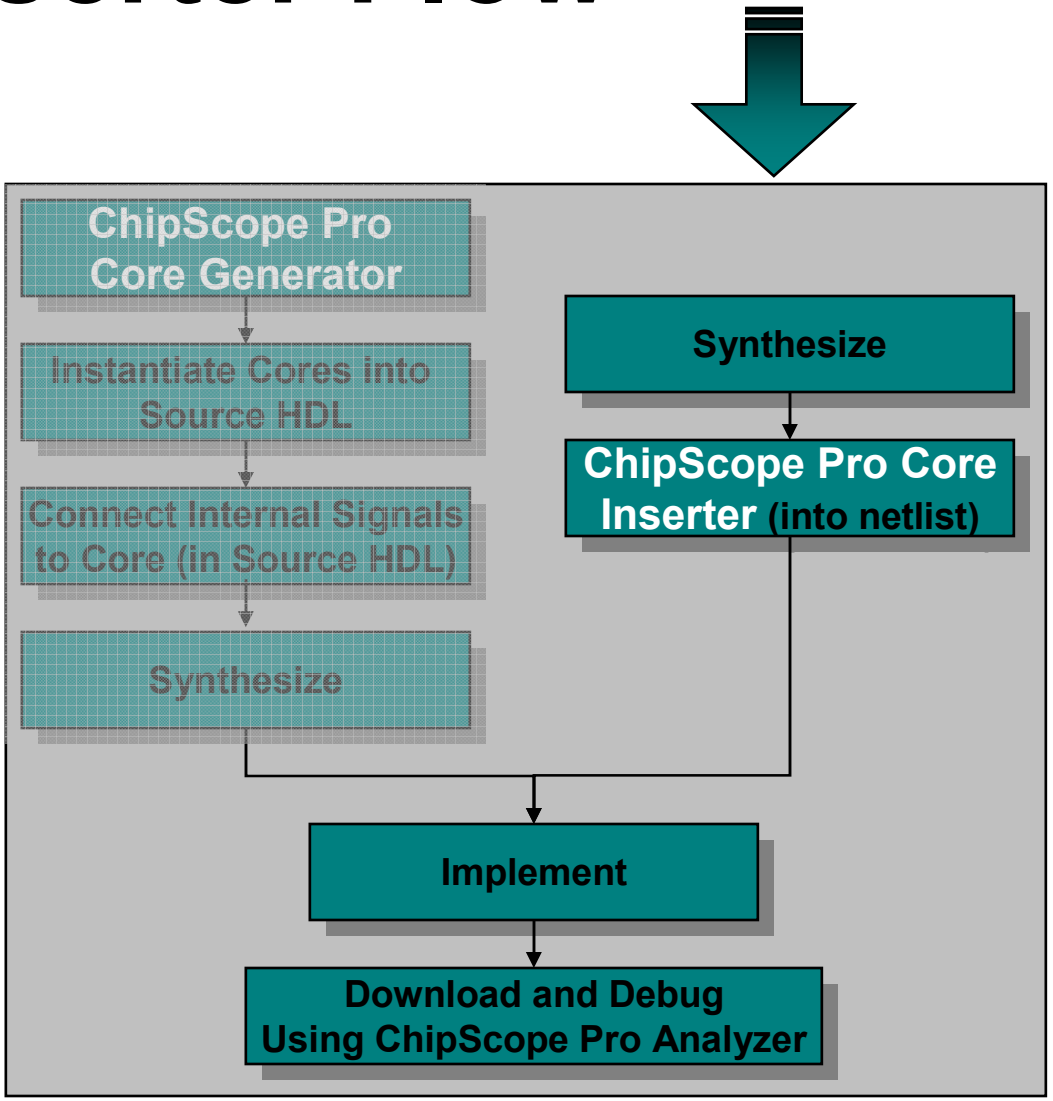
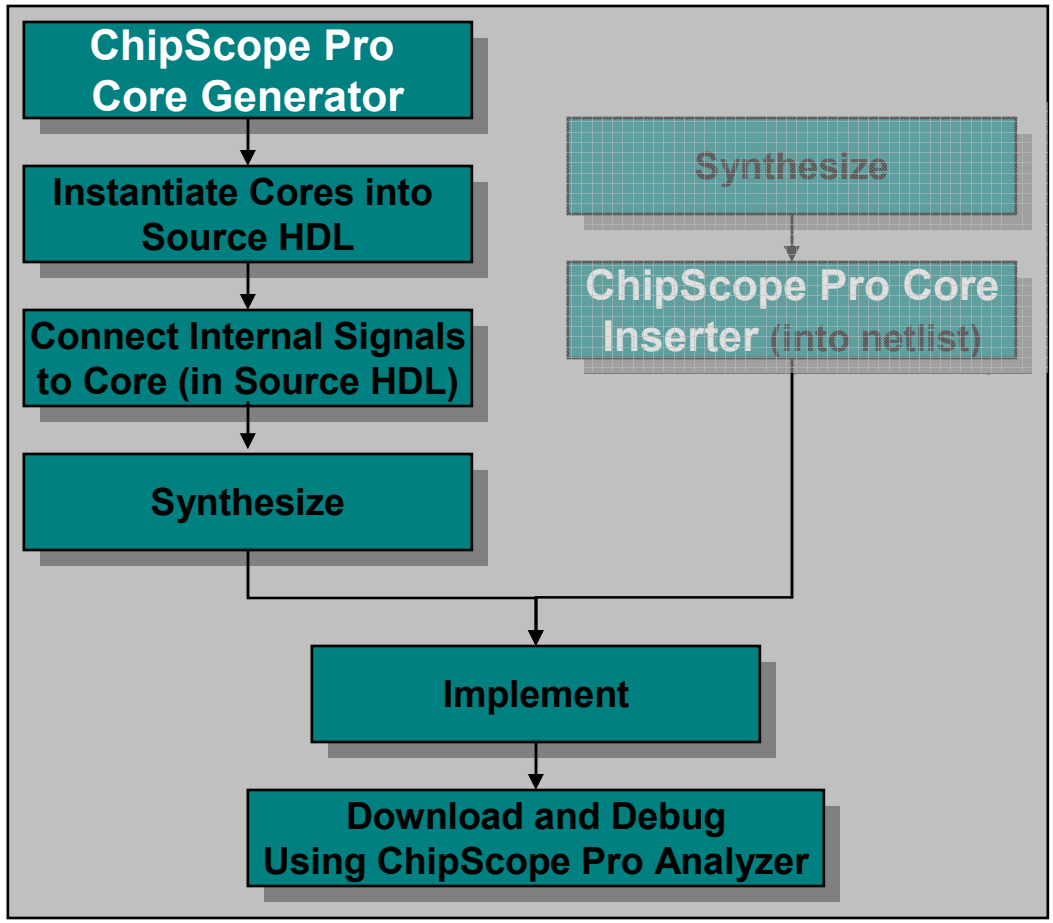
Core Inserter Flow

- Core Inserter inserts cores directly into the netlist
  - HDL code is untouched
  - Only post-synthesis nodes are available
  - Bypass this tool to remove cores
  - Inserter must perform the first portion of translate
  - Core generation and insertion are done together
  - ChipScope™ Pro analyzer Core Inserter is run from within Project Navigator



Core Generator Flow

- Generate cores that are instantiated directly into the HDL
  - Allows access to all HDL nodes
  - Requires changes to the code
  - Must comment out cores to remove them
  - Uses standard implementation flow
  - Core generation and insertion done separately



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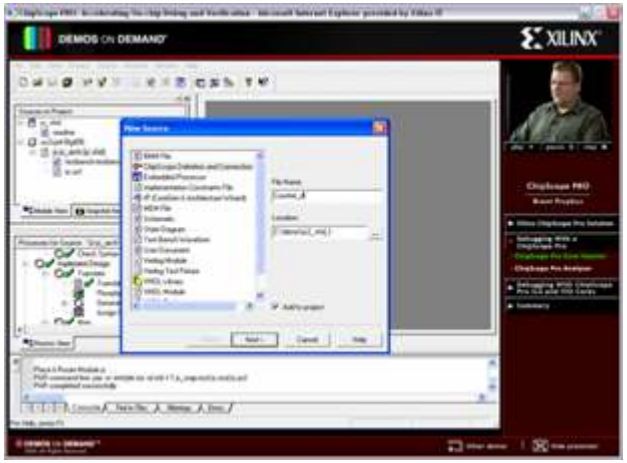
Summary

- Shorten debug time by up to 50 percent
  - Break the problem into manageable parts
  - ChipScope™ Pro analyzer enables rapid iteration
- Add ChipScope Pro analyzer cores at any time
  - Debug in three simple steps
- Specialized cores allow you to focus on solving problems
  - ILA for viewing results
  - VIO for driving changes
- Minimal impact to FPGA design
  - Design at system speed
  - Optimized cores consume minimal FPGA resources

Where Can I Learn More?

- Visit www.xilinx.com/chipscopepro
  - View recorded ChipScope™ Pro analyzer product demos
  - Access a 60-day free evaluation version of ChipScope Pro analyzer tools
  - Access ChipScope Pro analyzer documentation
    - User guide
    - At-a-glance summary of features
  - Obtain information on Agilent FPGA Dynamic Probe technology
    - Combine on-chip debug with the power of a logic analyzer



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