ChipScope Pro Debug lab

Targeting Spartan-3E Starter Kit

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ChipScope Pro Debug Lab

Introduction

This lab guides you through the process of inserting an ICON/ILA core into a design to perform on-chip verification using ChipScope Pro analyzer.

Objectives

After completing this lab, you will be able to:

- Insert ChipScope Definition and Connection (CDC) file to the project
- Add ILA Core and Customize it
- Implement and debug the design

Procedure

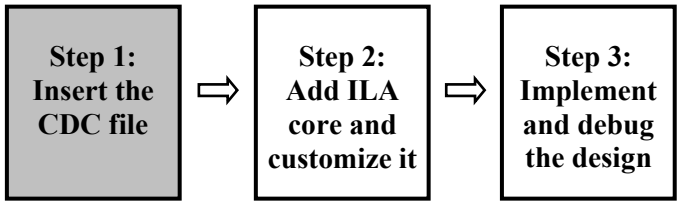
This demonstration comprises three primary steps:

1. Insert the CDC file,
2. Add ILA core and customize it,
3. Implement and debug the design.

Below each general instruction for a given procedure, you will find accompanying step-by-step directions and illustrated figures that provide more detail for performing the general instruction. If you feel confident about a specific instruction, feel free to skip the step-by-step directions and move on to the next general instruction in the procedure.

Insert the CDC file Step 1

General Flow for this lab:



Open the csp.ise project from the directory c:\xup\fpgaflow\labs\lab2.

1. If you have closed the ISE™ Project Navigator, select **Start → Programs → Xilinx Design Suite 10.1i → ISE → Project Navigator**
2. Select **File → Open Project** in the Project Navigator
3. Browse to the location **c:\xup\fpgaflow\labs\lab2** and open **csp.ise** project.

Insert ChipScope Definition and Connection File to the project.

1. In the Processes for Source window, double-click on **Create New Source**

   If you do not see the Create New Source process, ensure that an HDL source file is selected in the Sources in Project window.
2. In the New Source window, select **ChipScope Definition and Connection File** and enter ***debug*** as the file name
3. Click **Next**
4. **Associate Source** window appears, select **addr_mem** module and click Next.
5. New Source Wizard – Summary window appears. Verify the summary and click Finish.
6. debug.cdc file gets added to the project as shown in the figure 1.1.

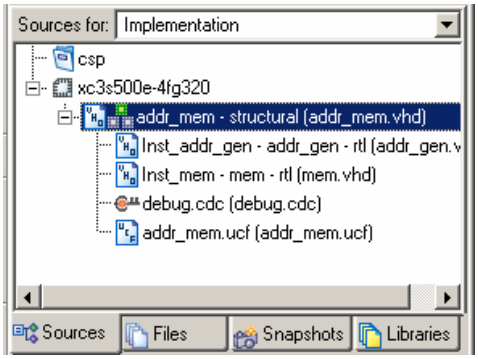
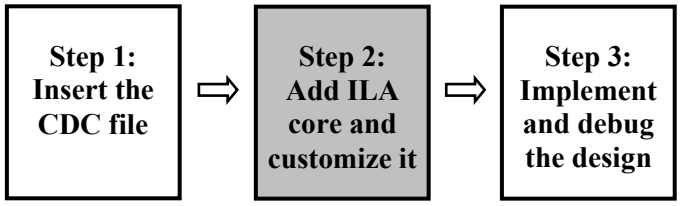


Figure 1.1 - Sources window

Add ILA core and customize it Step 2

General Flow for this lab:



Invoke the ChipScope Pro Inserter and add ILA core and connect the trigger port of ILA core to **addr** signal and data port of ILA core to **mem_data** signal.

❶ In the Sources for Project window double click on debug.cdc file to open the ChipScope Pro inserter.

❷ After completing the synthesis run, ChipScope Pro Inserter GUI opens as shown in Figure 2.1.

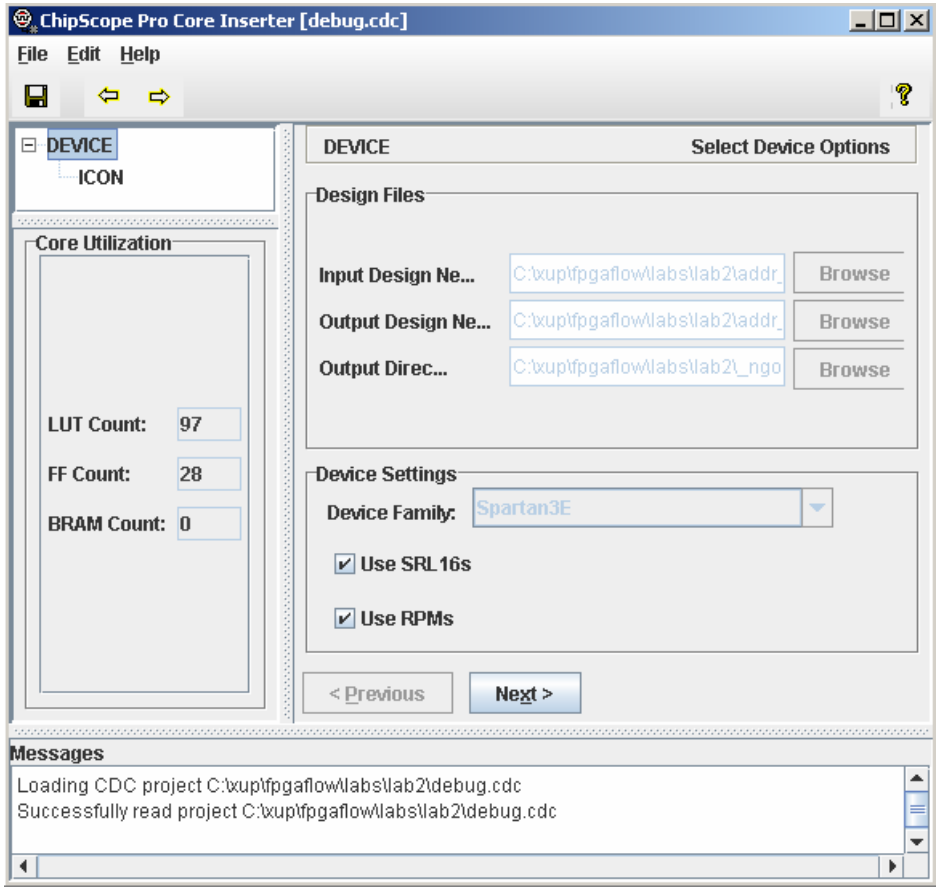


Figure 2.1 – ChipScope Pro Inserter GUI

❸ Click Next.

❹ Select **New ILA Unit. U0:ILA** gets added DEVICE window.

❺ Select **U0:ILA** in the DEVICE window to customize the ILA (Integrated Logic Analyzer) options (Figure 2.2).

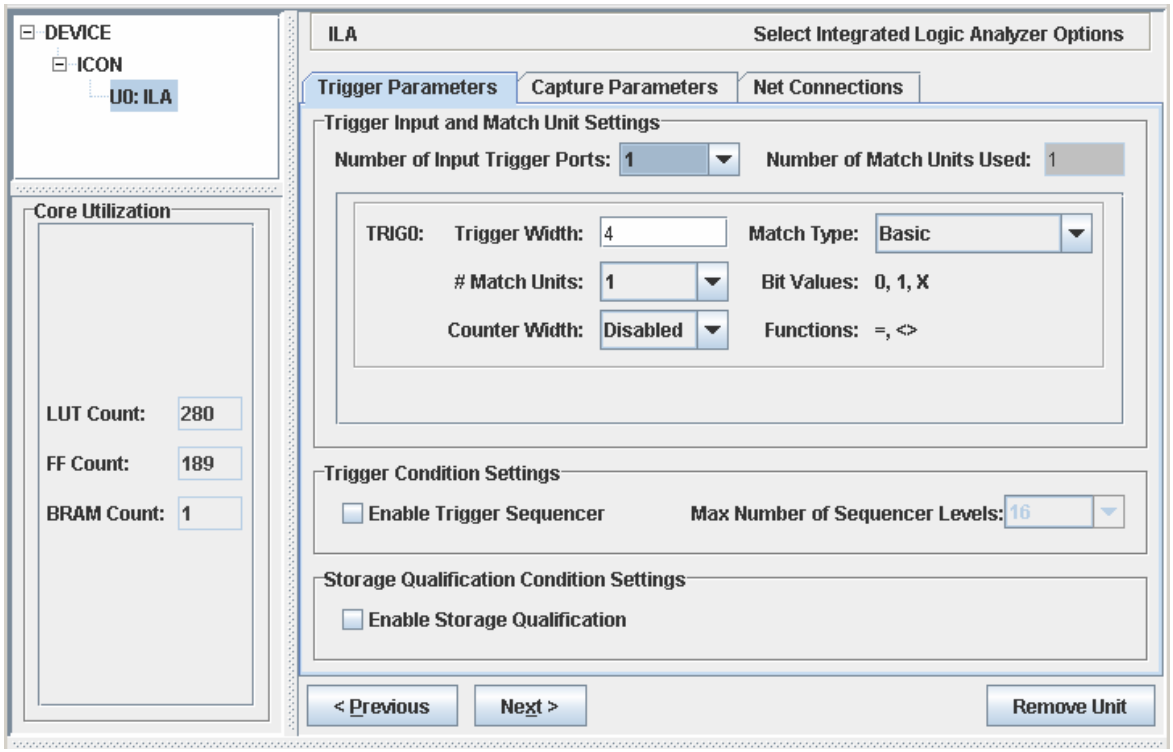


Figure 2.2 – ChipScope Pro Integrated Logic Analyzer (ILA) core Trigger Parameters.

❻ Customizing the ILA core includes three steps – customizing the Trigger Parameters, Capture Parameters and Net Connections.

❼ In the **Trigger Parameters** tab, enter the below mentioned values for the options.

- Trigger Width: 4
- Match Units: 1
- Counter Width: Disabled
- Match Type: Basic
- Trigger Sequencer: Unchecked
- Storage Qualification: Unchecked

❽ Now select the **Capture Parameters** tab and enter below mentioned values for the options (figure 2.3).

- Data Same as Trigger: Unchecked
- Data Width: 8
- Data Depth: 512
- Sample On: Rising Clock Edge

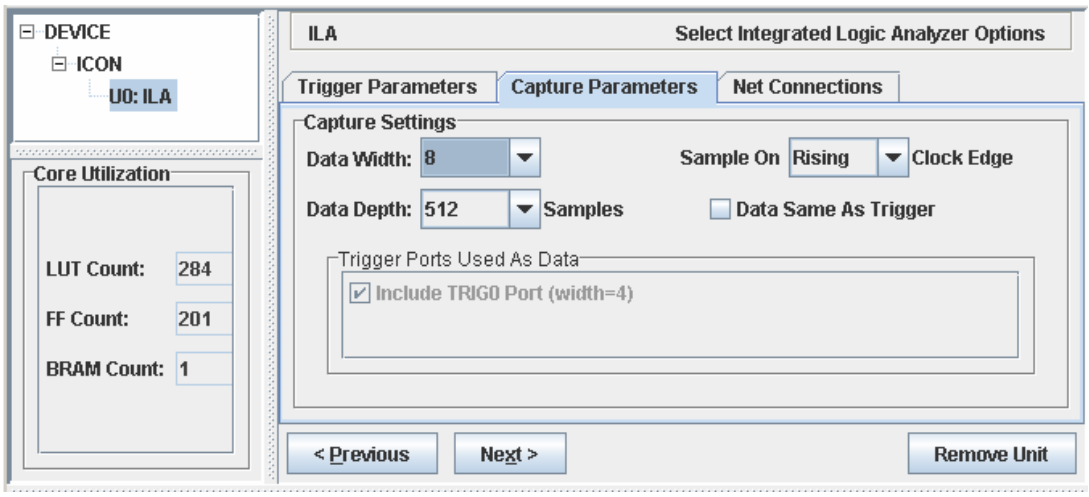


Figure 2.3 – ChipScope Pro ILA Core Capture Parameters

❾ Now select **Net Connections** tab. In this tab clock net, trigger nets and data nets needs to be connected to ILA core.

❿ In the Net Connections tab, click on **Modify connections** to make clock, trigger and data net connections.

❶ Select Net window appears (Figure 2.4).

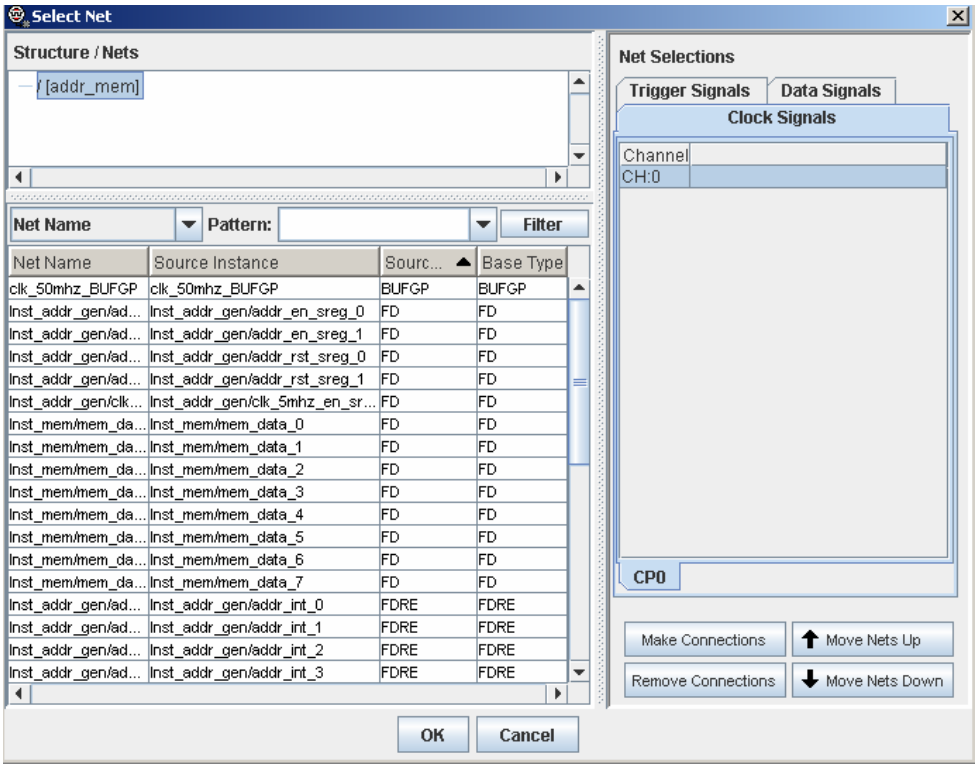


Figure 2.4 – Select Net window – Clock Signals tab

❷ In the Select Net window, select the **clock signals tab** in the Net selections window.

❸ Select the **clk_50mhz_bufgp** net and click on **Make Connections** option to connect this net as a clock input to ILA core. The *Remove connections* option can remove

a net connection. Move Net Up/Down options can be used move the net connections if you have multiple nets.

❹ After making the clock signal connection, select the **Trigger Signals** tab. Similar to connecting the clock net signal, connect the nets **Inst_addr_gen/addr_int<0>** to **Inst_addr_gen/addr_int<3>** as the trigger signals (figure 2.5).

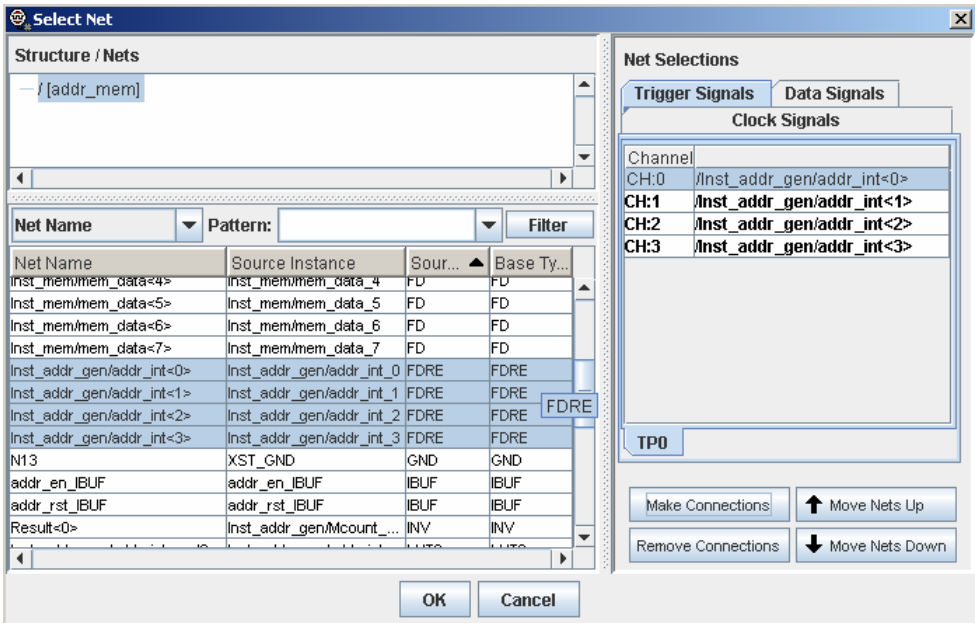


Figure 2.5 – Set Net window – Trigger Signals connection

❺ Now select the Data Signals tab. connect the nets **Inst_mem/mem_data<0>** to **Inst_mem/mem_data<7>** as the Data Signals (figure 2.6).

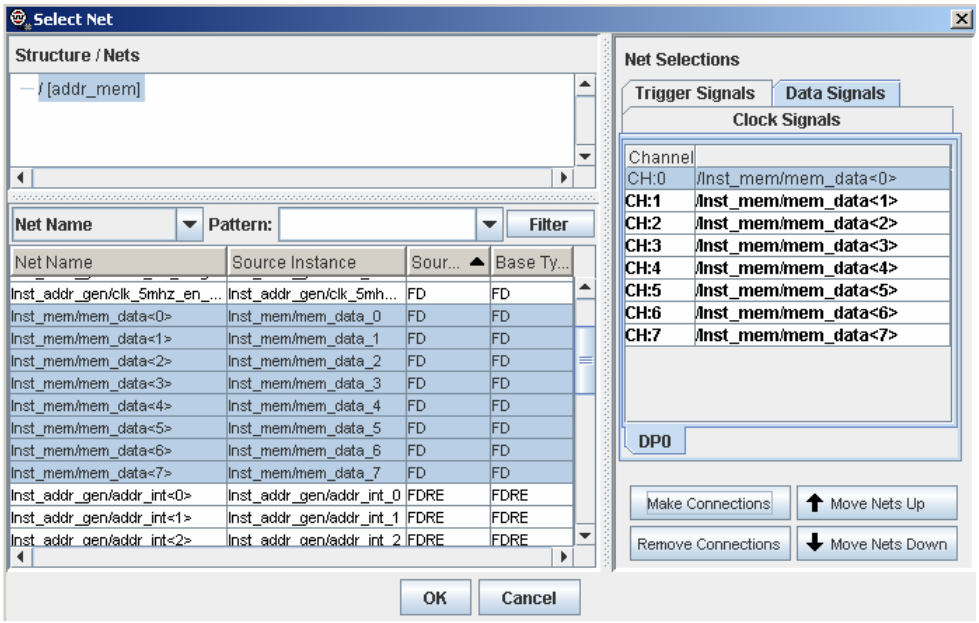
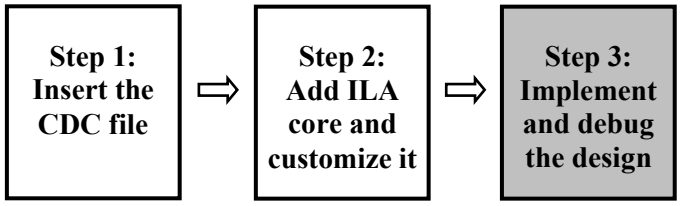


Figure 2.6 – Select Net window – Data Signals connection

❻ After making the clock, trigger and data signals connection, click OK to close the Select Net window. In the CSP Core Inserter window, select **Return to Project Navigator.** Save Project prompt appears, Select YES.

Implement and Debug the Design Step 3

General Flow for this lab:



Launch the ChipScope Pro analyzer and configure the FPGA.

1. In the Project Navigator *sources for project* window select *addr_mem* top module and in the *processes* window double click on the **Analyze Design Using ChipScope.**
2. After successful completion of Design Implementation and Program file generation, ChipScope Pro analyzer window appears.
3. Connect the Spartan 3E Starter kit to the power and connect the USB programming cable between the computer and the board. Then Power up the board. If you are using the board for the first time, maximum of 3 windows will pop up one after the other for Xilinx USB Cable Driver installation. Select automatic installation. Once the installation is complete the USB programming interface is ready for use.
4. In the ChipScope pr Analyzer window, click on **Open Cable/Search for Cable** option.

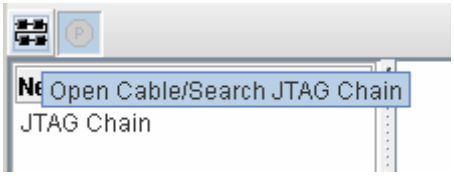


Figure 3.1 - Establish JTAG Connection

5. Spartan-3E board contains three devices in the JTAG chain: XC3S500E, XCF04S and XC2C64A Coolrunner CPLD. These devices will be detected along with Instruction Register (IR) Lengths and Device ID Codes.
6. Click OK. These three devices get added to JTAG Chain list. In the JTAG Chain List, right click XC3S500E device and select configure (Figure 3.2).

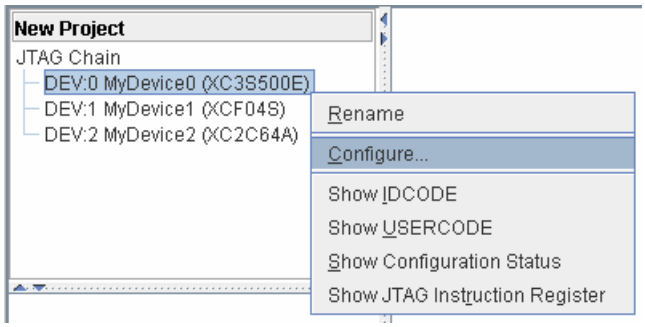


Figure 3.2 – Configure FPGA option

❼ *JTAG Configuration* window appears, click on **Select New File** and browse to c:\xup\fpgaflow\labs\lab2 and select **addr_mem.bit** and click Open. Then click OK to configure the FPGA with the bitstream.

❽ Once the configuration is complete, CSP analyzer will detect the ILA Core. Trigger setup, Waveform, Listing and Busplot windows gets added under the ILA core. Double click on the **Trigger Setup** and **waveform** windows to open them.

Setup the Trigger options and Capture the data for analysis.

❶ Select **File → Import** option. *Signal Import* window appears. Click on Select *New File* and pen **debug.cdc** file and click OK. Notice that signal names in the wave form window gets changed.

❷ In the waveform window, select all the signals and right click and select **Add to Bus → New Bus** (figure 3.3)**.**

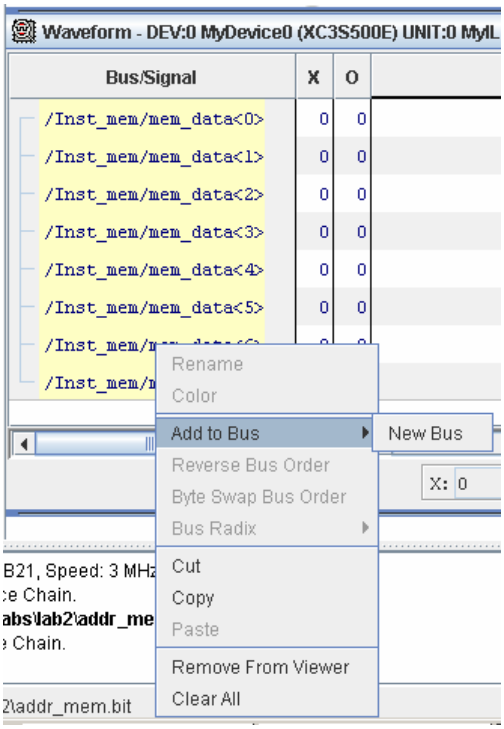


Figure 3.3 – Creating a Bus

❸ In the *Trigger Setup* window **Match Functions** tab select **radix** as **Hex** and enter the **value** as **9** and in the **Capture Settings** tab enter the **Depth** as **64** and **position** as **32.** Leave all other options at default values (figure 3.4).

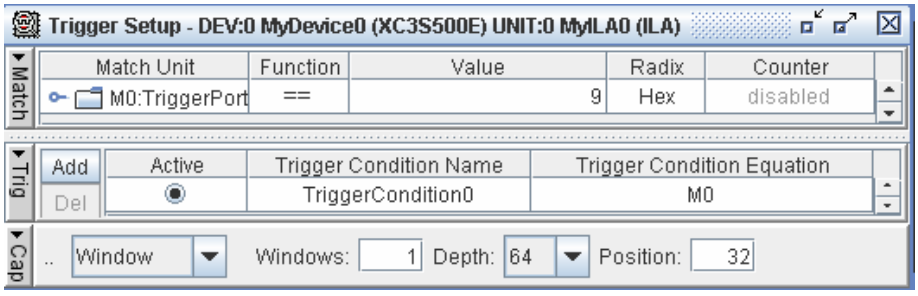


Figure 3.4 - Trigger Setup options

❹ Click on the **Apply Settings and Arm Trigger** option.

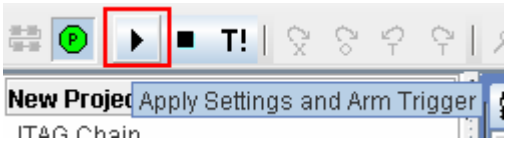


Figure 3.5 – Apply Settings and Arm trigger option

❺ ChipScope Pro Analyzer will show **Waiting for Upload** message. Please make sure that the slide switches SW0 (addr_rst) & SW1 (addr_ce) of Spartan 3E Starter kit are active LOW and active HIGH respectively. When the **addr** bus reaches the value **9** the status of **mem_data** bus will be captured. The status of mem_data bus, 32 sampels before the condition and 32 samples after the condition will be shown in the waveform window (figure 3.6).

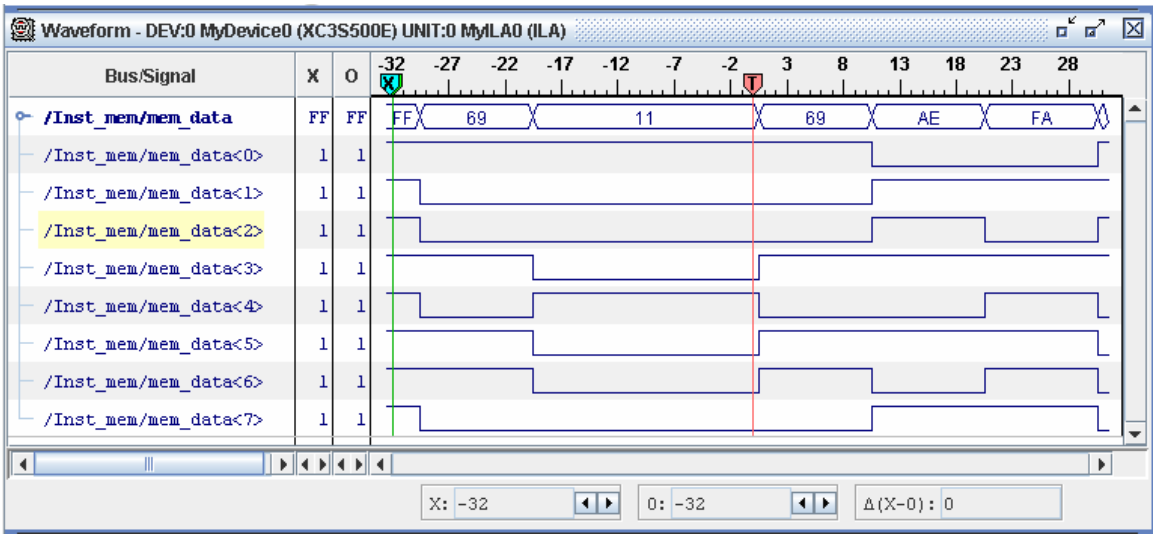


Figure 3.6 – Waveform window sowing the captured data

❻ After analyzing the captured data, select **JTAG Chain → Close Cable** option to close cable connection with the board. Close the ChipScope Pro analyzer.

Conclusion

In this lab, the steps of inserting a CDC File to the project, adding ILA Core and customizing it are demonstrated. You also performed the design implementation and verification of the design ChipScope Pro analyzer.