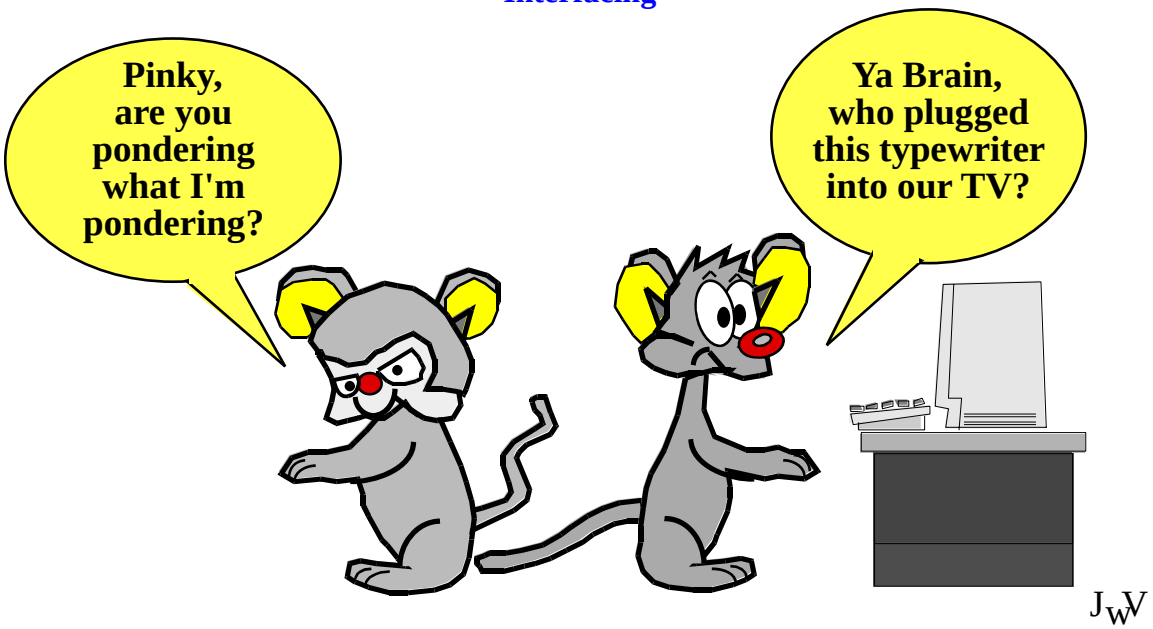
Interfacing



Lab7 • Interface motors to the microcontroller,
- Interface optical and mechanical sensors
- Layered software,
- Design cycle,
- Team work.

V_{OL} is defined as the voltage at maximum I_{OL}

family	example	V_{OL}	I_{OL}
standard TTL	7405	0.4 V	16 mA
Schottky TTL	74S05	0.5 V	20 mA
Low Power Schottky	74LS05	0.5 V	8 mA
High speed CMOS	74HC05	0.33 V	4 mA
high voltage TTL	7406	0.7 V	40 mA
high voltage TTL	7407	0.7 V	40 mA

Table 8.4. Output parameters for various open collector gates.

Table 34. I/O static characteristics

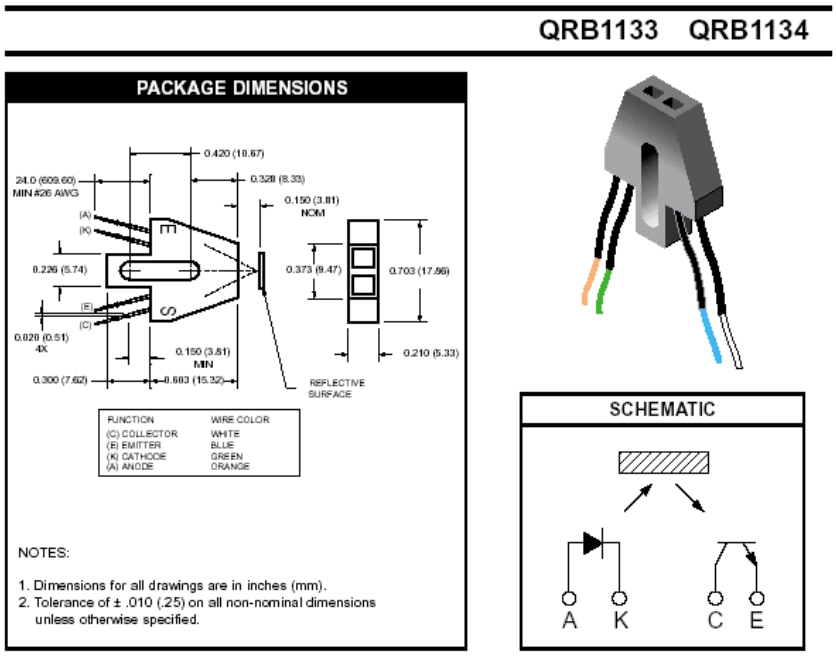
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Input low level voltage	TTL ports	–0.5		0.8	V
V_{IH}	Standard IO input high level voltage		2		V_{DD}+0.5	
	IO FT(1) input high level voltage		2		5.5V	
V_{IL}	Input low level voltage	CMOS ports	–0.5		0.35 V_{DD}	V
V_{IH}	Input high level voltage		0.65 V_{DD}		V_{DD}+0.5	
V_{hys}	Standard IO Schmitt trigger voltage hysteresis(2)		200			mV
	IO FT Schmitt trigger voltage hysteresis(2)		5% V_{DD}(3)			mV
I_{lkg}	Input leakage current (4)	$V_{SS} \le V_{IN} \le V_{DD}$ Standard I/Os			±1	µA
		V_{IN}= 5 V I/O FT			3	
R_{PU}	Weak pull-up equivalent resistor(5)	$V_{IN} = V_{SS}$	30	40	50	kΩ
R_{PD}	Weak pull-down equivalent resistor(5)	$V_{IN} = V_{DD}$	30	40	50	kΩ
C_{IO}	I/O pin capacitance			5		pF

1. FT = Five-volt tolerant.
2. Hysteresis voltage between Schmitt trigger switching levels. Based on characterization, not tested in production.
3. With a minimum of 100 mV.
4. Leakage could be higher than max. if negative current is injected on adjacent pins.
5. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This MOS/NMOS contribution to the series resistance is minimum (~10% order).

Table 35. Output voltage characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}(1)	Output low level voltage for an I/O pin when 8 pins are sunk at same time	TTL port I_{IO} = +8 mA 2.7 V < V_{DD} < 3.6 V		0.4	V
V_{OH}(2)	Output high level voltage for an I/O pin when 8 pins are sourced at same time		V_{DD}–0.4		
V_{OL} (1)	Output low level voltage for an I/O pin when 8 pins are sunk at same time	CMOS port I_{IO} =+ 8mA 2.7 V < V_{DD} < 3.6 V		0.4	V
V_{OH} (2)	Output high level voltage for an I/O pin when 8 pins are sourced at same time		2.4		
V_{OL}(1)(3)	Output low level voltage for an I/O pin when 8 pins are sunk at same time	I_{IO} = +20 mA 2.7 V < V_{DD} < 3.6 V		1.3	V
V_{OH}(2)(3)	Output high level voltage for an I/O pin when 8 pins are sourced at same time		V_{DD}–1.3		
V_{OL}(1)(3)	Output low level voltage for an I/O pin when 8 pins are sunk at same time	I_{IO} = +6 mA 2 V < V_{DD} < 2.7 V		0.4	V
V_{OH}(2)(3)	Output high level voltage for an I/O pin when 8 pins are sourced at same time		V_{DD}–0.4		

1. The I_{IO} current sunk by the device must always respect the absolute maximum rating specified in *Table 7* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.
2. The I_{IO} current sourced by the device must always respect the absolute maximum rating specified in *Table 7* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD}.
3. Based on characterization data, not tested in production.



Darlington TIP120 (NPN) TIP125(PNP)

h_{fe} =1000

I_{CE} up to 3A

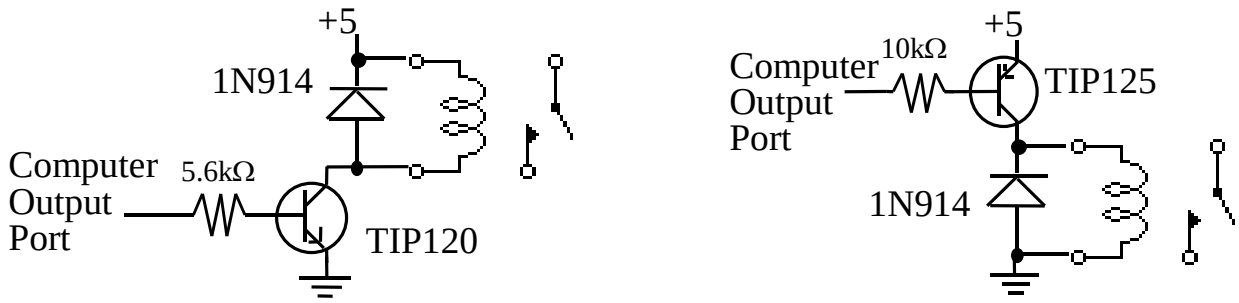


Figure 8.67. Two relay interfaces.

Also can be used to drive DC motor on/off

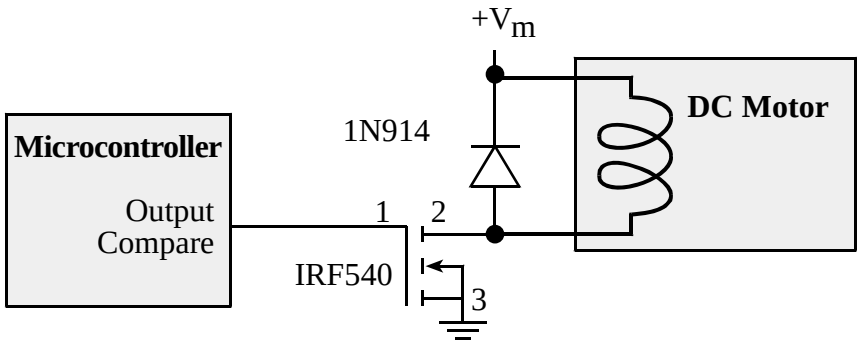


Figure 8.68. Motor interface using a high current MOSFET.

For more current, we can use the IRF540 MOSFET.

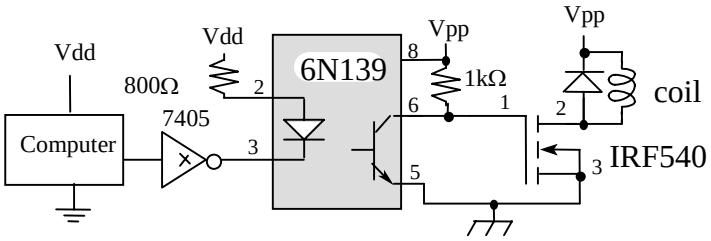


Figure 8.71. Another high-current isolated motor interface using a 6N139 and a MOSFET.

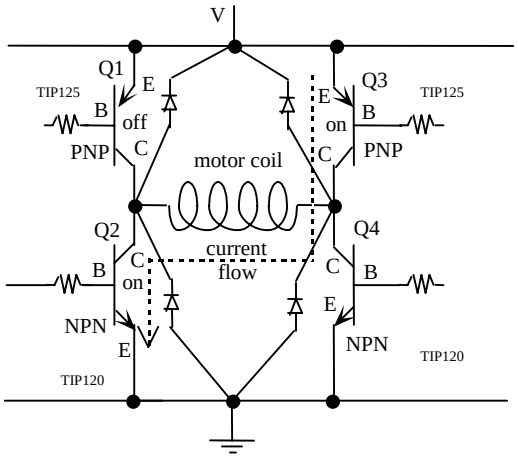
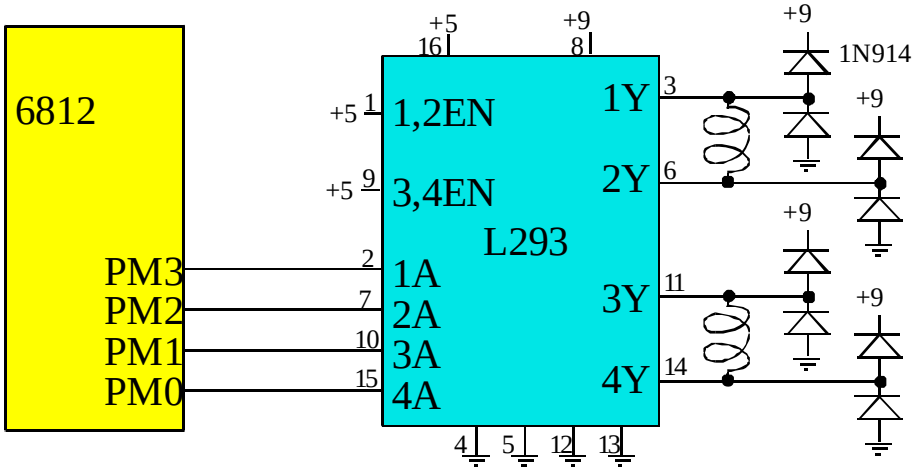


Figure 8.72. An H-bridge is used to drive current in both directions.

Outputs: two 4-wire bipolar stepper motors



Bipolar stepper motor interface using an L293 driver

DC motor interface to drive forward/backward/off