Introduction and Specification

Requirements and Background

The requirements for the final project are to create a resonant converter that is able to

1. Deliver 25 W of DC power
2. Operate at 6.78 MHz
3. Utilize a minimum input of 20V
4. Transmit power wirelessly (1 in)

Our strategy was to utilize existing boards from the labs in EE 365A. In lab 3, we built and analyzed a Class E amplifier, as seen in Figure 1.1. The Class E amplifier operated at 6.78 MHz and was designed for a 5 ohm load.

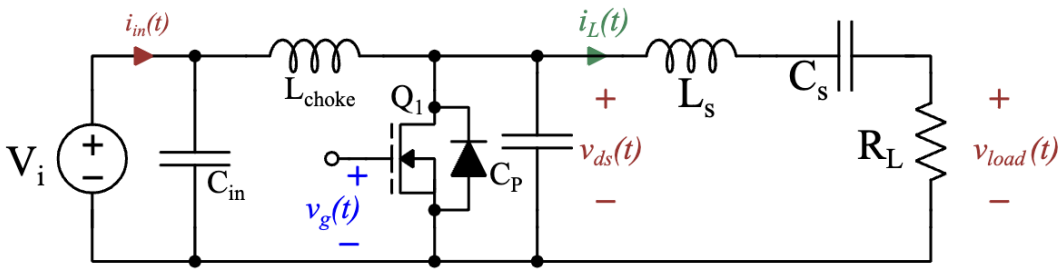

Figure 1.1: Class-E switched mode power amplifier

However, this circuit alone would not meet the requirements of the final project:

1. The output of this amplifier delivers AC power at the fundamental frequency
2. If we were to put 20V in the input, the peak voltage seen across the MOSFET would be Vds = 4*Vi = 80V, and our FET is only rated for 60V
3. We are not transmitting power wirelessly

Design Details

To address the problems discussed above, in order to meet the design requirements, we decided to convert the Class-E power amplifier to a Φ_2 inverter (Fig. 2). The Φ_2 inverter adds a second resonant point, that eliminates the second harmonic from the input.

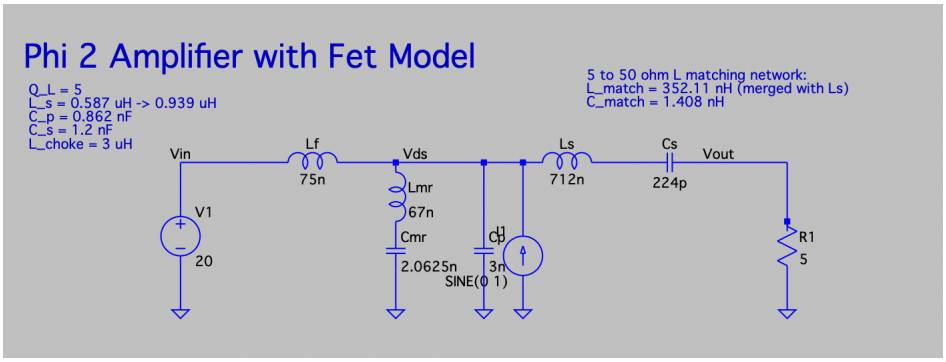

Fig 2. Φ_2 inverter simulation model

Eliminating the second harmonic addresses the concern regarding the voltage limitation given by the MOSFET by decreasing the peak voltage to Vds = 2*Vi = 80V, as seen in Fig 3.

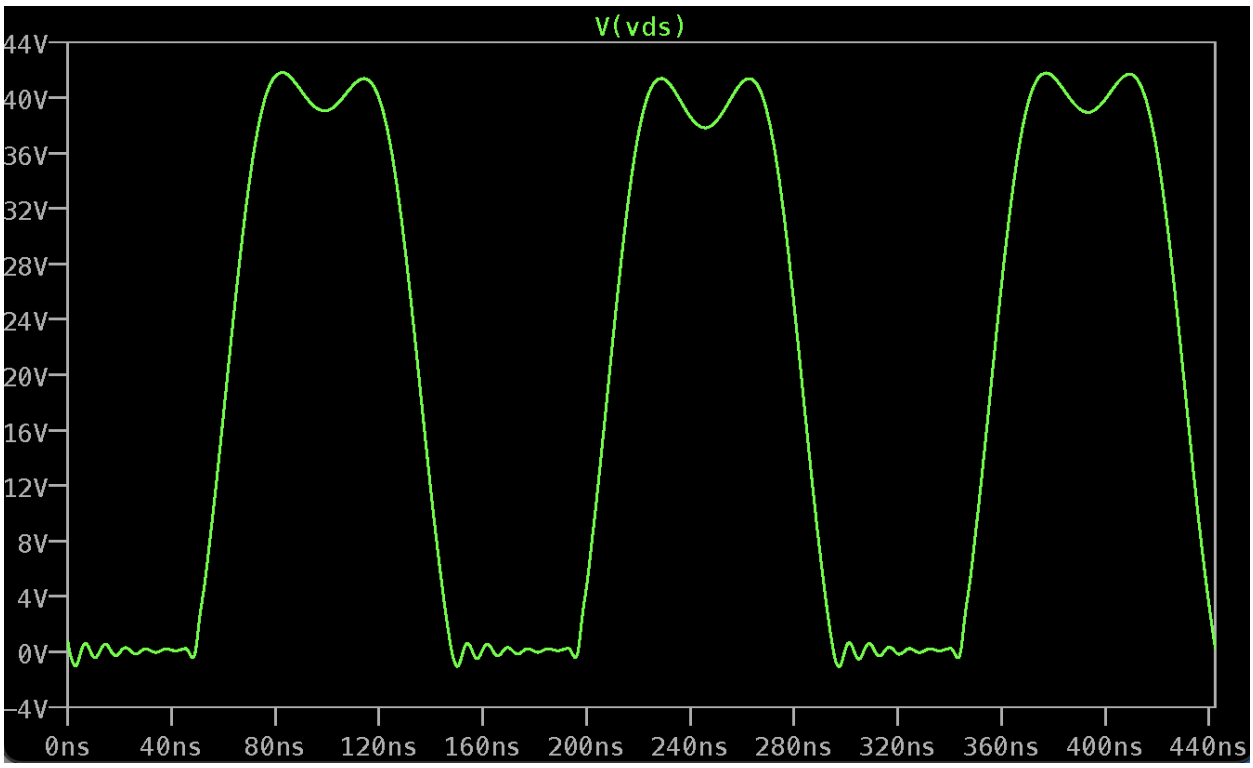

Fig 3. Φ_2 simulated voltage at switching node VDs “Bunny Ears”

Adding the input filter required some tuning to ensure we were zero voltage switching and not amplifying the third harmonic. When inspecting the switching node in our simulation, we paid close attention to the magnitude and phase at our three frequencies of interest.

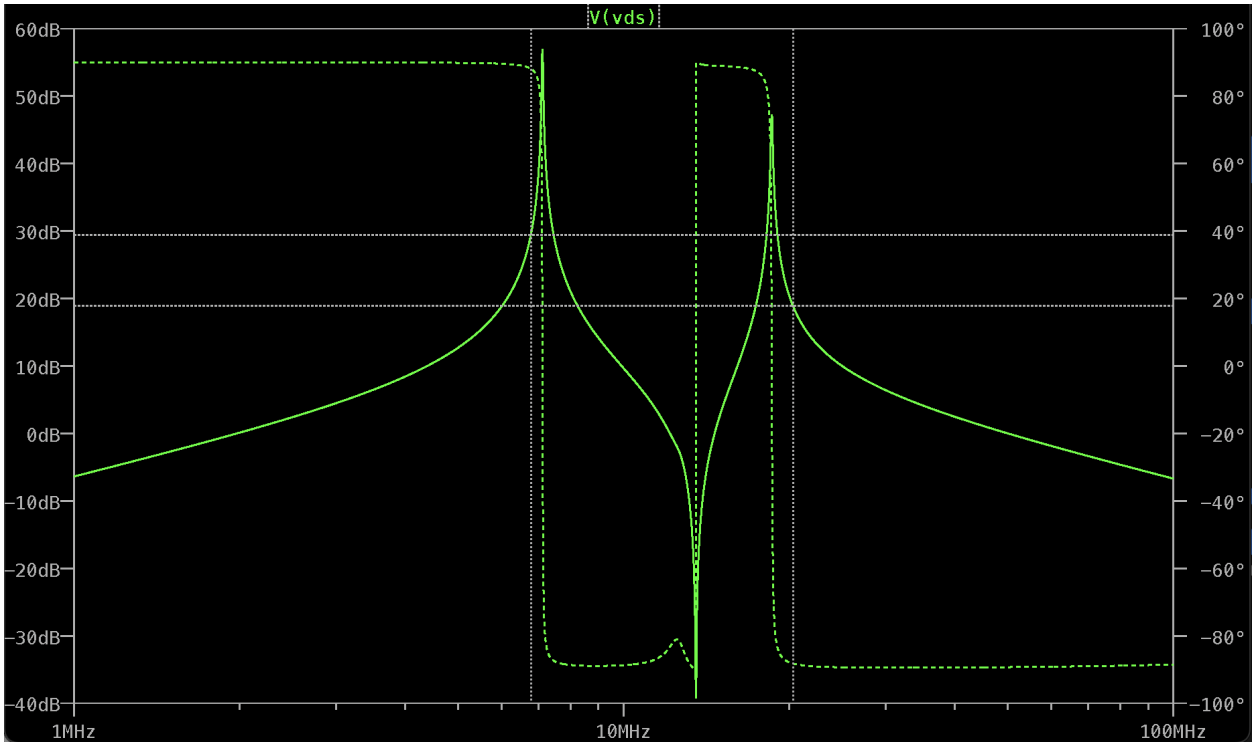

Fig 3. Φ_2 simulated ac sweep at the drain

As seen in Fig 3. Our design at our fundamental 6.78 MHz frequency had an impedance of 29dB, with a phase of 88°. This meant that we were indeed in the inductive region, and ZVS would be possible. Secondly, we wanted to make sure that our second harmonic 13.56 MHz represented a low impedance, so that it would be filtered out. Indeed we see an impedance of -35 dB. Finally, we wanted to ensure that third harmonic did not dominate the first: at 20.34 MHz, the impedance is 11 dB lower than the fundamental.

We can confirm all three of these points by the bunny ears seen in Fig. 2.

The next problem to tackle was the wireless power. We decided to use an air-core transformer on the output of our Φ_2, which carried its own set of challenges. First, we noted that there were many losses associated with a transformer. Firstly, at one inch, the coupling of our coils would be greatly impacted by parasitic capacitance, magnetizing inductance, and area of the coil. Furthermore, we wanted to ensure that the capacitance of the coil did not resonate with the coil itself such that near our fundamental frequency, such that the transformer would no longer act like a transformer.

Here we will discuss our simulation techniques, but we will further discuss the transformer below.

We noted that our transformer presented an enormous inductance. While our inverter was designed to operate at a 5 ohm load, it would not be suitable to attach a highly reactive load. As a result, we opted for a coupled-capacitor model for our transformer. This allowed us to consider

each side of the transformer as an inductor whose positive reactance could be canceled out with series capacitance at our frequency of interest.

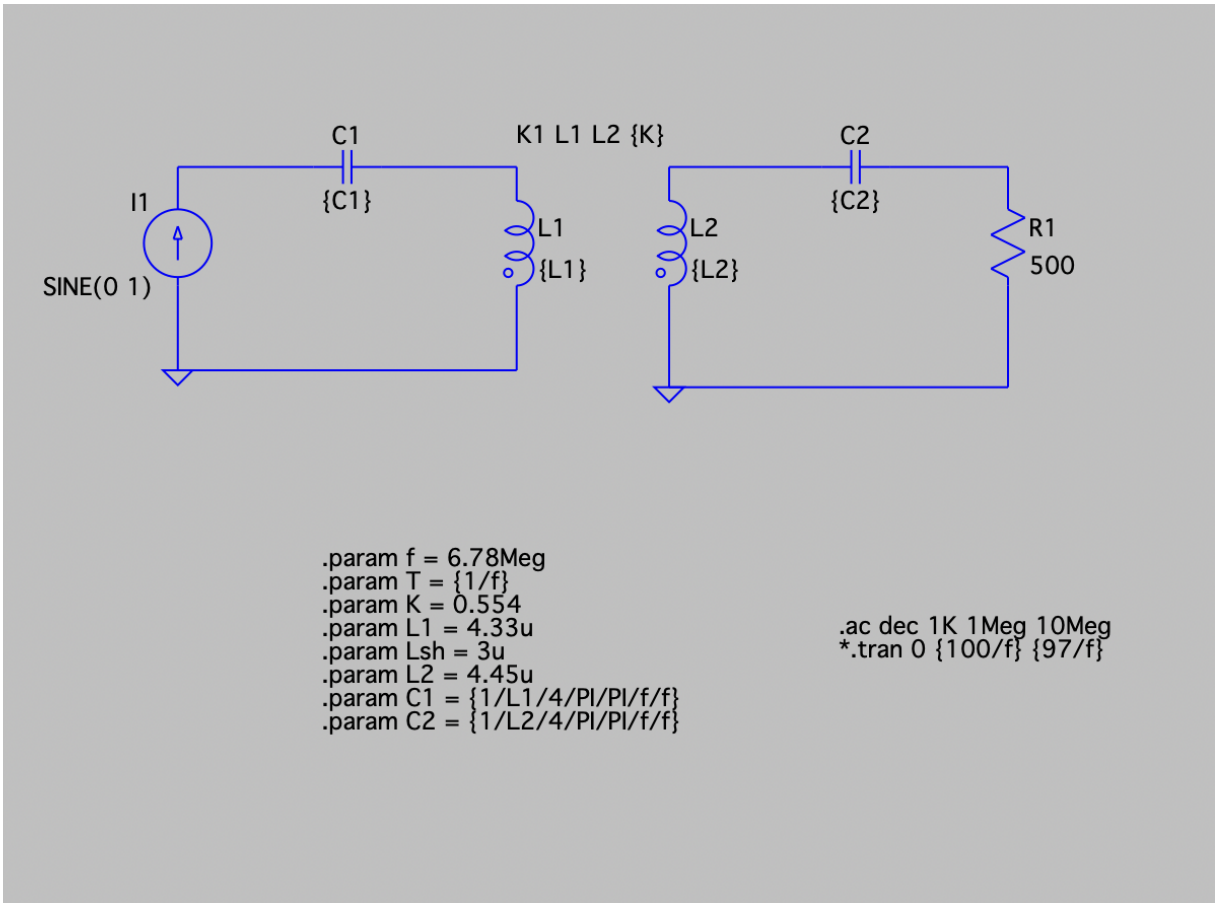

Fig 4. simulated coupled inductor model of transformer

We utilized the LTSpice model seen in Fig. 4 to calculate the appropriate series capacitor values. As seen in Fig. 5, we see some factor of our resistive load with 0° of phase. Now, it is just a matter of tuning the load resistor such that the primary side of the coil has an impedance of 5 + 0j ohms.

To address the final problem of DC power, we simply attach a rectifier. As a constant voltage source on its output, it transforms the resistors impedance to $R_{eff} = \frac{8}{\pi^2} R_{load}$. For the sake of the simulation, we did not include the rectifier.

Aside: while we realize that the square wave input of the rectifier would complicate the nature of a resistive load, we counted on the fact that our transformer would act as a filter, and the inverter would not see this nonlinear characteristic.

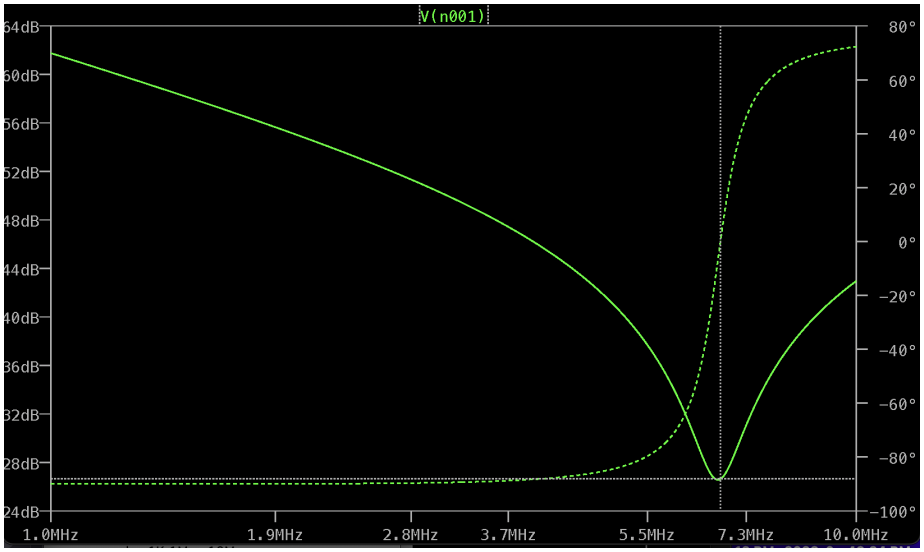

Fig 5. Impedance of simulated coupled inductor model of transformer

Final Simulation

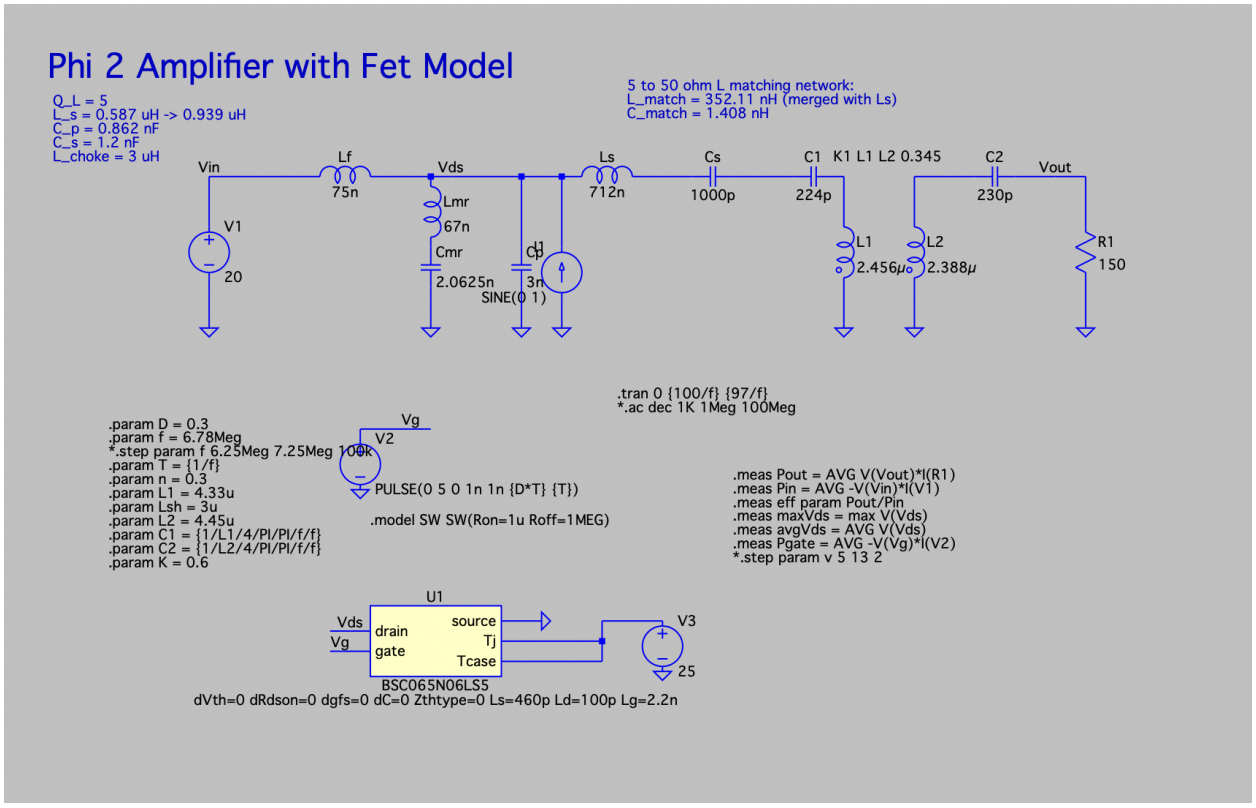

Fig 6. Model for Φ_2 inverter with “matched” transformer and load attached

Our final model is representative of our final board construction. All values are the same as what is on the modified Class D amplifier board. Here we integrate the Φ_2 model with the coupled inductors, with values that measured (discussed below). First, we conduct an ac sweep at our switching node to make sure that our Φ_2 looks right in the frequency domain.

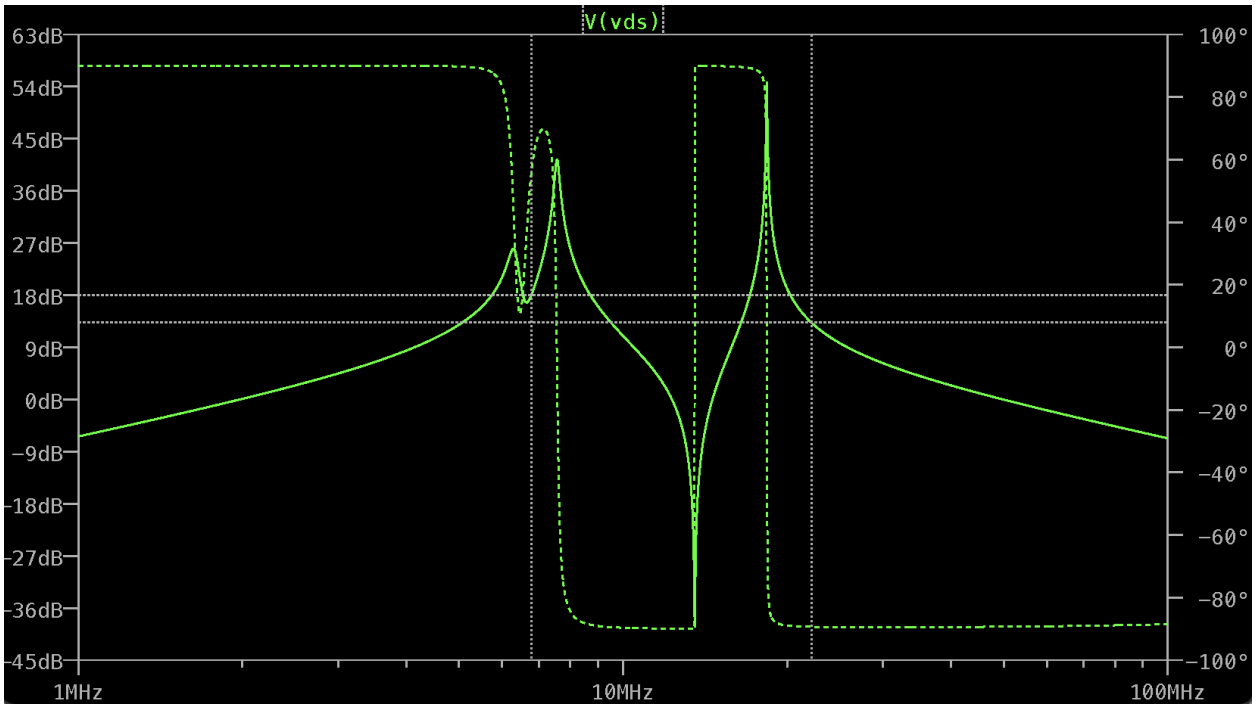

Fig 7. AC sweep at switching node of final model

Everything still seemed to be in spec, while notably, the difference in magnitude between the first and third harmonic is not as pronounced. Next we look at the time domain and see if we are below 60V peak at our switching node and that we are outputting 25 W of power.

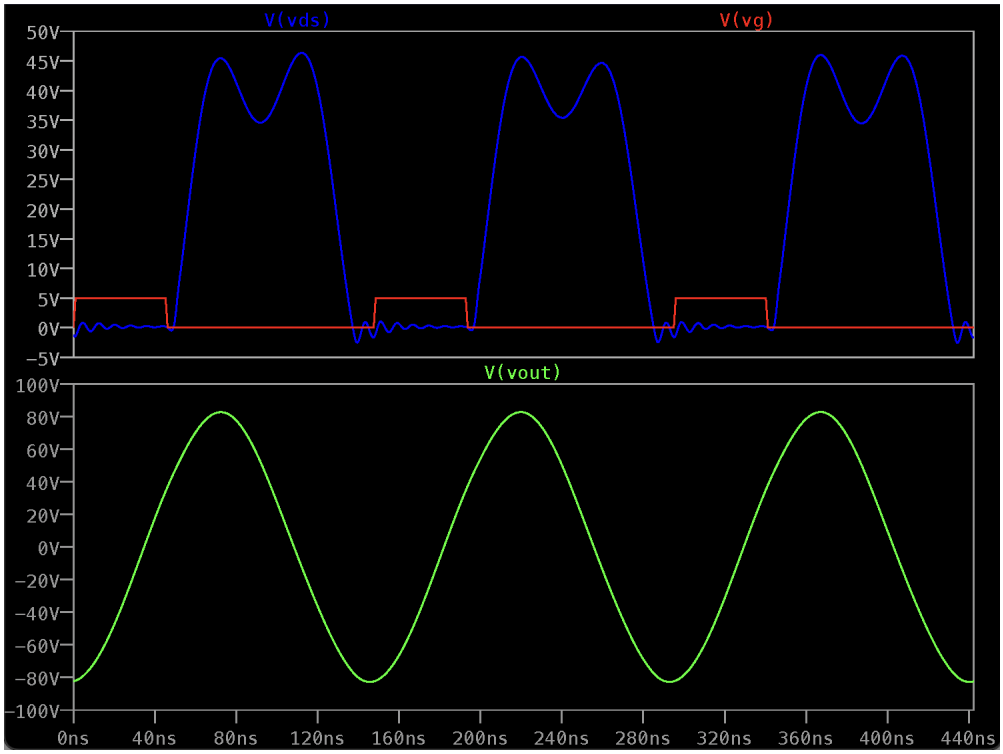

Fig 8. Time domain plot of our output voltage, Vds, and gate voltage Vg

As seen in Fig. 8, we are indeed below our 60V Vds requirement. Furthermore, we are outputting 25.068 W of power with an efficiency of 96%. Additionally, we are seeing bunny ears that are not skewed to one side, so the third harmonic doesn't seem to be too overpowering. Finally, we can see that we are indeed zero voltage switching, as Vgs and Vds seem to alternate in time.

Experimental Measurements

Characterization

We connected the NanoVNA to our transformer and characterized it in order to get our transformer model. We needed to get the coupling coefficient K, L1 (measuring primary, secondary open), and L2 (measuring secondary, primary open) and Lsh (primary open, secondary shorted).

Additionally, we also measured the impedance seen from the primary side with a 50 ohm load attached. We also measured the impedance seen by Vds while the transformer has a 50 ohm load attached to the secondary.

We calculated our coupling coefficient $K = \sqrt{\{L1 - Lsh)/L1}$. Using the values for L1 and L2, we added a series capacitor to cancel the reactance of of the transformer using the equation: $Cx = 1/(\omega s^2 * Lx)$. The results of our measurements can be seen in the following figures.

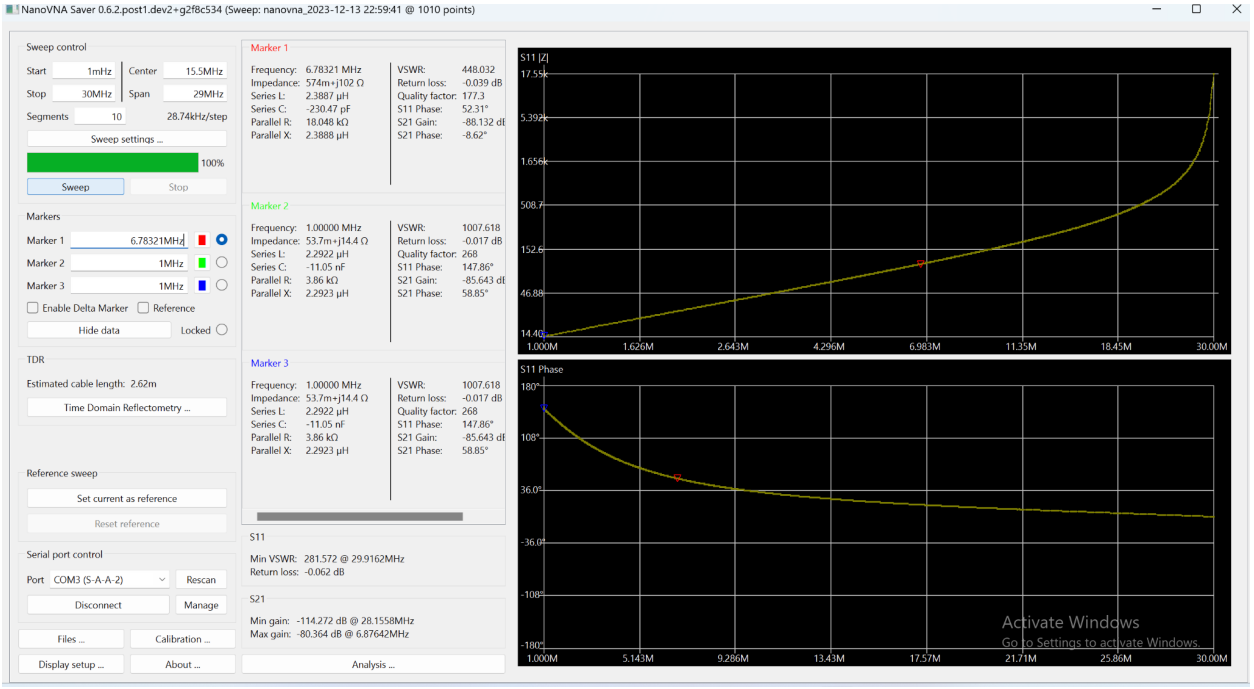

Fig 10. VNA Measurement of Transformer Primary Coil

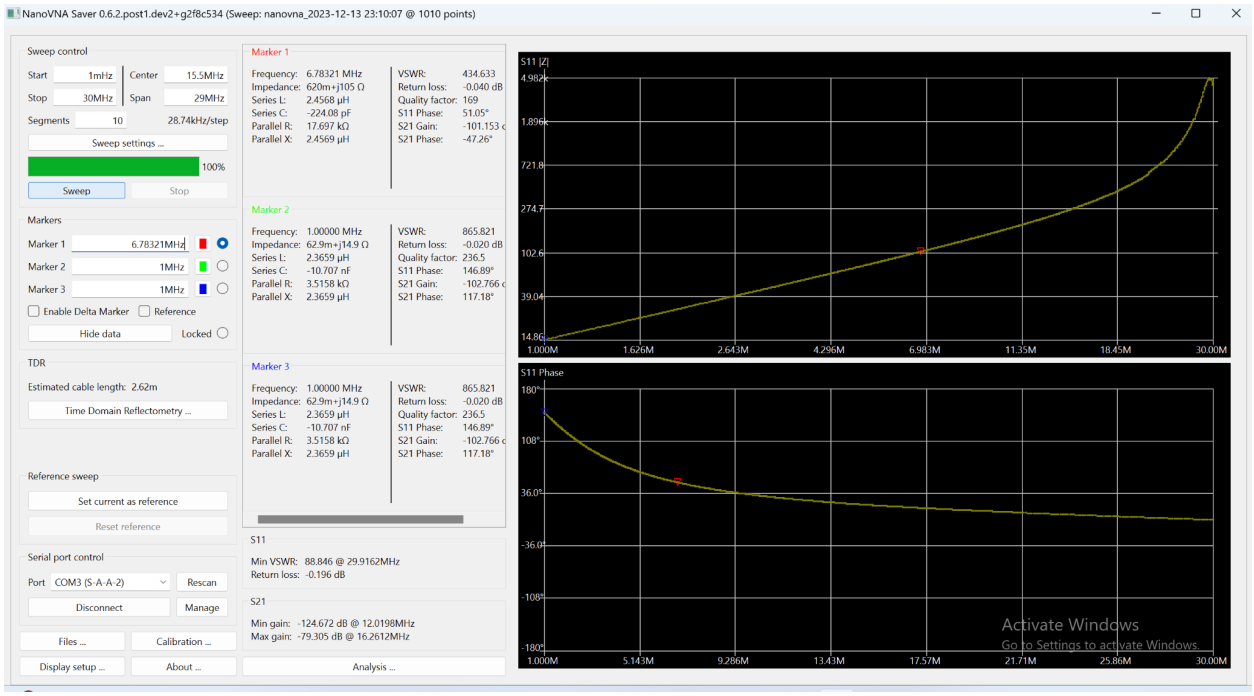

Fig 11. VNA Measurement of Transformer Secondary Coil

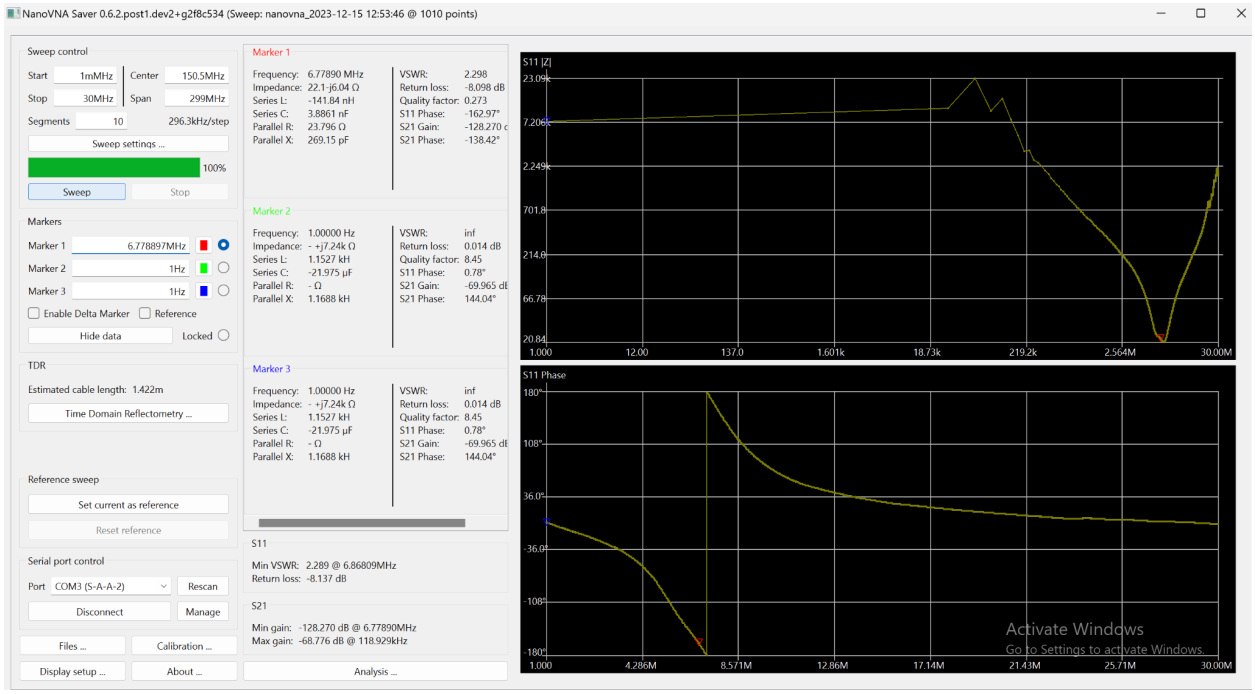

Fig 12. VNA Measurement with Canceling Series Caps and 50 Ohm Load At Output

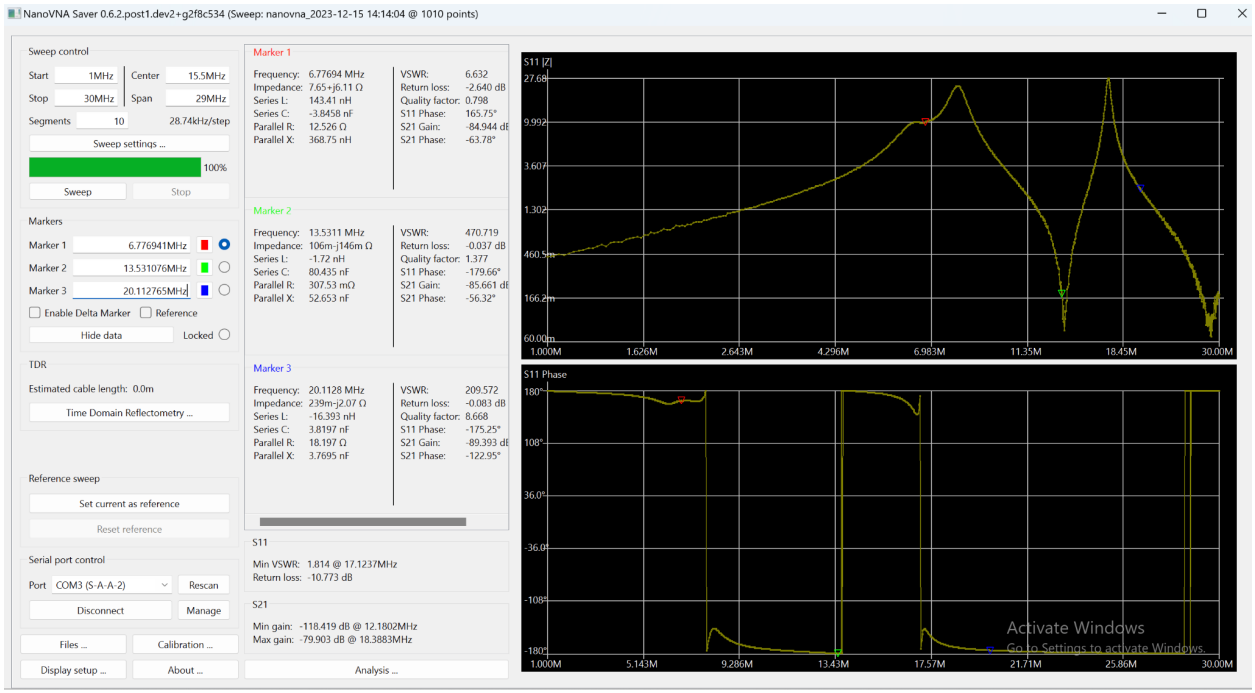

Fig 13. VNA Measurement of Vds with Transformer and 50 Ohm Load

Experiment

Figure 14 shows our experimental set up. Going from left to right, you can see the phi2 converter connected to our transformer, followed by the rectifier. Our rectifier is then connected to the DC load machine.

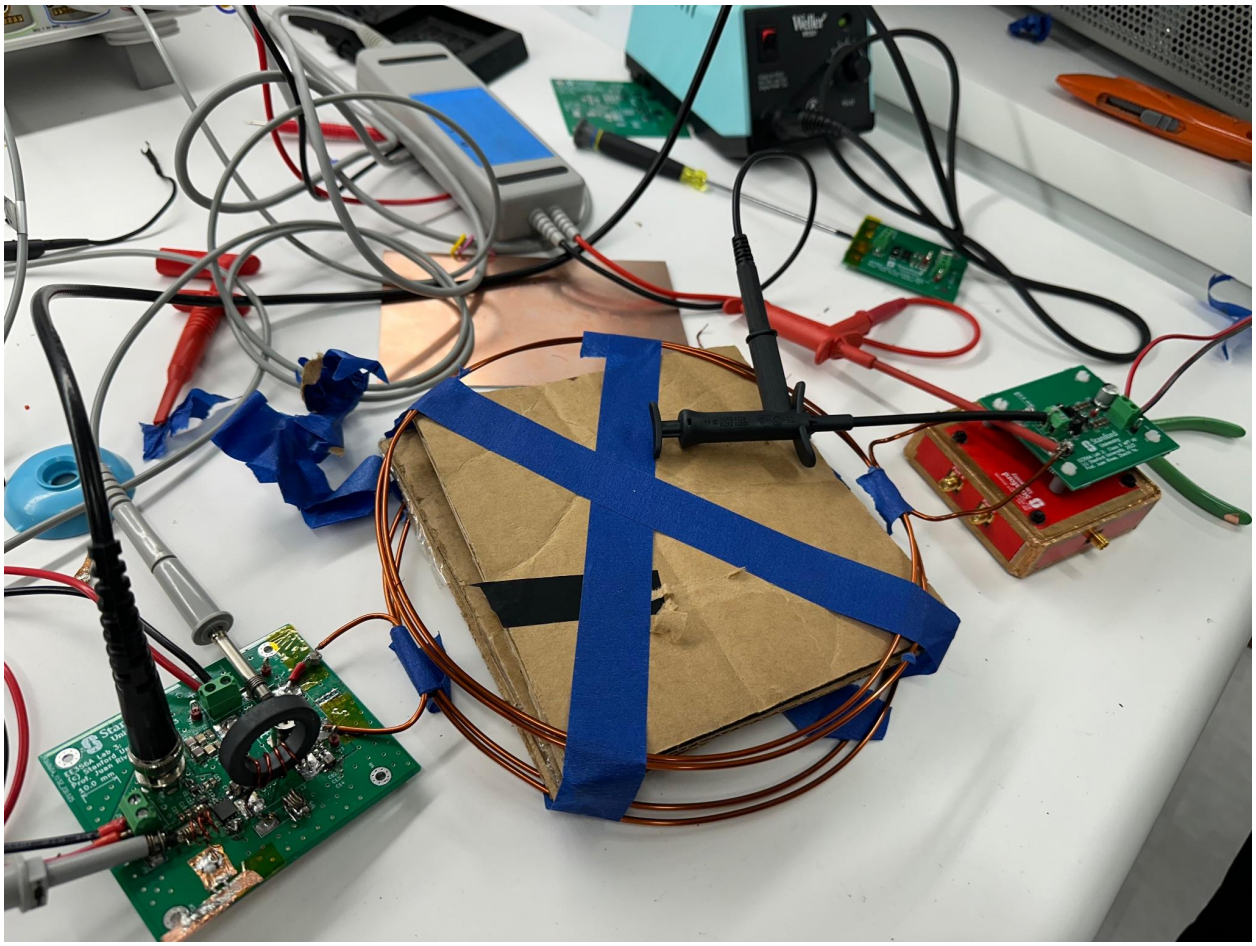

Fig 14. Experimental Setup

Next we ran a series of experiments sweeping the load, frequency, and voltage until we were able to achieve the highest output power transfer to the DC load machine. Our general approach was to start with a low input voltage of 10V until we found the optimal output power. We calculated the input power from the DC power supply voltage and current. We calculated the output power by reading the DC load machine voltage and current. We used the oscilloscope to measure our Vgs, Vds, and Vr (rectifier input voltage).

First, we swept through our load resistance as seen in Table 1. We found the 150 Ohms provided the highest output power. Then we swept the switching frequency and found that 6.42 MHz resulted in the highest output power as seen in Table 2. Next, having found the optimal switching frequency, we once again swept the load resistance and found 160 Ohms to be the most optimal load for power and efficiency as demonstrated in Table 3. Then, as shown in Table 4, we swept the input voltage using a switching frequency of 6.42 MHz using 160 and 100 Ohm load resistance. At 18V, we exceeded the voltage limit of the DC load machine while using 160 ohms. Additionally, to withstand the high voltage seen by the rectifier we placed an additional diode in series for each original diode in the rectifier We were able to achieve 27.9628W at 20 Vin and 6.42 MHz. Figures 15 and 16 demonstrate our ability to deliver power to the load.
Finally, we tried to sweep the load resistance while operating at 6.78 MHz and 20 Vin, but our fet quickly burned out. Our limited results can be seen in Table 5.

Fig 15. Oscilloscope Image of waveforms at 27.96W - Vgs (Yellow), Vds (Green), Vr (Pink)

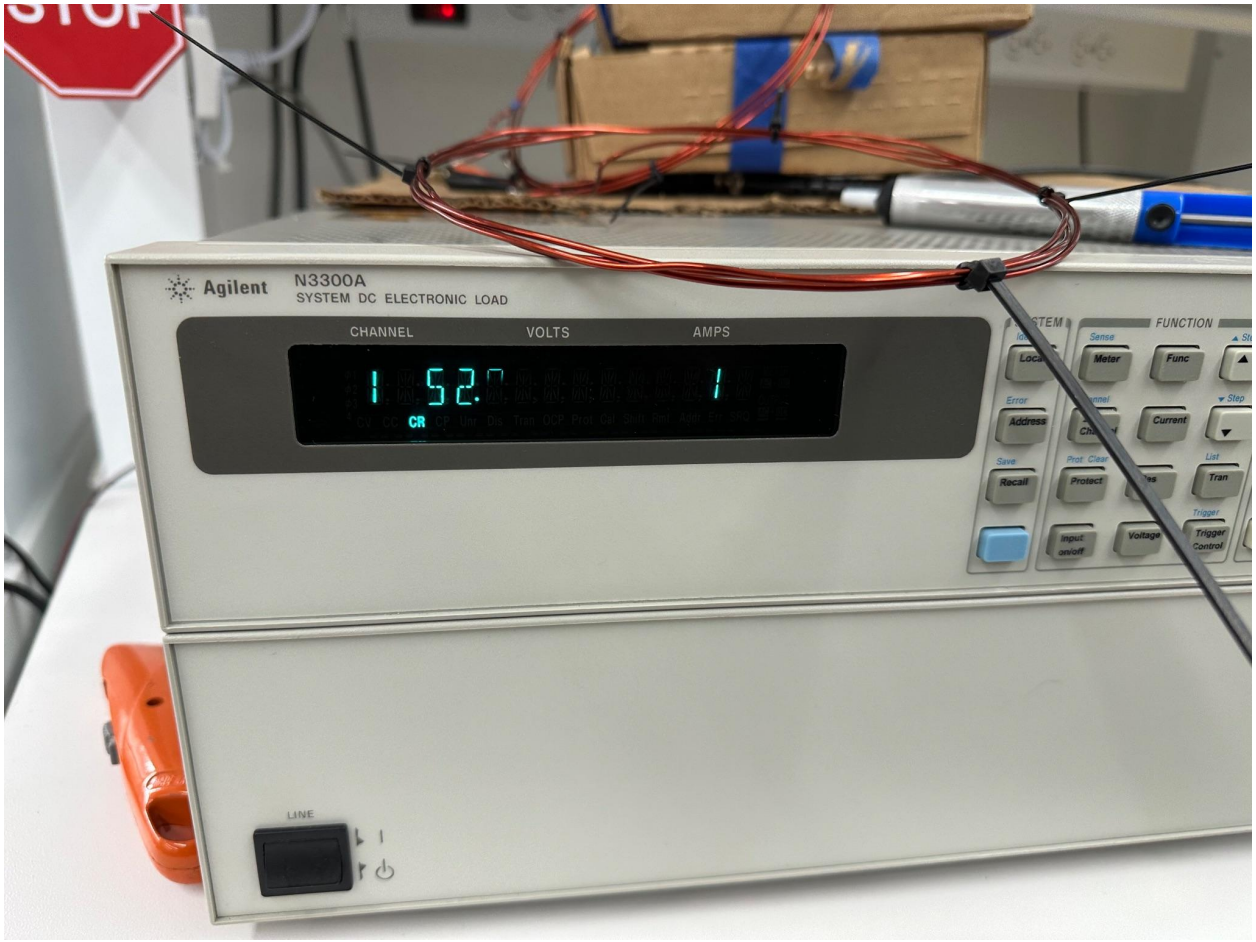

Fig 16. DC Load Machine at 27.96W

**Screen Refresh rate caused failure to capture all numbers -> 52.76Vdc @ .531A = 27.96W

Rload (Ohm)	Vin (V)	Iin (A)	Pin (W)	Vout DC (V)	Iout (A)	Pout (W)	Eff	Vds Max (V)	Vr Max (V)	Temp (C)	Fsw (Mhz)
5	10	0.26	2.6	1.1	0.217	0.2387	0.0918076923 1	22.1	3.2	55	6.78
10	10	0.28	2.8	2.09	0.207	0.4326 3	0.1545107143	22.5	4.5	55.5	6.78
20	10	0.3	3	3.833	0.192	0.735936	0.245312	22.5	6.5	56.3	6.78
30	10	0.34	3.4	5.364	0.18	0.96552	0.2839764706	23	8.3	60.4	6.78
40	10	0.37	3.7	6.78	0.17	1.1526	0.3115135135	23.1	9.8	62	6.78
50	10	0.39	3.9	8.065	0.161	1.298465	0.3329397436	23.1	11.2	64.3	6.78
60	10	0.4	4	9.22	0.154	1.41988	0.35497	22.1	12.1	64.5	6.78
70	10	0.44	4.4	10.283	0.148	1.521884	0.3458827273	23	13.5	67	6.78
80	10	0.44	4.4	11.4	0.14	1.596	0.3627272727	23.1	14.4	67	6.78
90	10	0.45	4.5	12.22	0.136	1.66192	0.3693155556	23.1	15	69	6.78
100	10	0.46	4.6	13.1	0.131	1.7161	0.3730652174	23.1	16.2	70	6.78
150	10	0.48	4.8	16.34	0.11	1.7974	0.3744583333	23.1	19	55	6.78
200	10	0.49	4.9	18.7	0.094	1.7578	0.3587346939	23.9	21.5	70	6.78
250	10	0.5	5	20.896	0.084	1.755264	0.3510528	23.9	23.2	74	6.78

Table 1. Sweeping Load Resistance

Fsw (Mhz)	Vin (V)	Iin (A)	Pin (W)	Vout DC (V)	Iout (A)	Pout (W)	Eff	Vds Max (V)	Vr Max (V)	Temp (C)	Rload (Ohm)
6.2	10	0.49	4.9	21.778	0.146	3.179588	0.6488955102	23.1	25.3	55	150
6.3	10	0.81	8.1	29	0.194	5.626	0.6945679012	22.3	34.1	55	150
6.35	10	1.01	10.1	33	0.221	7.293	0.7220792079	22.3	39.5	56	150
6.4	10	1.3	13	37.85	0.25	9.4625	0.7278846154	22.3	4.522.3	56.6	150
6.42	10	1.37	13.7	38.92	0.261	10.15812	0.7414686131	22.3	46.7	55	150
6.44	10	1.41	14.1	39.138	0.262	10.254156	0.7272451064	23.1	47	60	150
6.45	10	1.41	14.1	38.99	0.261	10.17639	0.7217297872	23.1	46.7	63.5	150
6.5	10	1.26	12.6	36.02	0.241	8.68082	0.6889539683	22.3	43.5	59	150
6.6	10	0.85	8.5	26.6	0.178	4.7348	0.5570352941	24.9	31.6	74	150
6.78	10	0.48	4.8	16.17	0.109	1.76253	0.36719375	23.1	19.1	73	150
6.9	10	0.36	3.6	12.79	0.086	1.09994	0.3055388889	23.1	15.5	62	150
7.1	10	0.28	2.8	9.667	0.065	0.628355	0.2244125	21.5	12.2	62	150

Table 2. Sweeping Switching Frequency

Rload (Ohm)	Vin (V)	Iin (A)	Pin (W)	Vout DC (V)	Iout (A)	Pout (W)	Eff	Vds Max (V)	Vr Max	Fsw (MHz)
5	10	0.26	2.6	1.1	0.217	0.2387	0.09180769231	22.1	3.2	6.42
10	10	0.39	3.9	3.025	0.302	0.91355	0.2342435897	24.7	6	6.42
50	10	0.74	7.4	14.43	0.288	4.15584	0.5616	24.7	20	6.42
60	10	0.83	8.3	17.141	0.287	4.919467	0.5927068675	24.7	22.8	6.42
70	10	0.92	9.2	19.97	0.285	5.69145	0.6186358696	24	26	6.42
100	10	1.15	11.5	28.09	0.282	7.92138	0.6888156522	23.9	35.4	6.42
120	10	1.28	12.8	33	0.276	9.108	0.7115625	23.5	40.4	6.42
160	**10**	**1.38**	**13.8**	**40.28**	**0.255**	**10.2714**	**0.7443043478**	**22.3**	**48**	6.42
180	10	1.32	13.2	41.67	0.233	9.70911	0.7355386364	23	50	6.42

Table 3. Sweeping Load Resistance at Fsw = 6.42 Mhz

Vin	Rload (Ohm)	Iin (A)	Pin (W)	Vout DC (V)	Iout (A)	Pout (W)	Eff	Vds Max (V)	Vr Max (V)	Fsw (MHz)
12	160	1.3	15.6	42.43	0.26	11.0318	0.7071666667	26.3	51.7	6.42
15	160	1.61	24.15	52.876	0.33	17.44908	0.7225291925	33.5	64.2	6.42
16	160	**1.7**	27.2	**56.36**	0.354	**19.95144**	**0.7335088235**	**35.1**	**68.3**	6.42
17	160	1.8	30.6	59.85	0.376	22.5036	0.7354117647	36.7	72.1	6.42
18	160	1.94	34.92	63.83	0.401	25.59583	0.7329848225	39.1	79	6.42
19	100	1.94	36.86	50.127	0.5	25.0635	0.6799647314	43.2	65	6.42
20	100	2.04	40.8	52.76	0.531	27.9628	0.6853627451	45.6	71	6.42

Table 4. Sweeping Input Voltage

Rload (Ohm)	Vin	Iin (A)	Pin (W)	Vout DC (V)	Iout (A)	Pout (W)	Eff	Vds Max (V)	Vr Max (V)	Fsw (MHz)
100	20	2.04	40.8	30.7	0.308	9.4556	0.231754902	45.6	71	6.78
160	20	1.2	24	42.716	0.268	11.447888	0.4769953333	X	X	6.78
200	20	FAILED	FAILED	FAILED	FAILED	FAILED	FAILED	FAILED	FAILED	6.78

Table 5. Sweeping Load Resistance at 6.78 MHz

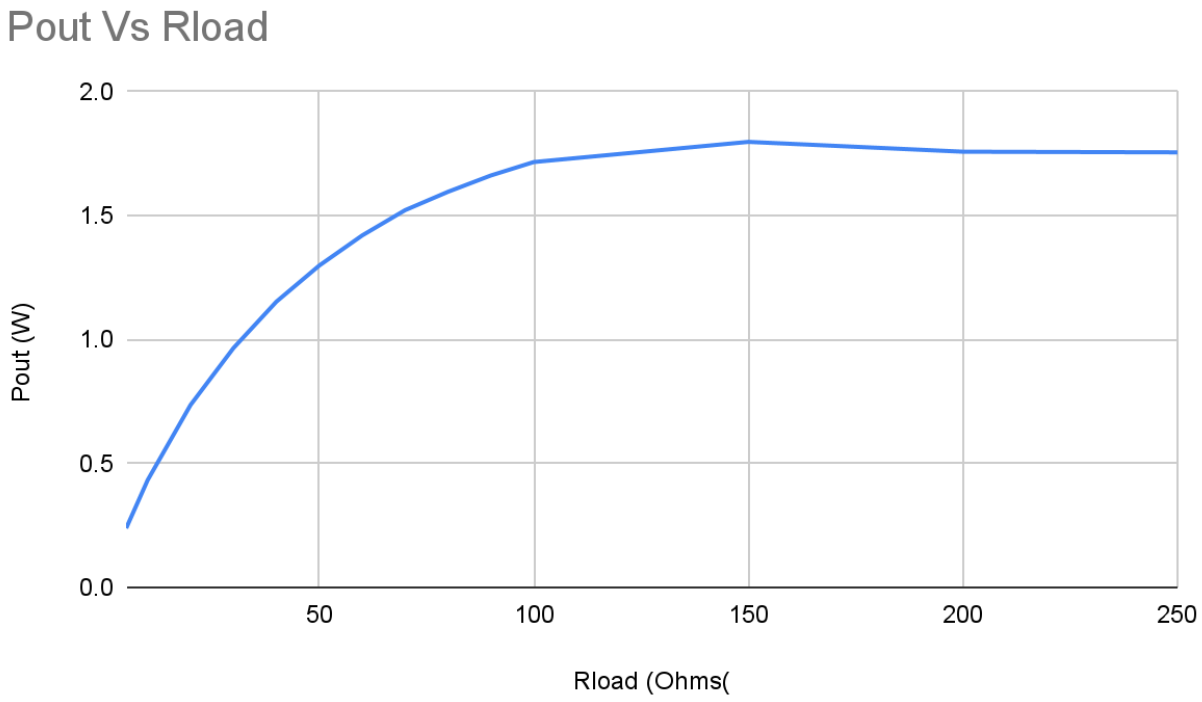

Fig 17. Pout Vs Rload

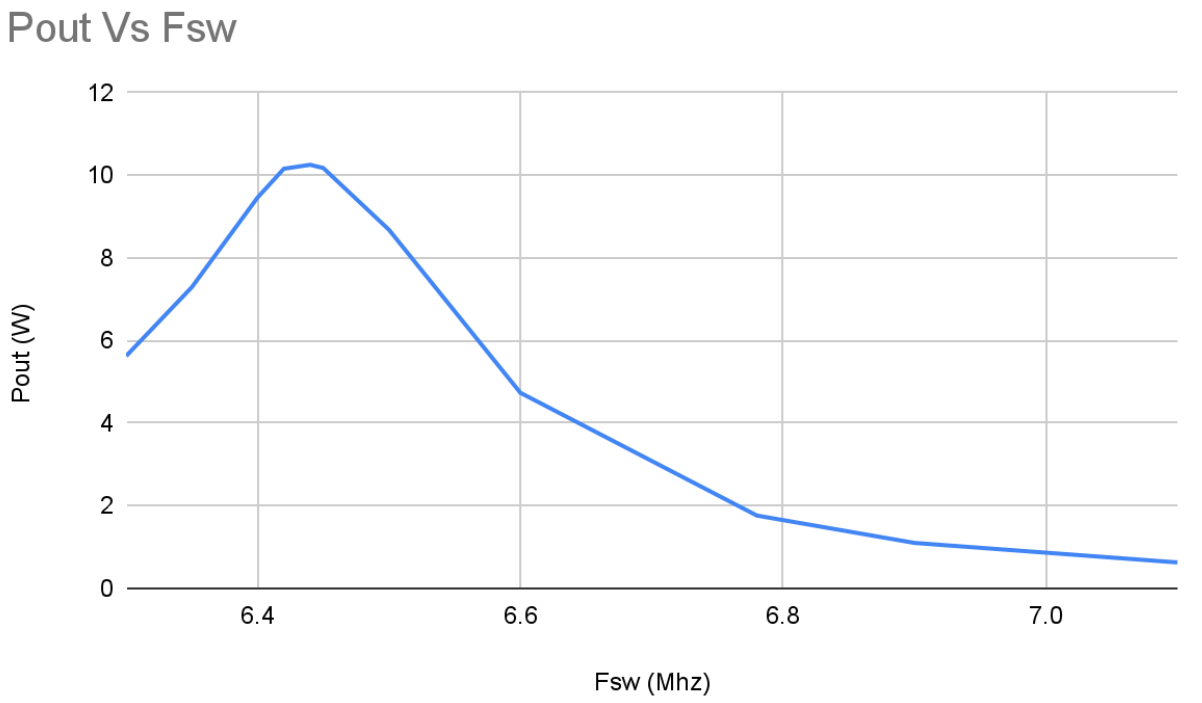

Fig 18. Pout Vs Fsw

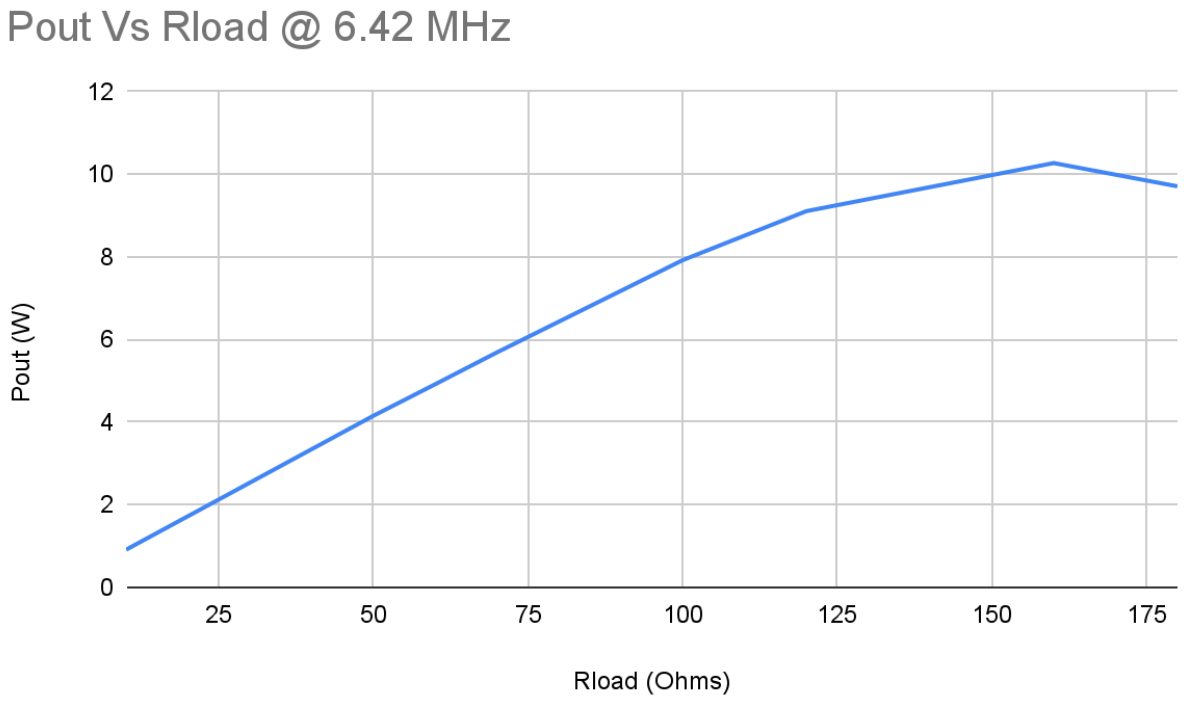

Fig 19. Pout Vs Rload

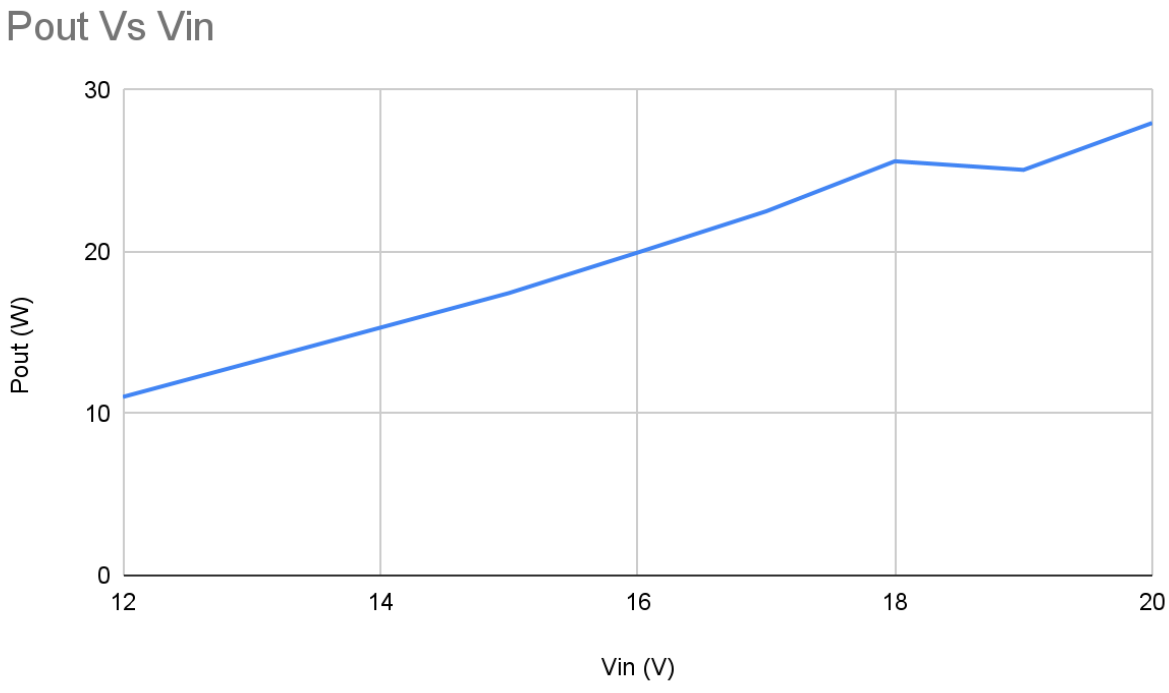

Fig 20. Pout Vs Vin
**Note 12 -18V with 160 Ohm load and 19-20V measured with 100 Ohm load

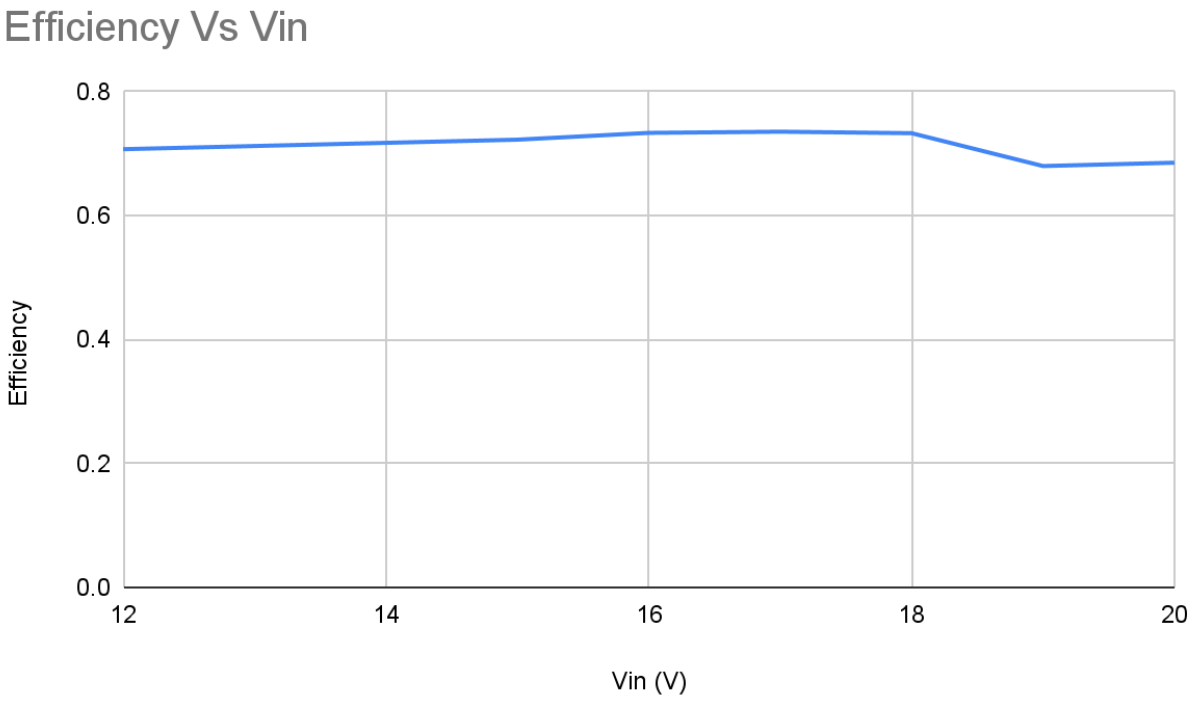

Fig 21. Efficiency Vs Vin
**Note 12 -18V with 160 Ohm load and 19-20V measured with 100 Ohm load

Comparison

We were able to match our simulation modestly well. Our measured impedance at Vds matched our simulation well. Our time domain response matched modestly well. Our Vds shows the same bunny ears and peak voltage. Yet, there is significant ripple in Vds while our Vgs is high. I suspect that this may have caused some unnecessary power loss and a reduction in our efficiency. Our output voltage in simulation is sinusoidal with a peak of ~80V and our measurement shows a 71V max square wave at the input of our rectifier. This deviation may also be due to the fact that we are not modeling our rectifier. Our board efficiency is also significantly lower. In simulation we achieved an efficiency of 96% but in reality, we only achieved ~ 68%. Also, our simulation operated at 6.78 MHz, while our circuit operated at 6.42 MHz. These differences are probably due to various parasitics unaccounted for. For example, probe capacitance, board parasitics, thermal variation, component variation. Regardless, our simulation was modestly close to what we were expecting. Better tuning may have helped match more closely.

Conclusion

We were able to design a Phi2 converter capable of wirelessly transferring 27.96W to a load with an efficiency of 68.53% while operating our circuit with 20V Vin at 6.42 MHz.