Lab 10

To Design and Implement Multiplexer & Demultiplexer

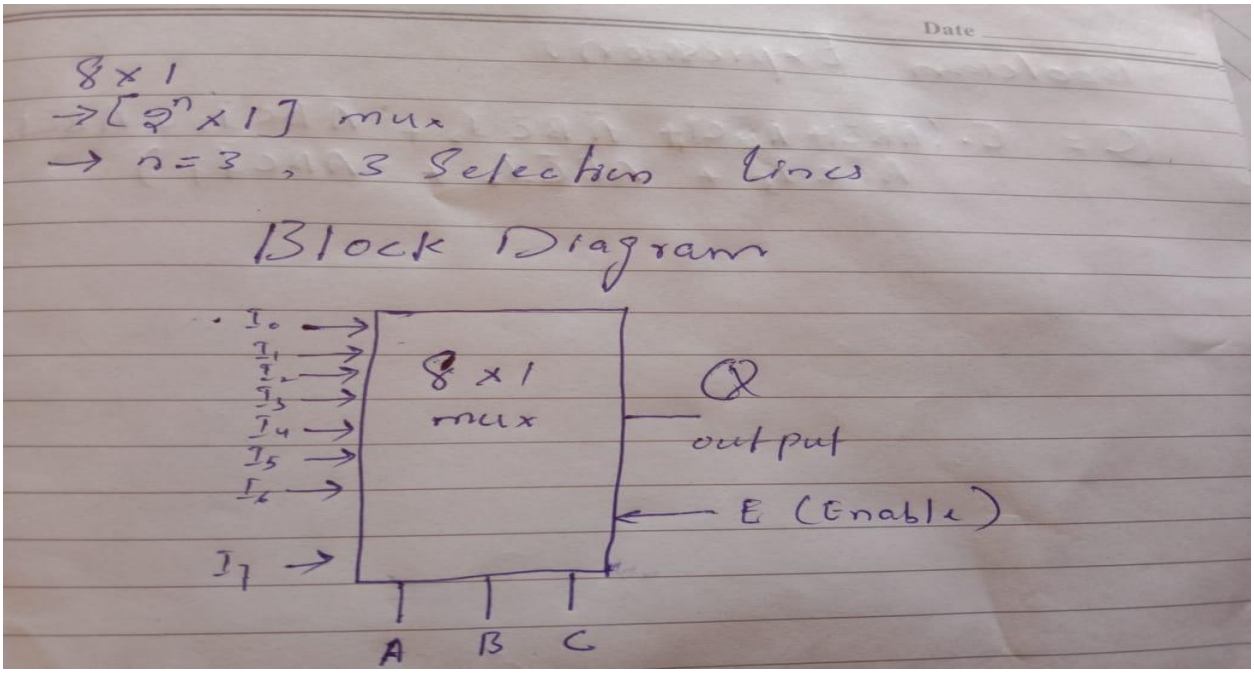
Note: For all the circuits in the tasks, your logic diagrams should be either hand drawn or from the software logicly. Keep them neat and legible. These circuits will be having many connections so, for simulations, make sure that you label the inputs and outputs clearly. Use Label tag in "logically". You can also edit the pictures of your outputs in "paint" easily.

Tasks

1. **Construct a logic circuit for 8 to 1 multiplexer with the help of truth table. Also write the Boolean expression for output(s). Simulate your circuit to verify the outputs.**

8 to 1 Mux

a) Block Diagram



b) Truth Table

Truth table

⇒ when Enable (E = 0) No matter what are inputs output will be 0 but when E = 1 output will be according to inputs

E	A	B	C	O
0	X	X	X	0
1	0	0	0	I_0
1	0	0	1	I_1
1	0	1	0	I_2
1	0	1	1	I_3
1	1	0	0	I_4
1	1	0	1	I_5
1	1	1	0	I_6
1	1	1	1	I_7

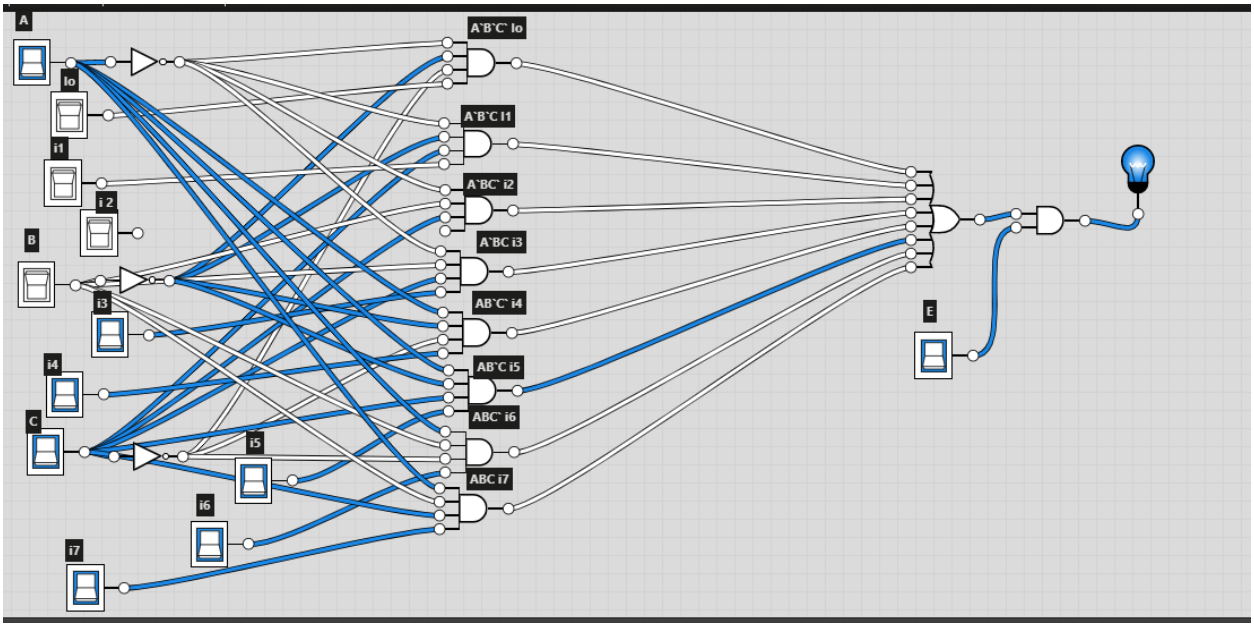
c) Boolean Expression

Date

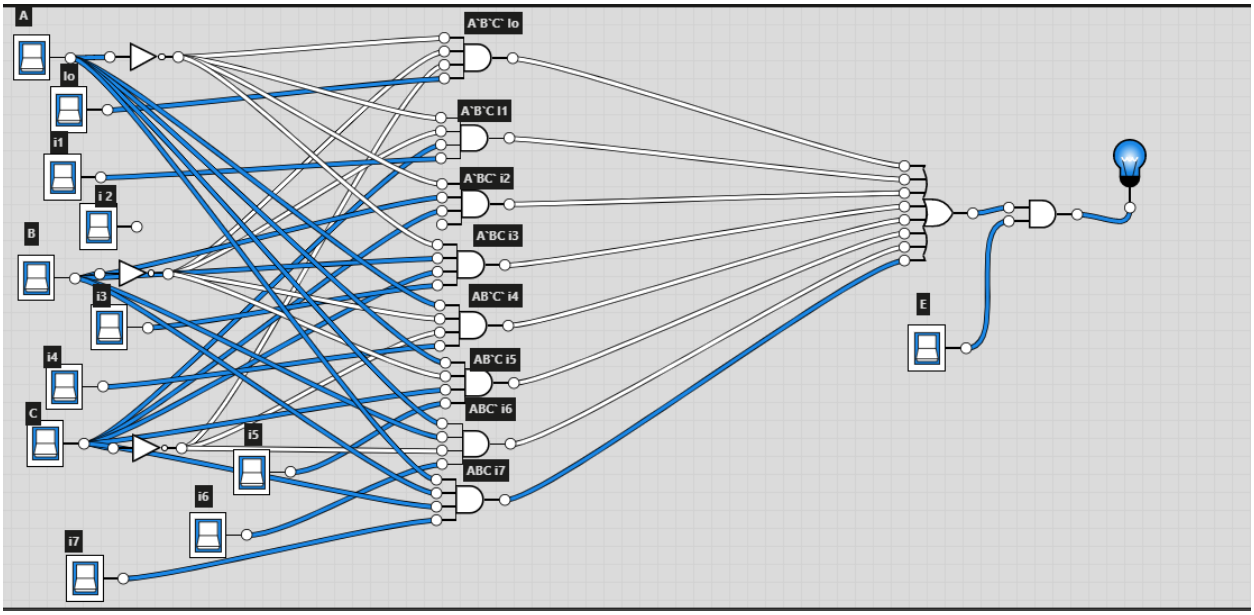
Boolean Expression:

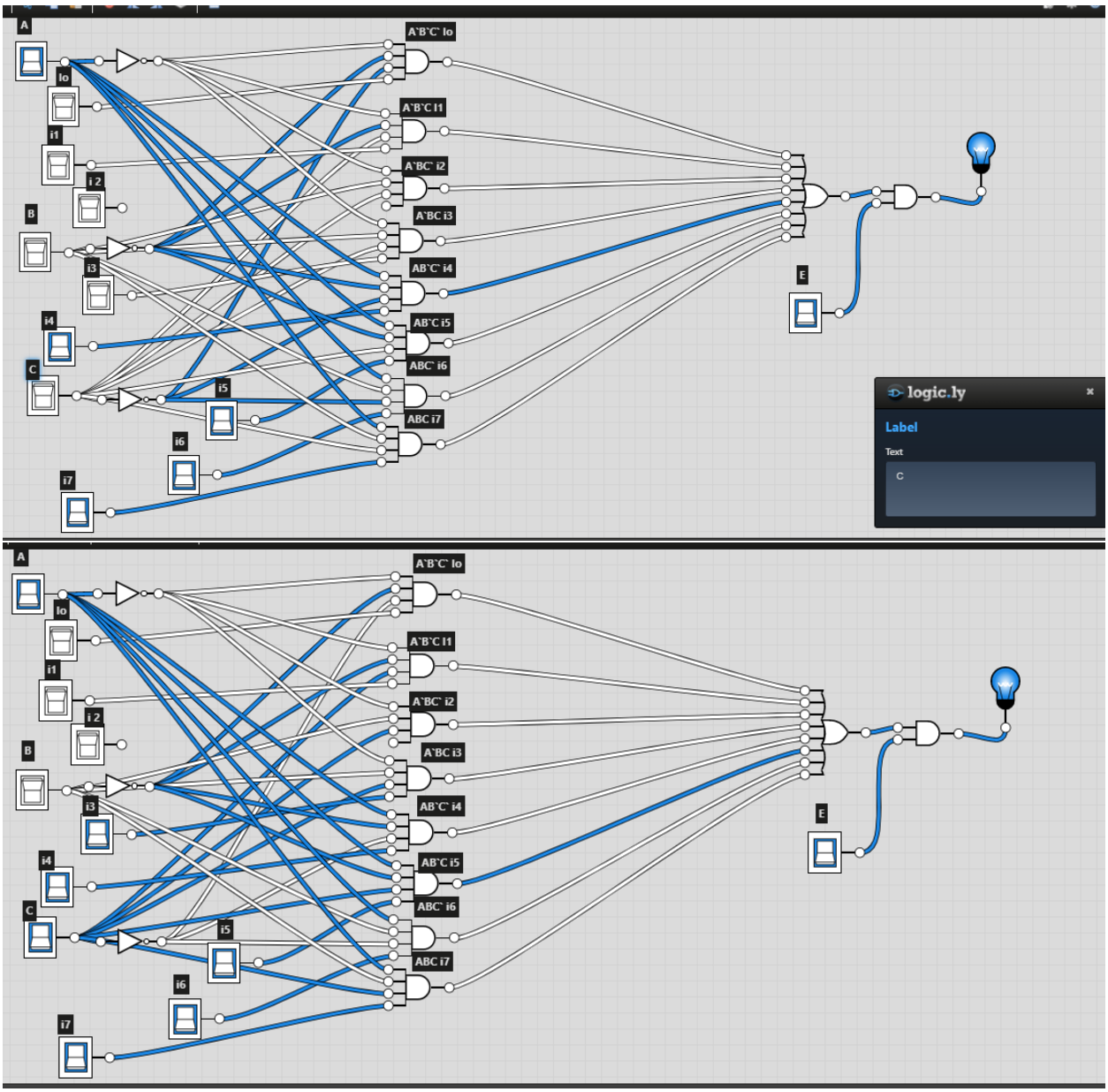
$$O = E.(\bar{A}\bar{B}\bar{C}I_0 + \bar{A}\bar{B}CI_1 + \bar{A}B\bar{C}I_2 + \bar{A}BCI_3 + A\bar{B}\bar{C}I_4 + A\bar{B}CI_5 + AB\bar{C}I_6 + ABCI_7)$$

d) Logic Diagram (from logicaly or hand drawn)



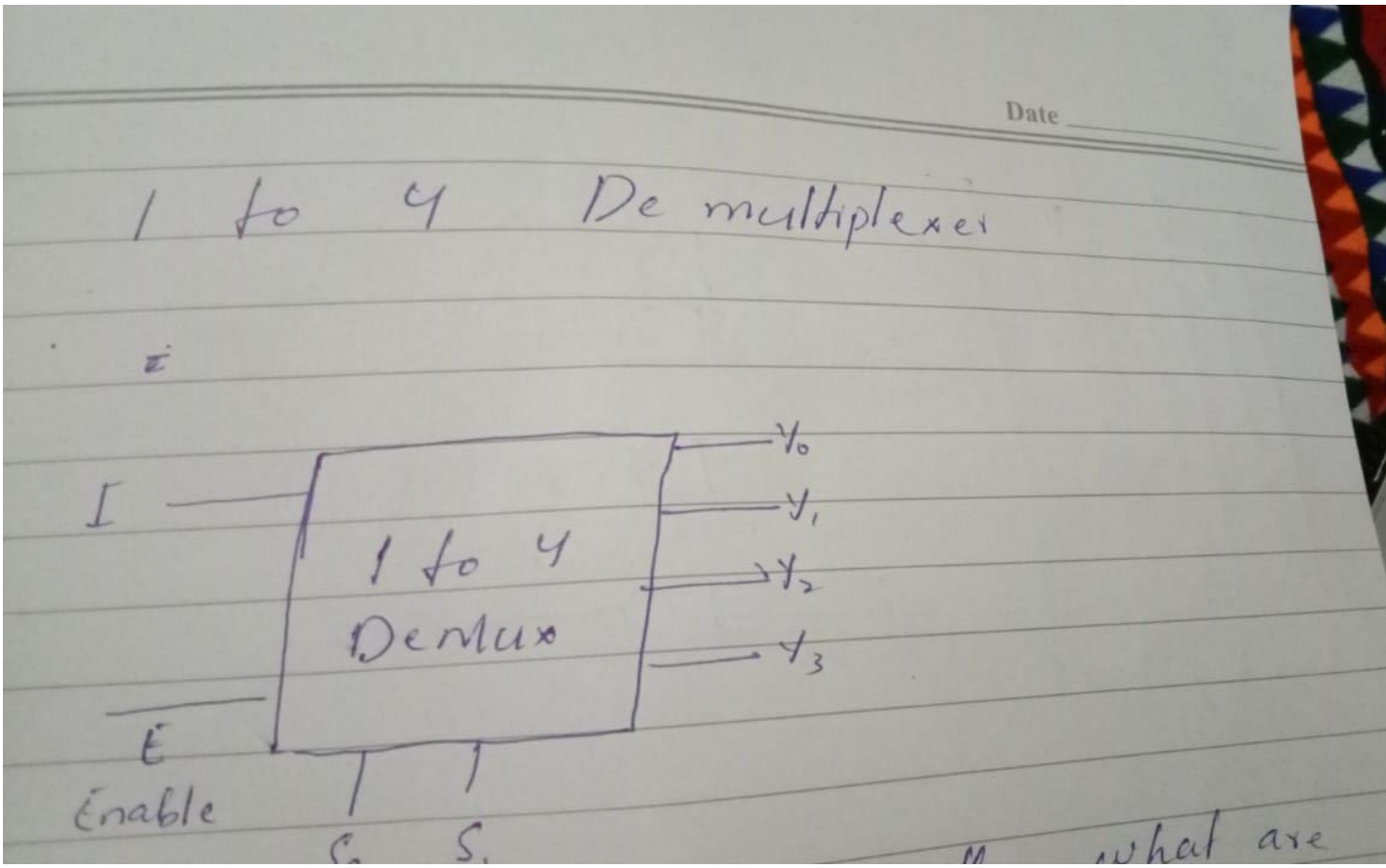
e) Software Simulation



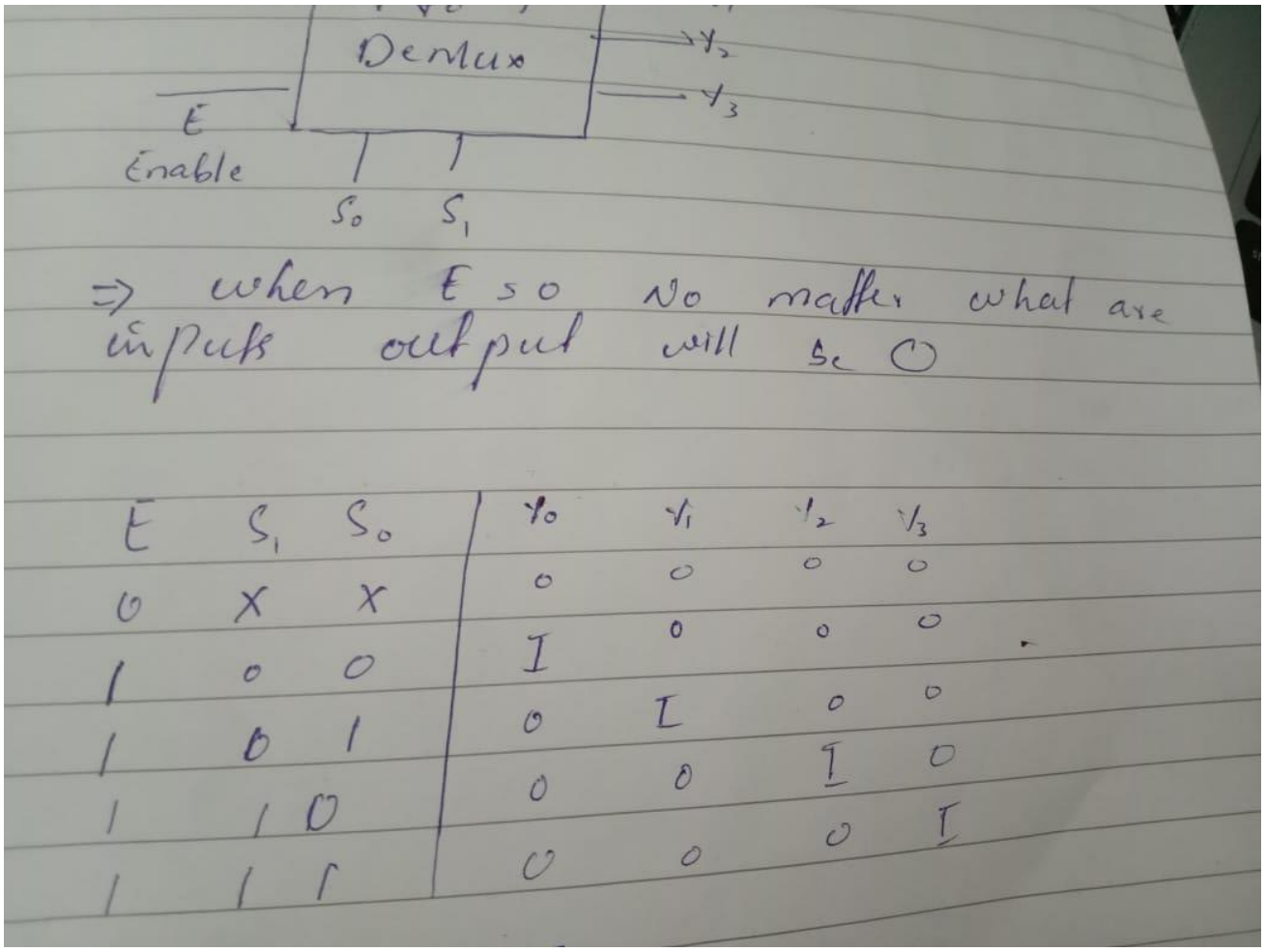


2. **Design a logic circuit for 1 to 4 line Demultiplexer. Also write the Boolean expression for output(s). Simulate your circuit to verify the outputs.**

a) Block Diagram



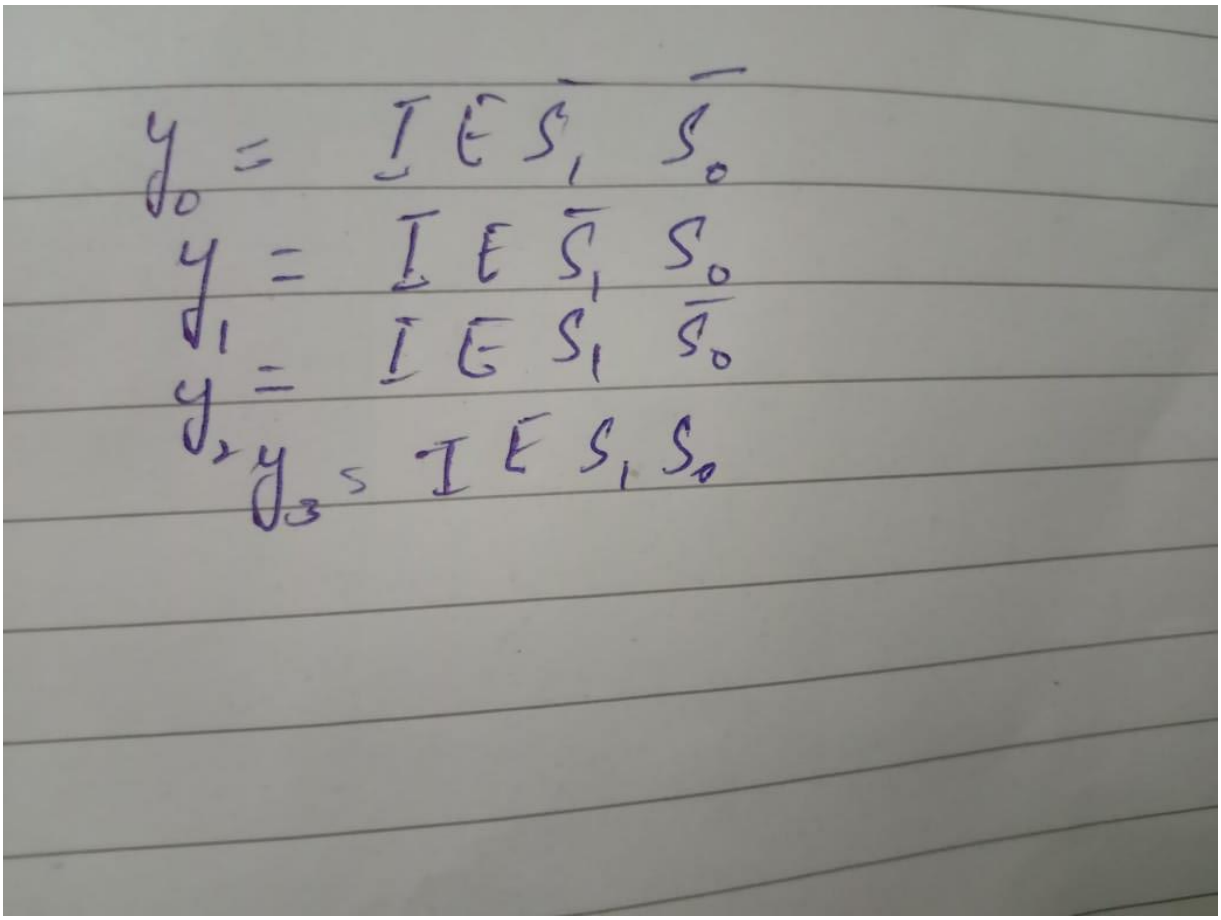
a) Truth Table



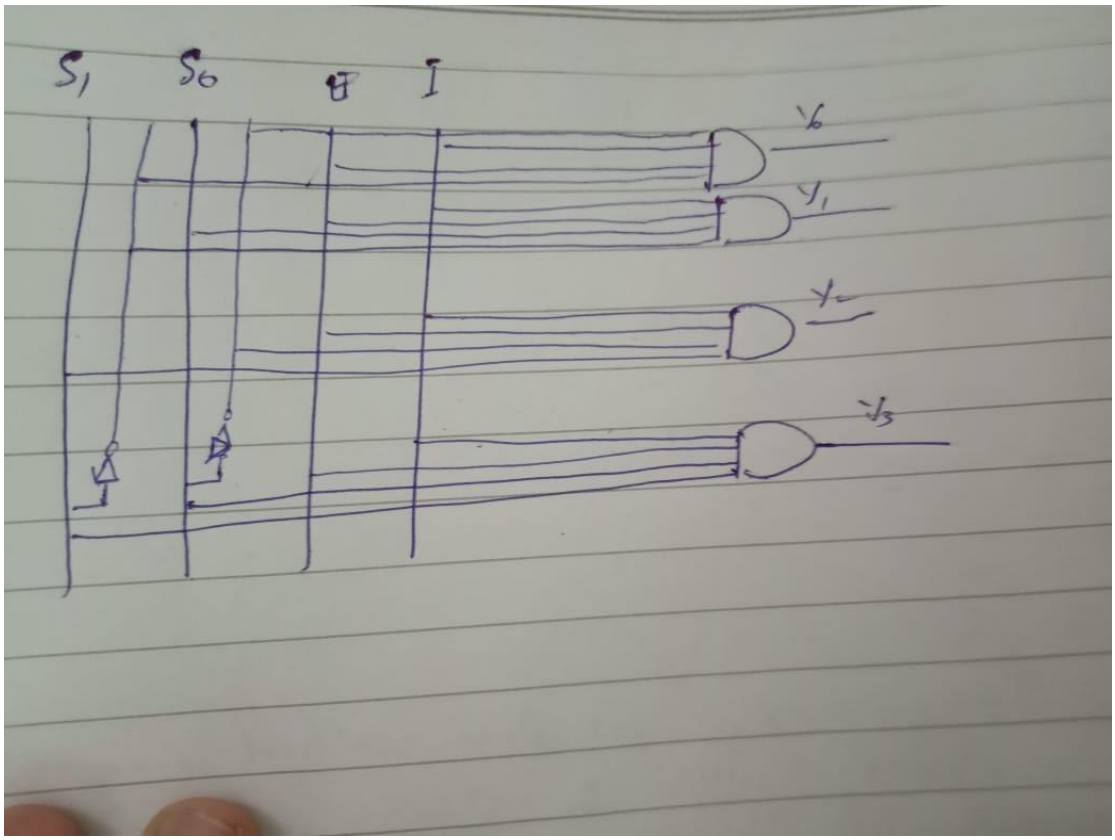
⇒ when E = 0 No matter what are inputs output will be 0

$\bar{E}$	S_1	S_0	Y_0	Y_1	Y_2	Y_3
0	X	X	0	0	0	0
1	0	0	I	0	0	0
1	0	1	0	I	0	0
1	1	0	0	0	I	0
1	1	1	0	0	0	I

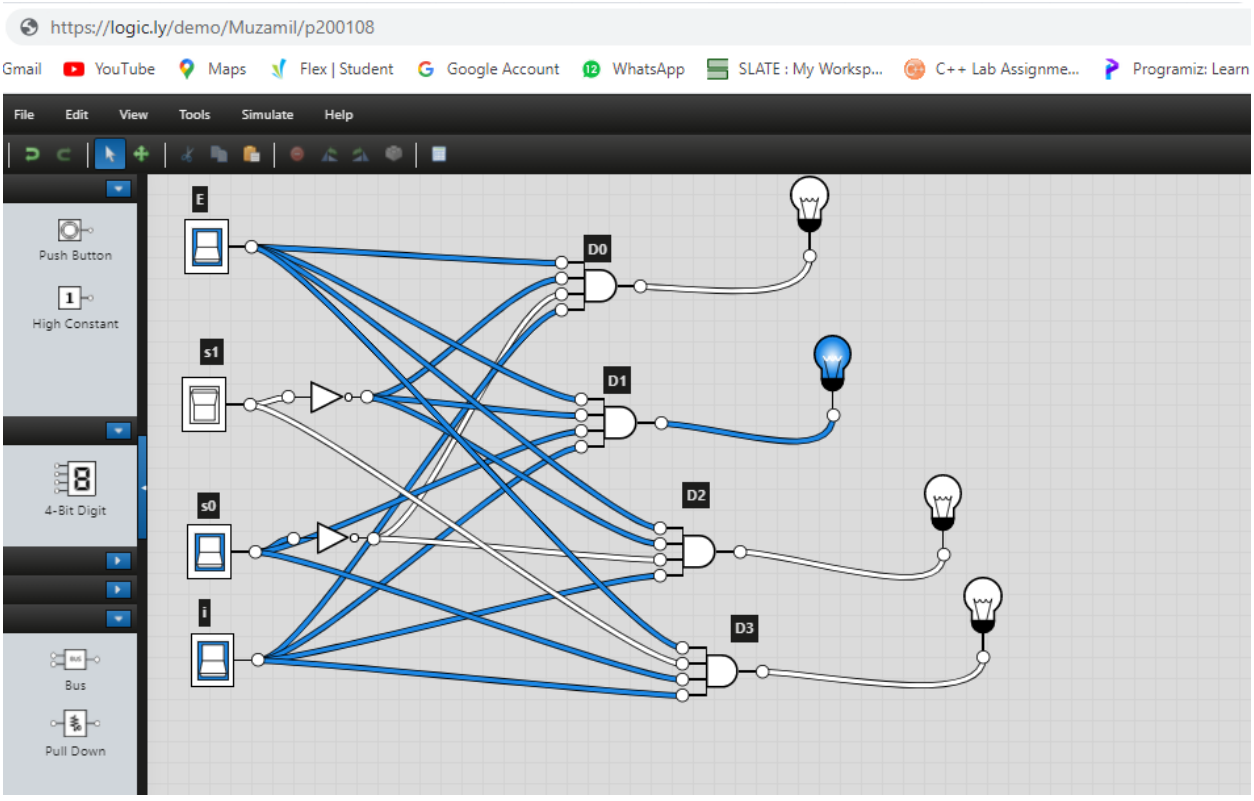
b) Boolean Expression

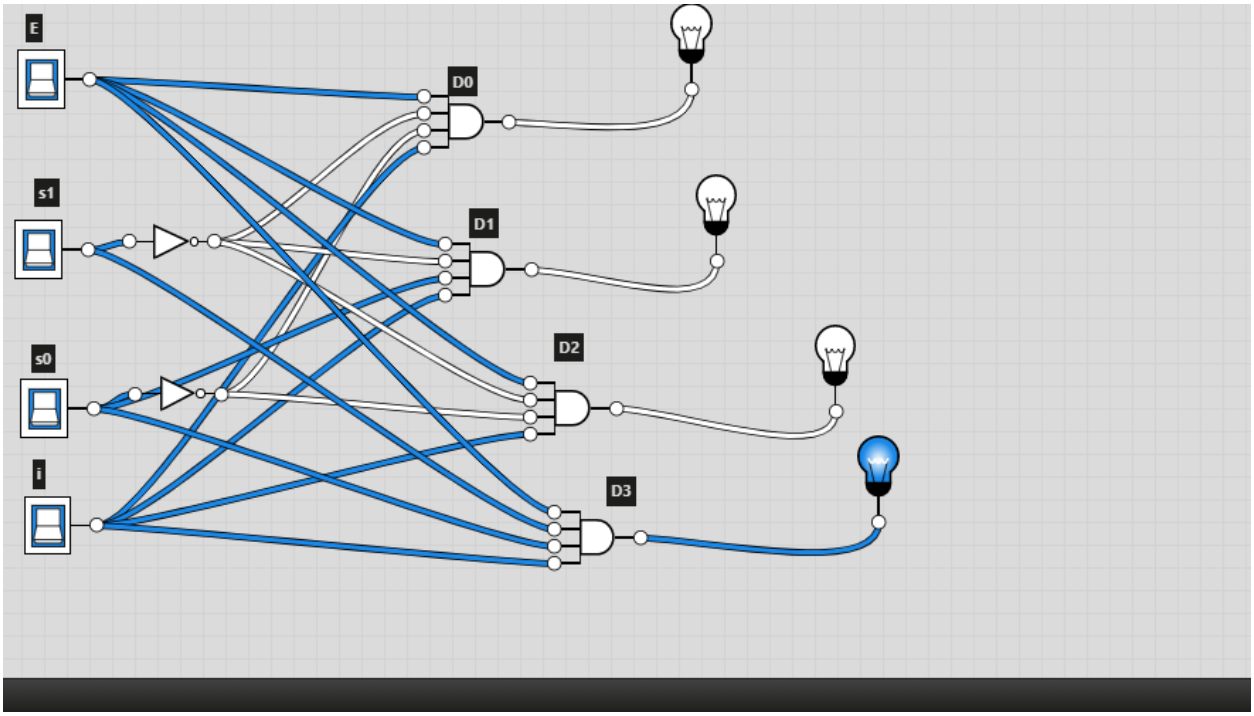


c) Logic Diagram



d) Software Simulation

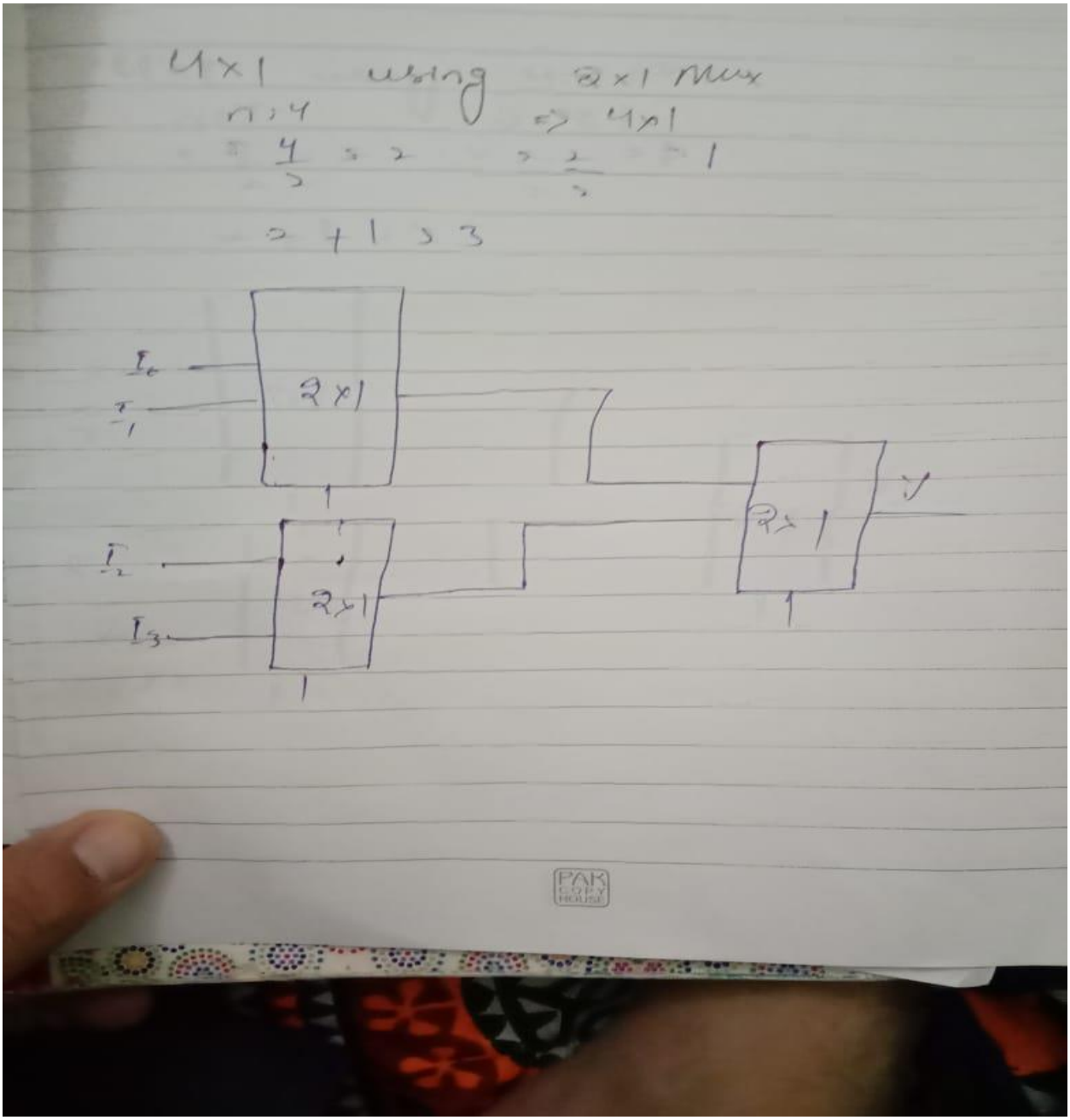




3. **Design a circuit for 4 to 1 Multiplexer using 2 to 1 Multiplexer(s). You can take help from google or the link below. Just ignore the coding language discussed in the link.**

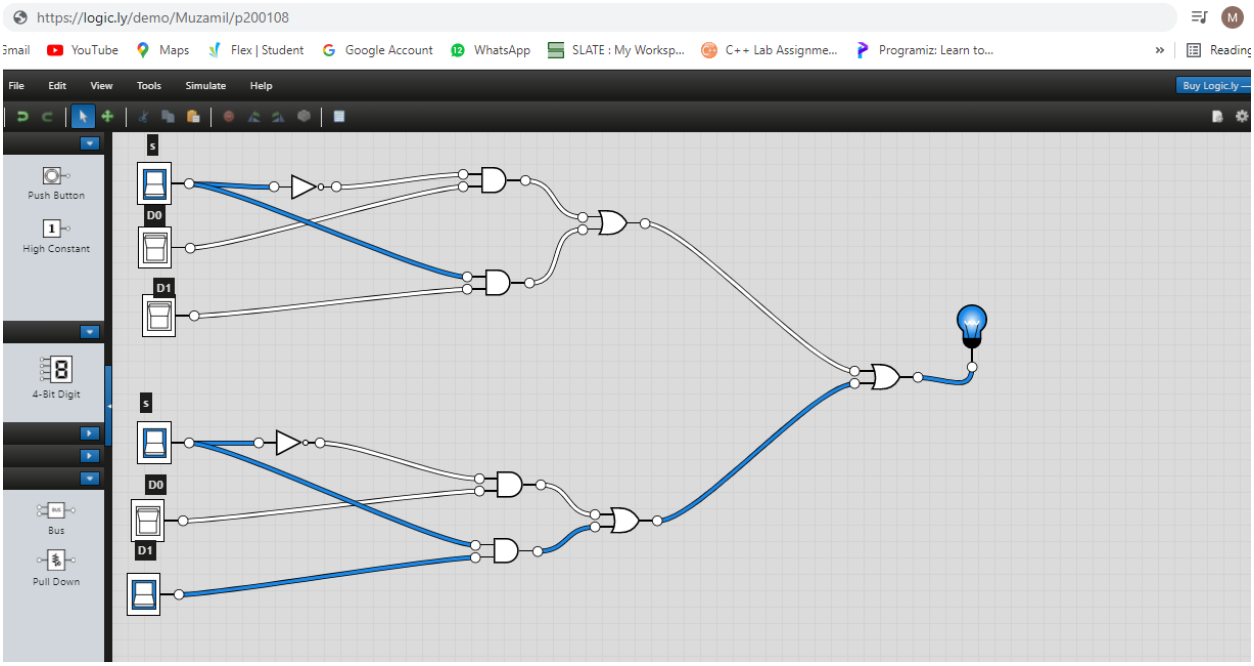
https://bravelearn.com/design-of-4x2-multiplexer-using-2x1-mux-in-verilog/

b) Block Diagram



c) Logic Circuit (on the basis of 2 to 1 Muxes used/follow the block diagram to draw this circuit)

*You need to connect three **2 x1 Multiplexers** in order to make one **4x1 Multiplexer**.*


https://logic.ly/demo/Muzamil/p200108
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Google Account
WhatsApp
SLATE : My Worksp...
C++ Lab Assignme...
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4-Bit Digit
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Pull Down
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