

## Lab 11

### To Explain the Working of LATCHES and Implement SR & D LATCH

**Note: For all the circuits in the tasks, your logic diagrams should be either hand drawn or from the software logically. Keep them neat and legible. These circuits will be having many connections so, for simulations, make sure that you label the inputs and outputs clearly. Use Label tag in “logically”. You can also edit the pictures of your outputs in “paint” easily.**

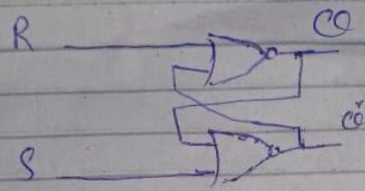
#### Tasks

1. Construct a logic circuit for SR LATCH. Simulate your circuit to verify the outputs. Also, show its working in terms of a timing diagram. You can take any random timing diagram and display it here. The waveforms should be hand-drawn (neatly).

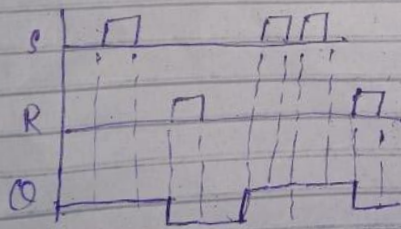
#### SR LATCH

- a) Logic Diagram   b) Truth Table   c) waveform

## Logic Diagram



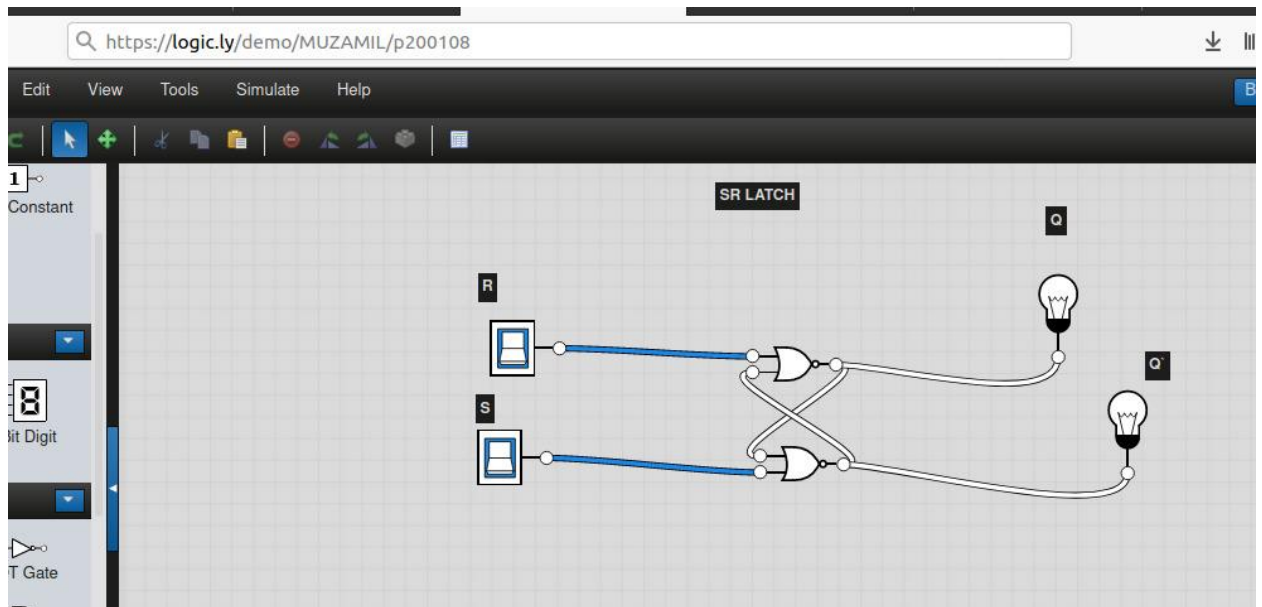
## Timing diagram



## Truth table

S	R	Q	Q
0	0	latch	latch
0	1	0	1
1	0	1	0
1	1	0	0

b) Software Simulation

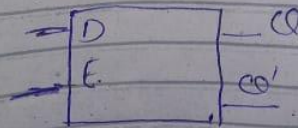
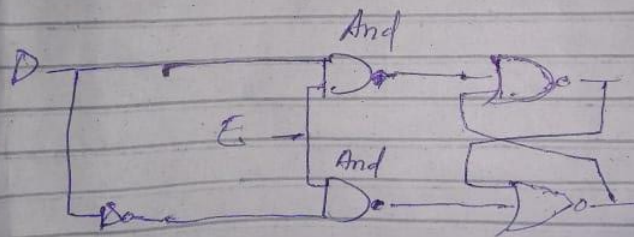


2. **Construct a logic circuit for D LATCH. Simulate your circuit to verify the outputs. Also, show its working in terms of a timing diagram. You can take any random timing diagram and display it here. The waveforms should be hand-drawn (neatly).**

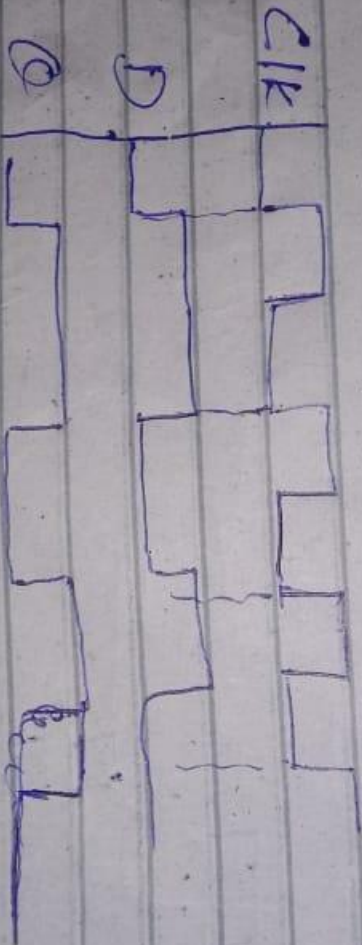
a) Logic Diagram and wave form and Truth table

# Truth table

E	D	Q	Q'
1	1	1	0
1	0	0	1
0	1	0	0'
0	0	0	0'



# Timing Diagram



## b) Software Simulation

