Lab 5

To Demonstrate the Working of Binary Adders

Note: You may draw all the logic diagrams with hand and paste the pictures here or on logicly software with your name, roll number & section mentioned in your workspace. Make sure that all of your connections are clearly visible and distinguishable.

Tasks

1. **Construct a logic circuit for half and full adder with the help of truth table. Also write the Boolean expression for output(s).**

Half Adder

a) Truth Table

A	B	output(S)	C
0	0	o	0
0	1	1	0
1	0	1	0
1	1	0	1

b) Boolean Expression (Simplified)

S=A'.B+AB'

C=A.B

c) logic diagram("It is degined in picture")

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Half Adder

Truth Table

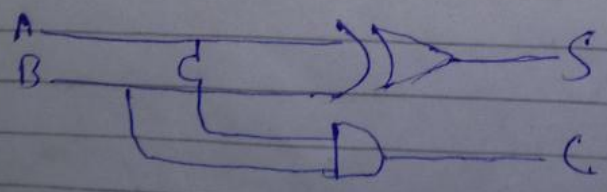
A	B	Sum	Carry(C)
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Boolean expression

$S = A\bar{B} + \bar{A}B = A \oplus B$

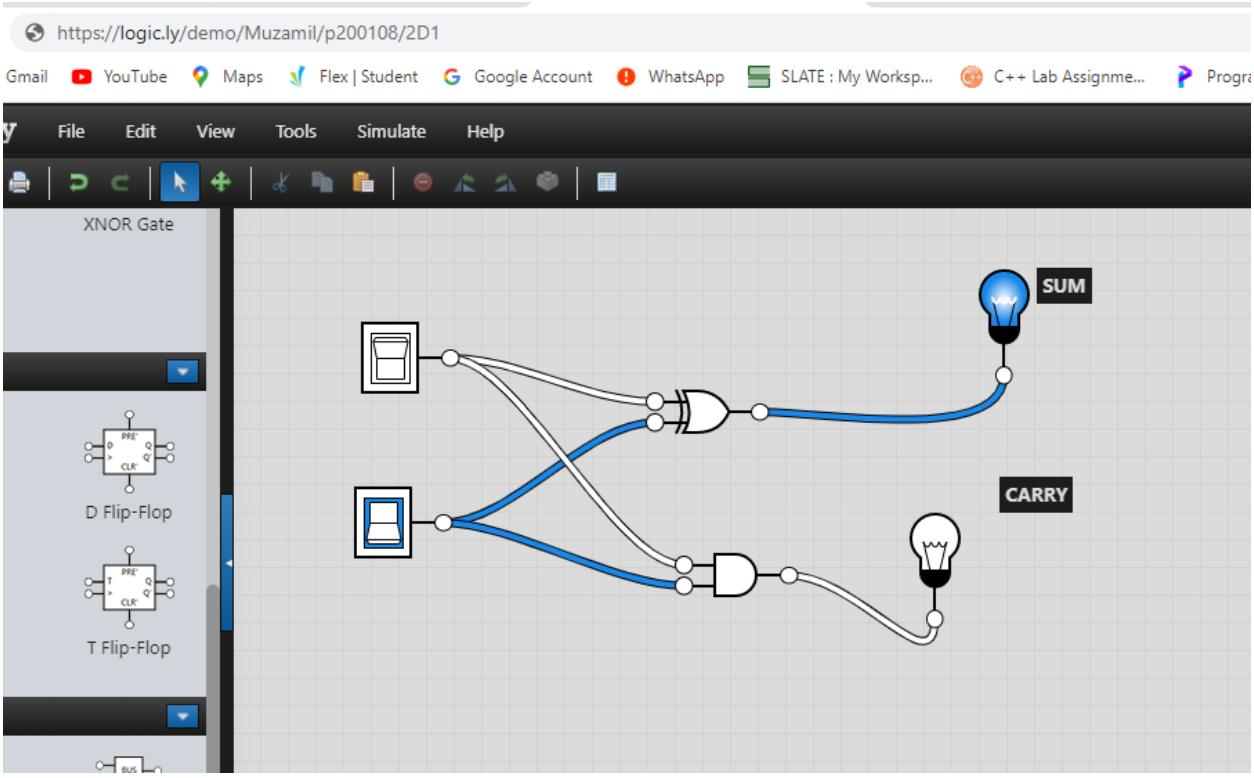
$C = AB$

Logic Diagram

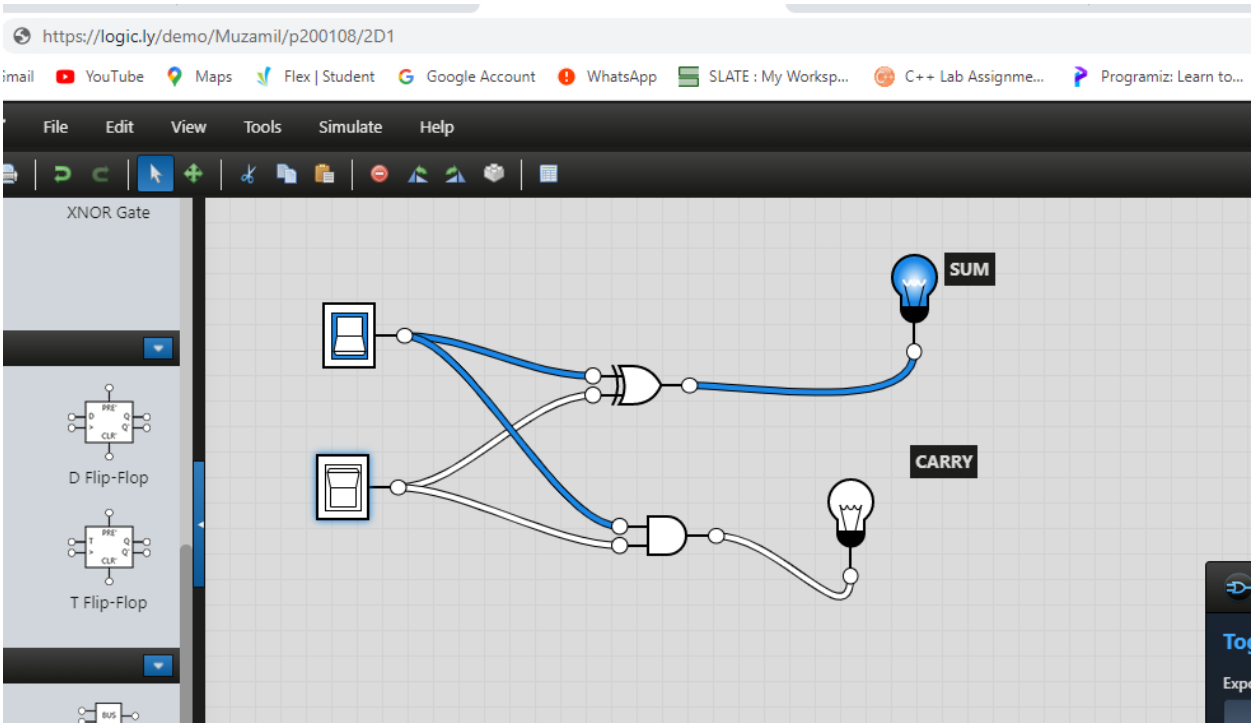


d) Software Simulation (Show here your results for each combination that gives a high output)

Inputs are 0 and 1 and output/ sum is 1 and carry is 0



Inputs are 1 and 0 and output/ sum is 1 and carry is 0



Full Adder

a) Truth Table

A	B	C	sum	carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

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Full Adder:

Truth table:

Inputs			outputs	
C_{in}	A	B	S	C
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

$\therefore S = \bar{A}B\bar{C_{in}} + A\bar{B}\bar{C_{in}} + \bar{A}\bar{B}C_{in} + A$

$S = \bar{C_{in}}(\bar{A}B + A\bar{B}) + C_{in}(\bar{A}\bar{B} + AB)$

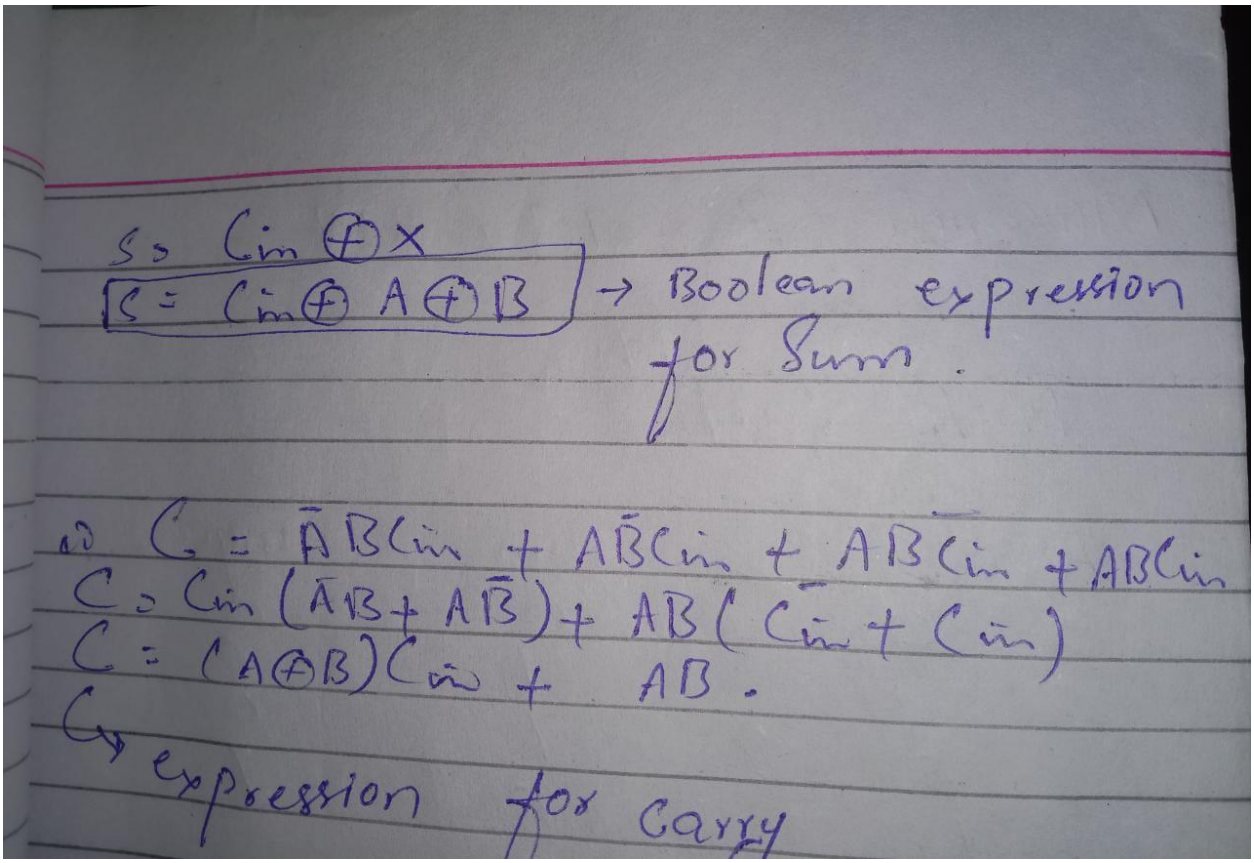
i. $\bar{A}B + A\bar{B} = A \oplus B$

ii. $\bar{A}\bar{B} + AB = A \odot B$

$S = \bar{C_{in}}(A \oplus B) + C_{in}(\bar{A} \odot B)$

$A \oplus B \rightarrow X$

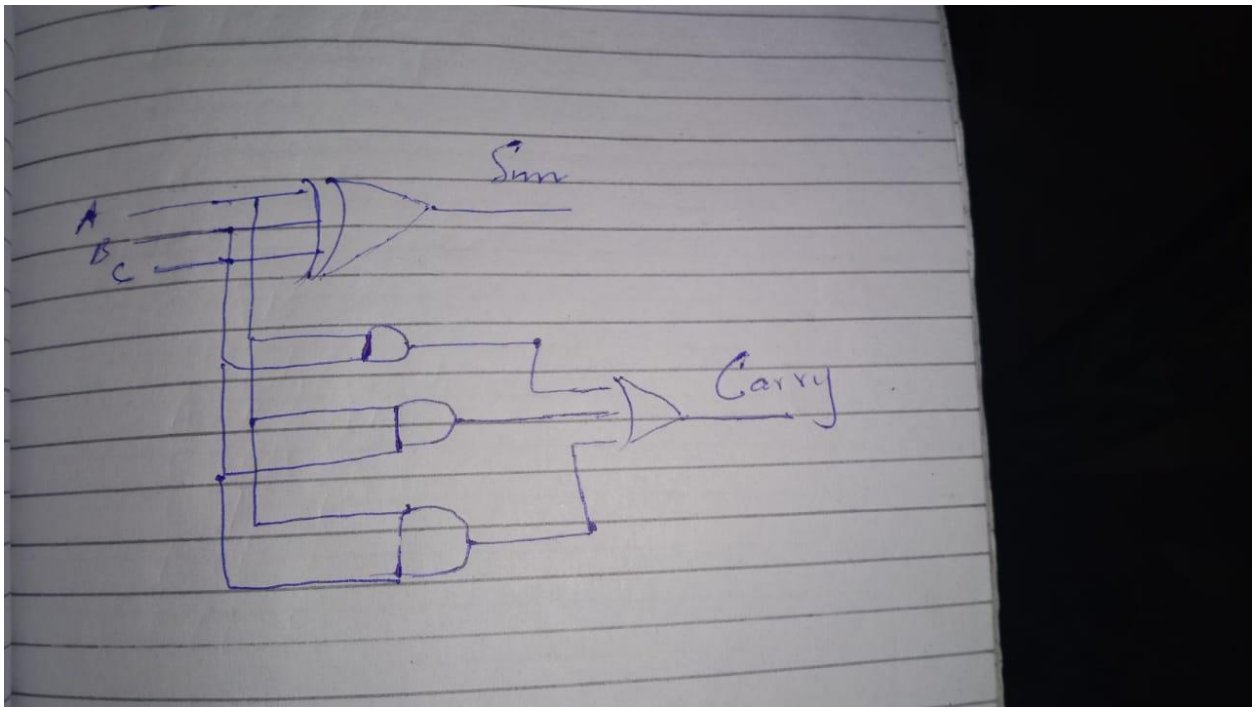
$\bar{A} \odot B \rightarrow \bar{X}$



b) Boolean Expression (Simplified)

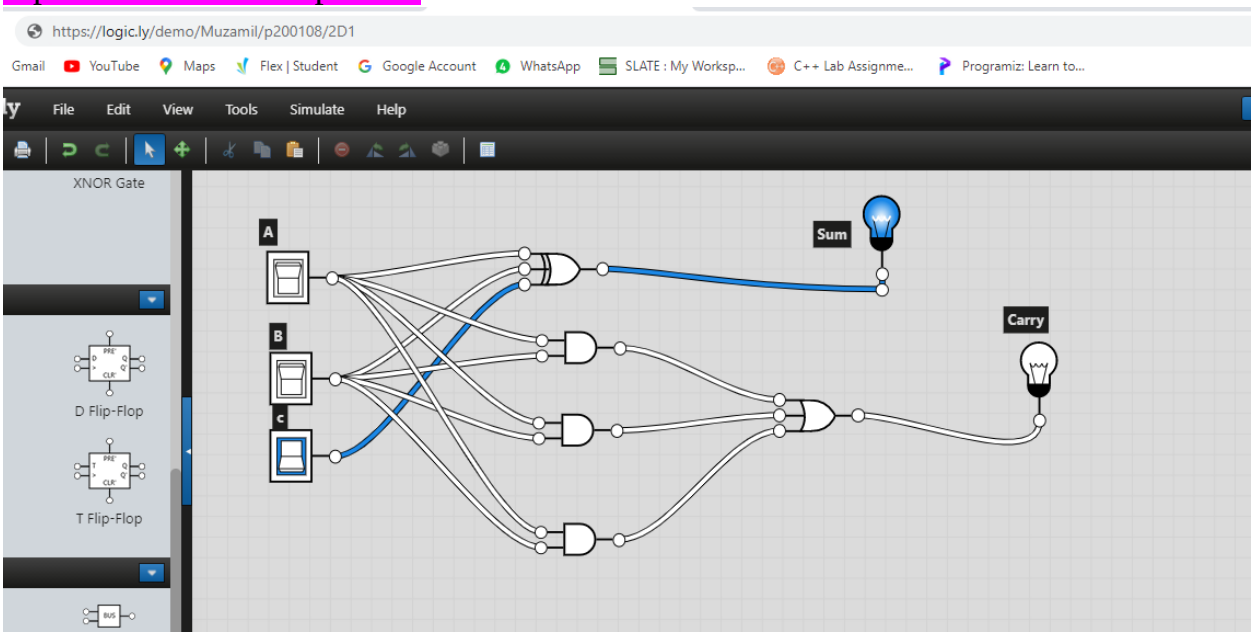
Expression is written in the picture

c) Logic Diagram

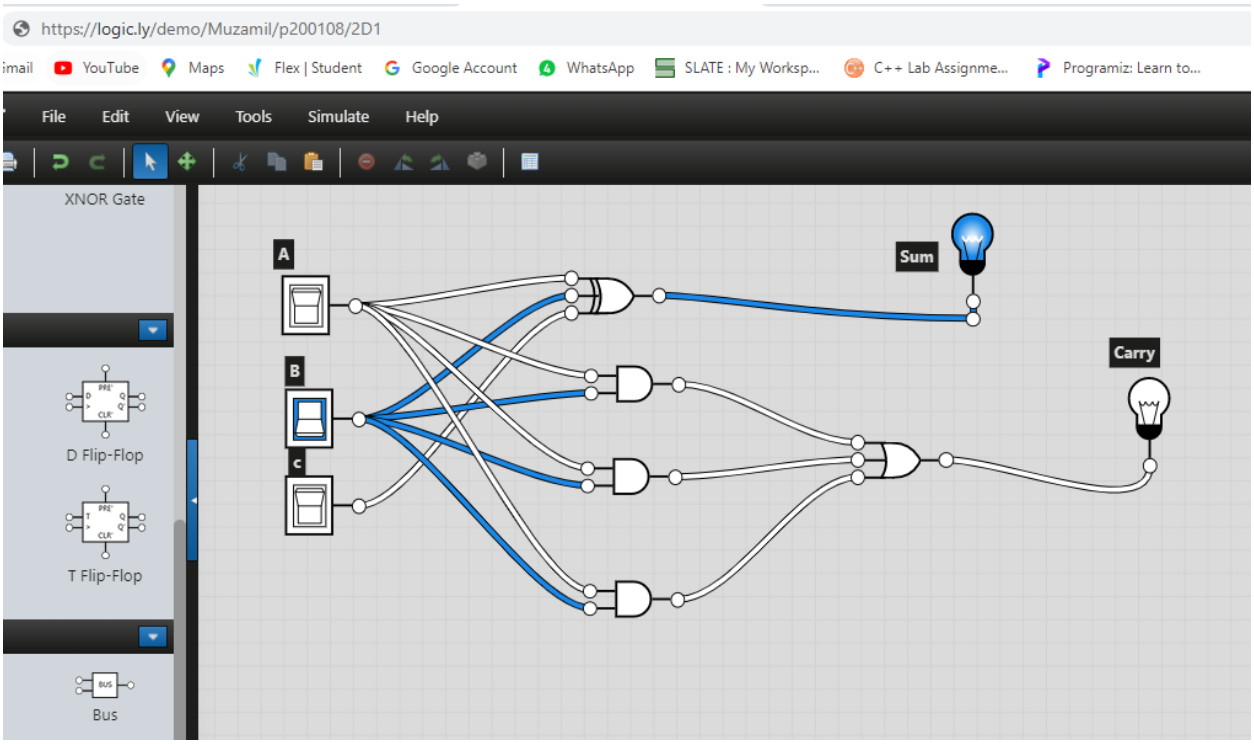


d) Software Simulation (Show here your results for each combination that gives a high output)

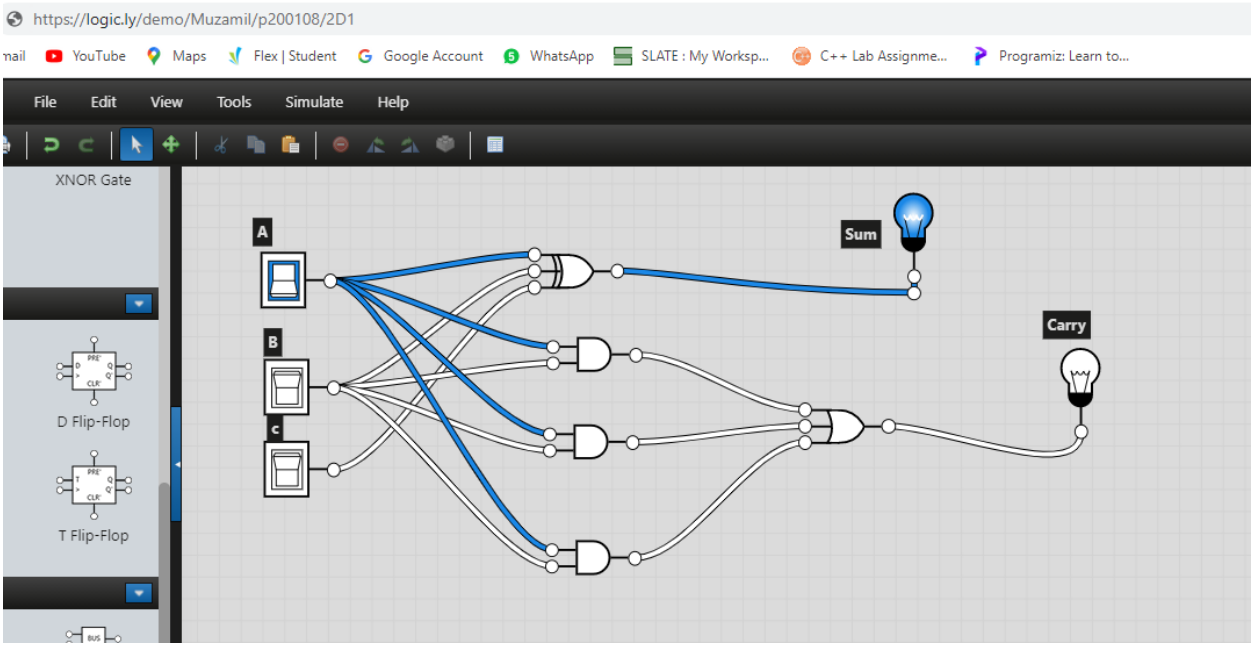
Inputs are 001 and ouput is 1



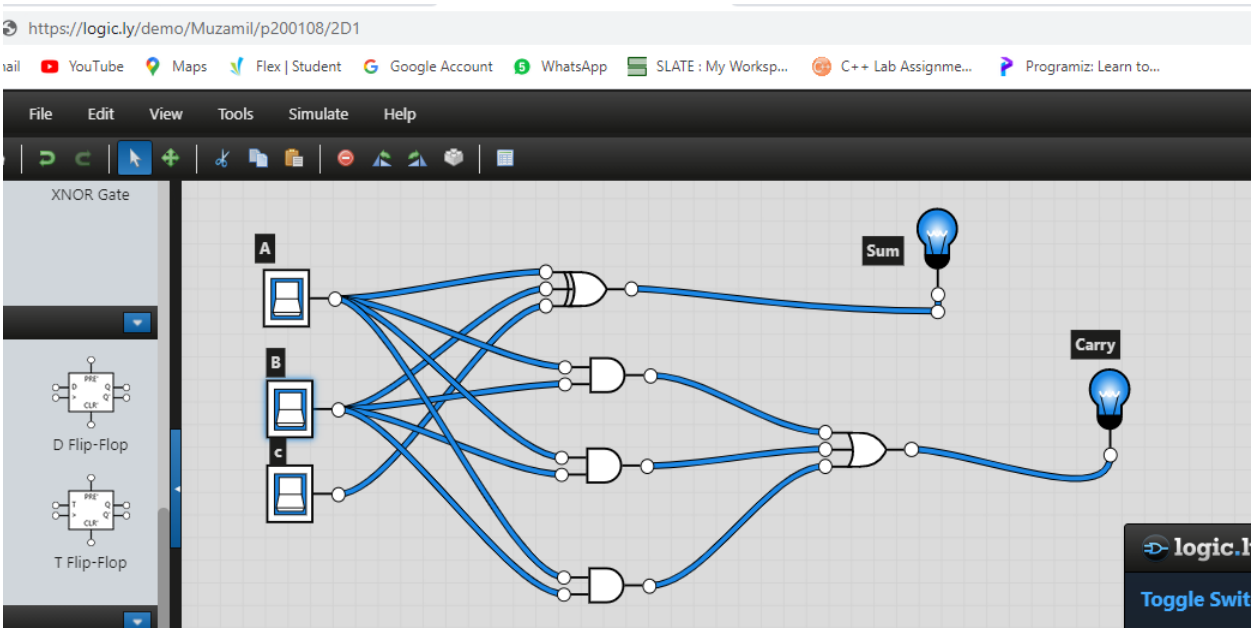
Inputs are 010 and output is 1



Inputs ARE 100 and output is 1

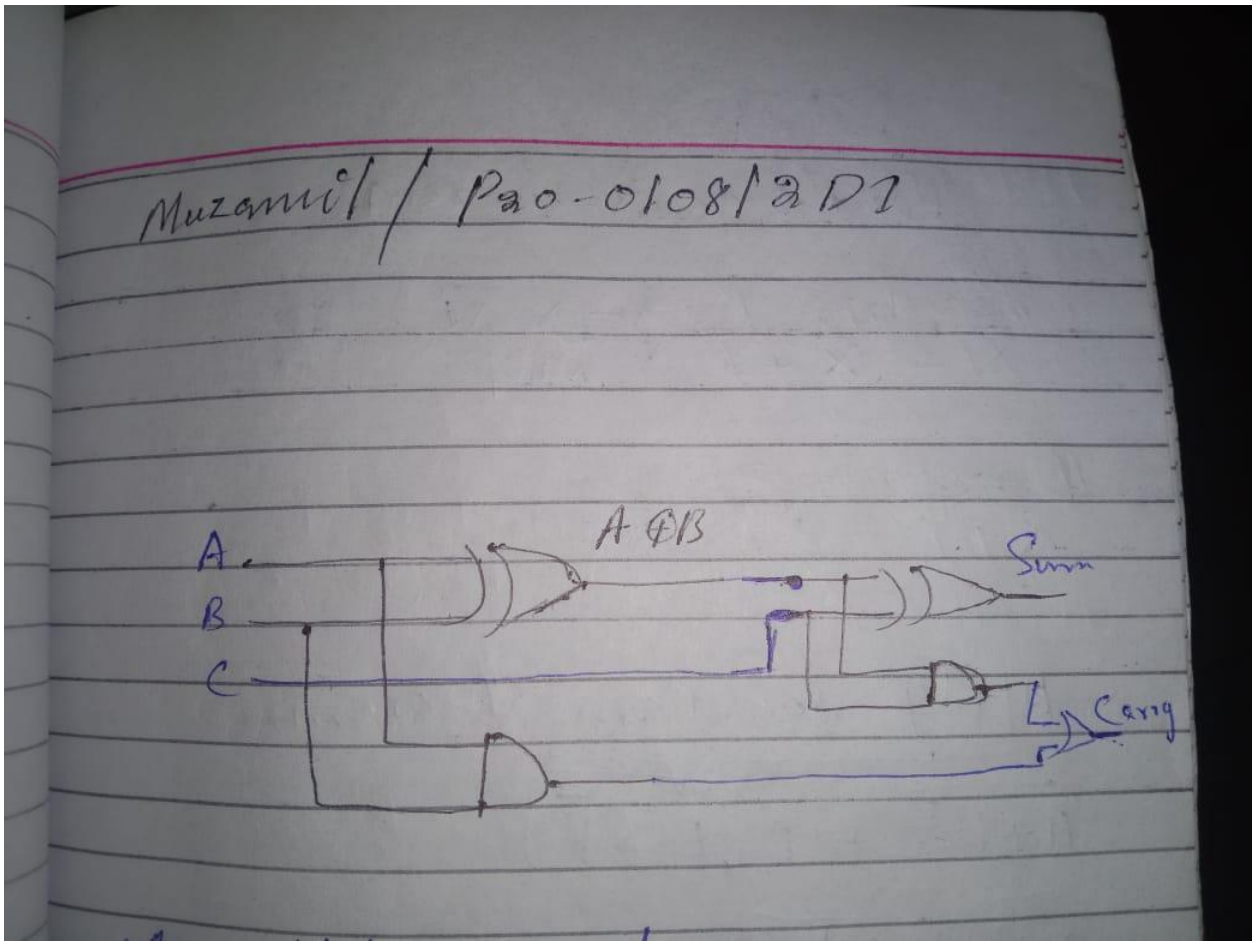


Inputs are 111 and output is 1



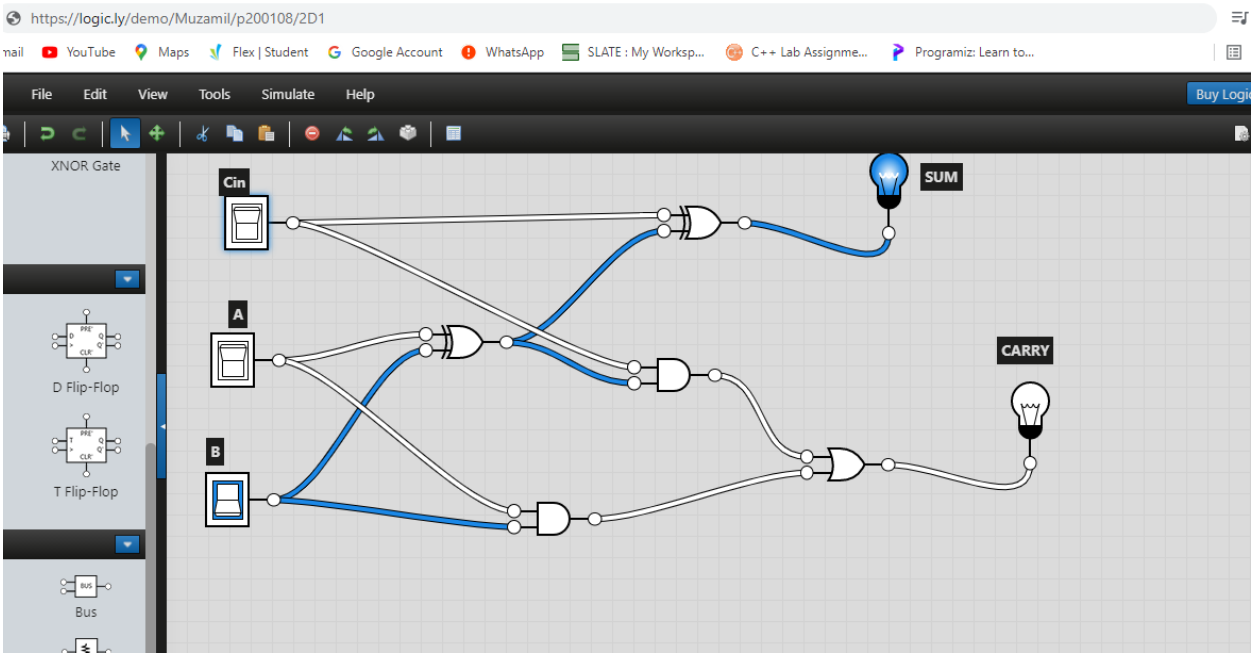
2. A full adder can be implemented using 2-half adders. Demonstrate the logic diagram for the said circuit. Simulate your circuit for the verification of results.

a) Logic Diagram of Full Adder using 2-Half Adders

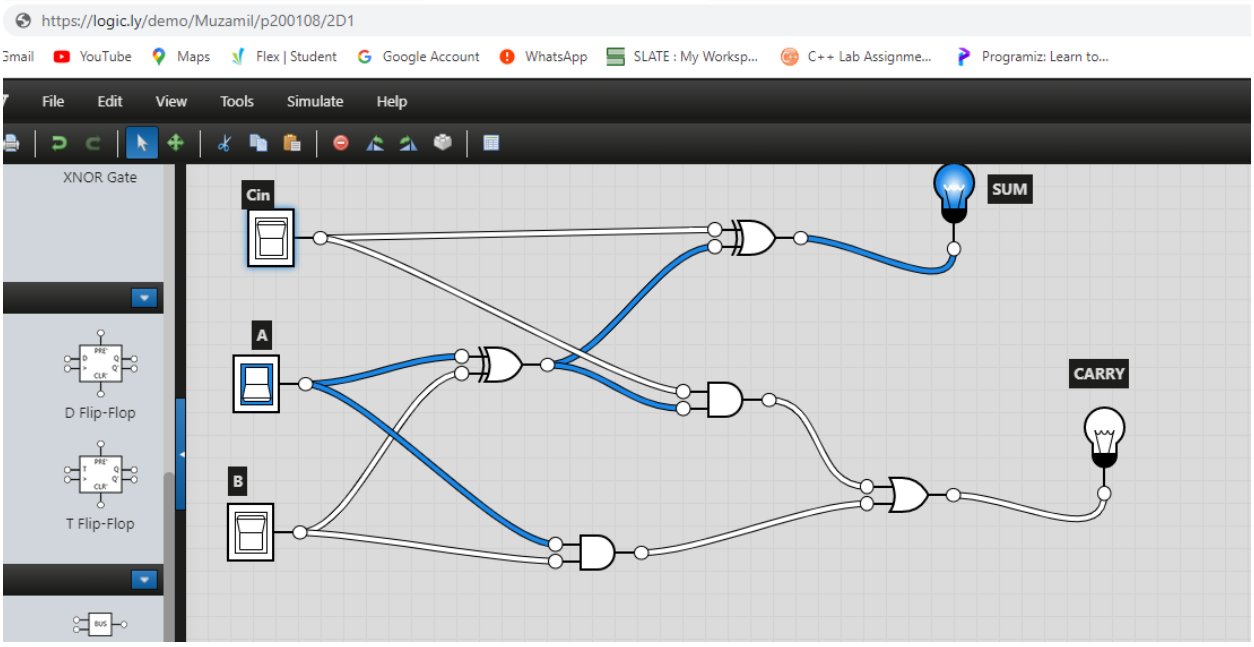


b) Software Simulation (Show here your results for each combination that gives a high output)

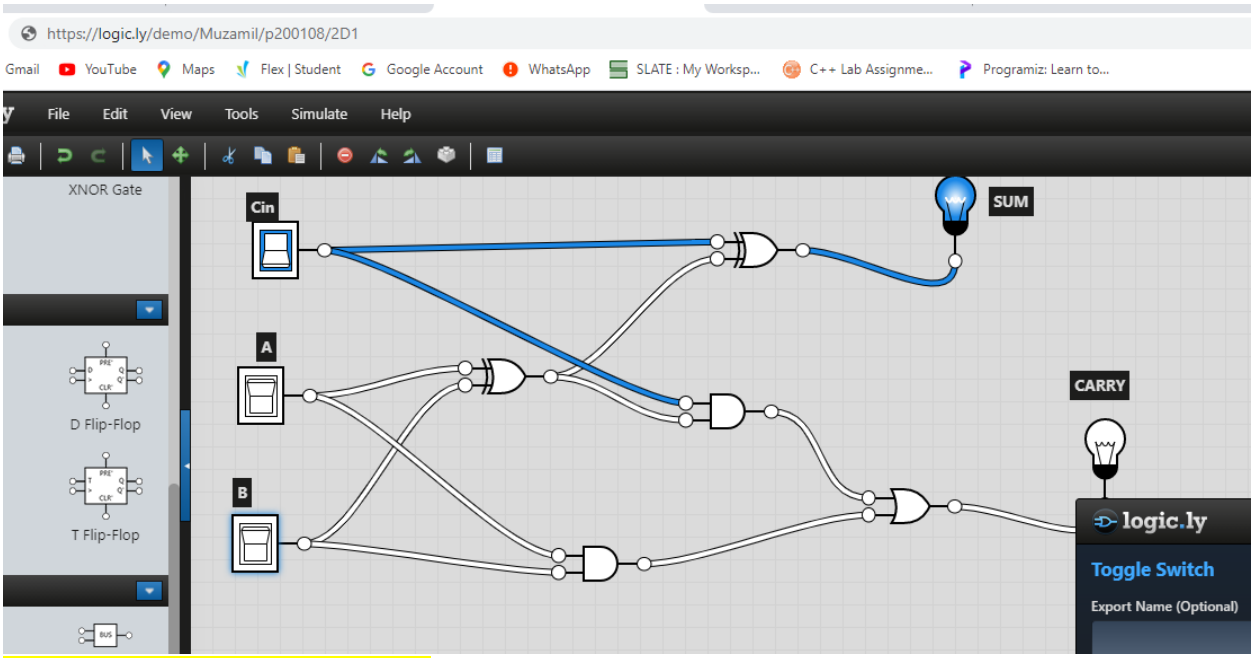
Inputs are 0 0 1 and output is 1



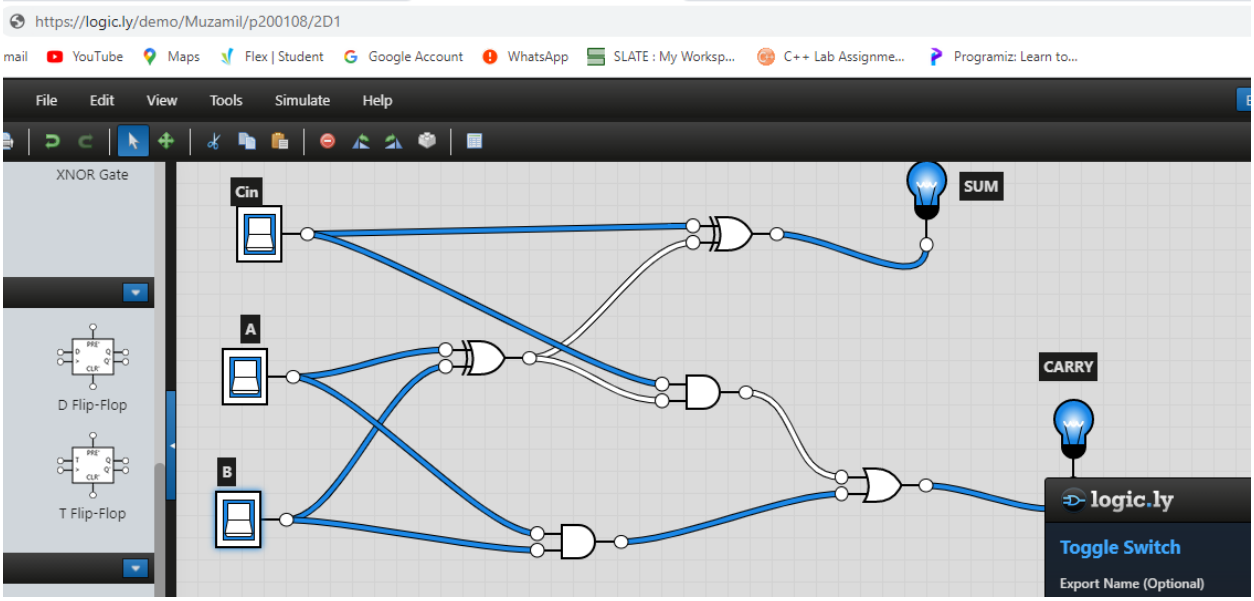
Inputs are 0 1 0 and output is 1



Inputs are 1 00 and output is 1



Inputs are 111 and output is 1



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LAB TASK #5
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