COSC 221: Computer Organization I

Fall 2013

Exam #1

Date: **Monday, October 7, 2013**

Time: **10:30 a.m. – 12:20 p.m.**

(Closed Notes*, Closed Books)

49/100

Last Name: Wonsey

First Name: Zane

Student ID#: 0102 1309

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* You may use the calc app on the iMac in front of you.
* No web browsing.
* Bring/use pencil and eraser.
* Any illegible answers will considered incorrect.

-51

A. True or False. Write the word *"True"* if the statement is true and *"False"* if the statement is false, in the spaces provided. (2 points each; **20 points**)

true 1. If a floating-point number is represented in normalized form, the most significant digit is non-zero.

true 2. The exponent of an IEEE Floating point number is encoded in 2's complement representation.

false 3. The sign extension operation does not affect the values of the numbers being represented.

true 4. Combinational logic circuits are structures whose outputs are dependent on past history of information that is stored internally.

true 5. Circuits that contain both p-type and n-type transistors are called CMOS circuits.

false 6. Given the two 2's complement integers A = 1110101 and B = 10101, we can state that A is greater than B.

false 7. A decoder is used to select one of many inputs.

false 8. If m is a power of 2, the number of select lines required for an m-input multiplexer is $\log_2 m$.

true 9. The following addition operation will generate an overflow 11100 + 11100.

true 10. Given *n* bits, the maximum unsigned integer that can be represented is given by 2^n.

/12

B. Problem Solving. (80 points)

1. (5 points) What is the hexadecimal equivalent of the decimal number **55**? Show how you obtained your answer.

32 16 8 4 2 1
1 1 0 1 1 1

16 + 16 + 16 + 7

16 | 55 r 7
16 | 3 r 3

x37

15 + 15 + 15 + 7 + 3

FFFA

0
1
2
3
4
5
6
7
8
9
a 10
b 11
c 12
d 13
e 14
f 15

2. (5 points) Exactly how many distinct items can be uniquely represented with 6 bits?

000000
32 16 8 4 2 1

64

-10

-17

3. What is the 6-bit string that represents **-8** if we use the following representations?

a. (3 points) Signed magnitude

001000

101000 -0

b. (3 points) 1's complement

110111 -0

c. (3 points) 2's complement

-0

111000

d. (3 points) Excess-32

+/- 16 8 4 2 1

000000

011000 -0

4. (5 points) Find the sum of the following 2s complement binary strings: **111101 + 110**.

-3 sign ext

sign extention problem

```
 111101
+000110
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 000011
```

overflow

-3

5. Identify both the 8-bit mask and the Boolean operation needed to accomplish each of the following objectives:

   a. (5 points) Round-off a given unsigned integer to the next closest even number less than or equal to the given number, e.g., 2 → 2, 5 → 4.

and XXXX XXXX
1111 1110
XXXX XXX0

-5

   b. (5 points) Convert any decimal digit into its corresponding ASCII value.
   Note: '0' = 0011 0000, '1' = 0011 0001, '2' = 0011 0010, …, '9' = 0011 1001.

8 = 0011 1000

XXXX XXXX
or 0011 0000
XX11 XXXX

-5

6. (5 points) Convert the decimal fraction **4.6215** to binary with minimum of 5 places to the right of the binary point. Show how you obtained each bit.

0100.100111110001

2 x .6215 = 1.243
2 x .243 = 0.486
2 x .486 = 0.972
2 x .972 = 1.944
2 x .944 = 1.888
2 x .888 = 1.776
2 x .776 = 1.552
2 x .552 = 1.104
2 x .104 = 0.208
2 x .208 = 0.416
2 x 0.416 = 0.832
2 x 0.832 = 1.664

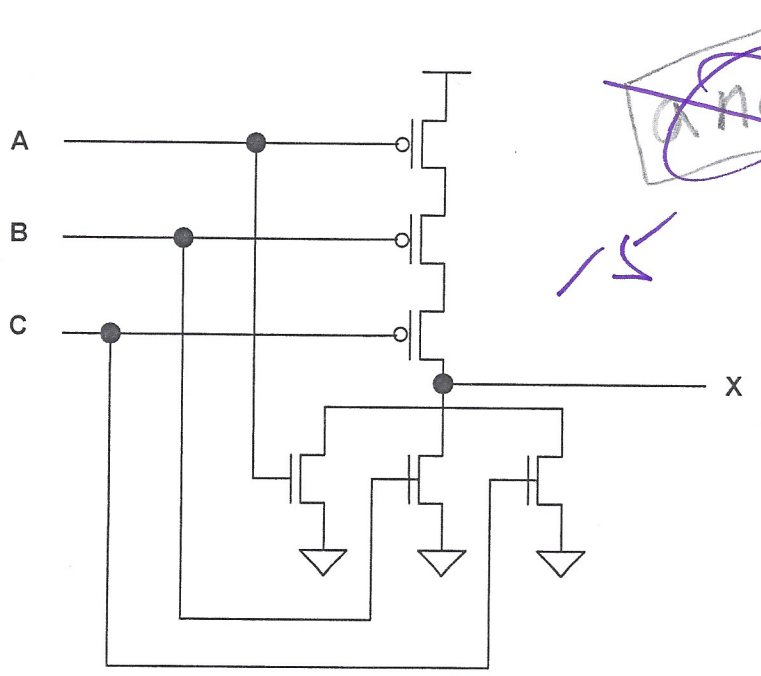
-10

7. (5 points) Give the single-precision IEEE 754 bit pattern for the following normalized binary value:

$1.1101010 \times 2^{-128}$

0000. 127 0's 11101010

8. (5 points) The following is a transistor-level circuit for a three-input logic gate. What logic gate does it represent?



and

3 input

NOR

-10

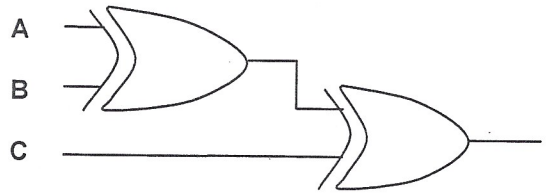
9. (5 points) Briefly describe what needs to be done in order to set the value of the data bit stored in an R-S latch to a 1.

quickly set R to 0 then change it back

-2

10. A three-input XOR gate can be represented using two 2-input XOR gates as shown below.

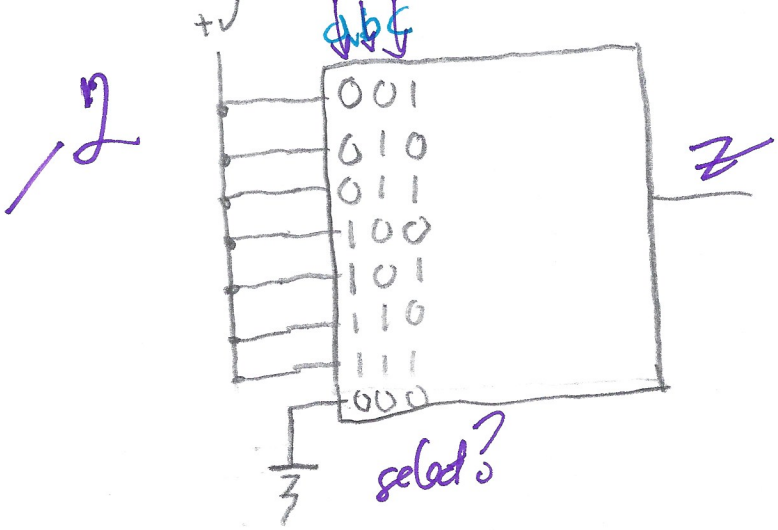
a. (5 points) Complete the truth table for this logic circuit.



A	B	C	Z = A XOR B XOR C
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

-2

b. (5 points) Implement the function Z using an 8-to-1 multiplexer. Label each line.



-2

-6

c. (5 points) Generate the gate-level logic circuit for the function Z using a PLA.