RK3399_EVB_TB_LPDDR4 Ver1.1

Version	Date	Author	Change Note	Approved
V1.0	2018.01.11	Linus.Lin	First edictor 基于《RK_EVB_SOCBOARD_3399_LPDDR4P366SD8_V12_20170801_LX》修改,更新page39	

Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3399_EVB_TB_LPDDR4_200P		
File:	00.Modify note		
Date:	Thursday, January 11, 2018	Rev:	V1.1
Designed by:	Linus	Sheet:	1 of 22

RK3399 I2C MAP

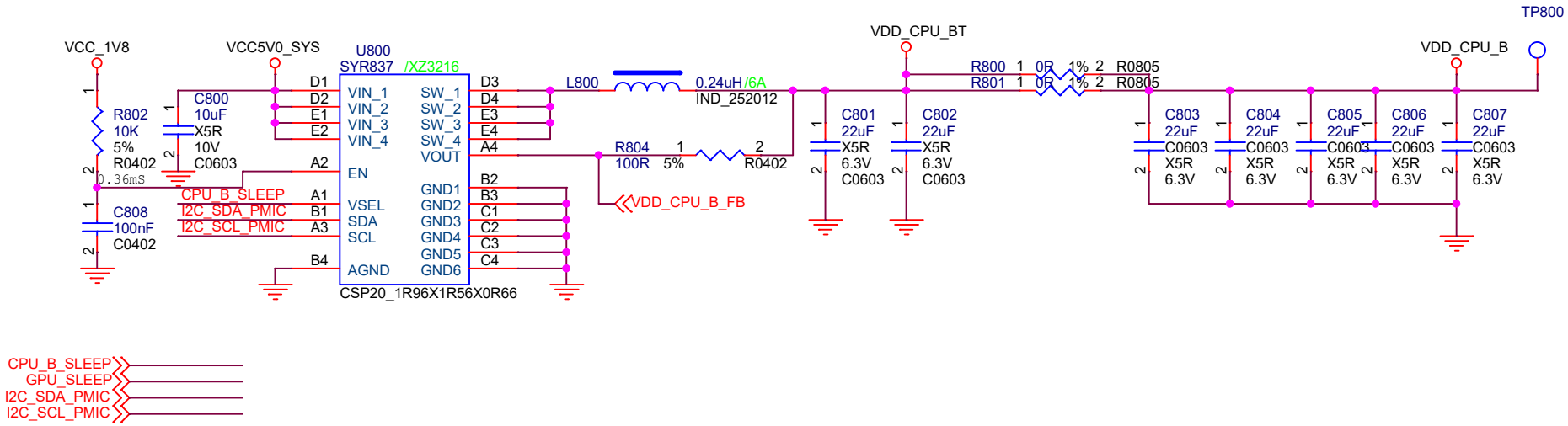
Port	Pin name	Domain	Bus name	Pull-up voltage	Slave Device	Slave Addr (MS 7Bits)	Note	Slave Bus Capability
I2C0	GPIO1_B7/SPI3_RXD/I2C0_SDA GPIO1_C0/SPI3_TXD/I2C0_SCL	PMUIO2 VCC1V8_PMU	I2C_SDA_PMIC I2C_SCL_PMIC	VCC1V8_PMU	MPS MP8865GQ	0x68,0x60	DC regulator	100kHz,400KHz FM, 3.4MHz HS mode
					Rohm BD99955MWV	0x12	Charger	10K-400KHz(SMBus)
					Rockchip RK808	0x1b	PMIC	
					Fairchild FUSB302B	0x44,0x46	USB-TypeC Mux	0-1MHz(FM+)
I2C1	GPIO4_A1/I2C1_SDA GPIO4_A2/I2C1_SCL	APIO5 VCC1V8_IO	I2C_SDA_AUDIO I2C_SCL_AUDIO	VCCA1V8_CODEC	Everest ES8316	0x10	Audio codec	
			I2C_SDA_CAM I2C_SCL_CAM	VCCA1V8_CODEC	Omnivision OV8858	0x6c,0x20	MIPI Camera	
I2C2	GPIO2_A0/VOP_D0/CIF_D0/I2C2_SDA GPIO2_A1/VOP_D1/CIF_D1/I2C2_SCL	APIO2 VCC1V8_IO	Other pin function					
I2C3	GPIO4_C0/I2C3_SDA/UART2B_RX GPIO4_C1/I2C3_SCL/UART2B_TX	APIO4 VCC3V0_IO	I2C_SDA_HDMI I2C_SCL_HDMI	VCC3V0_IO				
I2C4	GPIO1_B3/I2C4_SDA GPIO1_B4/I2C4_SCL	PMUIO2 VCC1V8_IO	I2C_SDA_MEMS I2C_SCL_MEMS	VCC1V8_PMU	Capellamicro CM3218	0x10,0x0c	ALS Sensor	
					AsahiKasei AK8963C		Compass	
					InverSense MPU6500	0x34	Accer+Gyro	
			I2C_SDA_TOUCH I2C_SCL_TOUCH	VCC1V8_TOUCH	Silead GSL3680	0x40	Touch panel	
I2C5	GPIO3_B2/MAC_RXER/I2C5_SDA GPIO3_B3/MAC_CLK/I2C5_SCL	APIO1 VCC3V3_LAN	I2C_SDA_PCIE I2C_SCL_PCIE	VCC3V3_IO				
I2C6	GPIO2_B1/SPI2_RXD/CIF_HREF/I2C6_SDA GPIO2_B2/SPI2_TXD/CIF_CLKIN/I2C6_SCL	APIO2 VCC1V8_IO	I2C_SDA_BAT I2C_SCL_BAT	VCC1V8_DVP	Chrome Battery	0x19	Battery	100KHz
I2C7	GPIO2_A7/VOP_D7/CIF_D7/I2C7_SDA GPIO2_B0/VOP_CLK/CIF_VSYNC/I2C7_SCL	APIO2 VCC1V8_IO	Other pin function					

Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics
Project:	RK3399_EVB_TB_LPDDR4_200P
File:	01.I2C Map
Date: Thursday, January 11, 2018	Rev: V1.1
Designed by: Linus	Sheet: 2 of 22

RK3399 Power Domain Map

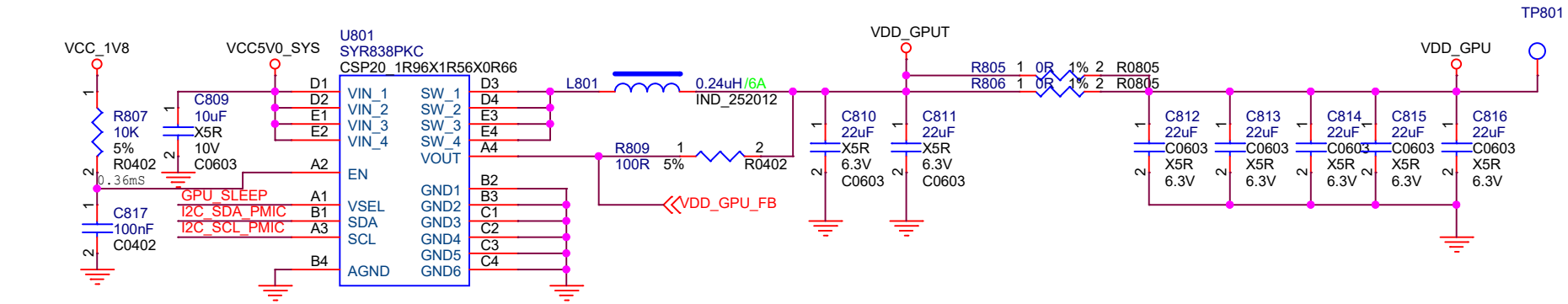
Part Port	Domain	Pin name in datasheet	I/O type	Power supply	Power source
Part C	PMUIO1	PMUIO1_gpio0ab	1.8V only	VCC1V8_PMU	RK808 VLDO3
Part E	PMUIO2	PMU1830_gpio1abcd	1.8V(Default) 3.0V	VCC1V8_PMU	RK808 VLDO3
Part I	APIO1	GMAC_gpio3abc	3.3V only	VCC1V8_IO VCC3V3_IO	RK808 Buck4 RK808 VSW2
Part L	APIO2	BT656_gpio2ab	1.8V(Default) 3.0V	VCC1V8_DVP	RK808 VLDO1
Part G	APIO3	WIFI/BT_gpio2cd	1.8V only	VCC1V8_WIFI	RK808 Buck4
Part K	APIO4	GPIO1830_gpio4cd	1.8V 3.0V(Default)	VCC_1V5 VCC3V0_IO	RK808 VLDO6 RK808 VLDO8
Part J	APIO5	AUDIO_gpio3d_gpio4a	1.8V(Default) 3.0V	VCCA1V8_CODEC	RK808 VLDO7
Part F	SDMMC0	SDMMC_gpio4b	1.8V 3.0V(Default)	VCC_SDIO	RK808 VLDO4

Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3399_EVB_TB_LPDDR4_200P		
File:	02.Power Domain Map		
Date:	Thursday, January 11, 2018	Rev:	V1.1
Designed by:	Linus	Sheet:	3 of 22

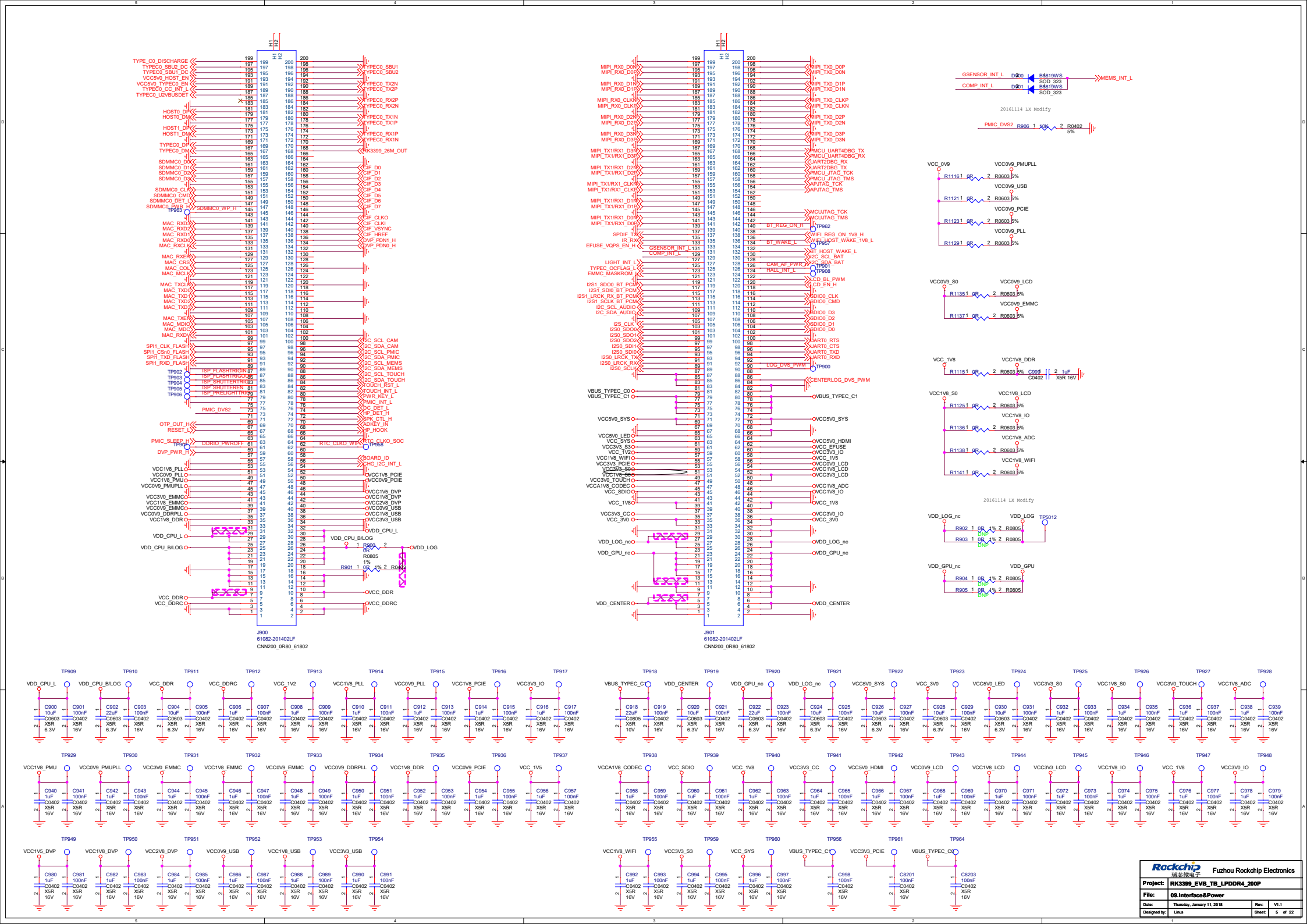


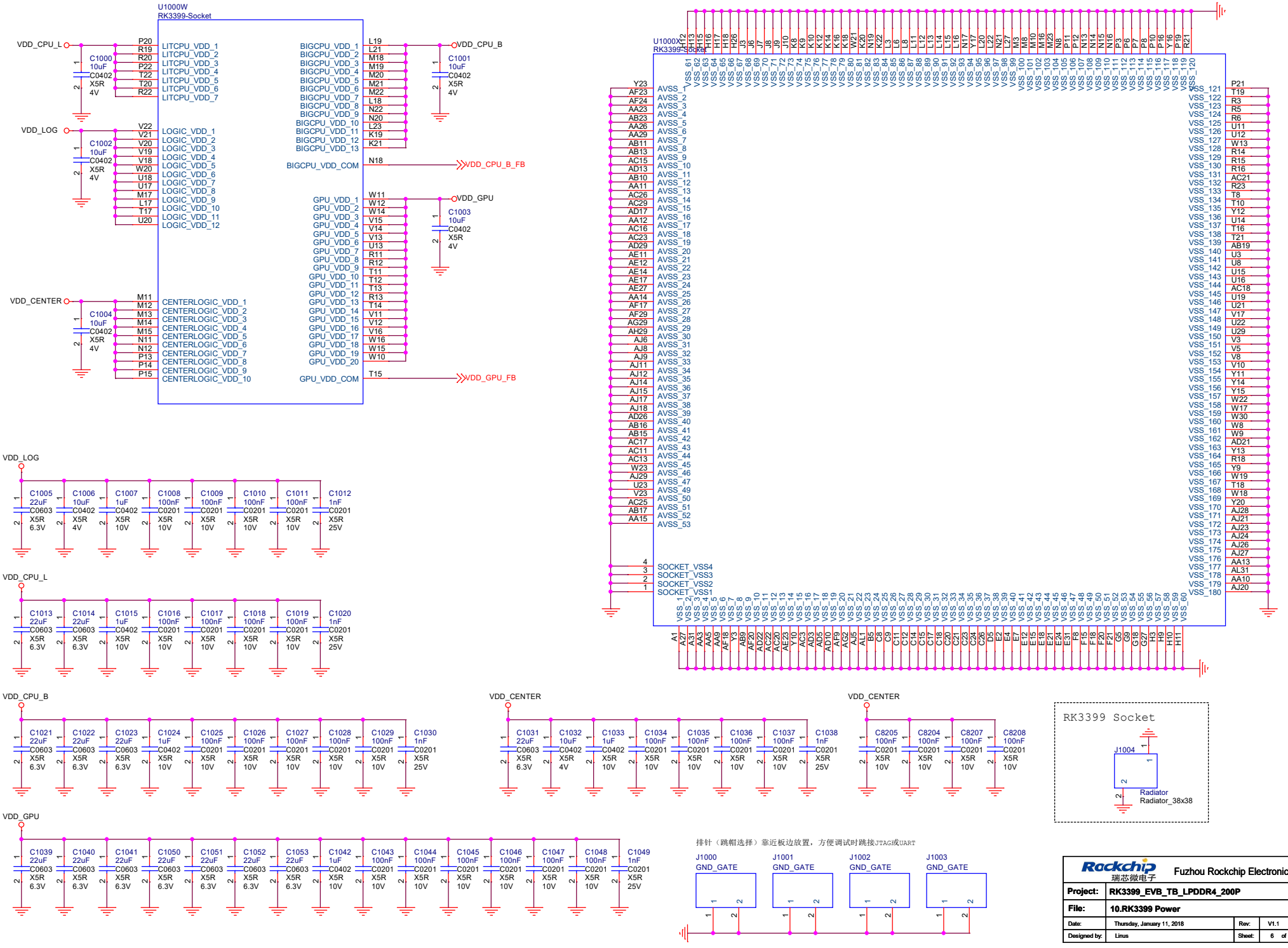
VDD_CPU_B

VDD_GPU

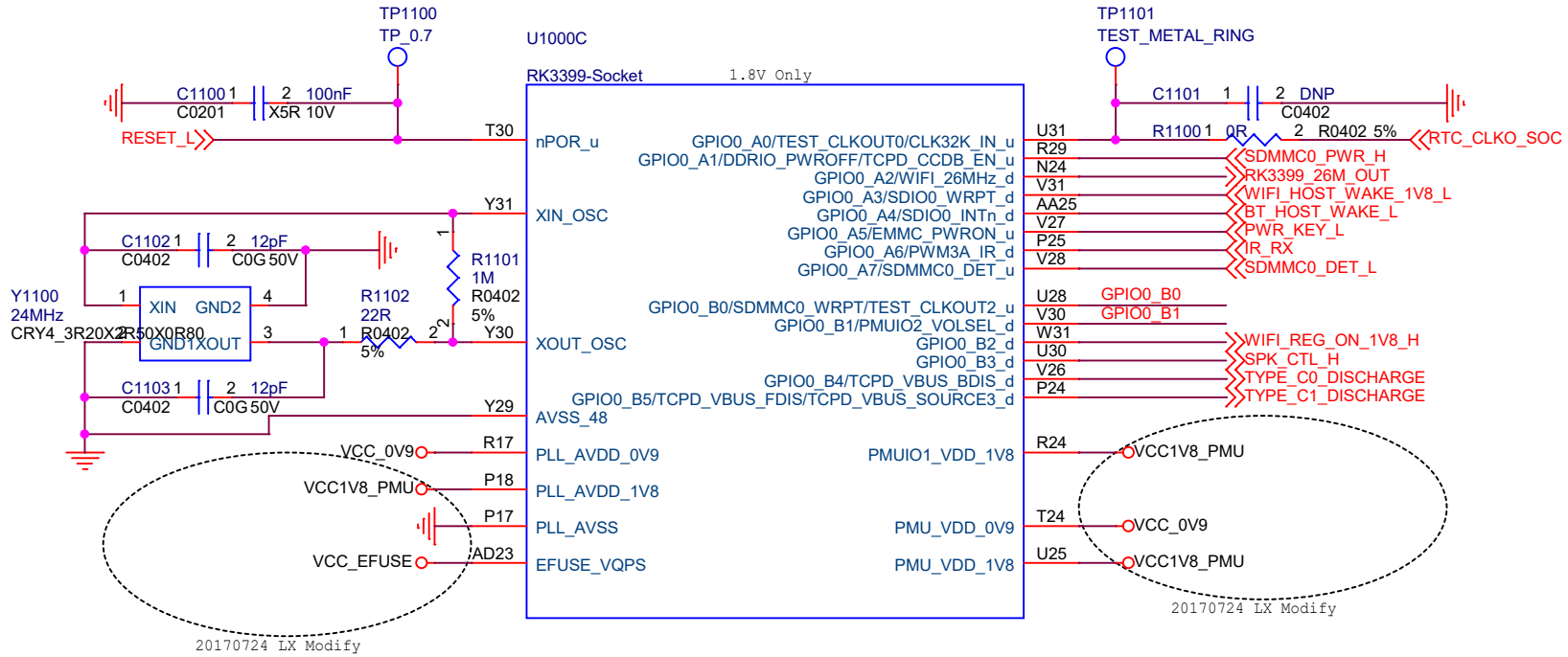


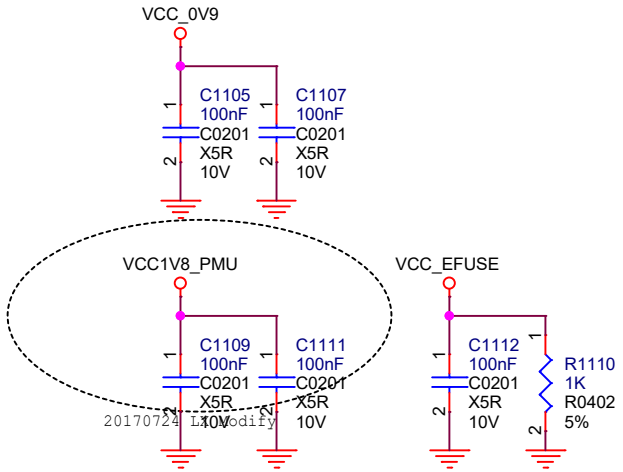
Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3399_EVB_TB_LPDDR4_200P		
File:	POWER		
Date:	Thursday, January 11, 2018	Rev:	V1.1
Designed by:	Linus	Sheet:	4 of 22

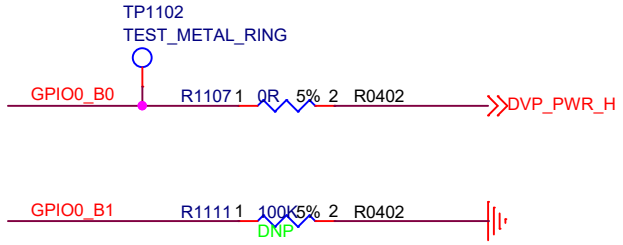

J900
61082-201402LF
CNN200_0R80_61802
J901
61082-201402LF
CNN200_0R80_61802
20161114 LX Modify
20161114 LX Modify
Rockchip 瑞芯微电子
Fuzhou Rockchip Electronics
Project: RK3399_EVB_TB_LPDDR4_200P
File: 09.Interface&Power
Date: Thursday, January 11, 2018
Rev: V1.1
Designed by: Linus
Sheet: 5 of 22



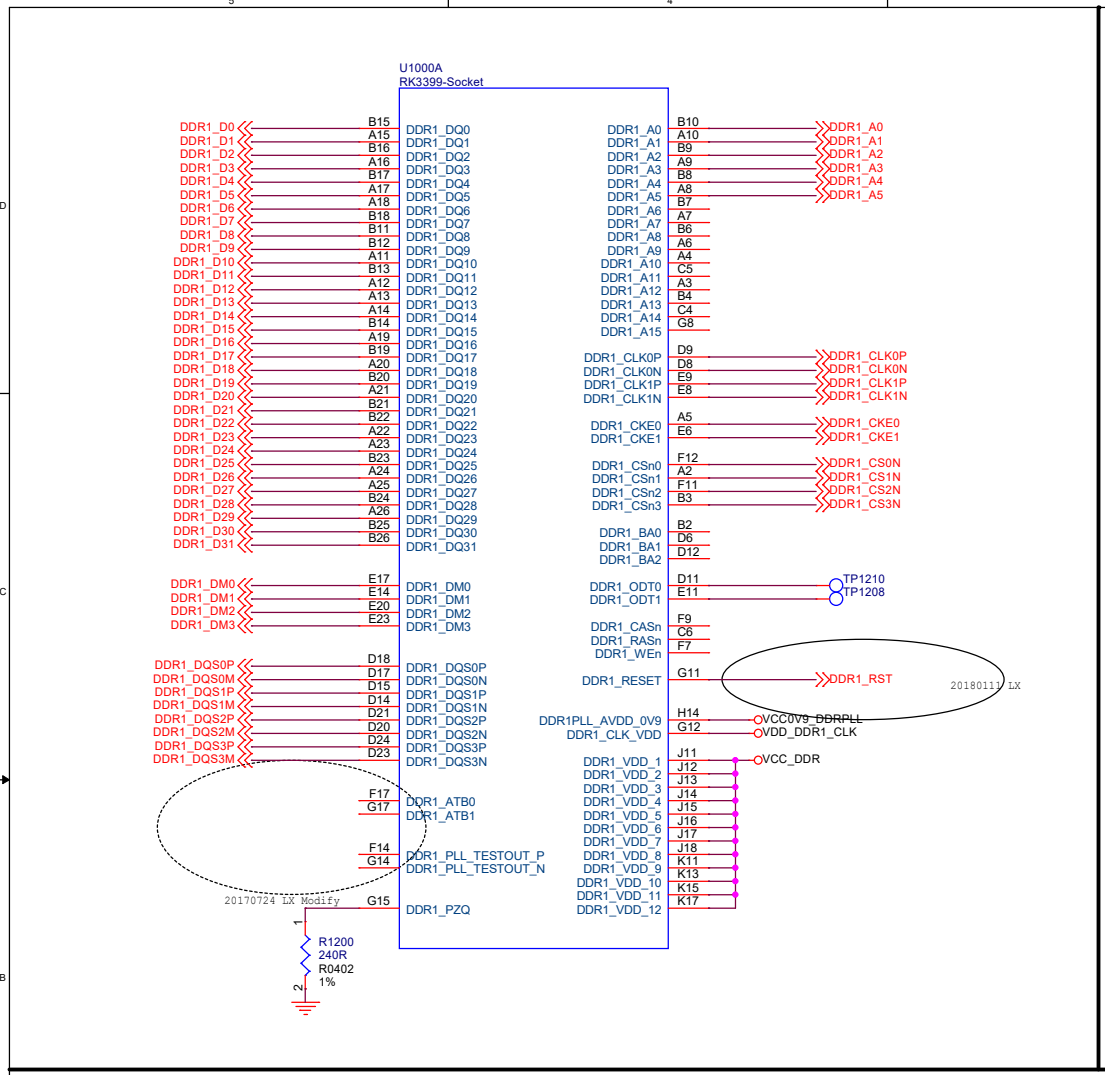
Fuzhou Rockchip Electronics	
Project:	RK3399_EVB_TB_LPDDR4_200P
File:	10.RK3399 Power
Date:	Thursday, January 11, 2018
Rev:	V1.1
Designed by:	Linus
Sheet:	6 of 22

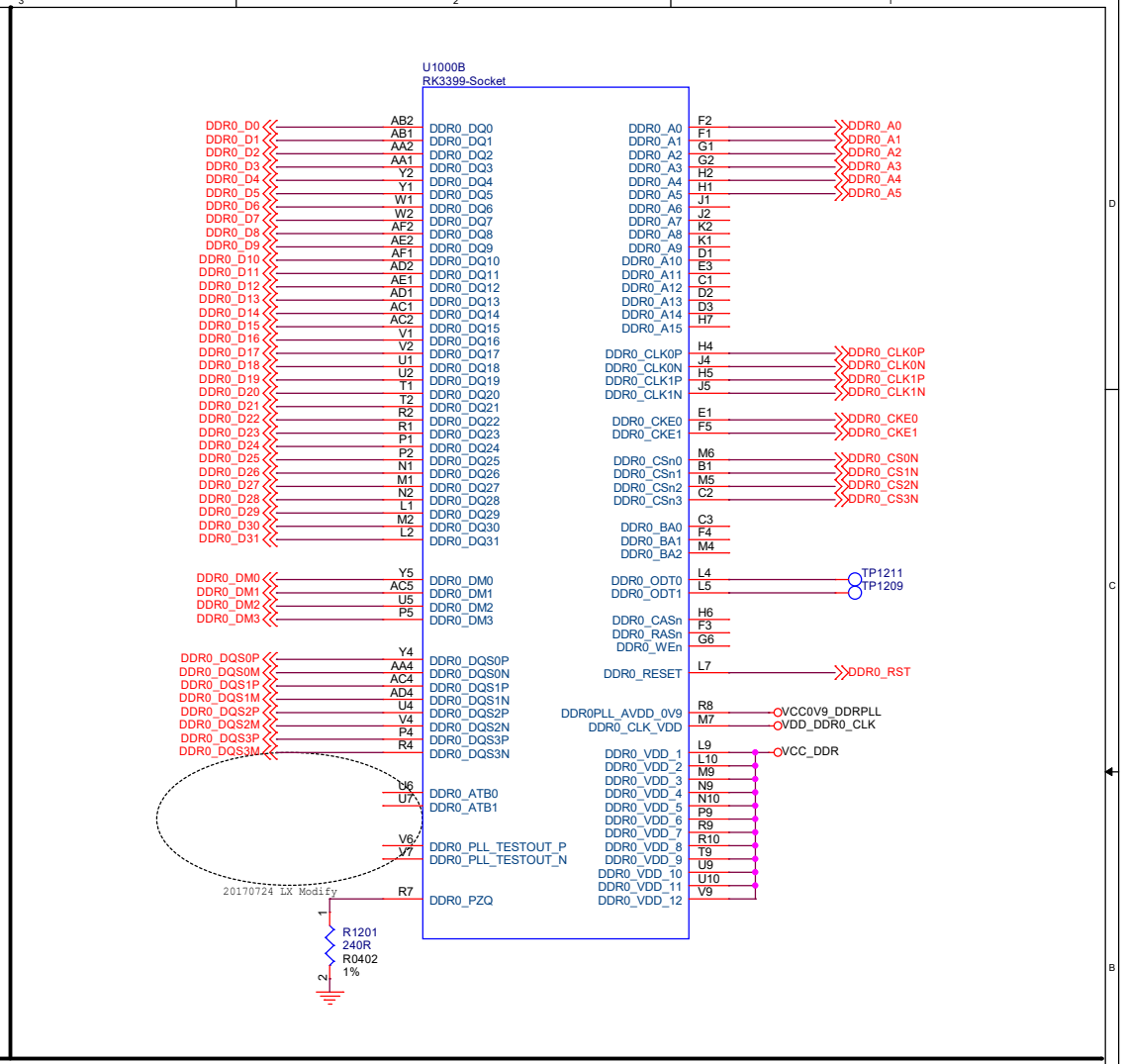




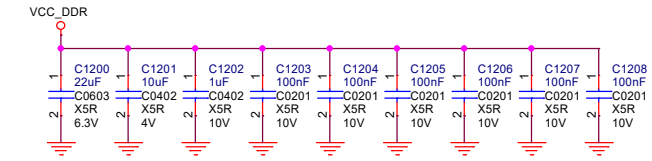


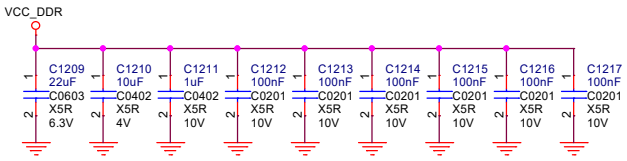
Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3399_EVB_TB_LPDDR4_200P		
File:	11.RK3399 PMU Controler		
Date:	Thursday, January 11, 2018	Rev:	V1.1
Designed by:	Linus	Sheet:	7 of 22

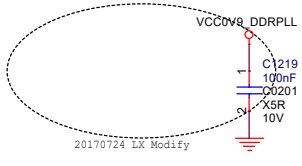


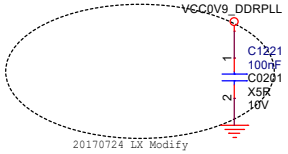


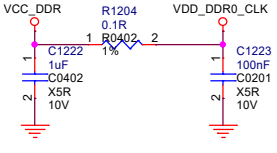
DDR FILTER

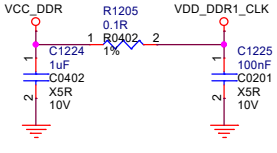




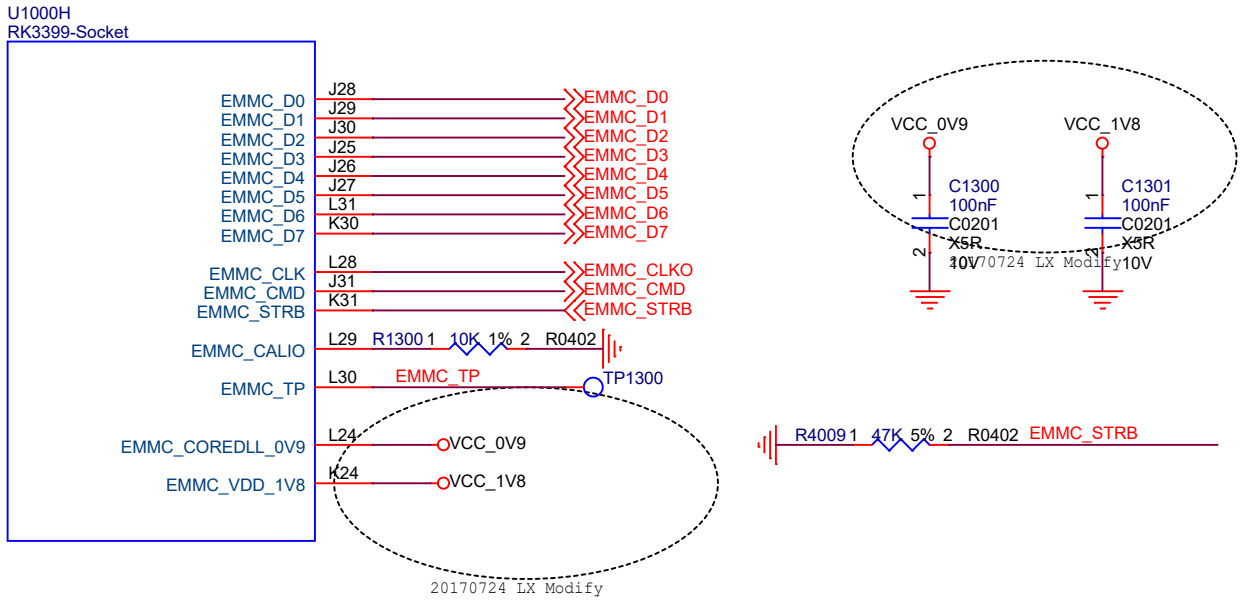


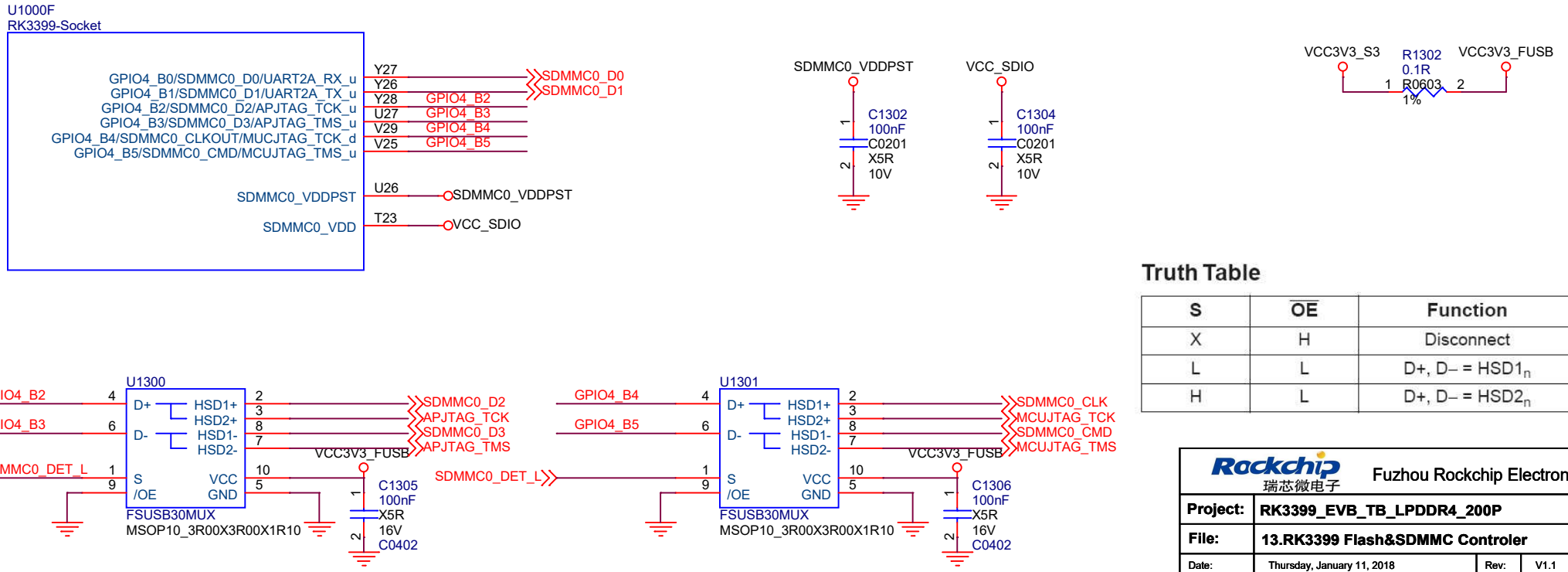






Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3399_EVB_TB_LPDDR4_200P		
File:	12.RK3399 DDR Controler		
Date:	Thursday, January 11, 2018	Rev:	V1.1
Designed by:	Linus	Sheet:	8 of 22

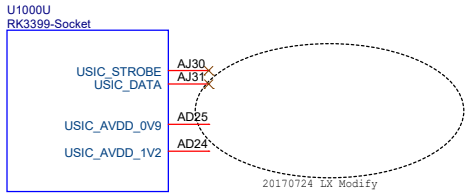


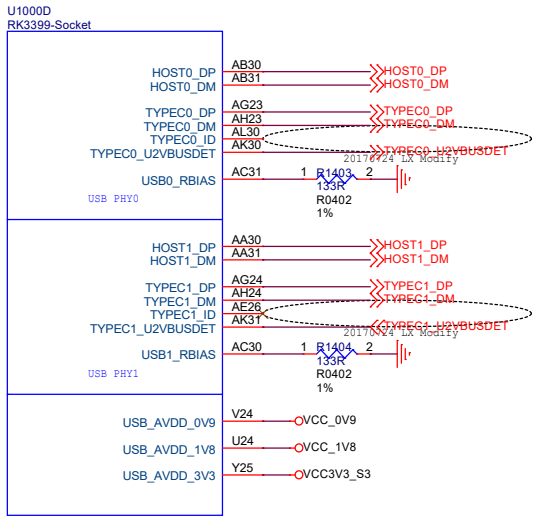


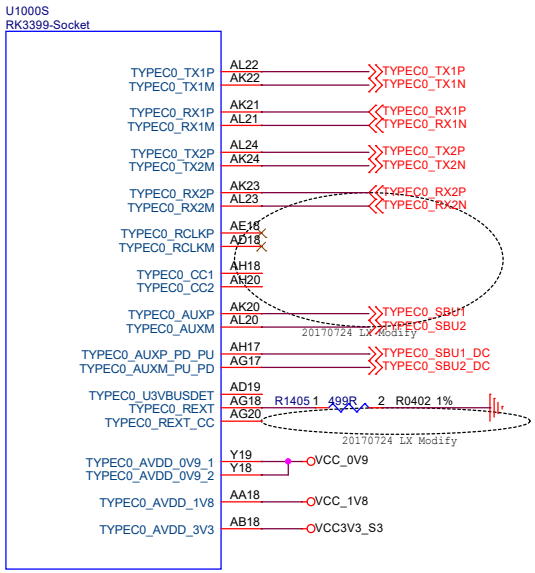
Truth Table

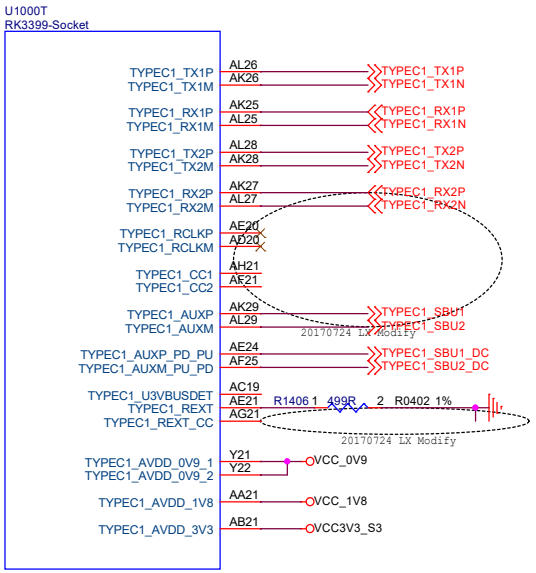
S	$\overline{OE}$	Function
X	H	Disconnect
L	L	D+, D– = $HSD1_n$
H	L	D+, D– = $HSD2_n$

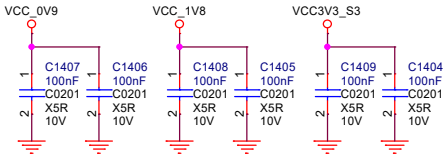
Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3399_EVB_TB_LPDDR4_200P		
File:	13.RK3399 Flash&SDMMC Controler		
Date:	Thursday, January 11, 2018	Rev:	V1.1
Designed by:	Linus	Sheet:	9 of 22



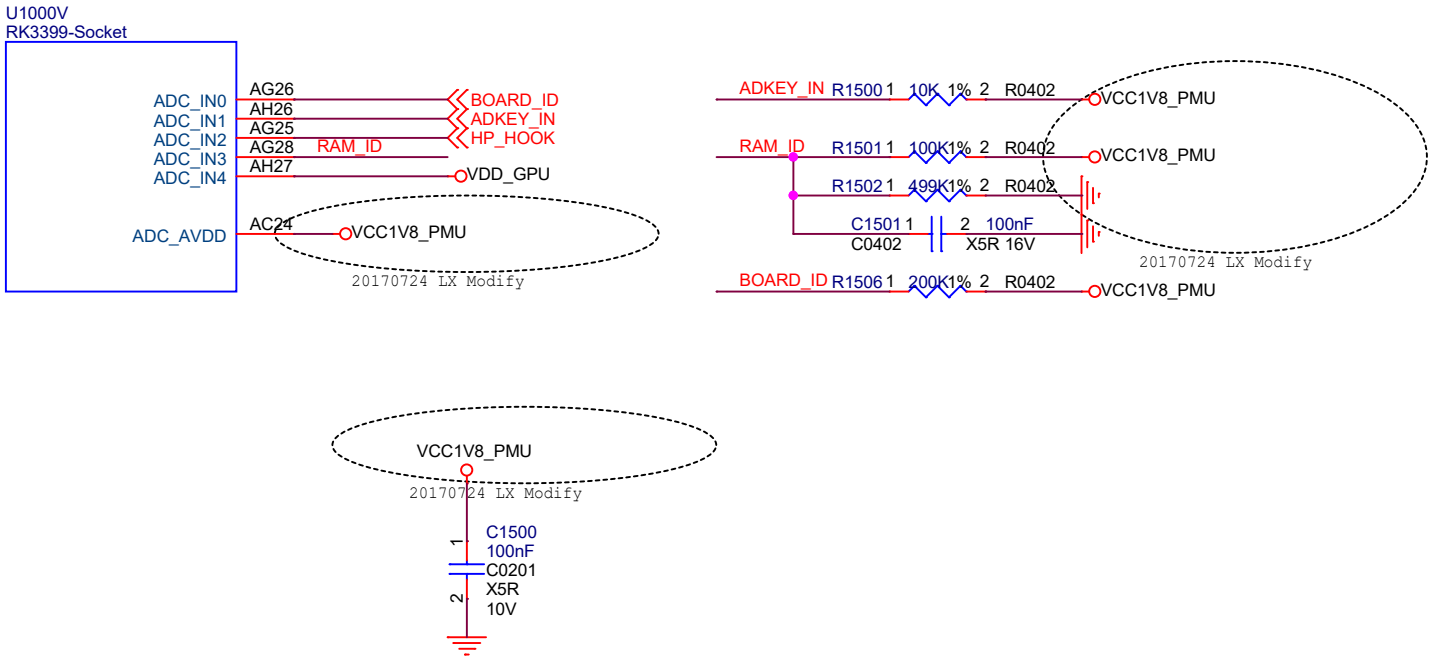




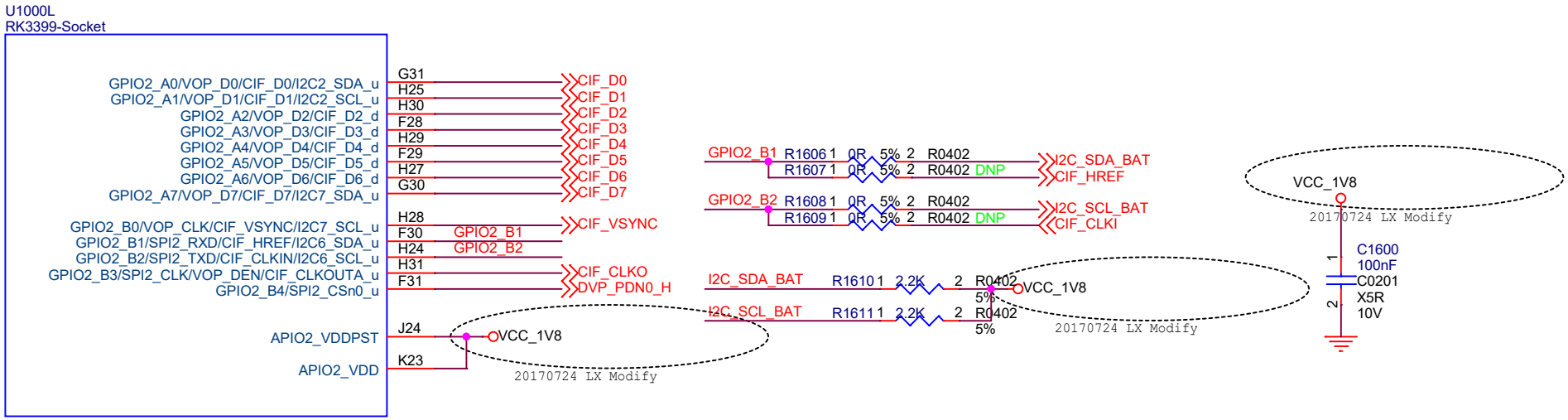


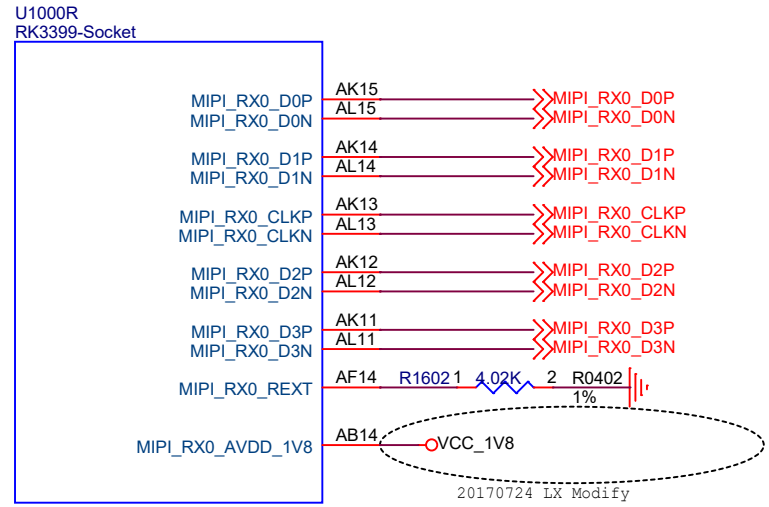


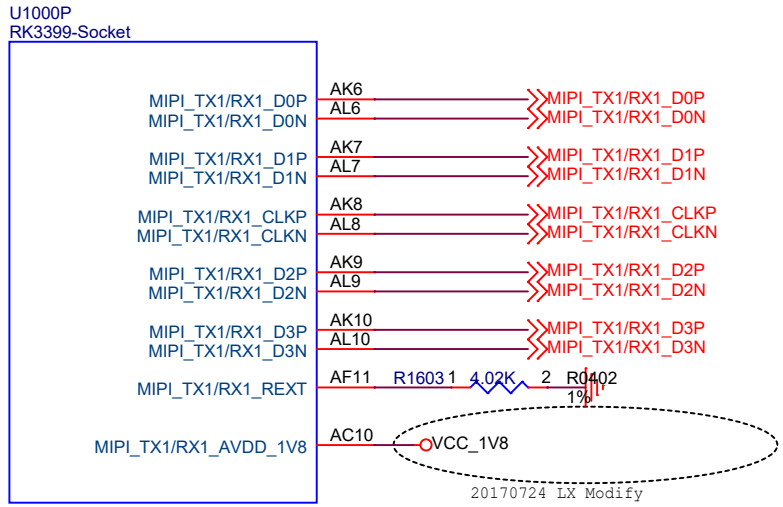
Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3399_EVB_TB_LPDDR4_200P		
File:	14.RK3399 USB/USIC Controler		
Date:	Thursday, January 11, 2018	Rev:	V1.1
Designed by:	Linus	Sheet:	10 of 22

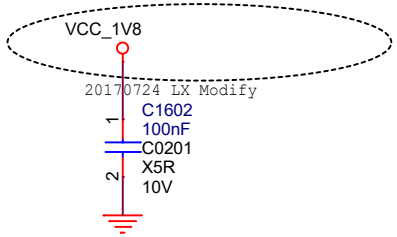


Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3399_EVB_TB_LPDDR4_200P		
File:	15.RK3399 SARADC		
Date:	Thursday, January 11, 2018	Rev:	V1.1
Designed by:	Linus	Sheet:	11 of 22

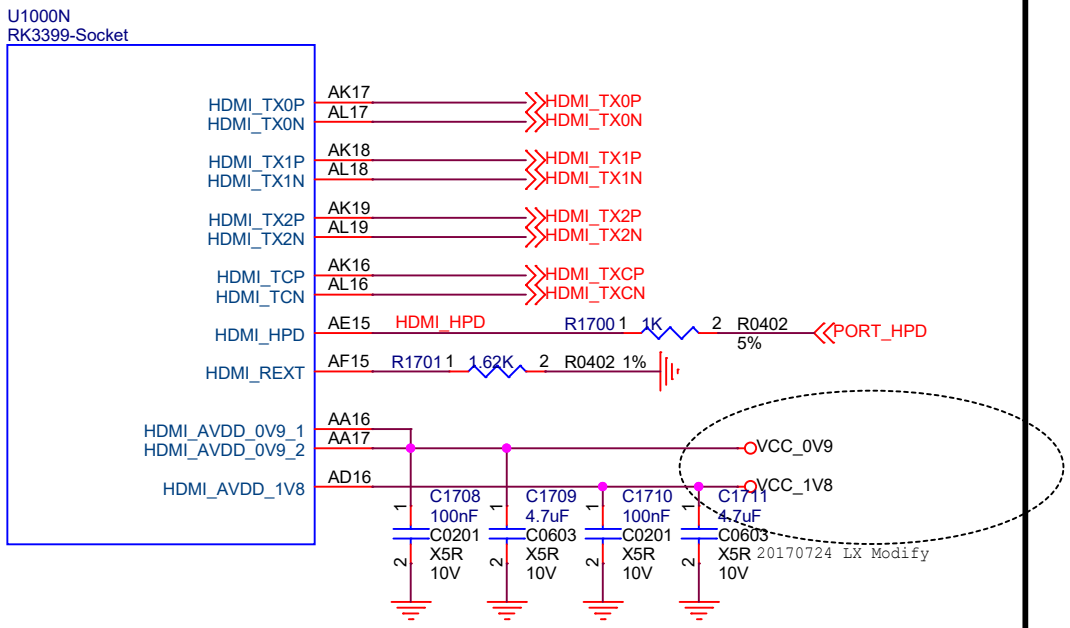


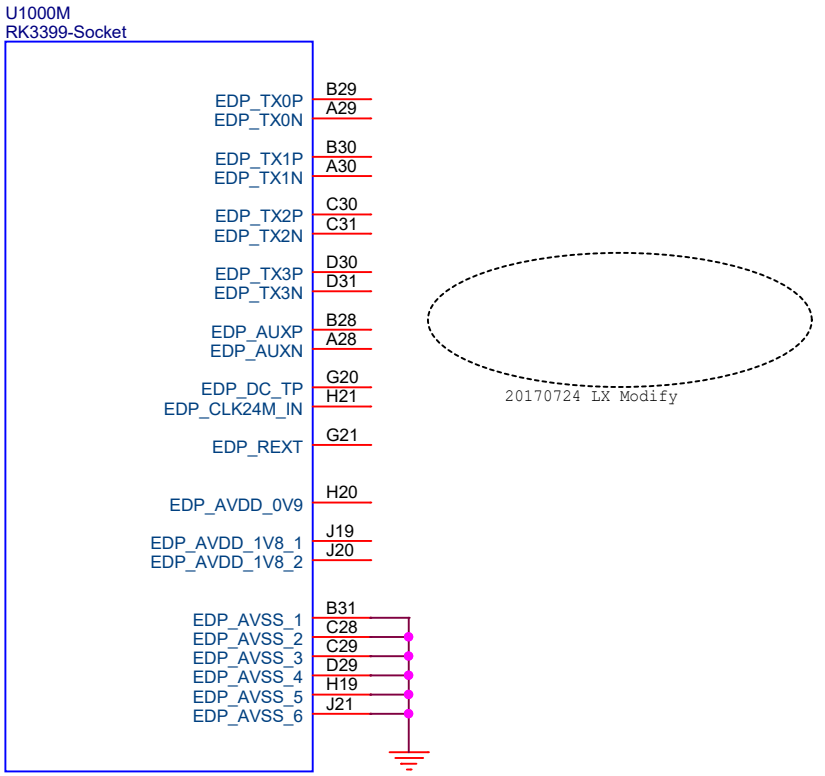


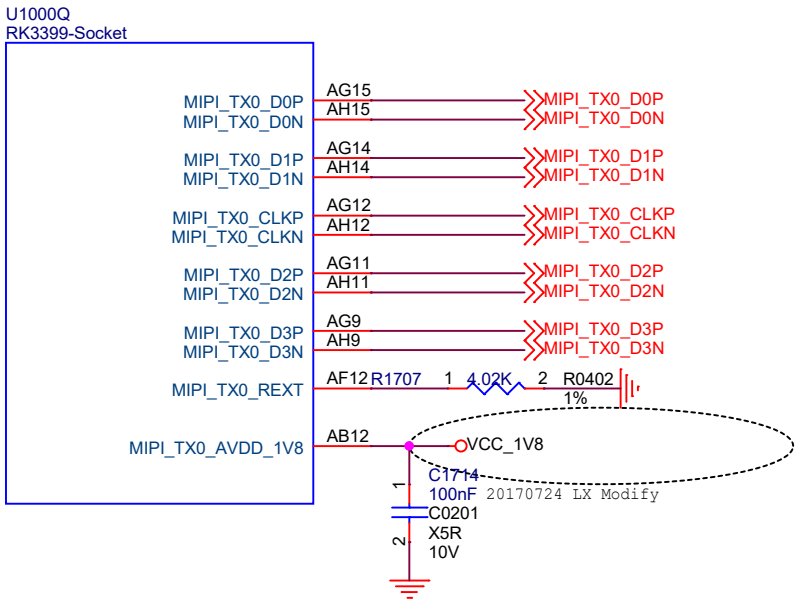




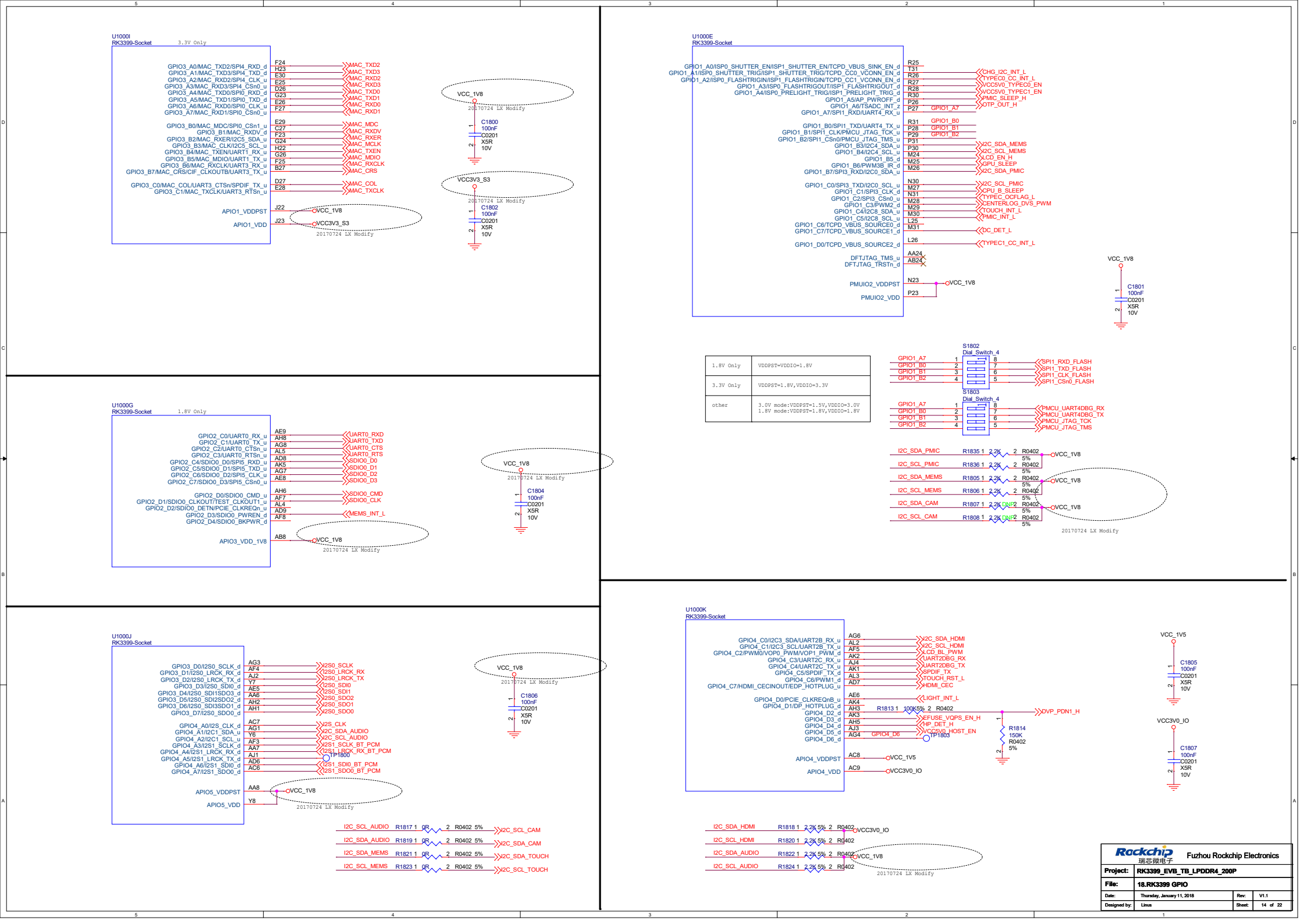
Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3399_EVB_TB_LPDDR4_200P		
File:	16.RK3399 DVP Interface		
Date:	Thursday, January 11, 2018	Rev:	V1.1
Designed by:	Linus	Sheet:	12 of 22

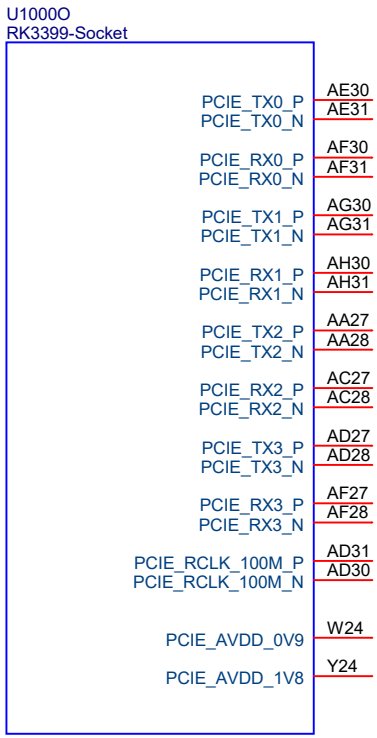






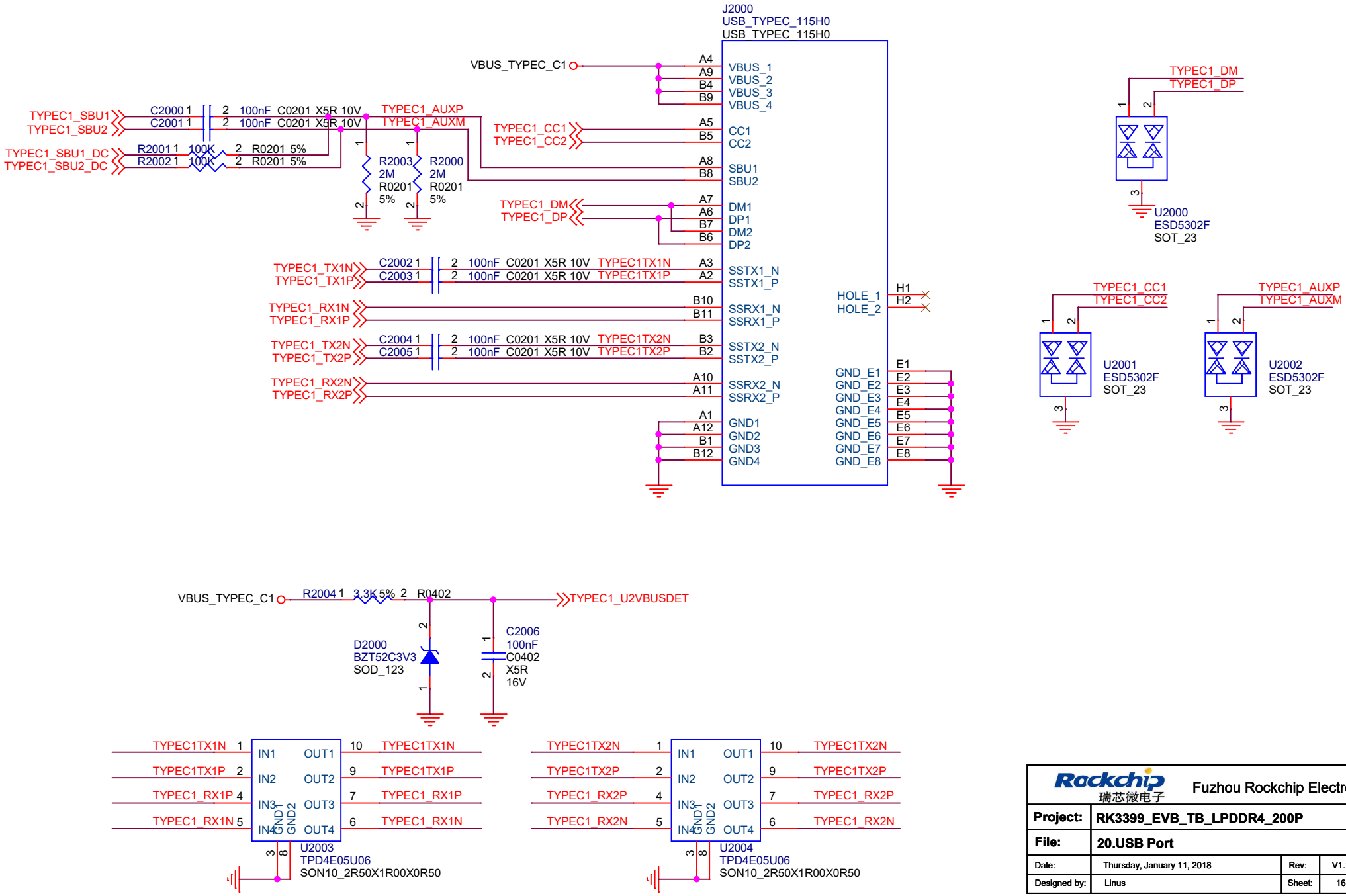
Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3399_EVB_TB_LPDDR4_200P		
File:	17.RK3399 Display Interface		
Date:	Thursday, January 11, 2018	Rev:	V1.1
Designed by:	Linus	Sheet:	13 of 22


U1000I
RK3399-Socket
3.3V Only
GPIO3_A0/MAC_TXD2/SPI4_RXD_d
GPIO3_A1/MAC_TXD3/SPI4_TXD_d
GPIO3_A2/MAC_RXD2/SPI4_CLK_u
GPIO3_A3/MAC_RXD3/SPI4_CSn0_u
GPIO3_A4/MAC_TXD0/SPI0_RXD_d
GPIO3_A5/MAC_TXD1/SPI0_TXD_d
GPIO3_A6/MAC_RXD0/SPI0_CLK_u
GPIO3_A7/MAC_RXD1/SPI0_CSn0_u
F24 MAC_TXD2
H23 MAC_TXD3
E30 MAC_RXD2
E25 MAC_RXD3
D26 MAC_TXD0
G23 MAC_TXD1
E26 MAC_RXD0
F27 MAC_RXD1
GPIO3_B0/MAC_MDC/SPI0_CSn1_u
GPIO3_B1/MAC_RXDV_d
GPIO3_B2/MAC_RXER/I2C5_SDA_u
GPIO3_B3/MAC_CLK/I2C5_SCL_u
GPIO3_B4/MAC_TXEN/UART1_RX_u
GPIO3_B5/MAC_MDIO/UART1_TX_u
GPIO3_B6/MAC_RXCLK/UART3_RX_u
GPIO3_B7/MAC_CRS/CIF_CLKOUTB/UART3_TX_u
E29 MAC_MDC
C27 MAC_RXDV
F23 MAC_RXER
G24 MAC_MCLK
H22 MAC_TXEN
G26 MAC_MDIO
F25 MAC_RXCLK
B27 MAC_CRS
GPIO3_C0/MAC_COL/UART3_CTSn/SPDIF_TX_u
GPIO3_C1/MAC_TXCLK/UART3_RTSn_u
D27 MAC_COL
E28 MAC_TXCLK
APIO1_VDDPST
APIO1_VDD
J22 VCC_1V8
J23 VCC3V3_S3
20170724 LX Modify
VCC_1V8
20170724 LX Modify
C1800 100nF C0201 X5R 10V
VCC3V3_S3
20170724 LX Modify
C1802 100nF C0201 X5R 10V
U1000E
RK3399-Socket
GPIO1_A0/ISP0_SHUTTER_EN/ISP1_SHUTTER_EN/TCPD_VBUS_SINK_EN_d
GPIO1_A1/ISP0_SHUTTER_TRIG/ISP1_SHUTTER_TRIG/TCPD_CC0_VCONN_EN_d
GPIO1_A2/ISP0_FLASHTRIGIN/ISP1_FLASHTRIGIN/TCPD_CC1_VCONN_EN_d
GPIO1_A3/ISP0_FLASHTRIGOUT/ISP1_FLASHTRIGOUT_d
GPIO1_A4/ISP0_PRELIGHT_TRIG/ISP1_PRELIGHT_TRIG_d
GPIO1_A5/AP_PWROFF_d
GPIO1_A6/TSADC_INT_z
GPIO1_A7/SPI1_RXD/UART4_RX_u
R25
T31 CHG_I2C_INT_L
R26 TYPEC0_CC_INT_L
R27 VCC5V0_TYPEC0_EN
R28 VCC5V0_TYPEC1_EN
R30 PMIC_SLEEP_H
P26 OTP_OUT_H
P27 GPIO1_A7
GPIO1_B0/SPI1_TXD/UART4_TX_u
GPIO1_B1/SPI1_CLK/PMCU_JTAG_TCK_u
GPIO1_B2/SPI1_CSn0/PMCU_JTAG_TMS_u
GPIO1_B3/I2C4_SDA_u
GPIO1_B4/I2C4_SCL_u
GPIO1_B5_d
GPIO1_B6/PWM3B_IR_d
GPIO1_B7/SPI3_RXD/I2C0_SDA_u
R31 GPIO1_B0
P28 GPIO1_B1
P29 GPIO1_B2
P31 I2C_SDA_MEMS
P30 I2C_SCL_MEMS
M24 LCD_EN_H
M25 GPU_SLEEP
M26 I2C_SDA_PMIC
GPIO1_C0/SPI3_TXD/I2C0_SCL_u
GPIO1_C1/SPI3_CLK_d
GPIO1_C2/SPI3_CSn0_u
GPIO1_C3/PWM2_d
GPIO1_C4/I2C8_SDA_u
GPIO1_C5/I2C8_SCL_u
GPIO1_C6/TCPD_VBUS_SOURCE0_d
GPIO1_C7/TCPD_VBUS_SOURCE1_d
N30 I2C_SCL_PMIC
M27 CPU_B_SLEEP
N31 TYPEC_OCFLAG_L
M28 CENTERLOG_DVS_PWM
M29 TOUCH_INT_L
M30 PMIC_INT_L
L25
M31 DC_DET_L
GPIO1_D0/TCPD_VBUS_SOURCE2_d
L26 TYPEC1_CC_INT_L
DFTJTAG_TMS_u
DFTJTAG_TRSTn_d
AA24
AB24
PMUIO2_VDDPST
PMUIO2_VDD
N23 VCC_1V8
P23
VCC_1V8
C1801 100nF C0201 X5R 10V
1.8V Only VDDPST=VDDIO=1.8V
3.3V Only VDDPST=1.8V,VDDIO=3.3V
other 3.0V mode:VDDPST=1.5V,VDDIO=3.0V 1.8V mode:VDDPST=1.8V,VDDIO=1.8V
S1802
Dial_Switch_4
GPIO1_A7
GPIO1_B0
GPIO1_B1
GPIO1_B2
SPI1_RXD_FLASH
SPI1_TXD_FLASH
SPI1_CLK_FLASH
SPI1_CSn0_FLASH
S1803
Dial_Switch_4
GPIO1_A7
GPIO1_B0
GPIO1_B1
GPIO1_B2
PMCU_UART4DBG_RX
PMCU_UART4DBG_TX
PMCU_JTAG_TCK
PMCU_JTAG_TMS
I2C_SDA_PMIC R1835 2.2K R0402 5% VCC_1V8
I2C_SCL_PMIC R1836 2.2K R0402 5% VCC_1V8
I2C_SDA_MEMS R1805 2.2K R0402 5%
I2C_SCL_MEMS R1806 2.2K R0402 5%
I2C_SDA_CAM R1807 2.2K DNP R0402 5%
I2C_SCL_CAM R1808 2.2K DNP R0402 5%
20170724 LX Modify
U1000G
RK3399-Socket
1.8V Only
GPIO2_C0/UART0_RX_u
GPIO2_C1/UART0_TX_u
GPIO2_C2/UART0_CTSn_u
GPIO2_C3/UART0_RTSn_u
GPIO2_C4/SDIO0_D0/SPI5_RXD_u
GPIO2_C5/SDIO0_D1/SPI5_TXD_u
GPIO2_C6/SDIO0_D2/SPI5_CLK_u
GPIO2_C7/SDIO0_D3/SPI5_CSn0_u
AE9 UART0_RXD
AH8 UART0_TXD
AG8 UART0_CTS
AL5 UART0_RTS
AD8 SDIO0_D0
AK5 SDIO0_D1
AG7 SDIO0_D2
AE8 SDIO0_D3
GPIO2_D0/SDIO0_CMD_u
GPIO2_D1/SDIO0_CLKOUT/TEST_CLKOUT1_u
GPIO2_D2/SDIO0_DETN/PCIE_CLKREQn_u
GPIO2_D3/SDIO0_PWREN_d
GPIO2_D4/SDIO0_BKPWR_d
AH6 SDIO0_CMD
AF7 SDIO0_CLK
AL4
AD9 MEMS_INT_L
AF8
APIO3_VDD_1V8
AB8 VCC_1V8
20170724 LX Modify
VCC_1V8
20170724 LX Modify
C1804 100nF C0201 X5R 10V
U1000J
RK3399-Socket
GPIO3_D0/I2S0_SCLK_d
GPIO3_D1/I2S0_LRCK_RX_d
GPIO3_D2/I2S0_LRCK_TX_d
GPIO3_D3/I2S0_SDI0_d
GPIO3_D4/I2S0_SDI1SDO3_d
GPIO3_D5/I2S0_SDI2SDO2_d
GPIO3_D6/I2S0_SDI3SDO1_d
GPIO3_D7/I2S0_SDO0_d
AG3 I2S0_SCLK
AF4 I2S0_LRCK_RX
AJ2 I2S0_LRCK_TX
Y7 I2S0_SDI0
AE5 I2S0_SDI1
AA6 I2S0_SDO2
AH2 I2S0_SDO1
AH1 I2S0_SDO0
GPIO4_A0/I2S_CLK_d
GPIO4_A1/I2C1_SDA_u
GPIO4_A2/I2C1_SCL_u
GPIO4_A3/I2S1_SCLK_d
GPIO4_A4/I2S1_LRCK_RX_d
GPIO4_A5/I2S1_LRCK_TX_d
GPIO4_A6/I2S1_SDI0_d
GPIO4_A7/I2S1_SDO0_d
AC7 I2S_CLK
AG1 I2C_SDA_AUDIO
Y6 I2C_SCL_AUDIO
AF3 I2S1_SCLK_BT_PCM
AA7 I2S1_LRCK_RX_BT_PCM
AJ1 TP1800
AD6 I2S1_SDI0_BT_PCM
AC6 I2S1_SDO0_BT_PCM
APIO5_VDDPST
APIO5_VDD
AA8 VCC_1V8
Y8
20170724 LX Modify
VCC_1V8
20170724 LX Modify
C1806 100nF C0201 X5R 10V
I2C_SCL_AUDIO R1817 0R R0402 5% I2C_SCL_CAM
I2C_SDA_AUDIO R1819 0R R0402 5% I2C_SDA_CAM
I2C_SDA_MEMS R1821 0R R0402 5% I2C_SDA_TOUCH
I2C_SCL_MEMS R1823 0R R0402 5% I2C_SCL_TOUCH
U1000K
RK3399-Socket
GPIO4_C0/I2C3_SDA/UART2B_RX_u
GPIO4_C1/I2C3_SCL/UART2B_TX_u
GPIO4_C2/PWM0/VOP0_PWM/VOP1_PWM_d
GPIO4_C3/UART2C_RX_u
GPIO4_C4/UART2C_TX_u
GPIO4_C5/SPDIF_TX_d
GPIO4_C6/PWM1_d
GPIO4_C7/HDMI_CECINOUT/EDP_HOTPLUG_u
AG6 I2C_SDA_HDMI
AL2 I2C_SCL_HDMI
AF5 LCD_BL_PWM
AK2 UART2DBG_RX
AJ4 UART2DBG_TX
AK1 SPDIF_TX
AL3 TOUCH_RST_L
AD7 HDMI_CEC
GPIO4_D0/PCIE_CLKREQnB_u
GPIO4_D1/DP_HOTPLUG_d
GPIO4_D2_d
GPIO4_D3_d
GPIO4_D4_d
GPIO4_D5_d
GPIO4_D6_d
AE6 LIGHT_INT_L
AK4
AH3 R1813 100K5% DVP_PDN1_H
AK3 EFUSE_VQPS_EN_H
AH5 HP_DET_H
AJ3 VCC5V0_HOST_EN
AG4 GPIO4_D6 TP1803
R1814 150K R0402 5%
APIO4_VDDPST
APIO4_VDD
AC8 VCC_1V5
AC9 VCC3V0_IO
VCC_1V5
C1805 100nF C0201 X5R 10V
VCC3V0_IO
C1807 100nF C0201 X5R 10V
I2C_SDA_HDMI R1818 2.2K 5% R0402 VCC3V0_IO
I2C_SCL_HDMI R1820 2.2K 5% R0402
I2C_SDA_AUDIO R1822 2.2K 5% R0402 VCC_1V8
I2C_SCL_AUDIO R1824 2.2K 5% R0402
20170724 LX Modify
Rockchip 瑞芯微电子 Fuzhou Rockchip Electronics
Project: RK3399_EVB_TB_LPDDR4_200P
File: 18.RK3399 GPIO
Date: Thursday, January 11, 2018 Rev. V1.1
Designed by: Linus Sheet: 14 of 22



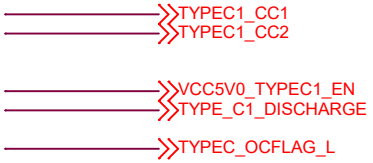
Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3399_EVB_TB_LPDDR4_200P		
File:	19.RK3399 PCI-E		
Date:	Thursday, January 11, 2018	Rev:	V1.1
Designed by:	Linus	Sheet:	15 of 22

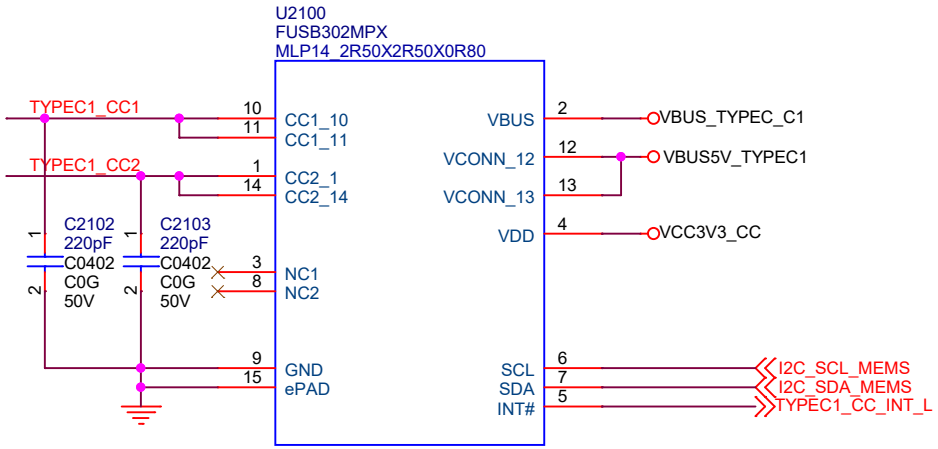
USB Type-C Port

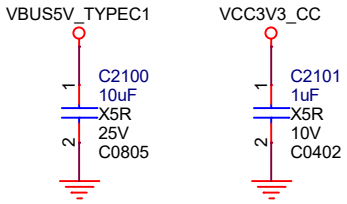


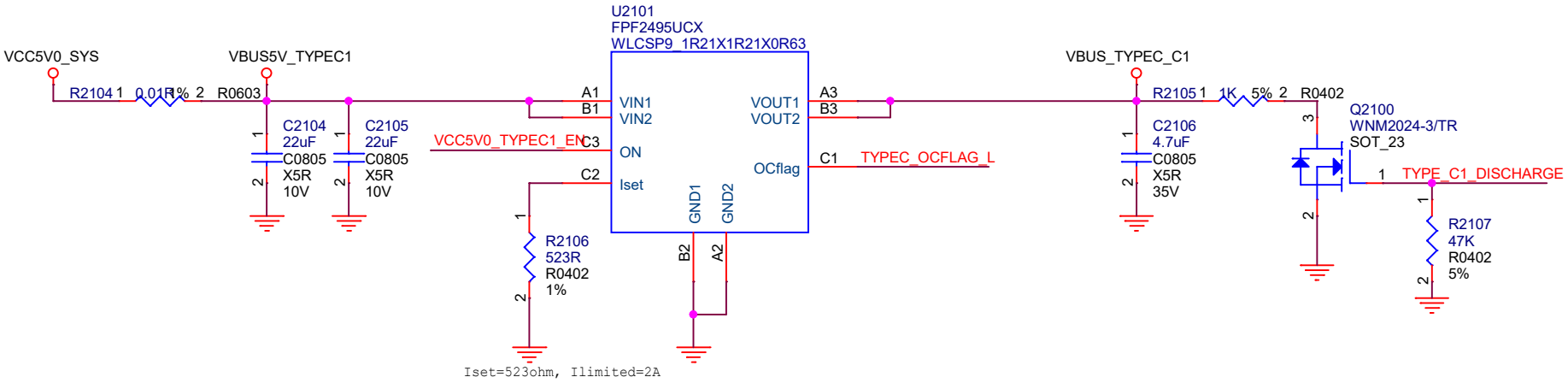
Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3399_EVB_TB_LPDDR4_200P		
File:	20.USB Port		
Date:	Thursday, January 11, 2018	Rev:	V1.1
Designed by:	Linus	Sheet:	16 of 22

USB Type-C pd/cc

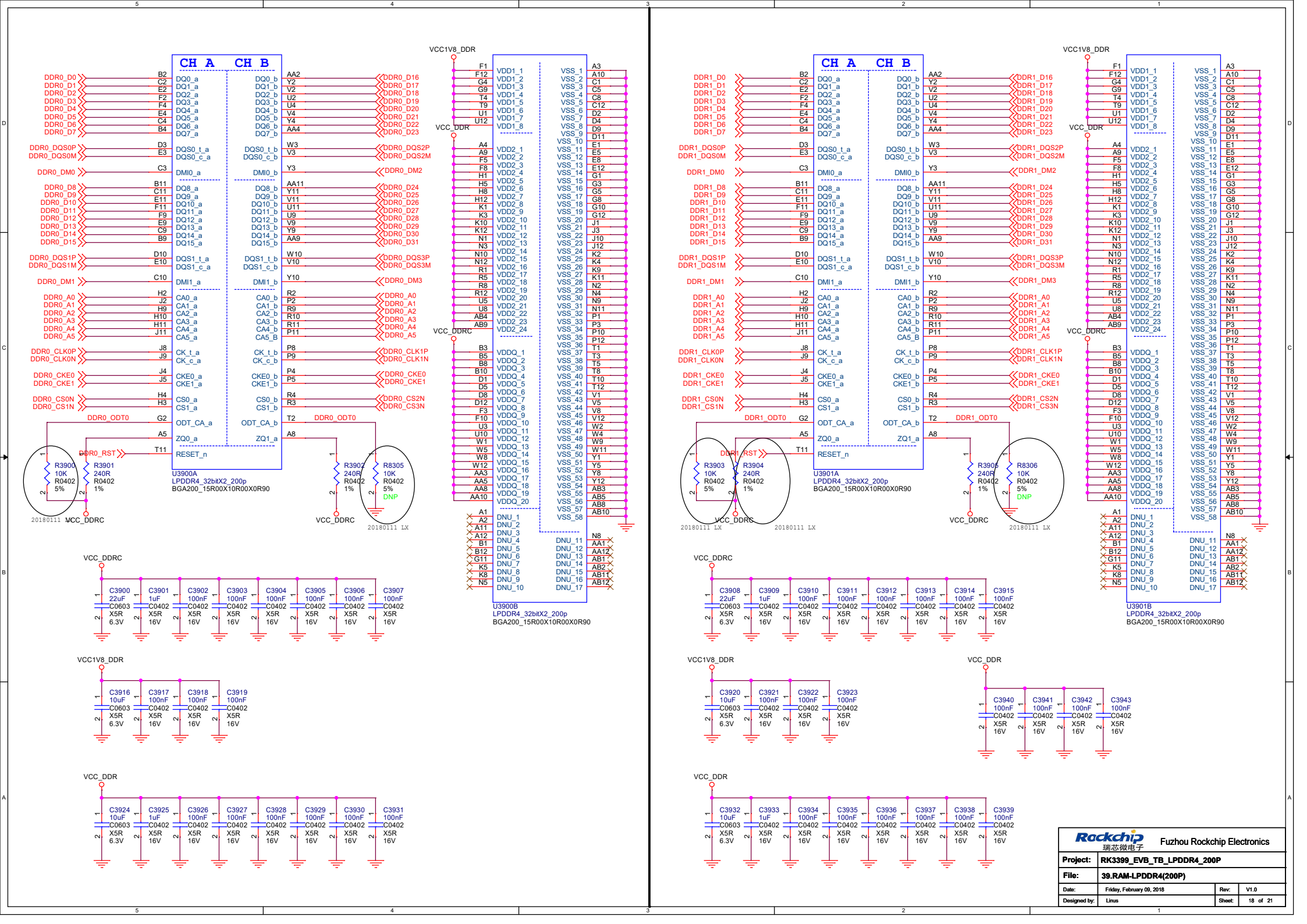




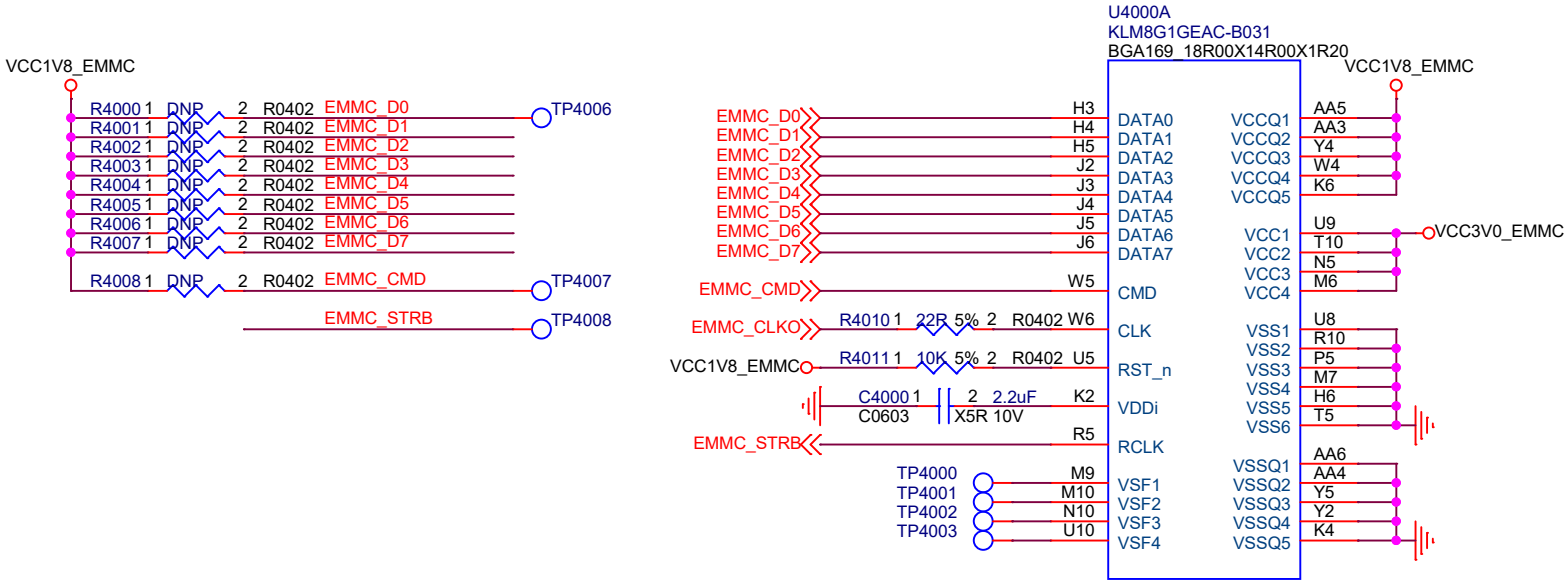


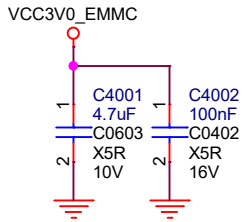


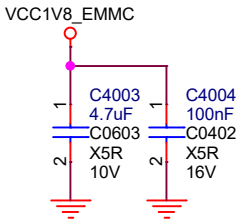
Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3399_EVB_TB_LPDDR4_200P		
File:	21.USB TYPE-C PD/CC		
Date:	Thursday, January 11, 2018	Rev:	V1.1
Designed by:	Linus	Sheet:	17 of 22


CH A
CH B
U3900A
LPDDR4_32bitX2_200p
BGA200_15R00X10R00X0R90
U3900B
LPDDR4_32bitX2_200p
BGA200_15R00X10R00X0R90
U3901A
LPDDR4_32bitX2_200p
BGA200_15R00X10R00X0R90
U3901B
LPDDR4_32bitX2_200p
BGA200_15R00X10R00X0R90
VCC1V8_DDR
VCC_DDR
VCC_DDRC
DDR0_ODT0
DDR1_ODT0
DDR0_RST
DDR1_RST
R3900 10K R0402 5%
R3901 240R R0402 1%
R3902 240R R0402 1%
R8305 10K R0402 5% DNP
R3903 10K R0402 5%
R3904 240R R0402 1%
R3905 240R R0402 1%
R8306 10K R0402 5% DNP
20180111 LX
C3900 22uF C0603 X5R 6.3V
C3901 1uF C0402 X5R 16V
C3902 100nF C0402 X5R 16V
C3903 100nF C0402 X5R 16V
C3904 100nF C0402 X5R 16V
C3905 100nF C0402 X5R 16V
C3906 100nF C0402 X5R 16V
C3907 100nF C0402 X5R 16V
C3908 22uF C0603 X5R 6.3V
C3909 1uF C0402 X5R 16V
C3910 100nF C0402 X5R 16V
C3911 100nF C0402 X5R 16V
C3912 100nF C0402 X5R 16V
C3913 100nF C0402 X5R 16V
C3914 100nF C0402 X5R 16V
C3915 100nF C0402 X5R 16V
C3916 10uF C0603 X5R 6.3V
C3917 100nF C0402 X5R 16V
C3918 100nF C0402 X5R 16V
C3919 100nF C0402 X5R 16V
C3920 10uF C0603 X5R 6.3V
C3921 100nF C0402 X5R 16V
C3922 100nF C0402 X5R 16V
C3923 100nF C0402 X5R 16V
C3924 10uF C0603 X5R 6.3V
C3925 1uF C0402 X5R 16V
C3926 100nF C0402 X5R 16V
C3927 100nF C0402 X5R 16V
C3928 100nF C0402 X5R 16V
C3929 100nF C0402 X5R 16V
C3930 100nF C0402 X5R 16V
C3931 100nF C0402 X5R 16V
C3932 10uF C0603 X5R 6.3V
C3933 1uF C0402 X5R 16V
C3934 100nF C0402 X5R 16V
C3935 100nF C0402 X5R 16V
C3936 100nF C0402 X5R 16V
C3937 100nF C0402 X5R 16V
C3938 100nF C0402 X5R 16V
C3939 100nF C0402 X5R 16V
C3940 100nF C0402 X5R 16V
C3941 100nF C0402 X5R 16V
C3942 100nF C0402 X5R 16V
C3943 100nF C0402 X5R 16V
Rockchip 瑞芯微电子
Fuzhou Rockchip Electronics
Project: RK3399_EVB_TB_LPDDR4_200P
File: 39.RAM-LPDDR4(200P)
Date: Friday, February 09, 2018
Rev: V1.0
Designed by: Linus
Sheet: 18 of 21

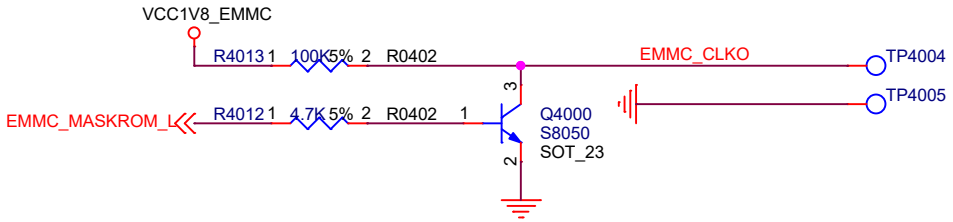
eMMC FLASH





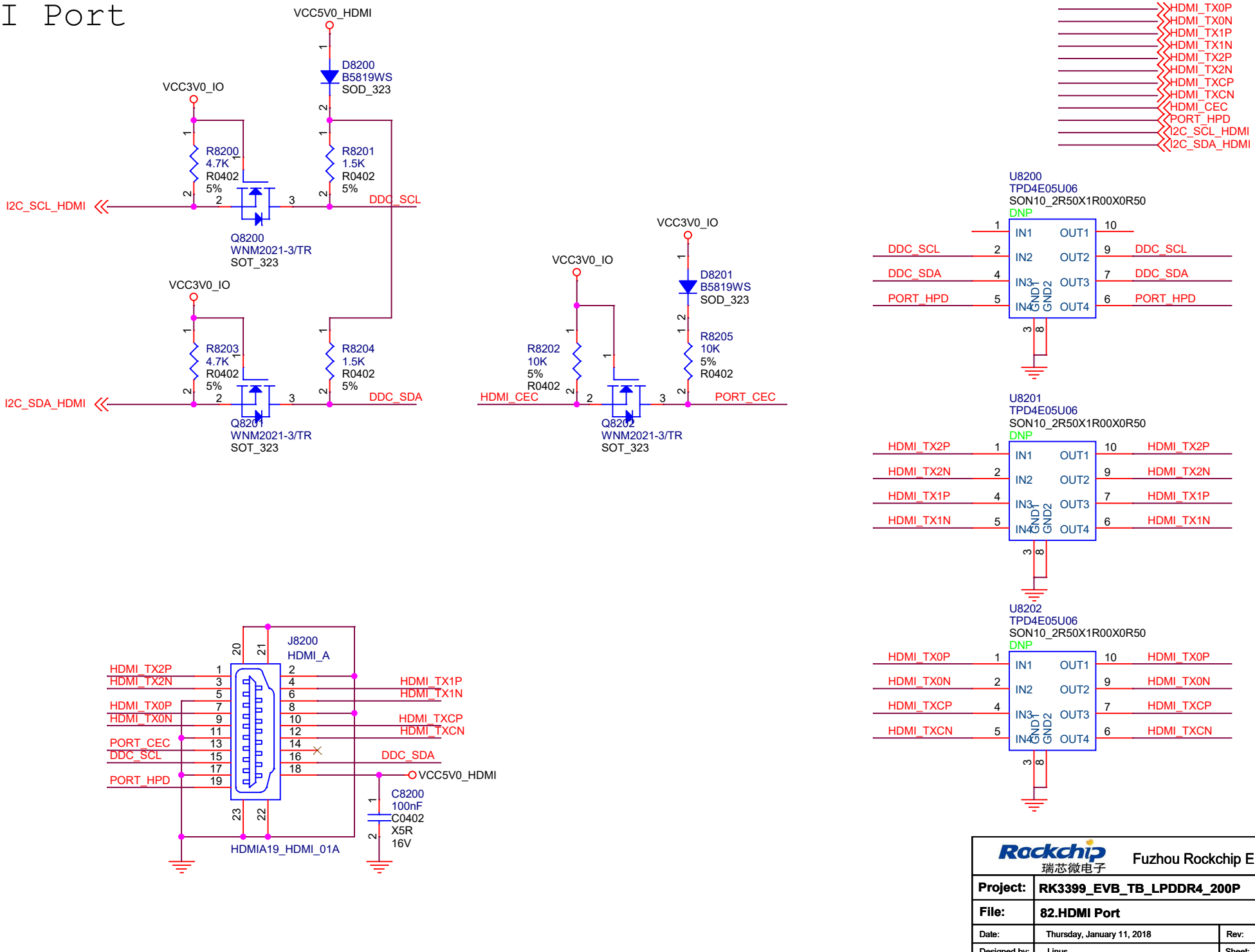


Note:
Reserve PAD for Update.



Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3399_EVB_TB_LPDDR4_200P		
File:	40.Memory-eMMC		
Date:	Thursday, January 11, 2018	Rev:	V1.1
Designed by:	Linus	Sheet:	19 of 22

HDMI Port



Rockchip 瑞芯微电子	Fuzhou Rockchip Electronics		
Project:	RK3399_EVB_TB_LPDDR4_200P		
File:	82.HDMI Port		
Date:	Thursday, January 11, 2018	Rev:	V1.1
Designed by:	Linus	Sheet:	21 of 22