

# **AW-CM256SM**

**IEEE 802.11a/b/g/n/ac Wi-Fi with  
Bluetooth 4.2  
Combo Stamp Module**

01

## **Datasheet**

**Version 1.0**

## Revision History

Document Release	Date	Modification	Initials	Approved
Version 0.1	2015/10/26	First Release	Amos Fu	Chihhao Liao
Version 0.2	2016/07/26	1. Add the table of contents 2. Change the Connector Pin-out Definitions <ul style="list-style-type: none"> <li>● Change the diagram</li> <li>● Pin21 NC→ VIN_LDO_OUT</li> <li>● Pin23 NC→ VIN_LDO</li> <li>● Pin37 NC→ GPIO_6</li> <li>● Pin38 ERCX_LTERX→GPIO_3</li> <li>● Pin39 ERCX_LTETX→GPIO_5</li> </ul>	Licheng Wang	Chihhao Liao
Version 0.3	2016/08/17	Add Pin29 NC→GPIO_7	Licheng Wang	Chihhao Liao
Version 0.4	2016/08/22	1. Update the Block Diagram 2. Change Pin29 definition	Licheng Wang	Chihhao Liao
Version 0.5	2016/12/22	1. Update General Specifications 2. Update ESD rate	Licheng Wang	Chihhao Liao
Version 0.6	2016/12/28	1. Update General Specifications 2. Update VBAT Specifications	Licheng Wang	Chihhao Liao
Version 0.7	2017/02/16	1. Update General Specifications 2. Update Recommended Operating Conditions 3. Update Mechanical Dimensions 4. Remove Power consumption	Licheng Wang	Chihhao Liao
Version 0.8	2017/02/22	Update General Specifications	Licheng Wang	Chihhao Liao
Version 0.9	2017/04/11	1. Update to BT4.2 2. Update General Specifications	Licheng Wang	Chihhao Liao
Version 1.0	2017/04/14	1. Add 4-5 Frequency Reference	Licheng Wang	Chihhao Liao

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## 1. Introduction

**AzureWave Technologies, Inc.** introduces the pioneer of the IEEE 802.11 a/b/g/n/ac WIFI with Bluetooth 4.2 combo SDIO and UART Stamp Module --- **AW-CM256SM**. The AW-CM256SM IEEE 802.11 a/b/g/n/ac WIFI with Bluetooth 4.2 combo module is a highly integrated wireless local area network (WLAN) solution to let users enjoy the digital content through the latest wireless technology without using the extra cables and cords. It combines with Bluetooth 4.2 and provides a complete 2.4GHz Bluetooth system which is fully compliant to Bluetooth 4.2 and v2.1 that supports EDR of 2Mbps and 3Mbps for data and audio communications. It enables a high performance, cost effective, low power, compact solution that easily fits onto the SDIO and UART combo stamp module.

Compliant with the IEEE 802.11a/b/g/n/ac standard, AW-CM256SM uses Direct Sequence Spread Spectrum (DSSS), Orthogonal Frequency Division Multiplexing (OFDM), BPSK, QPSK, CCK and QAM baseband modulation technologies.

Compare to 802.11n technology, 802.11ac standard makes big improvement on speed and range.

AW-CM256SM module adopts Cypress solution. The module design is based on the Cypress CYW43455 single chip.

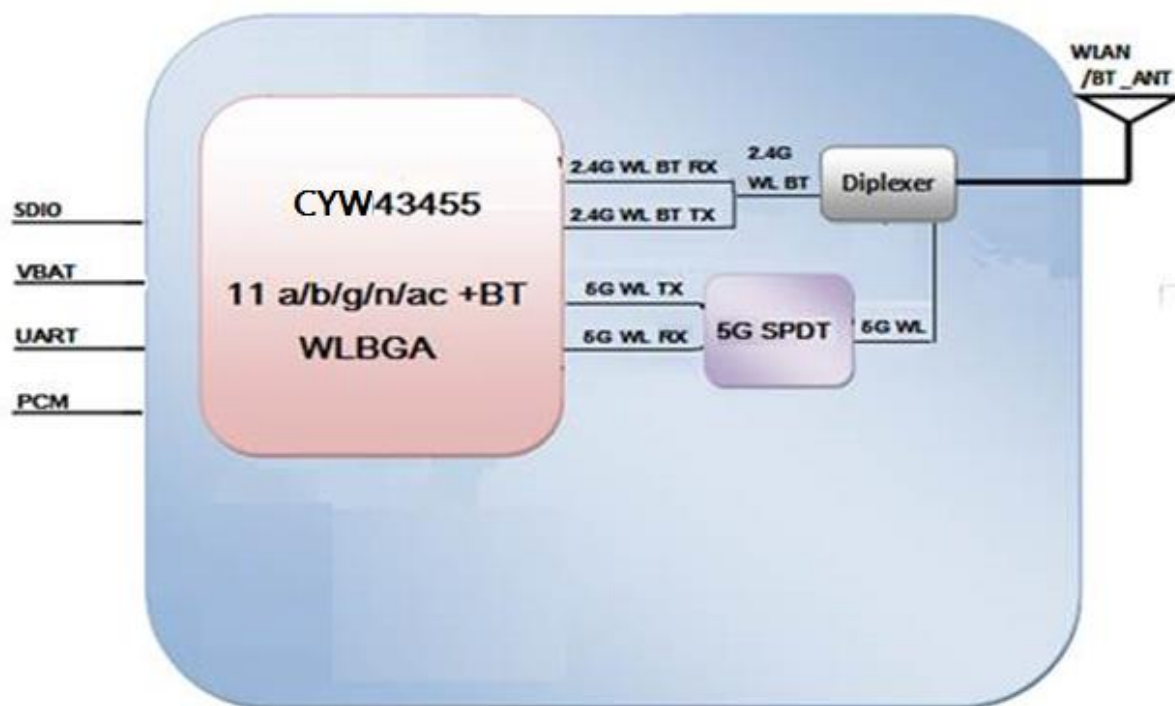
## 2. Features

High speed wireless connection up to 433.3Mbps transmit/receive PHY rate using 80MHz bandwidth

- ◆ 1 antennas to support 1(Transmit) × 1(Receive) technology and Bluetooth
- ◆ WCS (Wireless Coexistence System)
- ◆ Low power consumption and high performance
- ◆ Enhanced wireless security
- ◆ Fully qualified Bluetooth BT4.2
- ◆ Enhanced Data Rate(EDR) compliant for both 2Mbps and 3Mbps supported
- ◆ Fully speed operation with Piconet and Scatternet support
- ◆ High speed UART and PCM for Bluetooth
- ◆ 12mm(L) x 12mm(W) x1.65mm(H) LGA package
- ◆ Dual - band 2.4 GHz and 5GHz 802.11 a/b/g/n/ac
- ◆ External Crystal



### 3. Block Diagram



## 4. General Specifications

<b>Model Name</b>	<b>AW-CM256SM</b>
<b>Product Description</b>	<b>IEEE 802.11 a/b/g/n/ac Wi-Fi with Bluetooth 4.2 combo stamp module</b>
<b>BlueTooth Standard</b>	IEEE 802.11a/b/g/n/ac, Wi-Fi compliant / Bluetooth4.2 Standard
<b>Host Interface</b>	Wi-Fi :SDIO , BT : UART
<b>Major Chipset</b>	CYW43455
<b>Wi-Fi SSV/PID</b>	1A3B / 2256
<b>Dimension</b>	12 mm X 12mm x 1.65 mm
<b>Weight</b>	0.45 g
<b>Operating Conditions</b>	
<b>Voltage</b>	VBAT: 3.2 ~ 4.8V ; typical: 3.6V VIO : 1.8 ~ 3.3V
<b>Temperature</b>	-20~75°C
<b>Storage temperature</b>	-40~85°C
<b>Electrical Specifications</b>	
<b>Frequency Range</b>	Wi-Fi: 2.4 GHz ISM Bands 2.412-2.472 GHz/ 5.15-5.25 GHz (FCC UNII-low band) for US/Canada and Europe 5.25-5.35 GHz (FCC UNII-middle band) for US/Canada and Europe 5.47-5.725 GHz for Europe 5.725-5.825 GHz (FCC UNII-high band) for US/Canada BT: 2402MHz~2483MHz
<b>Number of Channels</b>	802.11b: USA, Canada and Taiwan – 1 ~ 11 Most European Countries – 1 ~ 13 802.11g: USA and Canada – 1 ~ 11 Most European Countries – 1 ~ 13 802.11n: USA and Canada – 1 ~ 11 Most European Countries – 1 ~ 13 802.11a: USA – 36, 40, 44, 48, 52, 56, 60, 64, 100, 104, 108, 112, 116, 120, 124, 128, 132, 136, 140, 149, 153, 157, 161, 165
<b>Modulation</b>	Wi-Fi: 802.11a/g/n/ac: OFDM 802.11b: CCK(11, 5.5Mbps), DQPSK(2Mbps), BPSK(1Mbps) BT: Header GFSK Payload 2M: 4-DQPSK

	<b>Payload 3M: 8DPSK</b>
<b>Output Power</b>	<b>Wi-Fi:</b> 802.11a: 15 dBm +/- 1.5 dBm (54Mbps) 802.11b: 18 dBm +/- 1.5 dBm (11Mbps) 802.11g: 16 dBm +/- 1.5 dBm (54Mbps) 802.11n @2.4GHz: 15 dBm +/- 1.5 dBm (HT20 MCS7) 802.11n @2.4GHz: 14 dBm +/- 1.5dBm (HT40 MCS7) 802.11n @5GHz: 15 dBm +/- 1.5 dBm (HT20 MCS7) 802.11n @5GHz: 13 dBm +/- 1.5 dBm (HT40 MCS7) 802.11ac @5GHz: 14 dBm +/- 1.5 dBm (VHT20 MCS8) 802.11ac @5GHz: 13 dBm +/- 1.5 dBm (VHT40 MCS9) 802.11ac @5GHz: 12 dBm +/- 1.5 dBm (VHT80 MCS9) <b>BT: Output Power ≤ 12 dBm (Conductive)</b>
<b>Receive Sensitivity</b>	<b>WLAN:</b> <b>2.4G:</b> 11b (11Mbps): -87 dBm (Typical) 11g (54Mbps): - 76 dBm (Typical) 11n (HT20 MCS7): -74 dBm (Typical) 11n (HT40 MCS7): -71 dBm (Typical) <b>5G:</b> 11a (54Mbps) : -73 dBm (Typical) 11n (HT20 MCS7): -71 dBm (Typical) 11n (HT40 MCS7): -68 dBm (Typical) 11ac (VHT20 MCS8): -66 dBm (Typical) 11ac (VHT40 MCS9): -63 dBm (Typical) 11ac (VHT80 MCS9): -59 dBm (Typical) <b>Bluetooth:</b> GFSK: -88 dBm π/4-DQPSK: -95 dBm 8-DPSK: -88 dBm
<b>Operating Range</b>	<b>Wi-Fi: Open Space: (300m) / Indoor:(100m)</b> <b>(The transmission speed may vary according to the environment)</b> <b>BT: 10m~20m (depending on environment and NB model)</b>
<b>ESD rating</b>	<b>HBM: &gt;1KV per JEDEC EID/JESD22-A114</b> <b>CDM: &gt;250V per JEDEC EIA/JESD22-C101</b>



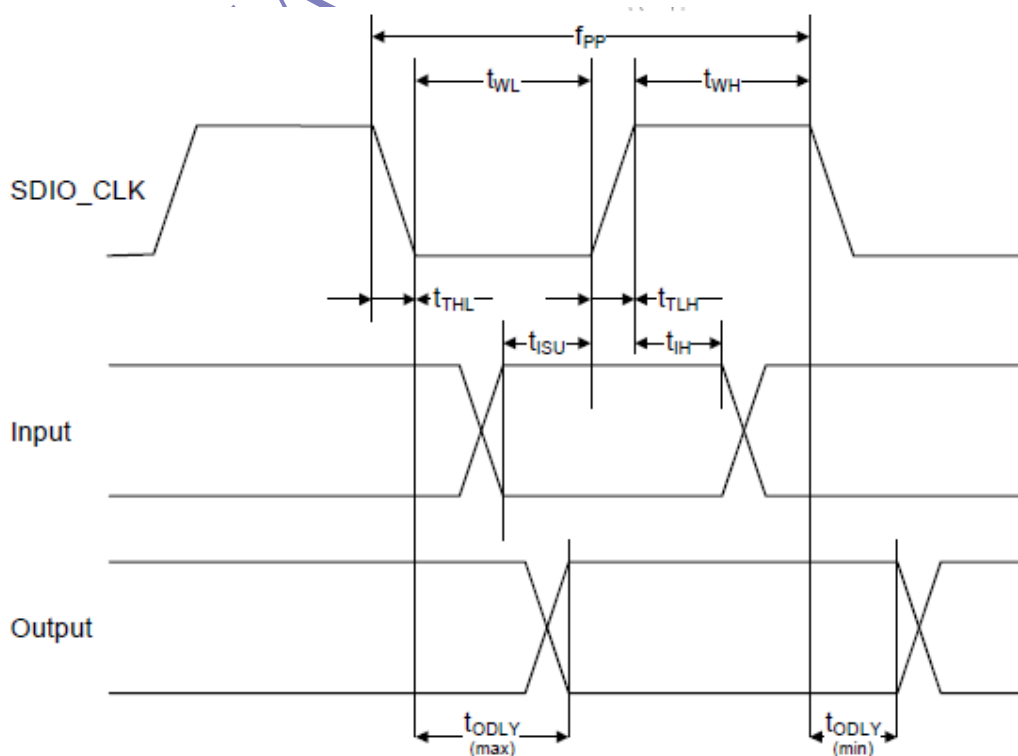
## 4-1. Recommended Operating Conditions

Symbol	Parameter	Type	Min	Typ	Max	Units
V <sub>BAT</sub>	Power supply for Internal Regulators and FEM	Input	3.2	3.6	4.8	V
V <sub>DDIO</sub>	DC supply voltage for digital I/O	Input	1.8	-	3.3	V

## 4-2. DC Characteristics for Host I/O

Symbol	Parameter	Condition	Min	Typ	Max	Units
Digital I/O pins						
V <sub>IH</sub>	Input high voltage (V <sub>DDIO</sub> )	V <sub>DDIO</sub> =1.8V	1.17	-	-	V
V <sub>IL</sub>	Input low voltage (V <sub>DDIO</sub> )	V <sub>DDIO</sub> =1.8V	-	-	0.63	V
V <sub>OH</sub>	Output High Voltage @ 2mA	V <sub>DDIO</sub> =1.8V	1.35	-	-	V
V <sub>OL</sub>	Output Low Voltage @ 2mA	V <sub>DDIO</sub> =1.8V	-	-	0.45	V
V <sub>IH</sub>	Input high voltage (V <sub>DDIO</sub> )	V <sub>DDIO</sub> =3.3V	2.0	-	-	
V <sub>IL</sub>	Input low voltage (V <sub>DDIO</sub> )	V <sub>DDIO</sub> =3.3V	-	-	0.8	
V <sub>OH</sub>	Output High Voltage @ 2mA	V <sub>DDIO</sub> =3.3V	2.9	-	-	
V <sub>OL</sub>	Output Low Voltage @ 2mA	V <sub>DDIO</sub> =3.3V	-	-	0.4	

## 4-3. SDIO Host Interface Specification



## SDIO Timing Data

Symbol	Parameter	Condition	Min	Max	Units
$f_{pp}$	CLK Frequency	Normal	0	25	MHz
		High Speed	0	50	
$t_{WH}$	CLK High Time	Normal	10	-	ns
		High Speed	7	-	
$t_{WL}$	CLK Low Time	Normal	10	-	
		High Speed	7	-	
$t_{TLH}$	CLK rise Time	Normal	-	10	
		High Speed	-	3	
$t_{THL}$	CLK fall Time	Normal	-	10	
		High Speed	-	3	
$t_{ISU}$	Input Setup Time	Normal	5	-	
		High Speed	6	-	
$t_{IH}$	Input Hold Time	Normal	5	-	
		High Speed	2	-	
$t_{ODLY}$	Output Delay Time	Normal	-	14	
		High Speed	-	14	

## 4-4. UART Interface

The AW-NM256SM shares a single UART for Bluetooth . The UART is a standard 4-wire interface (RX, TX, RTS, and CTS) with adjustable baud rates from 9600 bps to 4.0 Mbps. The interface features an automatic baud rate detection capability that returns a baud rate selection. Alternatively, the baud rate may be selected through a vendor-specific UART HCI command.

UART has a 1040-byte receive FIFO and a 1040-byte transmits FIFO to support EDR. Access to the FIFOs is conducted through the AHB interface through either DMA or the CPU. The UART supports the Bluetooth 4.0 UART HCI specification: H4, a custom Extended H4, and H5. The default baud rate is 115.2 Kbaud.

The UART supports the 3-wire H5 UART transport, as described in the Bluetooth specification (“Three-wire UART Transport Layer”). Compared to H4, the H5 UART transport reduces the number of signal lines required by eliminating the CTS and RTS signals.

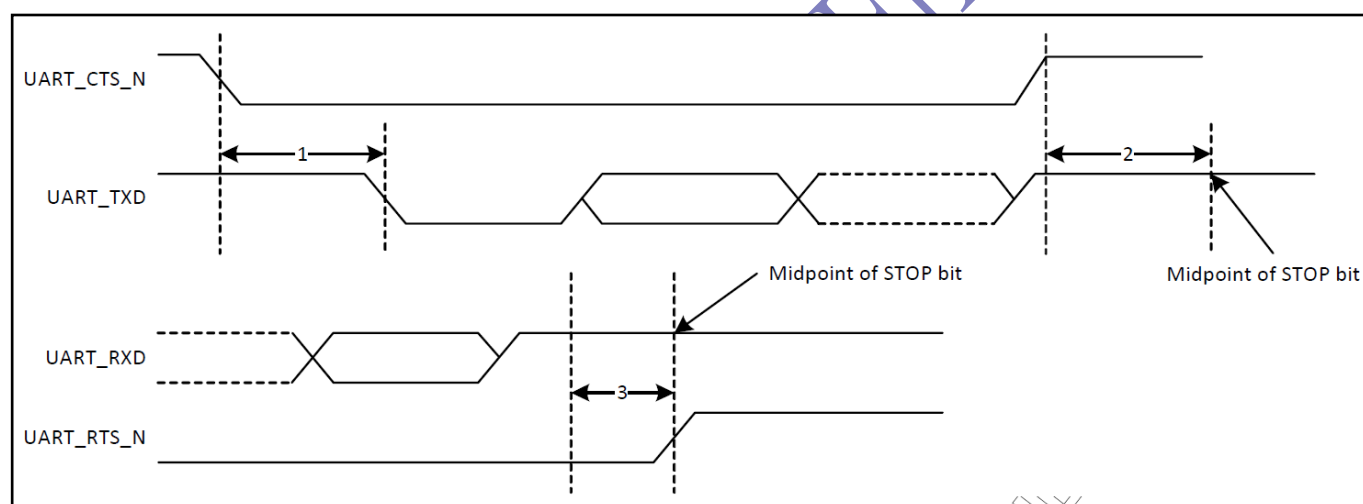
Normally, the UART baud rate is set by a configuration record downloaded after device reset, or by automatic baud rate detection, and the host does not need to adjust the baud rate. Support for changing the baud rate during normal HCI UART operation is included through a vendor-specific command that allows the host to adjust the contents of the baud rate registers. The AW-NM256SM UARTs operate correctly with the host UART as long as the combined baud rate error of the two devices is within  $\pm 2\%$ .

## UART Interface Signals

PIN No.	Name	Description	Type
42	BT_UART_TXD	Bluetooth UART Serial Output. Serial data output for the HCI UART Interface	O
43	BT_UART_RXD	Bluetooth UART Series Input. Serial data input for the HCI UART Interface	I
41	BT_UART_RTS_N	Bluetooth UART Request-to-Send. Active-low request-to-send signal for the HCI UART interface	O
44	BT_UART_CTS_N	Bluetooth UART Clear-to-Send. Active-low clear-to-send signal for the HCI UART interface.	I

## UART Timing

UART Timing



UART Timing Specifications

Ref No.	Characteristics	Minimum	Typical	Maximum	Unit
1	Delay time, UART_CTS_N low to UART_TXD valid	–	–	1.5	Bit periods
2	Setup time, UART_CTS_N high before midpoint of stop bit	–	–	0.5	Bit periods
3	Delay time, midpoint of stop bit to UART_RTS_N high	–	–	0.5	Bit periods

## .Power-Up Sequence and Timing

#### 4-4. Sequencing of Reset and Regulator Control Signals

The AW-NM256SM has three signals that allow the host to control power consumption by enabling or disabling the Bluetooth, WLAN, and internal regulator blocks. These signals are described below. Additionally, diagrams are provided to indicate proper sequencing of the signals for various operational states. The timing values indicated are minimum required values; longer delays are also acceptable.

##### Note:

- The WL\_REG\_ON and BT\_REG\_ON signals are ORed in the AW-NM256SM. The diagrams show both signals going high at the same time (as would be the case if both REG signals were controlled by a single host GPIO). If two independent host GPIOs are used (one for WL\_REG\_ON and one for BT\_REG\_ON), then only one of the two signals needs to be high to enable the AW-NM256SM regulators.
- The AW-NM256SM has an internal power-on reset (POR) circuit. The device will be held in reset for a maximum of 110 ms after VDDC and VDDIO have both passed the POR threshold. Wait at least 150 ms after VDDC and VDDIO are available before initiating SDIO accesses.

#### Description of Control Signals

The AW-NM256SM has two signals that enable or disable the Bluetooth and WLAN circuits and the internal regulator blocks, allowing the host to control power consumption.

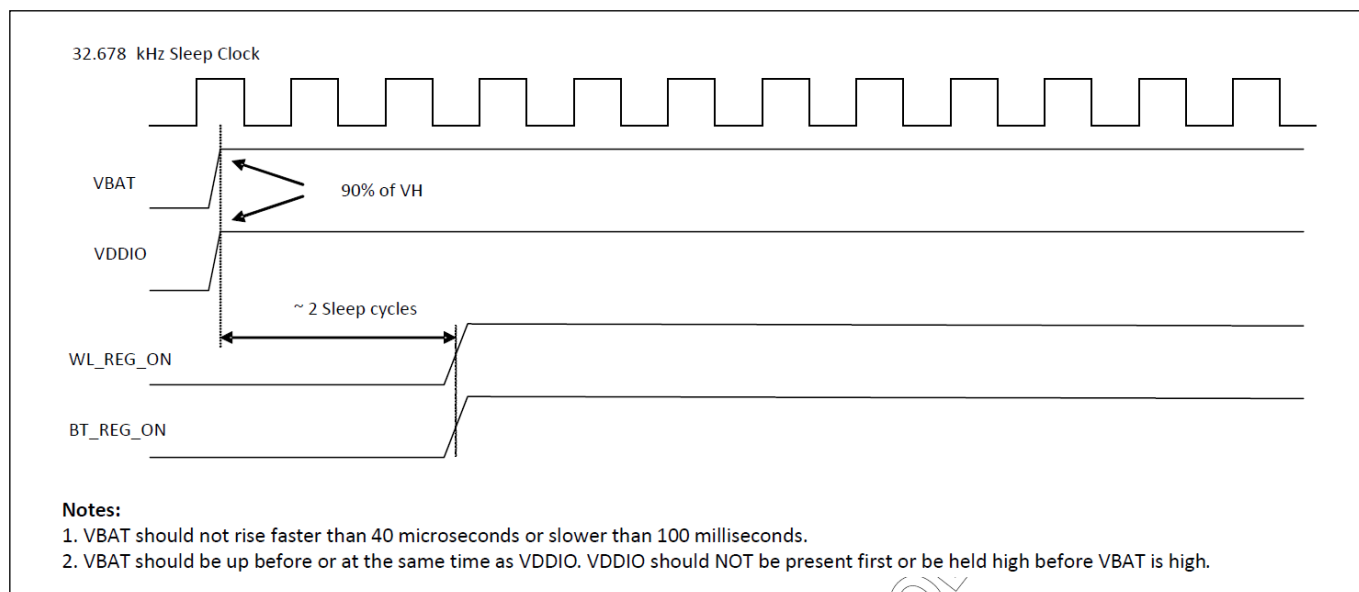
**Power-Up/Power-Down/Reset Control Signals**

Signal	Description
WL_REG_ON	This signal is used by the PMU (with BT_REG_ON) to power up the WLAN section. It is also ORgated with the BT_REG_ON input to control the internal AW-NMNF regulators. When this pin is high, the regulators are enabled and the WLAN section is out of reset. When this pin is low, the WLAN section is in reset. If BT_REG_ON and WL_REG_ON are both low, the regulators are disabled. This pin has an internal 200 kΩ pull-down resistor that is enabled by default. It can be disabled through programming.
BT_REG_ON	This signal is used by the PMU (with WL_REG_ON) to decide whether or not to power down the internal AW-NM256SM regulators. If both BT_REG_ON and WL_REG_ON are low, the regulators will be disabled. When this pin is low and WL_REG_ON is high, the BT section is in reset. This pin has an internal 200 kΩ pull-down resistor that is enabled by default. It can be disabled through programming.

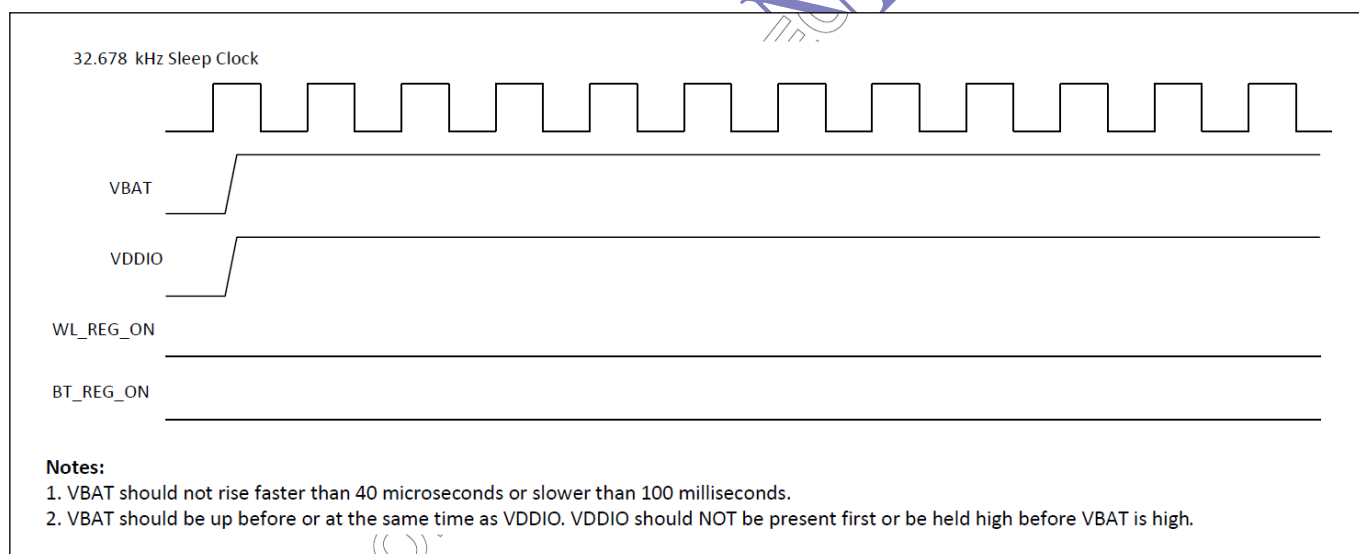
**Note:** For both the WL\_REG\_ON and BT\_REG\_ON pins, there should be at least a 10 msec time delay between consecutive toggles (where both signals have been driven low). This is to allow time for the CBUCK regulator to discharge. If this delay is not followed, then there may be a VDDIO in-rush current on the order of 36 mA during the next PMU cold start.

## Control Signal Timing Diagrams

**WLAN = ON, Bluetooth = ON**

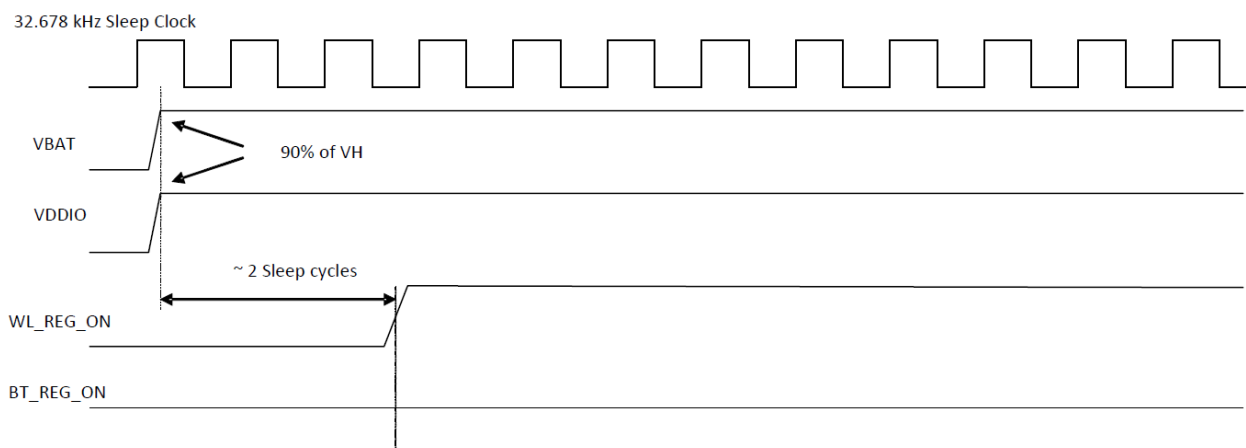


**WLAN = OFF, Bluetooth = OFF**





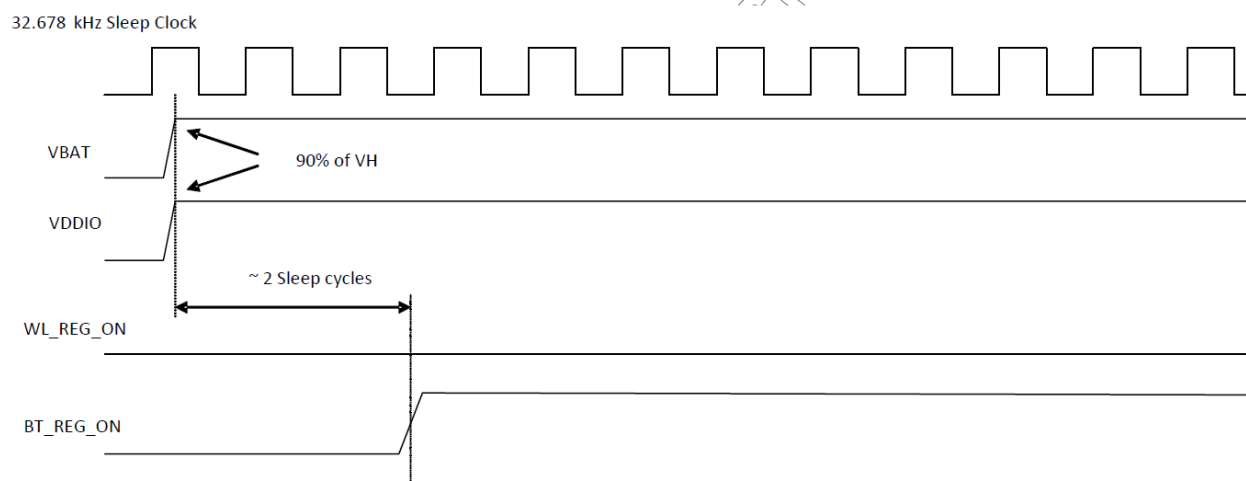
# WLAN = ON, Bluetooth = OFF



## Notes:

1. VBAT should not rise faster than 40 microseconds or slower than 100 milliseconds.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

# WLAN = OFF, Bluetooth = ON



## Notes:

1. VBAT should not rise faster than 40 microseconds or slower than 100 milliseconds.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

## 4-5. Frequency Reference

An external crystal is used for generating all radio frequencies and normal operation clocking. As an alternative, an external frequency reference driven by a temperature-compensated crystal oscillator (TCXO) signal may be used. No software settings are required to differentiate between the two. In addition, a low-power oscillator (LPO) is provided for lower power mode timing.

### External 32.768KHz Low-Power Oscillator

The AW-NM256SM uses a secondary low frequency clock for low-power-mode timing. Either the internal low-precision LPO or an external 32.768 kHz precision oscillator is required. The internal LPO frequency range is approximately 33 kHz  $\pm$  30% over process, voltage, and temperature, which is adequate for some applications. However, one trade-off caused by this wide LPO tolerance is a small current consumption increase during power save mode that is incurred by the need to wake-up earlier to avoid missing beacons. Whenever possible, the preferred approach is to use a precision external 32.768 kHz clock that meets the requirements listed in below.

**External 32.768 kHz Sleep Clock Specifications**

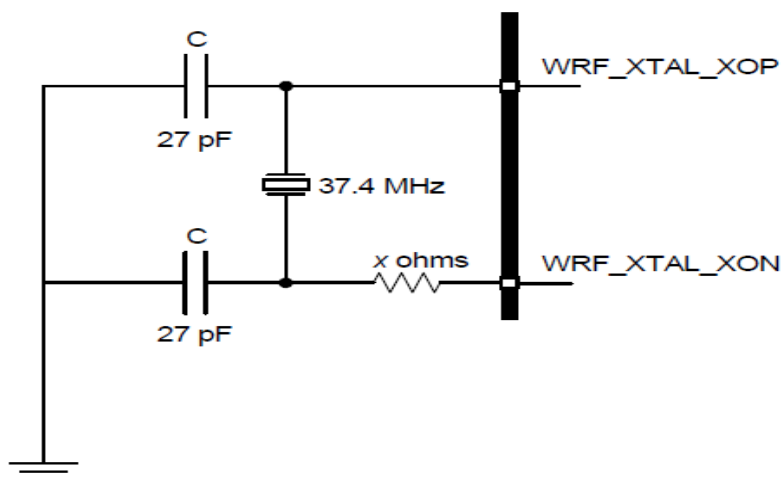
Parameter	LPO Clock	Units
Nominal input frequency	32.768	kHz
Frequency accuracy	$\pm 200$	ppm
Duty cycle	30–70	%
Input signal amplitude	200–3300	mV, p-p
Signal type	Square-wave or sine-wave	–
Input impedance <sup>a</sup>	>100k	$\Omega$
	<5	pF
Clock jitter (during initial start-up)	<10,000	ppm

a. When power is applied or switched off.

## Crystal Interface and Clock Generation

The AW-NM256SM can use an external crystal to provide a frequency reference. The recommended configuration for the crystal oscillator including all external components is shown in below. Consult the reference schematics for the latest configuration.

**Recommended Oscillator Configuration**



A fractional-N synthesizer in the AW-NM256SM generates the radio frequencies, clocks, and data/packet timing, enabling it to operate using a wide selection of frequency references. The recommended default frequency reference is a **37.4 MHz crystal**. The signal characteristics for the crystal interface are listed in below

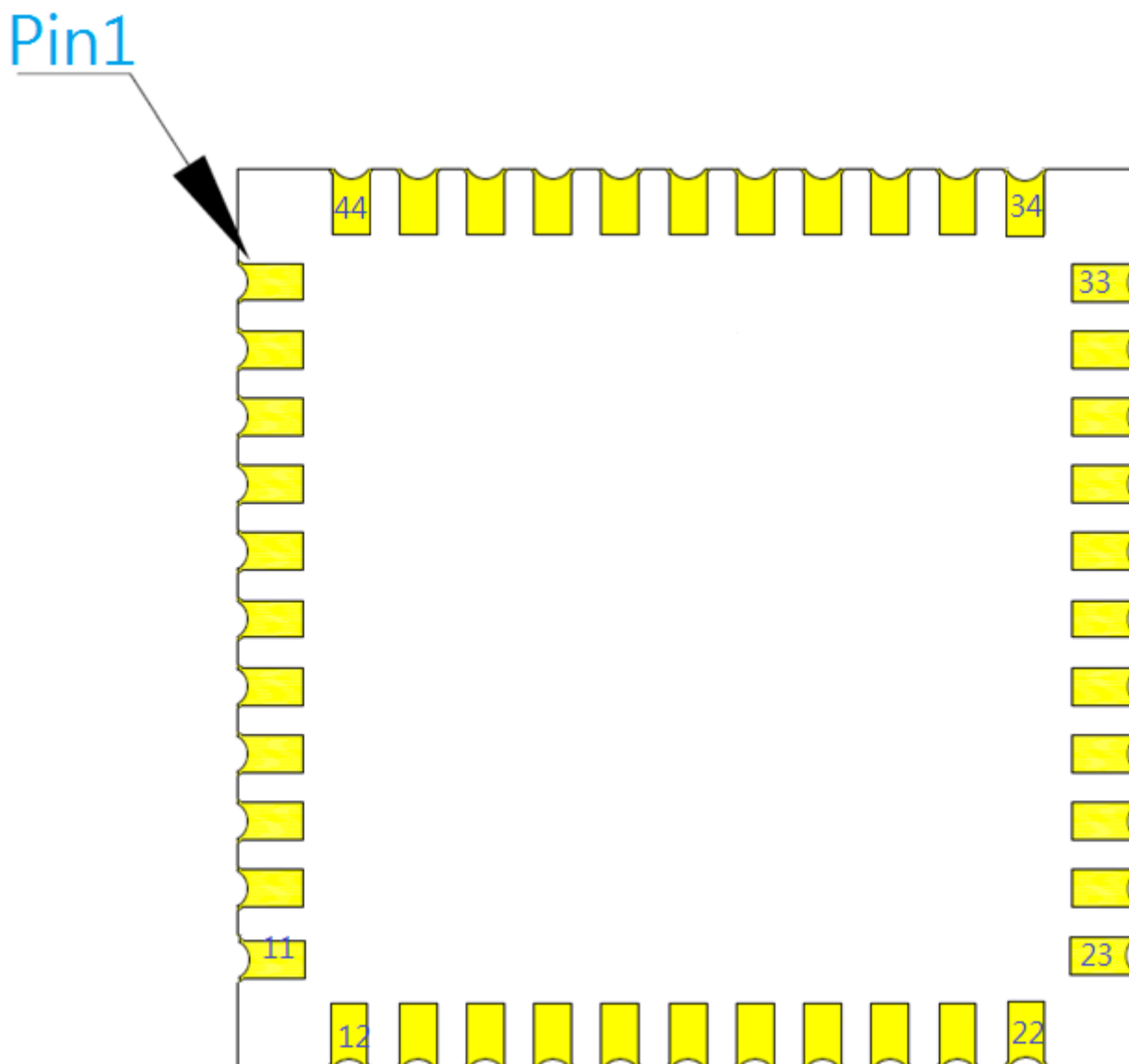
**Crystal Oscillator and External Clock—Requirements and Performance (Cont.)**

Parameter	Conditions/Notes	Crystal <sup>a</sup>			External Frequency Reference <sup>b c</sup>			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
WRF_XTAL_XOP Input high level	DC-coupled digital signal	–	–	–	1.0	–	1.26	V
WRF_XTAL_XOP input voltage (see Figure 6 on page 30)	IEEE 802.11a/b/g operation only	–	–	–	400	–	1200	mV <sub>p-p</sub>
WRF_XTAL_XOP input voltage (see Figure 6 on page 30)	IEEE 802.11n/ac AC-coupled analog input	–	–	–	1	–	–	V <sub>p-p</sub>
Duty cycle	37.4 MHz clock	–	–	–	40	50	60	%
Phase Noise <sup>g</sup> (IEEE 802.11b/g)	37.4 MHz clock at 10 kHz offset	–	–	–	–	–	–129	dBc/Hz
	37.4 MHz clock at 100 kHz offset	–	–	–	–	–	–136	dBc/Hz
Phase Noise <sup>g</sup> (IEEE 802.11a)	37.4 MHz clock at 10 kHz offset	–	–	–	–	–	–137	dBc/Hz
	37.4 MHz clock at 100 kHz offset	–	–	–	–	–	–144	dBc/Hz
Phase Noise <sup>g</sup> (IEEE 802.11n, 2.4 GHz)	37.4 MHz clock at 10 kHz offset	–	–	–	–	–	–134	dBc/Hz
	37.4 MHz clock at 100 kHz offset	–	–	–	–	–	–141	dBc/Hz
Phase Noise <sup>g</sup> (IEEE 802.11n, 5 GHz)	37.4 MHz clock at 10 kHz offset	–	–	–	–	–	–142	dBc/Hz
	37.4 MHz clock at 100 kHz offset	–	–	–	–	–	–149	dBc/Hz
Phase Noise <sup>g</sup> (IEEE 802.11ac, 5 GHz)	37.4 MHz clock at 10 kHz offset	–	–	–	–	–	–148	dBc/Hz
	37.4 MHz clock at 100 kHz offset	–	–	–	–	–	–155	dBc/Hz

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## 5. Connector Pin-out Definitions

### AW-NM256SM Top View PCB Layout Footprint



Note: The pin name and direction are defined on module side.



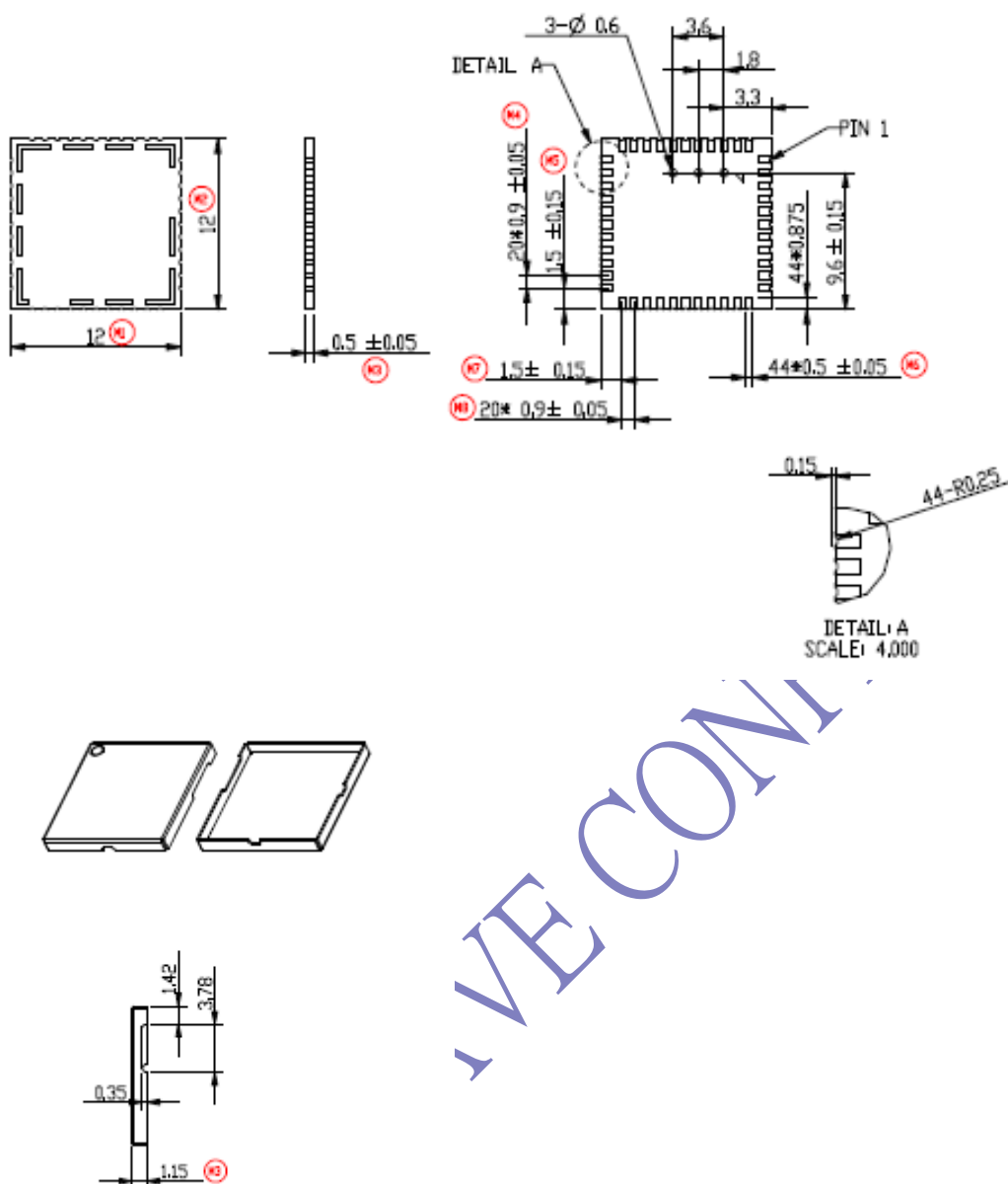
Pin No	Definition	Basic Description	Type
1	GND	Ground.	GND
2	WL_BT_ANT	WLAN/BT RF TX/RX path.	RF
3	GND	Ground.	GND
4	NC	Floating Pin, No connect to anything.	Floating
5	NC	Floating Pin, No connect to anything.	Floating
6	BT_WAKE	BT Device Wake	I
7	BT_HOSTWAKE	BT Host Wake	O
8	NC	Floating Pin, No connect to anything.	Floating
9	VBAT	3.3V power pin	VCC
10	XTAL_IN	Crystal Input(37.4MHz)	I
11	XTAL_OUT	Crystal Output(37.4MHz)	O
12	WL_REG_ON	Used by PMU to power up or power down the internal regulators used by the WLAN section. Also, when deasserted, this pin holds the WLAN section in reset. This pin has an internal 200k ohm pull down resistor that is enabled by default. It can be disabled through programming.	I
13	WL_SDIO_HOSTWAKE	WL Host Wake	O
14	SDIO_DATA2	SDIO Data Line 2	I/O
15	SDIO_DATA3	SDIO Data Line 3	I/O
16	SDIO_CMD	SDIO Command Input	I/O
17	SDIO_CLK	SDIO Clock Input	I
18	SDIO_DATA0	SDIO Data Line 0	I/O
19	SDIO_DATA1	SDIO Data Line 1	I/O
20	GND	Ground.	GND
21	VIN_LDO_OUT	Internal Buck voltage generation pin	VCC
22	VDDIO	1.8V-3.3V VDDIO supply for WLAN and BT	VCC
23	VIN_LDO	Internal Buck voltage generation pin	VCC
24	SUSCLK_IN	External 32K or RTC clock	I
25	BT_PCM_OUT	PCM data Out	O
26	BT_PCM_CLK	PCM Clock	I/O
27	BT_PCM_IN	PCM data Input	I
28	BT_PCM_SYNC	PCM Synchronization control	O
29	GPIO_7	SDIO mode selection pin 1.8V:pull up, connect to 1.8V 3.3V:pull down, connect to GND with using a 10K resistor or less	I
30	NC	Floating Pin, No connect to anything.	Floating



31	GND	Ground.	GND
32	NC	Floating Pin, No connect to anything.	Floating
33	GND	Ground.	GND
34	BT_REG_ON	Used by PMU to power up or power down the internal regulators used by the Bluetooth section. Also, when deasserted, this pin holds the Bluetooth section in reset. This pin has an internal 200k ohm pull down resistor that is enabled by default. It can be disabled through programming.	I
35	NC	Floating Pin, No connect to anything.	Floating
36	GND	Ground.	GND
37	GPIO_6	GPIO configuration pin	I/O
38	GPIO_3	GPIO configuration pin	I/O
39	GPIO_5	GPIO configuration pin	I/O
40	GPIO_2	GPIO configuration pin	I/O
41	BT_UART_RTS_N	High-Speed UART RTS	O
42	BT_UART_TXD	High-Speed UART Data Out	O
43	BT_UART_RXD	High-Speed UART Data In	I
44	BT_UART_CTS_N	High-Speed UART CTS	I

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## 6. Mechanical Dimensions



## 7. Assembly note

- AW-CM256SM removed from the vacuum packaging must be within 168 hours do SMT process and had finished Reflow.
- If AW- CM256SM cannot reflow finished within the specified time, it must be according to the baking conditions 2 hours at temperature of 125 degrees C and then re-bake for vacuum packaging.
- Reflow (Reflow) temperature need to be based on the size of the motherboard (generally in accordance with the solder paste used by customers Reflow Profile may be).
- Need to pick up the WIFI module, operating in accordance with ESD protection norms.