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AN210403

Hardware Design Guidelines for DRP Applications Using EZ-PD USB Type-C Controllers

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Associated Part Family: CYPD212x, CYPD3125, CYPD4x25, CYPD5x25, CYPD5126, CYPD612X, CYPD622X

Related Application Notes: Click here

To get the latest version of this application note, please visit http://www.cypress.com/AN210403.

AN210403 provides hardware design and PCB layout guidelines for designing a Dual Role Power (DRP) application (for example, a notebook with a Type-C port) using EZ-PD™ CCG2, CCG3, CCG4, CCG5, CCG5C, CCG6, CCG6F, CCG6SF, and CCG6DF USB Type-C controllers. The application note also demonstrates DRP application examples using Cypress evaluation kits as reference.

Contents

Abbreviations

Abbreviation	Description
ABUS	analog output bus
AC	alternating current
ADC	analog-to-digital converter
AHB	AMBA (advanced microcontroller bus architecture) high-performance bus, an ARM® data transfer bus
API	application programming interface
APOR	analog power-on reset
BMC	Bi-Phase Mark Coding
BR	bit rate
BRA	bus request acknowledge
BRQ	bus request
CAN	controller area network
CC	Configuration Channel
CCG5	Cypress' fifth Generation USB Type-C Controller
CI	carry in
CMP	Compare
CO	carry out
CPU	central processing unit
CRC	cyclic redundancy check
CSN	Current Sense Negative Input
CSP	Current Sense Positive Input
CT	continuous time
DAC	digital-to-analog converter
DC	direct current
DFP	Downstream Facing Port
DI	digital or data input
DMA	direct memory access
DNL	differential nonlinearity
DO	digital or data output
DRP	Dual Role Power

Abbreviation	Description
DSI	digital signal interface
DSM	deep-sleep mode
ECO	external crystal oscillator
EEPROM	electrically erasable programmable read only memory
EMCA	Electronically Marked Cable Assembly
EMIF	external memory interface
FB	Feedback
FIFO	first in first out
FSR	full scale range
GPIO	general purpose I/O
HCI	host-controller interface
HFCLK	high-frequency clock
I^2C	inter-integrated circuit
IDE	integrated development environment
ILO	internal low-speed oscillator
IMO	internal main oscillator
INL	integral nonlinearity
I/O	input/output
IOR	I/O read
IOW	I/O write
IRES	initial power on reset
IRA	interrupt request acknowledge
IRQ	interrupt request
ISR	interrupt service routine
IVR	interrupt vector read
LRb	last received bit
LRB	last received byte
LSb	least significant bit
LSB	least significant byte

Abbreviation	Description
LUT	lookup table
MISO	master-in-slave-out
MMIO	memory mapped input/output
MOSI	master-out-slave-in
MSb	most significant bit
MSB	most significant byte
PC	program counter
PCH	program counter high
PCL	program counter low
PD	power down
PGA	programmable gain amplifier
PM	power management
PMA	CCG4 memory arbiter
POR	power-on reset
PPOR	precision power-on reset
PRS	pseudo random sequence
PSRR	power supply rejection ratio
PSSDC	power system sleep duty cycle
PWM	pulse width modulator
RAM	random-access memory
RCP	Reverse Current Protection
RETI	return from interrupt
RF	radio frequency
ROM	read only memory
RW	read/write
SAR	successive approximation register
SC	switched capacitor
SCB	serial communication block
SCP	Short Circuit Protection
SIE	serial interface engine

Abbreviation	Description
SIO	special I/O
SE0	single-ended zero
SNR	signal-to-noise ratio
SOF	start of frame
SOI	start of instruction
SOP	Start of Packet
SP	stack pointer
SPD	sequential phase detector
SPI	serial peripheral interconnect
SPIM	serial peripheral interconnect master
SPIS	serial peripheral interconnect slave
SRAM	static random-access memory
SROM	supervisory read only memory
SSADC	single slope ADC
SSC	supervisory system call
SYSCLK	system clock
SWD	serial wire debug
TC	terminal count
TD	transaction descriptors
TRNG	True Random Number Generator
UART	universal asynchronous receiver/transmitter
UFP	Upstream Facing Port
USB	universal serial bus
USBIO	USB I/O
USB PD	USB Power Delivery
WCO	watch crystal oscillator
WDT	watchdog timer
WDR	watchdog reset

1 Introduction

The USB Power Delivery (PD) Specification Revision 3.0, Version 2.0 defines power delivery up to 100 W (20 V at 5 A) over existing USB standards. The USB Type-C Cable and Connector Specification Revision 2.0 details a new reversible and sub-3-mm slim connector design that supports 100 W of power along with USB and non-USB signals such as DisplayPort.

Cypress provides a portfolio of USB Type-C and PD controllers, including EZ-PD CCG1, EZ-PD CCG2, EZ-PD CCG3, EZ-PD CCG4, EZ-PD CCG5, EZ-PD CCG5C, EZ-PD CCG6, EZ-PD CCG6F, EZ-PD CCG6SF, and CCG6DF.

CCG1 is Cypress' first-generation Type-C and PD controller, which supports up to two USB ports with PD. CCG1 has 32 KB flash and 4 KB SRAM memory. CCG1 is a fixed-function part and the functionality is implemented in the CCG1 device's firmware. CCG1 provides a USB Type-C and Power Delivery solution for notebooks, monitors, docking stations, power adapters, and USB Type-C cables.

CCG2 is Cypress' second-generation Type-C and PD controller, integrating one Type-C transceiver and termination resistors Rp, Rd, and Ra. CCG2 has 32 KB of flash and 4 KB of SRAM memory. It provides a complete USB Type-C and Power Delivery solution for Type-C notebook and cable designs.

CCG3 is Cypress' third-generation USB Type-C and PD controller, integrating one Type-C transceiver and termination resistors Rp, Rd, and Ra. CCG3 provides additional features such as a crypto engine for authentication, two integrated pairs of gate drivers to control the VBUS provider and consumer path, integrated VCONN and VBUS discharge FETs, integrated overvoltage and overcurrent protection, and USB 2.0 Billboard support. In addition, CCG3 has 128 KB of flash and 8 KB of SRAM memory.

CCG4 is Cypress' fourth-generation Type-C and PD controller, which includes two Type-C transceivers and termination resistors Rp and Rd. CCG4 has integrated VCONN FETs, 128 KB of flash, and 8 KB of SRAM memory. CCG4 provides a complete solution for dual Type-C port notebook and power adapter designs.

CCG5 is Cypress' fifth-generation Type-C and PD controller, which includes two Type-C transceivers and termination resistors Rp and Rd. CCG5 is an enhancement to CCG4 with integrated (Side Band Usage) SBU muxes, HS (High Speed) muxes, 20-V VBUS regulator and High-side current sense amplifier. CC and SBU pins are made high-voltage-tolerant to withstand VBUS to CC line-short faults. CCG5 provides a complete solution for dual Type-C port notebook and dock station designs. CCG5C is enhanced version of CCG5 which supports single port Type-C and PD control. CCG5C is pin-compatible to the CCG5 controller 40-pin QFN package.

CCG6 is Cypress' sixth-generation Type-C and PD controller, which includes a single Type-C transceiver and termination resistors Rp and Rd. CCG6 has an integrated Load Switch Controller in the VBUS provider path, which can protect the system from reverse current and short circuit faults. CCG6 also supports true random number generator for firmware authentication. CCG6F is an enhancement of CCG6 as it has an integrated PFET in the VBUS provider path. CCG6F controller supports Thermal Shutdown.

CCG6DF and CCG6SF are Cypress′ sixth-generation Type-C and PD controllers for Thunderbolt and Non-Thunderbolt platforms. CCG6DF includes two Type-C transceivers and termination resistors Rp and Rd while CCG6SF includes a single Type-C transceiver and termination resistors Rp and Rd. CCG6DF and CCG6SF have been enhanced from CCG6 by including the VBUS provider path load switch (5 V/3 A) on each port, which will reduce the system Bill-of-Material (BOM) cost. CCG6SF and CCG6DF controllers support Thermal Shutdown.

These Type-C and PD controllers are fully compliant with the USB PD and Type-C standards. Table 1 summarizes the differences among them.

Table 1. Feature Comparison of Cypress' USB Type-C and PD Controllers

Features	CCG1	CCG2	CCG3	CCG4	CCG5/5C	CCG6/ CCG6F	CCG6SF/ CCG6DF
Number of Type-C and PD Ports	1	1	1	2	2 / 1	1	1/2
Integrated Arm® Cortex®-M0 MCU at 48 MHz	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Memory (Flash, SRAM)	32 KB, 4 KB	32 KB, 4 KB	128 KB, 8 KB	128 KB, 8 KB	128 KB, 12 KB	128 KB, 12 KB	64 KB, 16 KB
Integrated Type-C Transceiver (Number)	Yes (1)	Yes (1)	Yes (1)	Yes (2)	Yes (2) / Yes (1)	Yes (1)	Yes (1) / Yes (2)
Integrated Type-C Resistors	No	Yes (Ra, Rp, Rd)	Yes (Ra, Rp, Rd)	Yes (Rp, Rd)	Yes (Rp, Rd)	Yes (Rp, Rd)	Yes (Rp, Rd)
Number of GPIOs	Up to 30	Up to 14	Up to 20	Up to 30	Up to 38 / Up to 15	Up to 17	Up to 20 / Up to 23
Number of Serial Communication Blocks (I^2C/SPI/UART)	1	2	4	4	4	4	4
Number of TCPWM Blocks (Each block can be configured as timer, counter, or pulse width modulator)	2	6	4	4	2	2	2
Integrated USB Billboard Device Class Full Speed USB 2.0 Device	No	No	Yes	No	No	No	No
Hardware Authentication Block (Crypto)	No	No	Yes	No	No	Yes TRNG only	Yes TRNG only

Features	CCG1	CCG2	CCG3	CCG4	CCG5/5C	CCG6/ CCG6F	CCG6SF/ CCG6DF
Integrated VCONN FETs	No	No	Yes (1 pair)	Yes (2 pairs)	Yes (2 pairs) / Yes (1 pair) With VCONN Overcurrent Protection	Yes (1 pair)	Yes (1 pair) / Yes (2 pairs)
Integrated VBUS Discharge FETs	No	No	Yes	No	Yes	Yes	Yes
Integrated 20-V VBUS NFET/PFET Gate Drivers	No	No	Yes (2 pairs)	No	No	No	No
Integrated SBU/AUX Analog Switch	No	No	Yes	No	Yes	Yes	Yes
Supply Voltage	1.8 V – 5.5 V	2.7 V – 5.5 V	2.7 V – 21.5 V	2.7 V – 5.5 V	2.7 V – 21.5 V/ 2.75 V– 21.5 V for CCG5C	2.75 V – 21.5 V	2.75 V – 21.5 V
VBUS Overvoltage Protection (OVP), Undervoltage Protection (UVP) and Overcurrent Protection (OCP)	Yes (Using external hardware circuitry)	Yes (Using external hardware circuitry)	Yes (Integrated)	Yes (Using external hardware circuitry)	Yes (Integrated)	Yes (Integrated)	Yes (Integrated)
Integrated ADCs for OVP, UVP, OCP Detection and Other Voltage or Current Measurements	1 channel (12-bit SAR)	1 channel (8-bit SAR)	2 channels (8-bit SAR)	4 channels (8-bit SAR)	4 channels / 1-channel (8-bit SAR)	1 channel (8-bit SAR)	1 channel (8-bit SAR)
Load Switch Controller for RCP and SCP	No	No	No	No	No	Yes	Yes
Integrated 20 V VBUS PFET	No	No	No	No	No	Included in CCG6F Only	No
Integrated VBUS Provider Switch	No	No	No	No	No	Yes (CCG6F only)	Yes (5 V/3 A)
Thermal Shutdown	No	No	No	No	No	Included in CCCG6F only	Yes
USB Battery Charger (BC) Revision 1.2 and Legacy Apple Charger Detection and Emulation	No	No	Yes	No	Yes	Yes	Yes
ESD Protection	Yes (Up-to 2.2 kV)	Yes (Up-to ± 8-kV contact discharge and up-to ±15-kV air discharge)	Yes (Up-to ± 8-kV contact discharge and up-to ±15-kV air discharge)	Yes (Up-to ± 8-kV contact discharge and up-to ±15-kV air discharge)	Yes (Up to ± 8-kV contact discharge and up to ±15-kV air discharge) / Human Body Model only for CCG5C	Yes (Human Body Model Only)	Yes (Human Body Model Only)
Packages	40-QFN, 16-SOIC, 35-CSP	24-QFN, 14-DFN, 20-CSP	40-QFN, 42-CSP, 16-SOIC	40-QFN	40-QFN 96-BGA/ 40-QFN	40-QFN/ 96-BGA	48-QFN 96-BGA

This application note provides information on designing USB Type-C DRP applications using CCG2, CCG3, CCG4 CCG5, CCG5C, CCG6, CCG6F, CCG6SF, and CCG6DF. CCG2, CCG3, CCG4, CCG5, CCG5C, CCG6, CCG6SF, and CCG6DF controllers have more integrated features as compared to CCG1, which help to reduce the BOM cost of DRP application design. See AN96527 – Designing USB Type-C Products Using Cypress' CCG1 Controllers for detailed information on USB Type-C designs using CCG1. This application note gives a brief overview of CCG2, CCG3, CCG4, CCG5, CCG5C, CCG6, CCG6SF, and CCG6DF, and explains the power subsystem required to kick start the design. It provides hardware guidelines for a successful notebook design with a single or dual Type-C port using Cypress' Type-C and PD controllers. The application note provides information on how to use the CCG4 Evaluation Kit (see Table 2 for Type-C PD controller evaluation kits) to demonstrate the DRP application.

Table 2. Type-C and PD Controller Evaluation Kits

Type-C PD Controller	Type-C PD Controller Evaluation Kit
CCG2	CY4521 EZ-PD CCG3 Evaluation Kit
CCG3	CY4531 EZ-PD CCG3 Evaluation Kit
CCG4	CY4541 EZ-PD CCG4 Evaluation Kit

This application note references the CY4541 EZ-PD CCG4 Evaluation Kit and is intended as supplemental information to the respective kit guide.

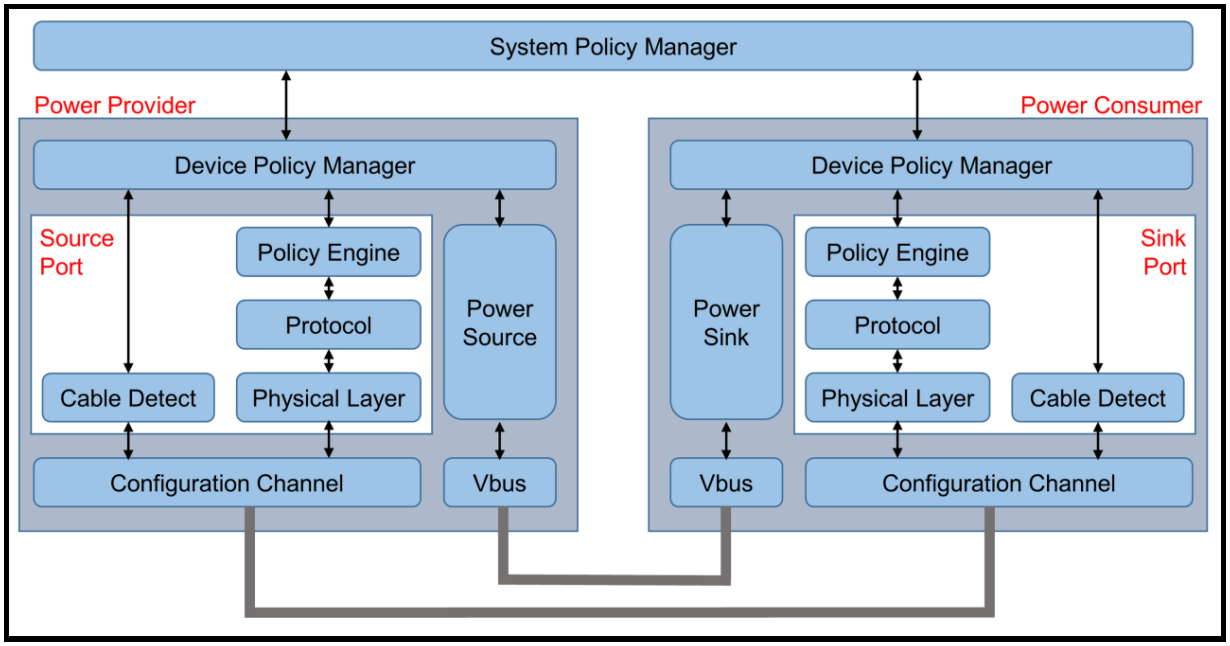
2 USB Power Delivery Specification

This section reviews the basics of USB power delivery. The USB PD specification defines how a PD-enabled USB port can get the required power from VBUS by negotiating with external power sources (such as wall warts).

A USB port providing power is known as a source, and a USB port consuming power is known as a sink. There is only one source port and one sink port in each PD connection. In the legacy USB specification, the USB port on host computer (such as a notebook or a PC) was always a source and the USB peripheral device was always a sink. The USB PD specification allows the source and sink to interchange their roles so that a USB peripheral device (such as an external self-powered hard disk or monitor) can supply power to a USB Host. These new power roles are independent of the USB data transfer roles between the USB Host and USB device. An example is a self-powered USB peripheral such as a monitor that can charge the battery of a notebook or PC, which is a USB Host.

Figure 1 shows logical block diagram of the Type-C and PD architecture.

Figure 1. Type-C and PD Architecture for Dual Role Power Applications



- **System Policy Manager:** The PD Specification defines a System Policy Manager that is implemented on the USB Host running as an operating system stack. For more details of System Policy, see the PD Specification.
- **Device Policy Manager:** The Device Policy Manager is the module running in the Power Provider or Power Consumer, which applies a Local Policy to each Port in the device via the Policy Engine.
- **Source Port:** The Source Port is the power provider port, which supplies power over VBUS. It is, by default, a USB port on the Host or Hub.
- **Sink Port:** The Sink Port is the USB power consumer port, which consumes power over VBUS. It is, by default, a USB port on a device.
- **Policy Engine:** The Policy Engine interprets the Device Policy Manager's input to implement the Policy for the port. It also directs the Protocol Layer to send messages.
- **Protocol:** The Protocol Layer creates the messages for communication between Port Partners.
- **Physical Layer:** The Physical Layer sends and receives messages over either VBUS or the configuration channel (CC) between Port Pairs.
- **Power Source:** The ability of a Power Delivery (PD) port to source power over VBUS. This refers to a Type-C port with Rp asserted on CC.
- **Power Sink:** The ability of a Power Delivery (PD) port to sink power from VBUS. This refers to a Type-C port with Rd asserted on CC.
- **Cable Detection Module:** The Cable Detection Module detects the presence of an Electronically Marked Cable Assembly (EMCA) cable attached to a Type-C port.

Dual-role devices can be developed by combining both provider and consumer elements in a single device.

When a USB Host and USB device are interconnected, they form a USB link pair, and each link partner has a configuration channel (CC) controller. Messages are then logically exchanged among Device Policy Managers within each PD controller. These messages are physically transferred over the CC, and a PD contract is set up between the link pair, and then power is delivered over VBUS.

The CC is a new signal pair in the Type-C signal definition—see Type-C Signal Definition.

2.1 Type-C Signal Definition

Figure 2 shows the USB Type-C Receptacle, Plug, and Flipped-Plug signals. Table 3, Figure 3, and Table 4 show the signals used on the USB Type-C receptacle and plug.

Figure 2. USB Type-C Plug, Receptacle, and Flipped-Plug Signals

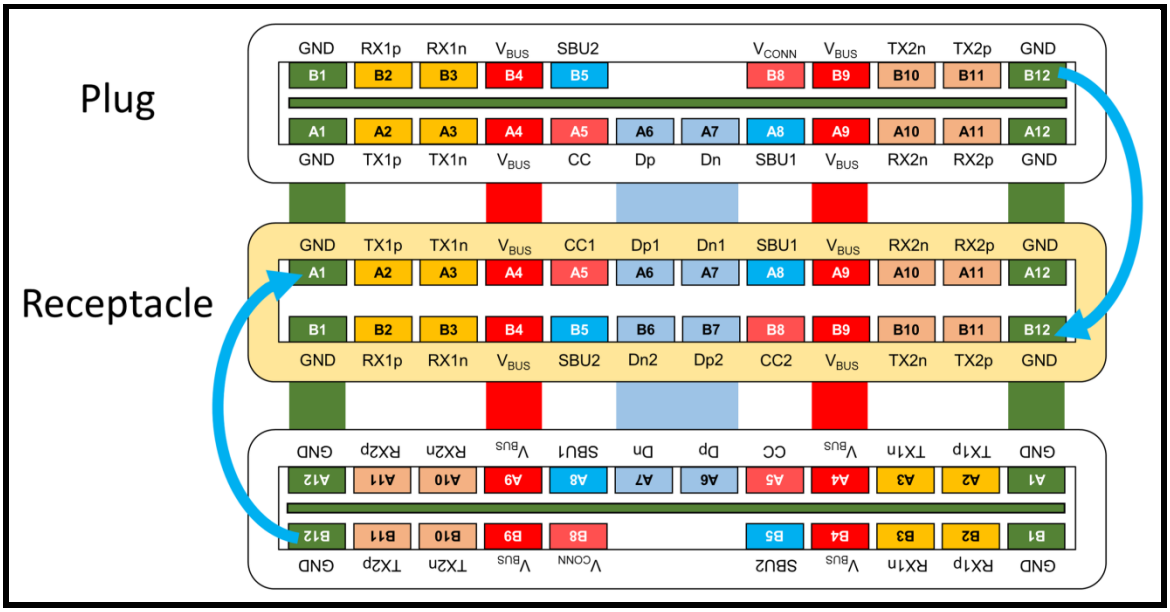


Table 3. USB Type-C Receptacle Signals

Signal Group	Signal	Description
USB 3.1	TX1p, TX1n, RX1p, RX1n, TX2p, TX2n, RX2p, RX2n	The SuperSpeed USB serial data interface defines a differential transmit pair and a differential receive pair. On a USB Type-C receptacle, two pairs of SuperSpeed USB signal pins are defined to enable the plug-flipping feature.
USB 2.0	Dp1, Dn1 Dp2, Dn2	The USB 2.0 serial data interface defines a differential pair. On a USB Type-C receptacle, two sets of USB 2.0 signal pins are defined to enable plug-flipping.
Configuration Channel	CC1, CC2	The CC in the receptacle detects the signal orientation and channel configuration.
Auxiliary signals	SBU1, SBU2	Sideband use. See the USB Type-C Cable and Connector Specification Revision 1.3 for more details.
Power	VBUS	USB cable bus power
	GND	USB cable return current path

Table 4. USB Type-C Plug Signals

Signal Group	Signal	Description
USB 3.1	TX1p, TX1n RX1p, RX1n TX2p, TX2n RX2p, RX2n	The SuperSpeed USB serial data interface defines a differential transmit pair and a differential receive pair. On a USB Type-C plug, two pairs of SuperSpeed USB signal pins are defined to enable the plug-flipping feature.
USB 2.0	Dp, Dn	On a USB Type-C plug, the USB 2.0 serial data interface defines differential pair.
Configuration Channel	CC	The CC in the plug is used for connection detection and interface configuration.
Auxiliary signals	SBU1, SBU2	Sideband use. See the USB Type-C Cable and Connector Specification Revision 1.3 for more details.
Power	VBUS	USB cable bus power
	VCONN	Type-C cable plug power
	GND	USB cable return current path

As shown in Figure 2, the USB Type-C receptacle has USB 3.1 (TX and RX pairs) and USB 2.0 (Dp and Dn) data buses, USB power (VBUS), ground (GND), CC signals (CC1 and CC2), and two sideband use (SBU) signal pins. As listed in Table 3 and Table 4, the descriptions of the USB Type-C plug and receptacle signals are the same, except for the CC and VCONN signals. The two sets of USB 2.0 and USB 3.1 signal locations in this layout facilitate the mapping of the USB signals independent of the plug orientation in the receptacle.

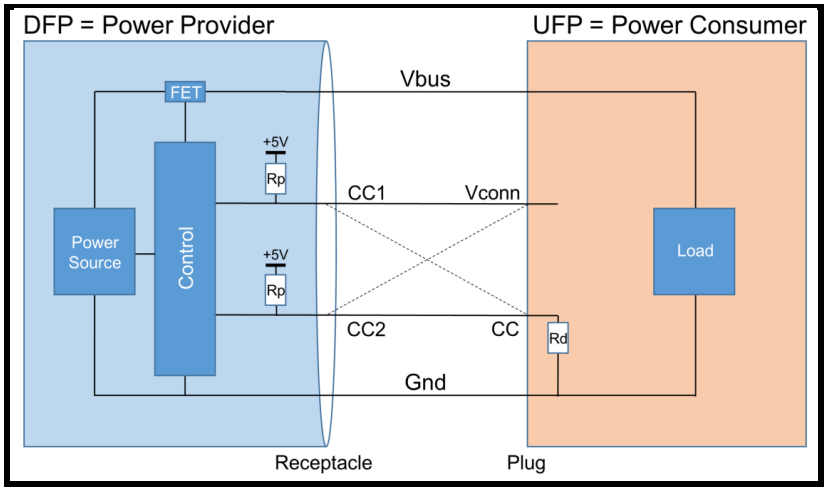
When a cable with the Type-C plug is inserted into the receptacle, one CC pin is used to establish signal orientation, and the other CC pin is repurposed as VCONN for powering the electronics in the USB Type-C cable (plug).

2.2 Type-C Ports

2.2.1 Downstream Facing Port and Upstream Facing Port

A Type-C downstream facing port (DFP) is by default a USB Host and a power source, whereas a Type-C upstream facing port (UFP) is by default a USB Device and a power sink. A DFP exposes Rp terminations on its CC pins (CC1 and CC2), while a UFP exposes Rd terminations on its CC pin, as shown in Figure 3.

Figure 3. Direct Connection of a Downstream Facing Port and Upstream Facing Port



DFPs, specifically those associated with the flow of data in a USB connection, are typically the USB ports on a Host such as a PC or a hub. In its default state, the DFP sources VBUS and VCONN. On the other hand, UFP sinks VBUS.

2.2.2 USB PD Dual Role Power

PD-enabled USB products (such as a notebook with a Type-C port) operate as a power provider and a power consumer. The USB PD specification refers to such USB Type-C port as Dual Role Power (DRPs).

DRP devices have the capability to detect the presence of the Rp and Rd resistors on the CC lines. A typical DRP device can perform the roles listed in Table 5.

Table 5. Roles of DRP Device

No.	Data Port Role (USB Host or Device)	Power Port Role (Power Provider or Power Consumer)
1	DFP	Source (Power Provider, Connect Rp and disconnect Rd)
2	DFP	Sink (Power Consumer, Disconnect Rp and connect Rd)
3	UFP	Source (Power Provider, Connect Rp and disconnect Rd)
4	UFP	Sink (Power Consumer, Disconnect Rp and connect Rd)

3 CCGx Devices Overview

Table 6 lists the available part numbers for CCG2, CCG3, CCG4, CCG5, CCG5C, CCG6, CCG6F, CCG6SF, and CCG6DF Type-C and PD controllers with their respective applications.

Table 6. Type-C PD Controller MPNs and Applications

Type-C PD Controller	Manufacturing Part Number	Role	Application	Package
CCG2	CYPD2122-24LQXIT	DRP	Notebooks	24-pin QFN
	CYPD2122-20FNXIT	DRP	Tablets	20-ball CSP
	CYPD2121-24LQXIT	DRP	Dock/Monitor Upstream Port	24-pin QFN
	CYPD2134-24LQXIT	DFP	Power Adapter	24-pin QFN
	CYPD2125-24LQXIT	DFP	Dock/Monitor Downstream Port	24-pin QFN
	CYPD2103-20FNXIT	Cable	Cable	20-ball CSP
	CYPD2119-24LQXIT	C-DP	UFP	24-pin QFN
	CYPD2120-24LQXIT	C-HDMI	UFP	24-pin QFN
	CYPD2103-14LHXIT	Cable	Cable	14-pin DFN
	CYPD2105-20FNXIT	Active Cable	Active Cable	20-ball CSP
	CYPD2104-20FNXIT	Accessory	Accessory	20-ball CSP
CCG3	CYPD3125-40LQXIT	DRP	Notebooks	40-pin QFN
	CYPD3121-40LQXIT	DFP	Monitor/Dock	40-pin QFN
	CYPD3135-40LQXIT	DFP	Power Adapter	40-pin QFN
	CYPD3122-40LQXIT	UFP	Monitor/Dock	40-pin QFN
	CYPD3120-40LQXIT	UFP	Dongle	40-pin QFN
	CYPD3105-42FNXIT	Cable	Thunderbolt Active Cable	42-pin CSP
CCG4	CYPD4225-40LQXIT	DRP	Dual Type-C Port Notebooks, Docking Stations	40-pin QFN
	CYPD4125-40LQXIT	DRP	Single Type-C Port Notebooks, Docking Stations	40-pin QFN
	CYPD4126-40LQXIT	DRP	Notebooks, desktops	40-pin QFN
	CYPD4226-40LQXIT	DRP	Notebooks, desktops	40-pin QFN
	CYPD4236-40LQXIT	DRP	Docking station	40-pin QFN
	CYPD4126-24LQXIT	DRP	Notebooks, desktops	24-pin QFN
	CYPD4136-24LQXIT	DRP	Docking station	24-pin QFN
CCG5	CYPD5125-40LQXIT[1]	DRP	Notebooks	40-pin QFN
	CYPD5225-96BZXIT	DRP	Notebooks, Docking Station	96-ball BGA
CCG5C	CYPD5126-40LQXIT	DRP	Notebooks, Desktops	40-pin QFN
	CYPD5137-40LQXIT	DRP	Docking Stations	40-pin QFN
CCG6	CYPD6125-40LQXIT	DRP	Notebooks and Desktops	40-pin QFN
	CYPD6137-40LQXIT	DRP	Docking Station	40-pin QFN
CCG6F	CYPD6126-96BZXI	DRP	Notebooks and Desktops	96-ball BGA
	CYPD6126-96BZXIT	DRP	Notebooks and Desktops	96-ball BGA
CCG6SF	CYPD6127-48LQXI	DRP	Notebooks and Desktops	48-pin QFN
CCG6DF	CYPD6227-96BZXI	DRP	Notebooks and Desktops	96-ball BGA

[1] Not recommended for new designs (NRND). See the CCG5C datasheet for pin-to-pin compatible replacement part.

3.1 Type-C PD Controller Power Subsystem

Table 7 provides the power domain details of Type-C and PD controllers and the recommended values of bypass capacitors to be used on the respective power supply pins.

Table 7. Type-C and PD Controller Power Subsystem

Type-C and PD Controller	Power Supply Pin	Power Supply Domain	Role	Valid Input Voltage Level	Value of Bypass Capacitor to GND
CCG2	VDDD	Supply to the core	DRP	3.0 V to 5.5 V	1 µF
			DFP	3.0 V to 5.5 V	
			UFP	2.7 V to 5.5 V	
	VDDIO	Supply to I/Os	DRP	1.71 V to VDDD	1 µF
			DFP		
			UFP		
	VCCD	The core voltage of the device is brought out to the pin. This pin cannot be used as a voltage source and is intended to connect only a decoupling capacitor. NA (This is an output pin.)			1 µF
	VCONN1 and VCONN2	Supply to power VCONN FETs	DRP	4.0 V to 5.5 V	NA
			DFP		NA
			UFP		NA
			Cable	4.0 V to 5.5 V	1 µF
CCG3	VBUS	Supply to the core **Note:** Either VBUS or VSYS can be provided.	DRP	4.0 V to 21.5 V	1 µF
			DFP		
			UFP		
	VSYS	Supply to the core **Note:** Either VBUS or VSYS can be provided.	DRP	2.7 V to 5.5 V	1 µF
			DFP		
			UFP		
	VDDD	Supply to the analog blocks in chip	DRP	VDDD is an output pin, which is intelligently switched between output of the VBUS regulator and unregulated VSYS.	1 µF
			DFP		
			UFP		
	VDDIO	Supply to the I/Os	DRP	1.71 V to VDDD Note that, VDDIO pin can be shorted to VDDD pin.	1 µF
			DFP		
			UFP		
	VCCD	The core voltage of the device is brought out to the pin. This pin cannot be used as a voltage source and is intended to connect only a decoupling capacitor.			1 µF
	V5V	Supply to power VCONN FETs	DRP	2.7 V to 5.5 V	1 µF
			DFP		
			UFP		
CCG4	VDDD	Supply to the core	DRP	3.0 V to 5.5 V	1 µF
			DFP	3.0 V to 5.5 V	
			UFP	2.7 V to 5.5 V	
	VDDIO	Supply to I/Os	DRP	1.71 V to VDDD	1 µF
			DFP		
			UFP		

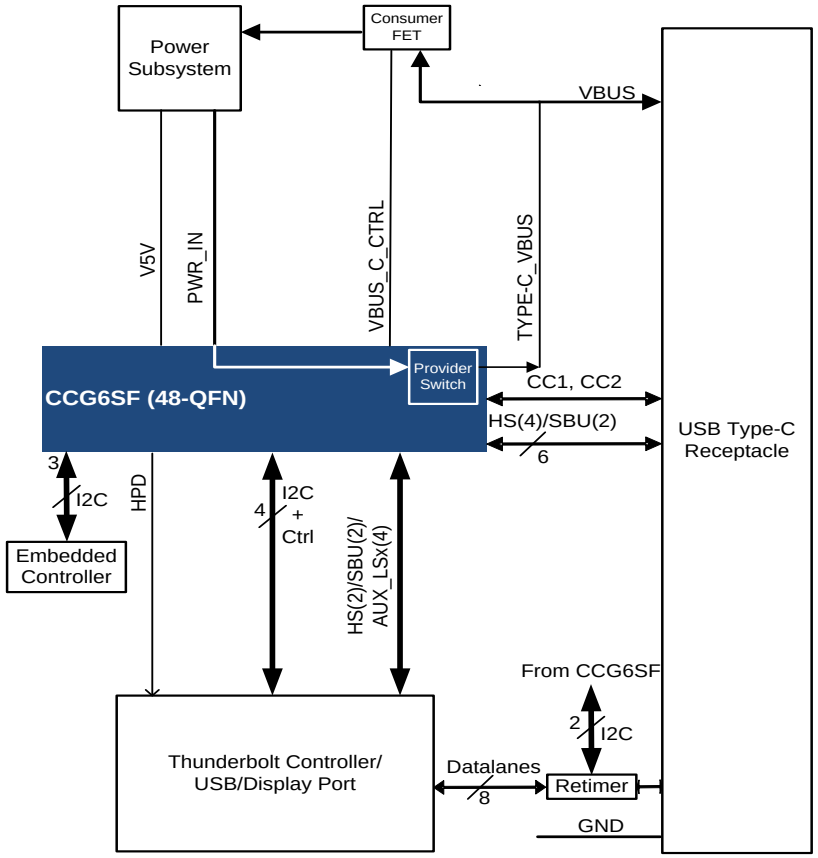
Type-C and PD Controller	Power Supply Pin	Power Supply Domain	Role	Valid Input Voltage Level	Value of Bypass Capacitor to GND
	VCCD	The core voltage of the device is brought out to the pin. This pin cannot be used as a voltage source and is intended to connect only a decoupling capacitor.			0.1 µF
	V5V_P1 and V5V_P2	Supply to power VCONN FETs	DRP	4.85 V to 5.5 V	0.1 µF
			DFP		
			UFP		
CCG5	VBUS	Supply to the core **Note:** Either VBUS or VSYS can be provided	DRP	4.0 V to 21.5 V	1 µF
			DFP		
			UFP		
	VSYS	Supply to the core **Note:** Either VBUS or VSYS can be provided.	DRP	3 V to 5.5 V	1 µF
			DFP		
			UFP		
	VDDD	Supply Input	DRP	3.0 V to 5.5 V	1 µF
			DFP	3.0 V to 5.5 V	
			UFP	2.7 V to 5.5 V	
	VDDIO	Supply to I/Os	DRP	1.71 V to VDDD	0.1 µF
			DFP		
			UFP		
	VCCD	The core voltage of the device is brought out to the pin. This pin cannot be used as a voltage source and is intended to connect only a decoupling capacitor.			0.1 µF
	V5V_P1 and V5V_P2	Supply to power VCONN FETs	DRP	4.85 V to 5.5 V	1 µF
			DFP		
			UFP		
CCG5C / CCG6 / CCG6F	VBUS	Supply to the core **Note:** Either VBUS or VSYS can be provided	DRP	4.0 V to 21.5 V	1 µF
			DFP		
			UFP		
	VSYS	Supply to the core **Note:** Either VBUS or VSYS can be provided.	DRP	3V to 5.5 V	1 µF
			DFP	3V to 5.5V	
			UFP	2.75 V to 5.5V	
	VDDD	Supply Input	DRP	3.0 V to 5.5 V	1 µF
			DFP	3.0 V to 5.5 V	
			UFP	2.7 V to 5.5 V	
	VDDIO	Supply to I/Os	DRP	1.8 V to VDDD	0.1 µF
			DFP		
			UFP		
	VCCD	The core voltage of the device is brought out to the pin. This pin cannot be used as a voltage source and is intended to connect only a decoupling capacitor.			0.1 µF
	V5V	Supply to power VCONN FETs	DRP	4.85 V to 5.5 V	1 µF
CCG6SF/ CCG6DF	VBUS	Supply to the core **Note:** Either VBUS or VSYS can be provided	DRP	4.0 V to 21.5 V	1 µF
			DFP	4.9 V to 5.5V	
			UFP	4.0 V to 21.5 V	
	VSYS	Supply to the core	DRP	3V to 5.5 V	1 µF
			DFP	3V to 5.5 V	

Type-C and PD Controller	Power Supply Pin	Power Supply Domain	Role	Valid Input Voltage Level	Value of Bypass Capacitor to GND
		Note: Either VBUS or VSYS can be provided	UFP	2.75 V to 5.5 V	
	VDDD	Supply input	DRP	3.0 V to 5.5 V	1 µF
			DFP	3.0 V to 5.5 V	
			UFP	2.7 V to 5.5 V	
	VDDIO	Supply to I/Os	DRP	1.8 V to VDDD	0.1 µF
			DFP		
			UFP		
	VCCD	The core voltage of the device is brought out to the pin. This pin cannot be used as a voltage source and is intended to connect only a decoupling capacitor.			0.1 µF
	V5V for CCG6SF V5V_P0 and V5V_P1 for CCG6DF	Supply to power VCONN FETs	DRP	4.85 V to 5.5 V	1 µF

4 Single Type-C Port DRP Application using CCG6SF controller

A CYPD6127-48LQXI CCG6SF controller is used as the reference.

Figure 4. Single Type-C Port Notebook Design Using CCG6SF



The following are the critical sections of the single Type-C notebook design using CCG6SF:

- Power Supply Design
- I²C Communication with Embedded Controller
- Dead Battery Charging
- Power Provider or Consumer (DRP) Role
- DisplayPort Connections
- Electrical Design Considerations

4.1 Power Supply Design

Cypress' CCG6SF Type-C PD Controller operates with two possible external supply voltages, VBUS or VSYS. The VDDIO supply powers the device I/Os as referred in Table 10. VDDD generates 3.3 V from an internal regulator; this can be shorted to VDDIO. VCCD is the output voltage from the core regulator and this pin is intended to connect only a decoupling capacitor. The VCCD pin cannot be used as a voltage source. CCG6SF has power supply inputs at the V5V pin for providing power to EMCA cables through integrated VCONN FETs. There are two VCONN FETs in CCG6SF to power CC1 and CC2 pins.

Figure 5. CCG6SF Power Supply Design

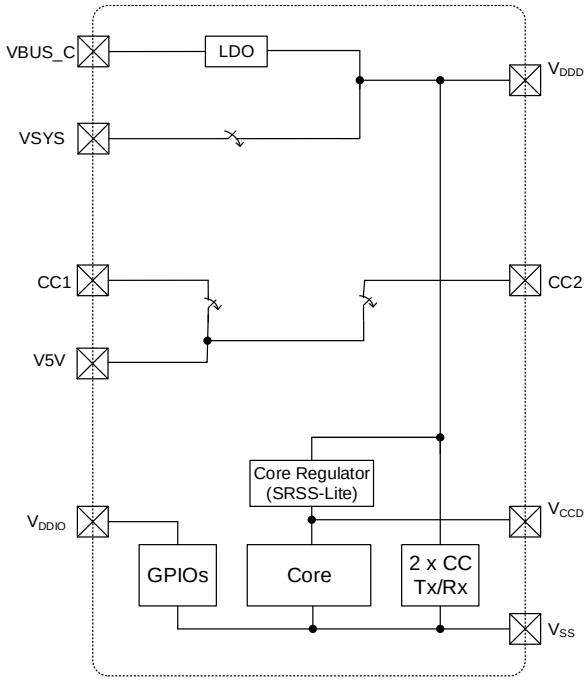


Table 8. CCG6SF Operating Voltage

Parameter	Min (V)	Typ (V)	Max (V)
VBUS	4.0	–	21.5
VSYS	2.75	–	5.5
VDDD	VSYS-0.05	–	VSYS
VDDIO	VDDD	–	VDDD
V5V	4.85	–	5.5

4.1.1 Reset and Clock

CCG6SF supports a power-on-reset (POR) mechanism; it also has an active LOW external reset (XRES) pin. The XRES pin can be used by external devices to reset the CCG6SF device. The XRES pin should be held LOW for a minimum of 5 µs to reset the CCG6SF device. This XRES pin should be tied through an RC circuit.

CCG6SF has integrated clock circuitry; external components such as a crystal or oscillator are not required.

4.1.2 Noise Suppression of Supply Voltages

Refer section Power supply Noise Suppression.

4.2 I²C Communication with Embedded Controller

See I2C Communication with Embedded Controller.

4.3 Dead Battery Charging

See Dead Battery Charging.

4.4 Power Provider/Consumer Role

This section explains the VBUS control, overvoltage, overcurrent, reverse current, and short circuit protection in a notebook design. A notebook design using a CCG6SF device is a power provider when running from its internal battery and a power consumer when being charged from the connected power sources such as power adapters, monitors, and self-powered hard discs.

4.4.1 Control of VBUS Provider Path and VBUS Consumer Path

A Battery Charger Controller (BCC) controls the charging (sinking of VBUS) or discharging (sourcing of VBUS) of the battery. CCG6SF device has an integrated 5 V/3 A provider load switch with load switch controller.

CCG6SF has integrated slew-rate control NFET gate drivers to drive external NFETs (20 V/3 A) on the VBUS consumer path. The consumer side only supports external NFET, and CCG6SF must be in active mode to enable the consumer-side NGDO.

See Provider Load Switch and Gate Driver for VBUS NFET (Functional overview) in CCG6DF/CCG6SF datasheet for more details.

4.4.2 Fault Protection Modes

CCG6SF has an integrated load switch with load switch controller in the VBUS provider path, which can protect the VBUS provider path from reverse current and short circuit faults caused due to external events. Load switch controller supports various protection modes such as VBUS Over Voltage Protection, VBUS Under Voltage Protection, VBUS Short Circuit Protection, VBUS Reverse Current Protection, and VBUS Over Current Protection. External Rsense resistor, 5 mΩ, in the VBUS provider path along with the integrated load switch controller measures the magnitude of current to sense over current, reverse current, and short circuit conditions.

Provider path will turn OFF when any fault is detected, and the protection modes can be enabled or disabled through firmware. The threshold for triggering or detecting the faults are configurable through firmware.

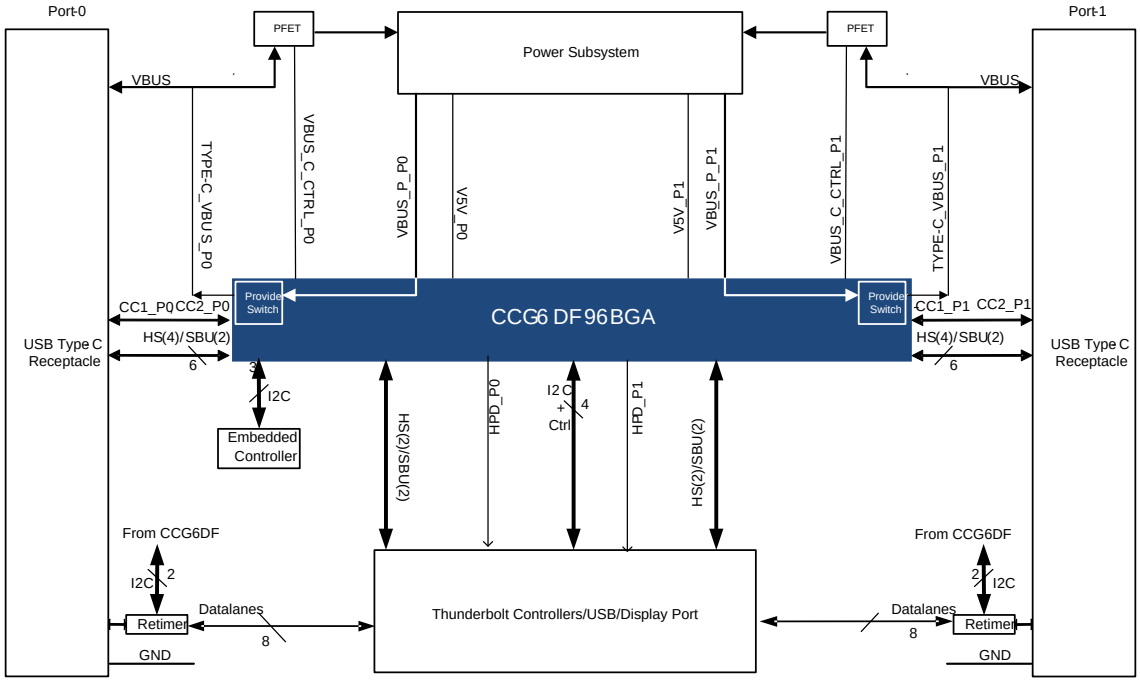
4.4.3 Control of VBUS Discharge Path

CCG6SF devices support high-voltage (21.5 V) VBUS discharge circuitry inside. After cable removal detection, the chips discharge the residual charge and bring the floating VBUS to less than 0.8 V.

5 Dual Type-C Port DRP Application Using CCG6DF

A CYPD6227-96BZXI CCG6DF controller is used as the reference.

Figure 6. Single Type-C Port Notebook Design Using CCG6DF



See the CCG6DF/CCG6SF datasheet for details.

The following are the critical sections of the single Type-C notebook design using CCG6SF:

- Power Supply Design
- I²C Communication with Embedded Controller
- Dead Battery Charging
- Power Provider or Consumer (DRP) Role
- DisplayPort Connections
- Electrical Design Considerations

5.1 Power Supply Design

Cypress' CCG6DF Type-C PD Controller operates with two possible external supply voltages, VBUS or VSYS. The VDDIO supply powers the device I/Os as referred in Table 10. VDDD generates 3.3 V from an internal regulator; this can be shorted to VDDIO. VCCD is the output voltage from the core regulator and this pin is intended to connect only a decoupling capacitor. The VCCD pin cannot be used as a voltage source. CCG6DF has power supply inputs at the V5V pin for providing power to EMCA cables through integrated VCONN FETs. There are two VCONN FETs in CCG6DF to power CC1 and CC2 pins.

Figure 7. CCG6DF Power Supply Design

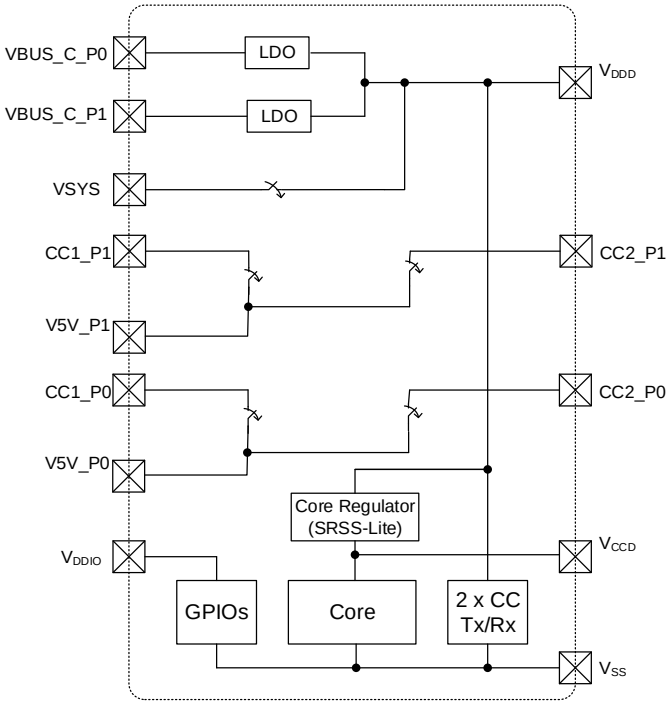


Table 9. CCG6DF Operating Voltage

Parameter	Min (V)	Typ (V)	Max (V)
VBUS	4.0	–	21.5
VSYS	2.75	–	5.5
VDDD	VSYS-0.05	–	VSYS
VDDIO	VDDD	–	VDDD
V5V	4.85	–	5.5

5.1.1 Reset and Clock

CCG6DF supports a power-on-reset (POR) mechanism; it also has an active LOW external reset (XRES) pin. The XRES pin can be used by external devices to reset the CCG6DF device. The XRES pin should be held LOW for a minimum of 5 µs to reset the CCG6DF device. This XRES pin should be tied through an RC circuit.

CCG6DF has integrated clock circuitry; external components such as a crystal or oscillator are not required.

5.1.2 Noise Suppression of Supply Voltages

See Power supply Noise Suppression.

5.2 I²C Communication with Embedded Controller

See I2C Communication with Embedded Controller.

5.3 Dead Battery Charging

See Dead Battery Charging.

5.4 Power Provider/Consumer Role

This section explains the VBUS control, overvoltage, overcurrent, reverse current, and short circuit protection in a notebook design. A notebook design using a CCG6DF device is a power provider when running from its internal battery and a power consumer when being charged from the connected power sources such as power adapters, monitors, and self-powered hard discs.

5.4.1 Control of VBUS Provider Path and VBUS Consumer Path

A Battery Charger Controller (BCC) controls the charging (sinking of VBUS) or discharging (sourcing of VBUS) of the battery. CCG6DF device has two integrated 5 V/3 A provider load switches with load switch controller, one per port.

See CCG6SF/CCG6DF Datasheet for details

5.4.2 Fault Protection Modes

CCG6DF has an integrated load switch per port with load switch controller in the VBUS Provider Path, which can protect the VBUS provider path from reverse current and short circuit faults caused due to external events.

See Fault Protection Modes for details.

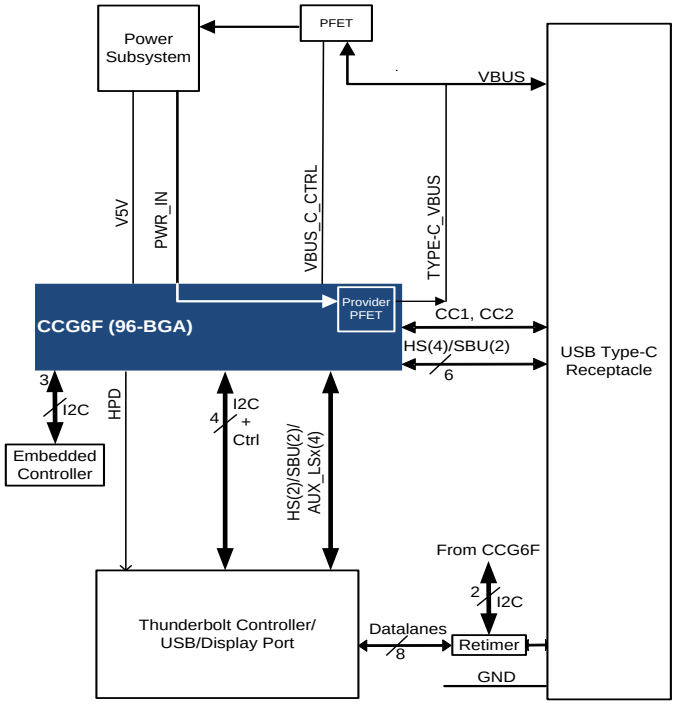
5.4.3 Control of VBUS Discharge Path

CCG6DF devices support high-voltage (21.5 V) VBUS discharge circuitry inside. After cable removal detection, the chips discharge the residual charge and bring the floating VBUS to less than 0.8 V.

6 Single Type-C Port DRP Application using CCG6 and CCG6F

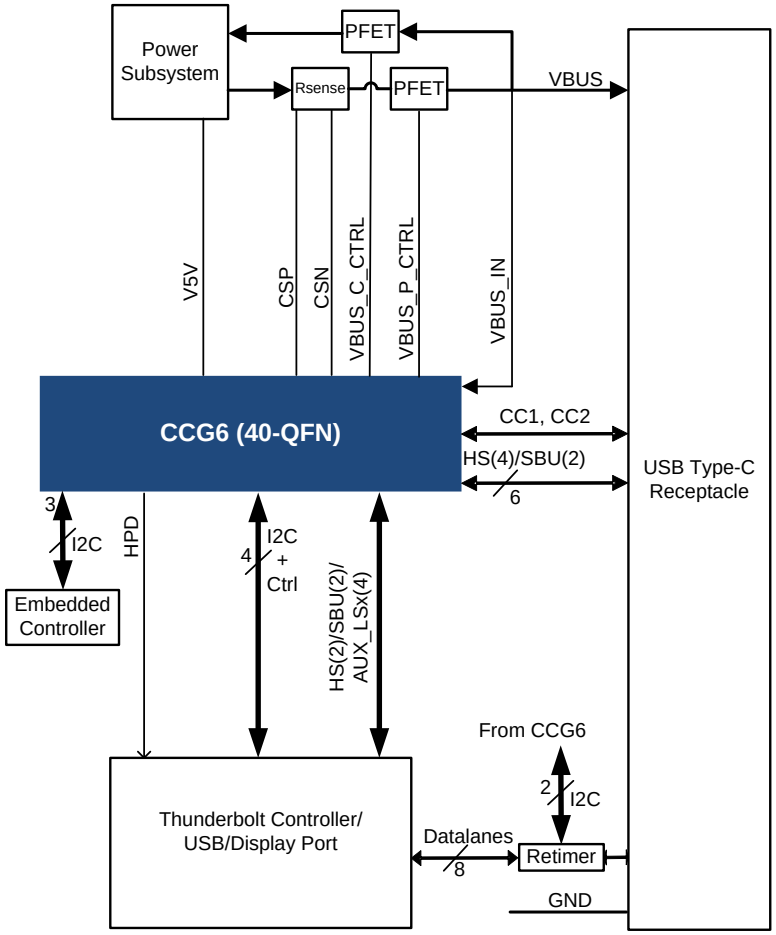
A CYPD6126-96BZXI CCG6F controller is used as the reference.

Figure 8. Single Type-C Port Notebook Design Using CCG6F



A CYPD6125-40LQXIT CCG6 controller is used as the reference.

Figure 9. Single Type-C Port Notebook Design Using CCG6



The following are the critical sections of the single Type-C notebook design using CCG6:

- Power Supply Design
- I²C Communication with Embedded Controller
- Dead Battery Charging
- Power Provider or Consumer (DRP) Role
- DisplayPort Connections
- Electrical Design Considerations

6.1 Power Supply Design

Cypress' CCG6/CCG6F Type-C PD Controller operates with two possible external supply voltages, VBUS or VSYS. The VDDIO supply powers the device I/Os as referred in Table 10. VDDD generates 3.3 V from an internal regulator; this can be shorted to VDDIO. VCCD is the output voltage from the core regulator and this pin is intended to connect only a decoupling capacitor. The VCCD pin cannot be used as a voltage source. CCG6/CCG6F has power supply inputs at the V5V pin for providing power to EMCA cables through integrated VCONN FETs. There are two VCONN FETs in CCG6/CCG6F to power CC1 and CC2 pins.

Figure 10. CCG6/CCG6F Power Supply Design

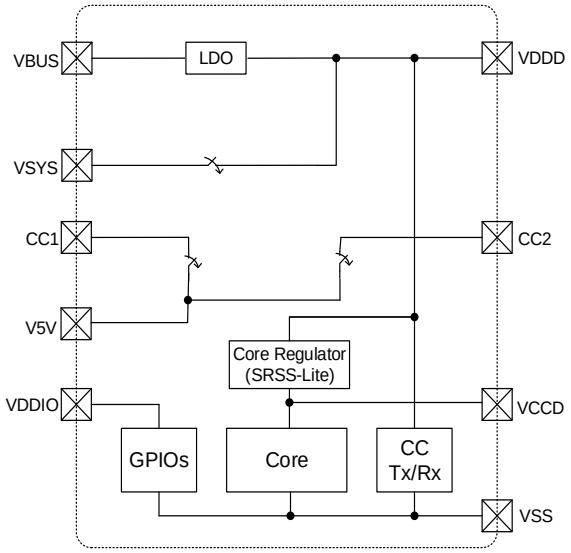


Table 10. CCG6/CCG6F Operating Voltage

Parameter	Min (V)	Typ (V)	Max (V)
VBUS	4.0	–	21.5
VSYS	2.75	–	5.5
VDDD	VSYS-0.05	–	VSYS
VDDIO	VDDD	–	VDDD
V5V	4.85	–	5.5

6.1.1 Reset and Clock

CCG6/CCG6F supports a power-on-reset (POR) mechanism; it also has an active LOW external reset (XRES) pin. The XRES pin can be used by external devices to reset the CCG6/CCG6F device. The XRES pin should be held LOW for a minimum of 5 µs to reset the CCG6/CCG6F device. This XRES pin should be tied through an RC circuit.

CCG6/CCG6F has integrated clock circuitry; external components such as a crystal or oscillator are not required.

6.1.2 Noise Suppression of Supply Voltages

See Power supply Noise Suppression.

6.2 I²C Communication with Embedded Controller

See I2C Communication with Embedded Controller.

6.3 Dead Battery Charging

See Dead Battery Charging.

6.4 Power Provider/Consumer Role

This section explains the recommended external hardware circuitry for VBUS control, overvoltage, overcurrent, reverse current, and short circuit protection in a notebook design. A notebook design using a CCG6/CCG6F device is a power provider when running from its internal battery and a power consumer when being charged from the connected power sources such as power adapters, monitors, and self-powered hard discs.

6.4.1 Control of VBUS Provider Path and VBUS Consumer Path

A Battery Charger Controller (BCC) controls the charging (sinking of VBUS) or discharging (sourcing of VBUS) of the battery. The CCG6 device consists of two I/Os with integrated PFET Gate drivers, namely, VBUS_P_CTRL and VBUS_C_CTRL, to control the VBUS provider (sourcing of power) or consumer (sinking of power) path connected to the BCC.

Figure 11 shows the recommended implementation to control this VBUS path.

Figure 11. CCG6 VBUS Provider and Consumer Path Control

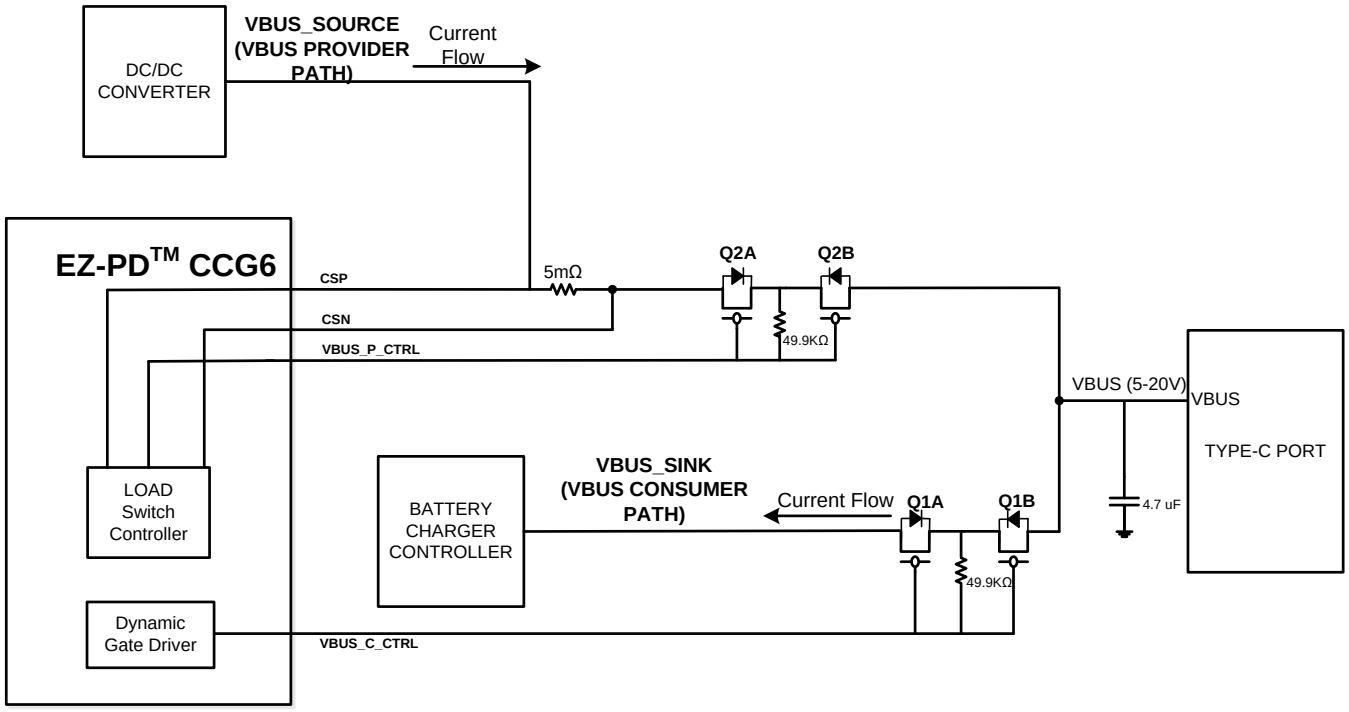
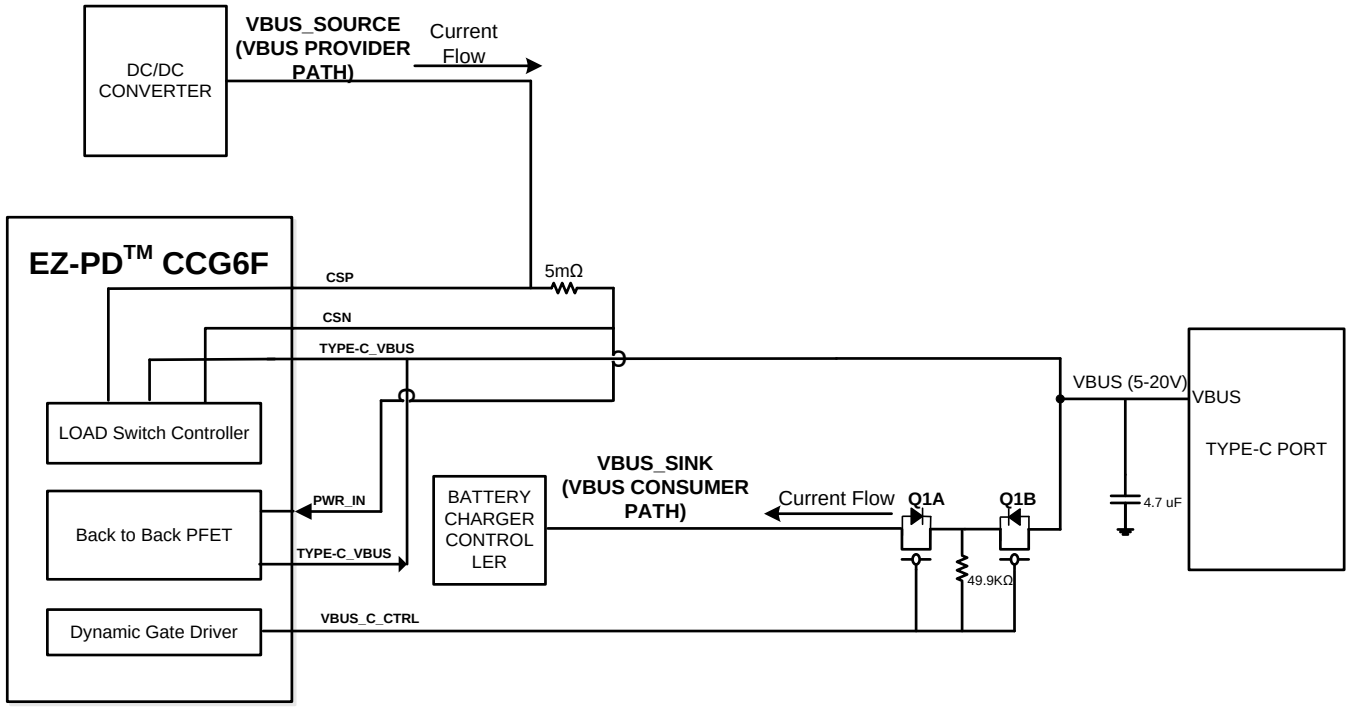


Figure 12. CCG6F VBUS Provider and Consumer Path Control

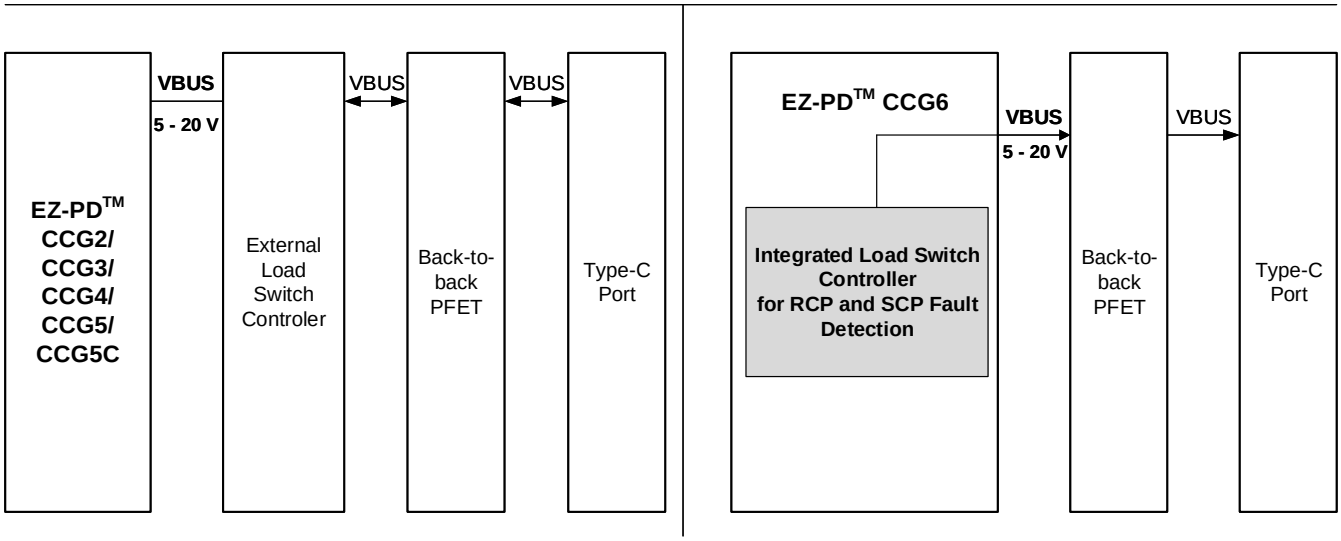


6.4.2 Reverse Current Protection and Short Circuit Protection

CCG6 has a built-in load switch controller in the VBUS Provider Path which can protect the VBUS Provider Path from Reverse Current and Short Circuit faults caused due to external events.

As shown in Figure 13, when CCG6 is used in DRP applications, no external load switch controller is required to protect the system from reverse current and short circuit faults. This can reduce the system BOM cost.

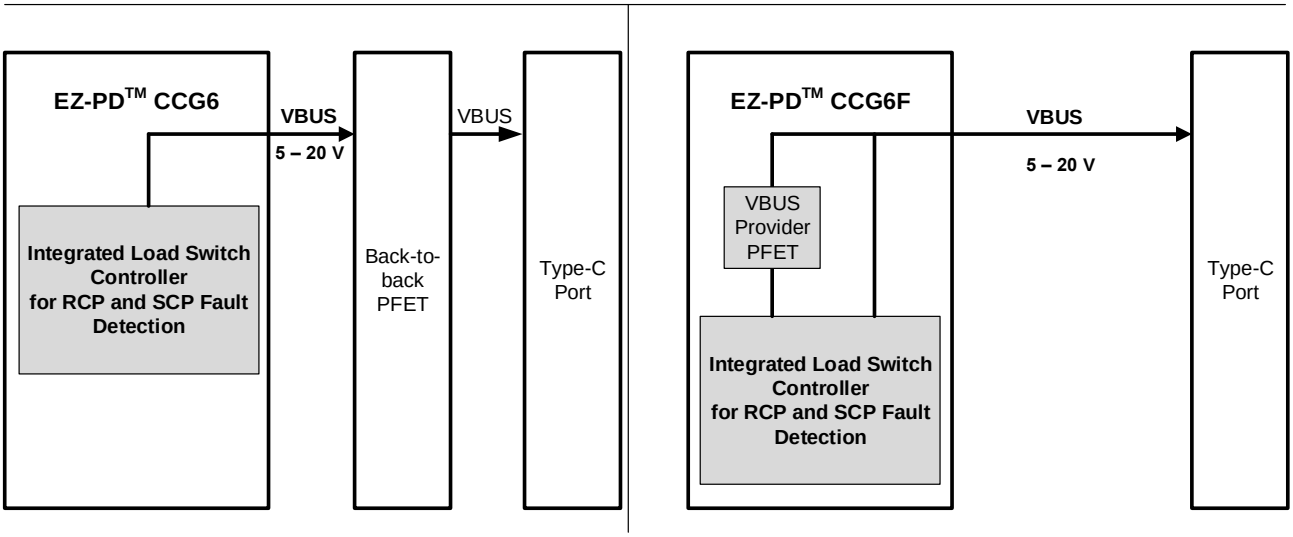
Figure 13. Load Switch Controller Advantage with CCG6 Compared with Previous Generation CCGx Products



CCG6F has a built-in load switch controller in the VBUS Provider Path, which can protect the VBUS Provider Path from Reverse Current and Short Circuit faults caused due to external events. CCG6F also includes a back-to-back PFET in the VBUS Provider Path.

As shown in Figure 14, when CCG6F is used in DRP applications, no external load switch controller is required to protect the system from reverse current and short circuit faults. The back to back PFET is integrated onto CCG6F. This can reduce the system BOM cost.

Figure 14. Differences between CCG6 and CCG6F with respect to Load Switch Controller

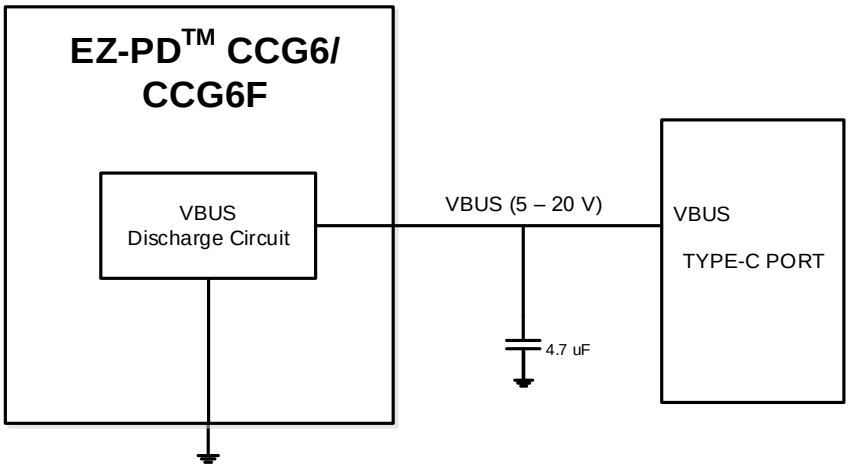


6.4.3 Control of VBUS Discharge Path

This section explains the critical need of the VBUS discharge circuitry. Depending on the connected downstream device, the VBUS voltage varies as illustrated by the following example scenarios:

- Example Scenario 1: A UFP device sinking 100 W of power (20 V, 5 A) is disconnected from a Type-C port, and immediately another UFP device sinking 25 W of power (5 V, 5 A) is connected to the same Type-C port.
- Example Scenario 2: A notebook changes its power role from the provider (sourcing 100 W of power) to consumer (sinking 45 W of power).

Figure 15. VBUS Discharge Control Circuitry



In Scenario 1, the VBUS capacitor shown in Figure 15 may not have discharged fully from the original 20 V when the second UFP device is connected. This could cause an overvoltage on the second UFP device, which requires 5 V on VBUS.

In Scenario 2, a similar overvoltage could occur when the power role is swapped. To prevent this scenario, the CCG6/CCG6F device provides a built-in VBUS discharge circuit that provides a discharge path for the VBUS capacitor. This avoids overvoltage scenarios like example scenarios 1 and 2.

For additional information on VBUS Discharge, see the USB Power Delivery section in CCG6 Technical Reference Manual

6.4.4 Overvoltage Protection (OVP) for VBUS

An OVP circuit is required on VBUS to prevent damage to the system if VBUS exceeds the maximum voltage negotiated by the CCG6/CCG6F controller. CCG6/CCG6F has a built-in OVP circuit; therefore, no external circuit is required.

Figure 16. OVP Circuit

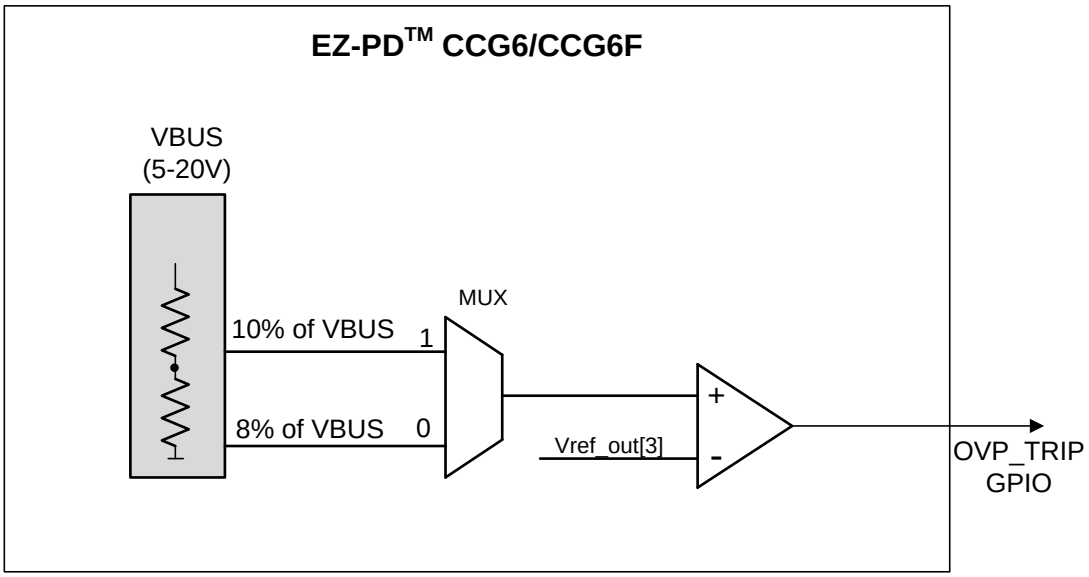


Table 11 provides the value of OVP trip voltage (1.2 times V_{BUS}) for possible VBUS voltages.

Table 11. Values of OVP Trip Voltage at Different VBUS Voltages

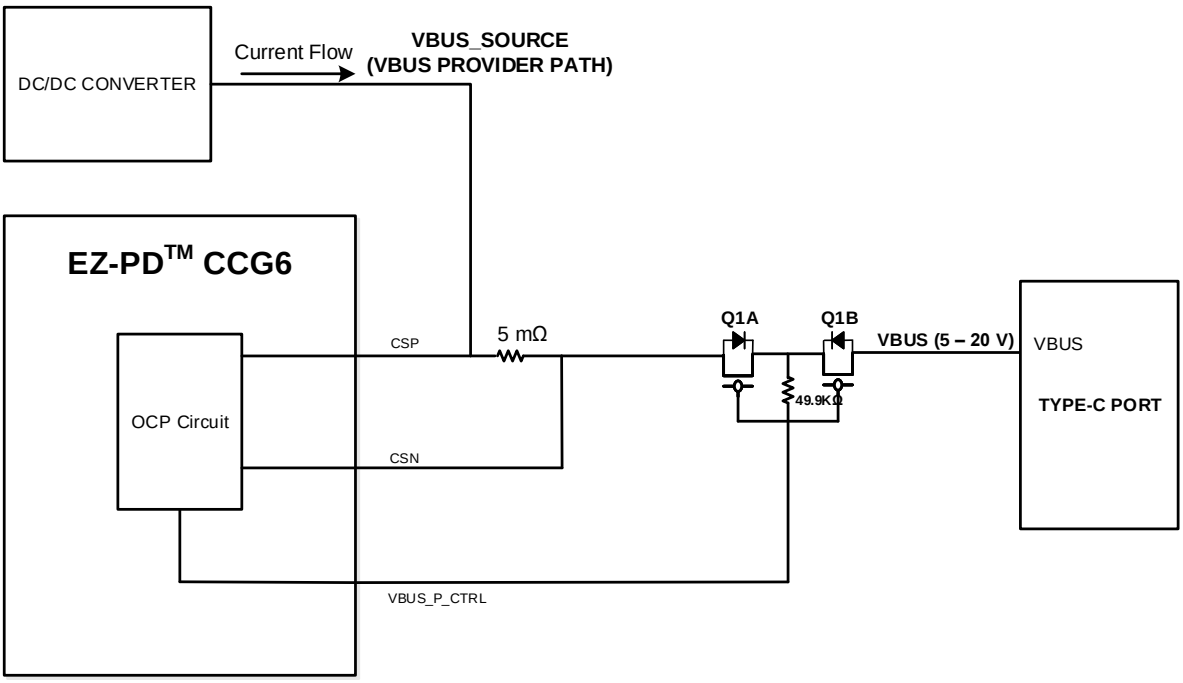
VBUS Voltage (V)	OVP Trip Voltage (V)
5	6
9	10.8
15	18
20	24

A CCG6/CCG6F device has a built-in OVP circuit. The inputs to the comparator are a reference voltage (vref_out) from REFGEN module and either 8% or 10% of the VBUS. Based on the chosen VBUS voltage input to the MUX the reference value (vref_out[3]) shall be programmed. For example when an user chooses 8% of VBUS as input to the comparator, then vref_out[3] in the reference generator shall be programmed to 0.48 V ((8 * 6) / 100) to detect OVP at 6V when VBUS voltage is at 5 V. The reference input to the comparator is programmable through Firmware, hence the OVP trip voltage is also programmable through Firmware. Any overvoltage event will be detected by the OVP circuit and notified via the OVP_TRIP pin.

6.4.5 Overcurrent Protection (OCP) for VBUS

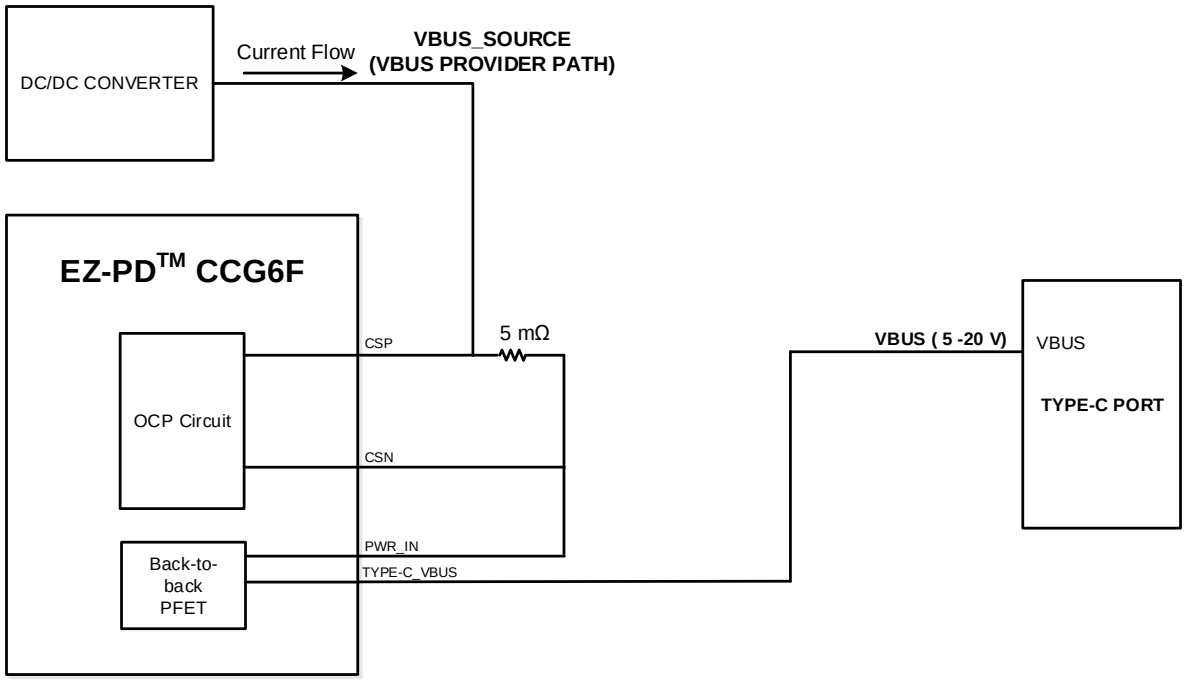
An OCP circuit is required on VBUS to prevent damage to the system if the VBUS current exceeds the maximum current negotiated by the CCG6 controller. As shown in Figure 17 CCG6 has a built-in OCP circuitry; therefore, no external circuitry is required for OCP implementation.

Figure 17. OCP Circuitry



CCG6 has a built-in current sense monitor circuitry and built-in comparator that detect any overcurrent event on VBUS. The VBUS_P_CTRL signal will be triggered in the overcurrent scenario and the CCG6 device turns OFF VBUS by turning OFF the power provider FETs Q1A and Q1B as shown in Figure 17. CCG6 also disconnects itself from the Type-C port to shut off the VBUS. The value at which OC can trigger is programmable using Firmware.

Figure 18. OCP Circuitry for CCG6F



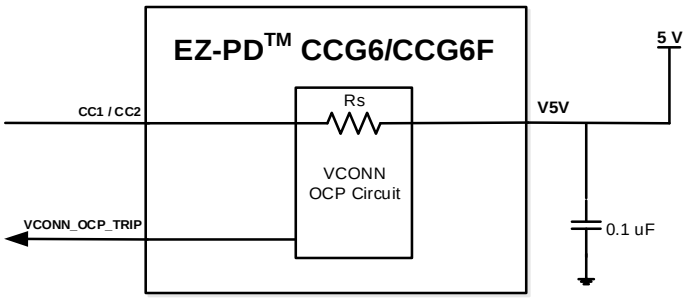
CCG6F has a built-in current sense monitor circuitry and built-in comparator that detect any overcurrent event on VBUS. In the overcurrent scenario, the CCG6F device turns OFF VBUS by turning OFF the back-to-back power provider FETs. CCG6F also disconnects itself from the Type-C port to shut off the VBUS. The value at which OC can trigger is programmable using Firmware.

For additional information on OCP for VBUS, see the USB Power Delivery section in CCG6 Technical Reference Manual

6.4.6 Overcurrent Protection (OCP) for VCONN

In a notebook design, VCONN supplies power to the EMCA attached to it. An OCP circuit is required on VCONN to prevent damage to the system when the VCONN current exceeds 550mA. As shown in Figure 19, CCG6/CCG6F has a built-in VCONN OCP circuit; therefore, no external circuitry is required to implement OCP for VCONN in a notebook design using CCG6/CCG6F.

Figure 19. OCP for VCONN

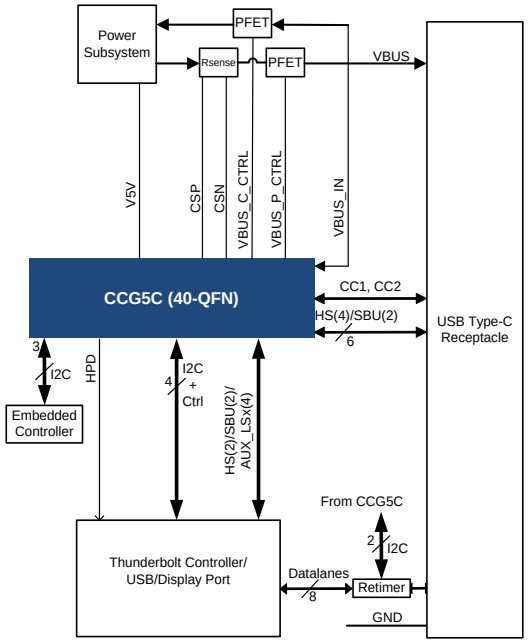


For additional information on OCP for VCONN, see the USB Power Delivery section in CCG6 Technical Reference Manual

7 Single Type-C Port DRP Application Using CCG5C

A CYPD5126-40LQXIT CCG5C controller is used as the reference.

Figure 20. Single Type-C Port Notebook Design Using CCG5C



The following are the critical sections of the single Type-C notebook design using CCG5C:

- Power Supply Design
- I²C Communication with Embedded Controller
- Dead Battery Charging
- Power Provider or Consumer (DRP) Role.
- DisplayPort Connections
- Electrical Design Considerations

7.1 Power Supply Design

Cypress' CCG5C Type-C PD Controller operates with two possible external supply voltages, VBUS or VSYS as referred in Table 12. The VDDIO supply powers the device I/Os as referred in Table 12. VDDD generates 3.3 V from an internal regulator; this can be shorted to VDDIO. VCCD is the output voltage from the core regulator and this pin is intended to connect only a decoupling capacitor. The VCCD pin cannot be used as a voltage source. CCG5C has power supply inputs at the V5V pin for providing power to EMCA cables through integrated VCONN FETs. There are two VCONN FETs in CCG5C to power CC1 and CC2 pins.

Figure 21. CCG5C Power Supply Design

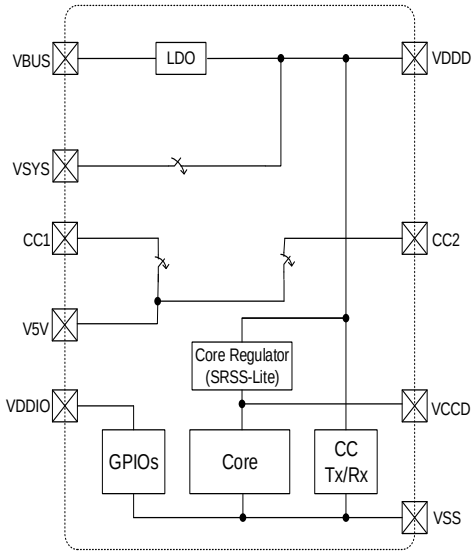


Table 12. CCG5C Operating Voltages

Parameter	Min (V)	Typ (V)	Max (V)
VBUS	4.0	–	21.5
VSYS	2.75	–	5.5
VDDD	VSYS-0.05	–	VSYS
VDDIO	VDDD	–	VDDD
V5V	4.85	–	5.5

7.1.1 Reset and Clock

CCG5C supports a power-on-reset (POR) mechanism and it also has an active LOW external reset (XRES) pin. The XRES pin can be used by external devices to reset the CCG5C device. The XRES pin should be held LOW for a minimum of 5 µs to reset the CCG5C device. This XRES pin should be tied through an RC circuit.

CCG5C has an integrated clock circuitry; external components such as a crystal or oscillator are not required.

7.1.2 Noise Suppression of Supply Voltages

See Power supply Noise Suppression.

7.2 I²C Communication with Embedded Controller

See I2C Communication with Embedded Controller.

7.3 Dead Battery Charging

See Dead Battery Charging.

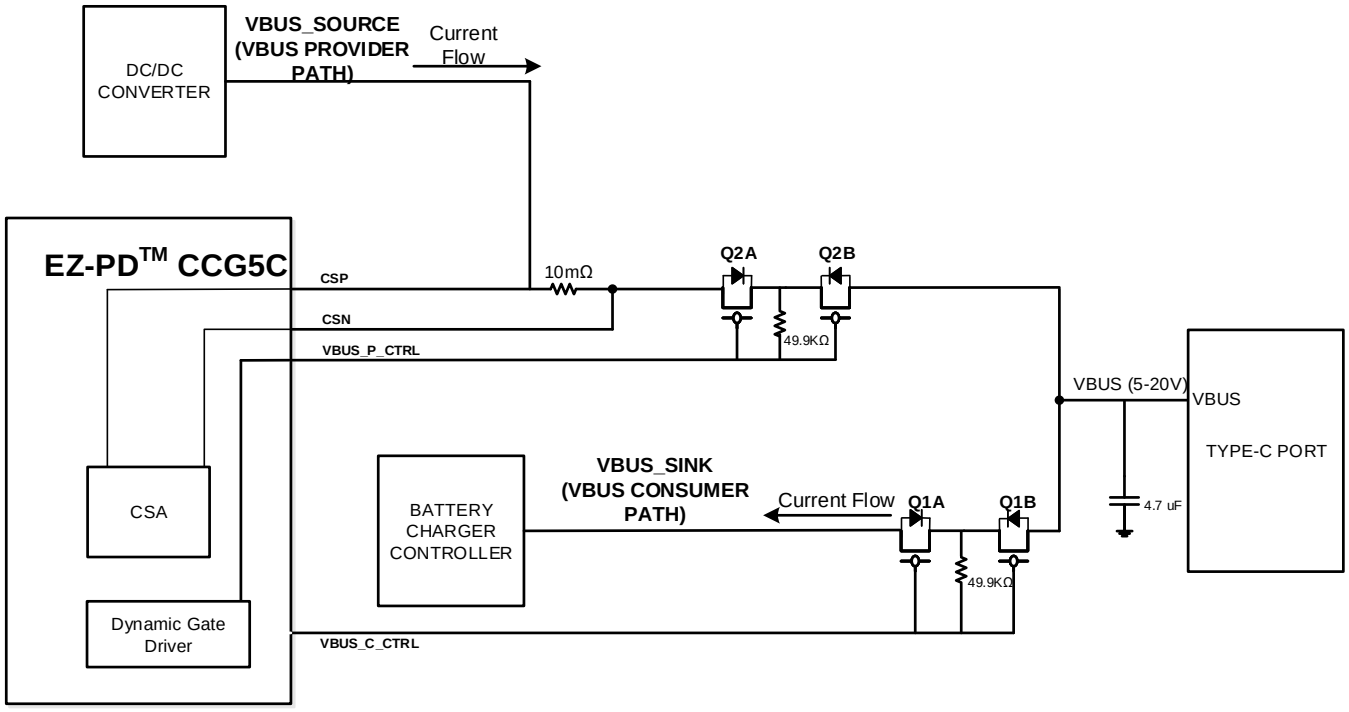
7.4 Power Provider/Consumer Role

This section explains the recommended external hardware circuitry for VBUS control, overvoltage and overcurrent protection in a notebook design. A notebook design using a CCG5C device is a power provider when running from its internal battery and a power consumer when being charged from a DFP (such as a power adapter) or a DRP (such as a monitor or external, self-powered hard disc).

7.4.1 Control of VBUS Provider Path and VBUS Consumer Path

A Battery Charger Controller (BCC) controls the charging (sinking of VBUS) or discharging (sourcing of VBUS) of the battery. The CCG5C device consists of two I/O's, VBUS_P_CTRL and VBUS_C_CTRL, to control the VBUS provider (sourcing of power) or consumer (sinking of power) path connected to the BCC. Figure 22 shows the recommended implementation to control this VBUS path.

Figure 22. CCG5C VBUS Provider and Consumer Path Control

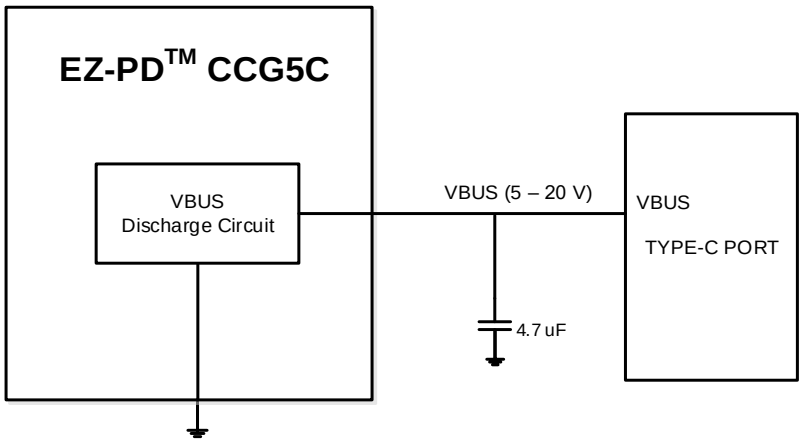


7.4.2 Control of VBUS Discharge Path

This section explains the critical need of the VBUS discharge circuitry. Depending on the connected downstream device, the VBUS voltage varies as illustrated by the following example scenarios:

- Example Scenario 1: A UFP device sinking 100 W of power (20 V, 5 A) is disconnected from a Type-C port, and immediately another UFP device sinking 25 W of power (5 V, 5 A) is connected to the same Type-C port.
- Example Scenario 2: A notebook changes its power role from provider (sourcing 100 W of power) to consumer (sinking 45 W of power).

Figure 23. VBUS Discharge Control Circuitry



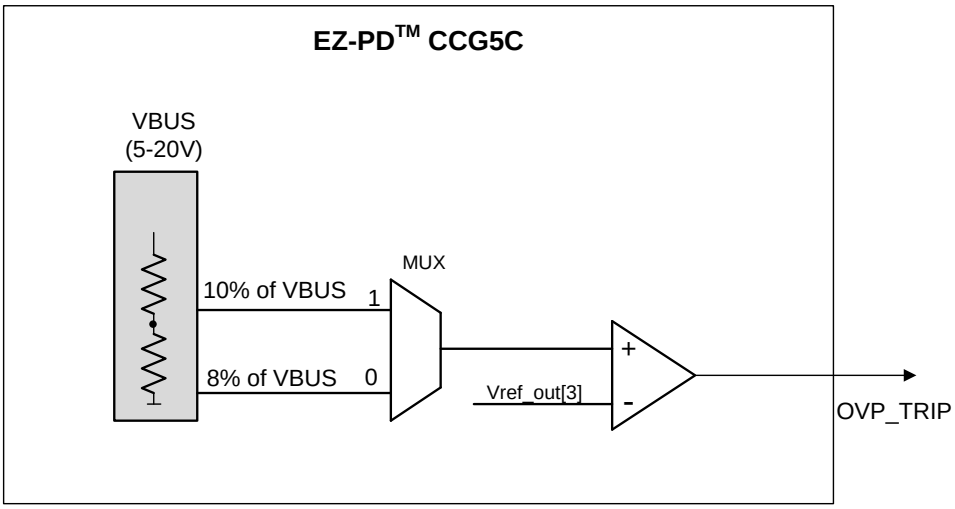
In Scenario 1, the VBUS capacitor shown in Figure 23 may not have discharged fully from the original 20 V when the second UFP device is connected. This could cause an overvoltage on the second UFP device, which requires 5 V on VBUS.

In Scenario 2, a similar overvoltage could occur when the power role is swapped. To prevent this scenario, the CCG5C device provides a built-in VBUS discharge circuit that provides a discharge path for the VBUS capacitor. This avoids overvoltage scenarios like example scenarios 1 and 2.

7.4.3 Overvoltage Protection (OVP) for VBUS

An OVP circuit is required on VBUS to prevent damage to the system if VBUS exceeds the maximum voltage negotiated by the CCG5C controller. CCG5C has a built-in OVP unit and hence no external circuitry is required.

Figure 24. OVP Circuit



According to the USB PD specification, the maximum voltage at VBUS can be 20 V. Table 13 provides the value of the OVP trip voltage (1.2 times V_{BUS}) for possible VBUS voltages.

Table 13. Values of OVP Trip Voltage at Different VBUS Voltages

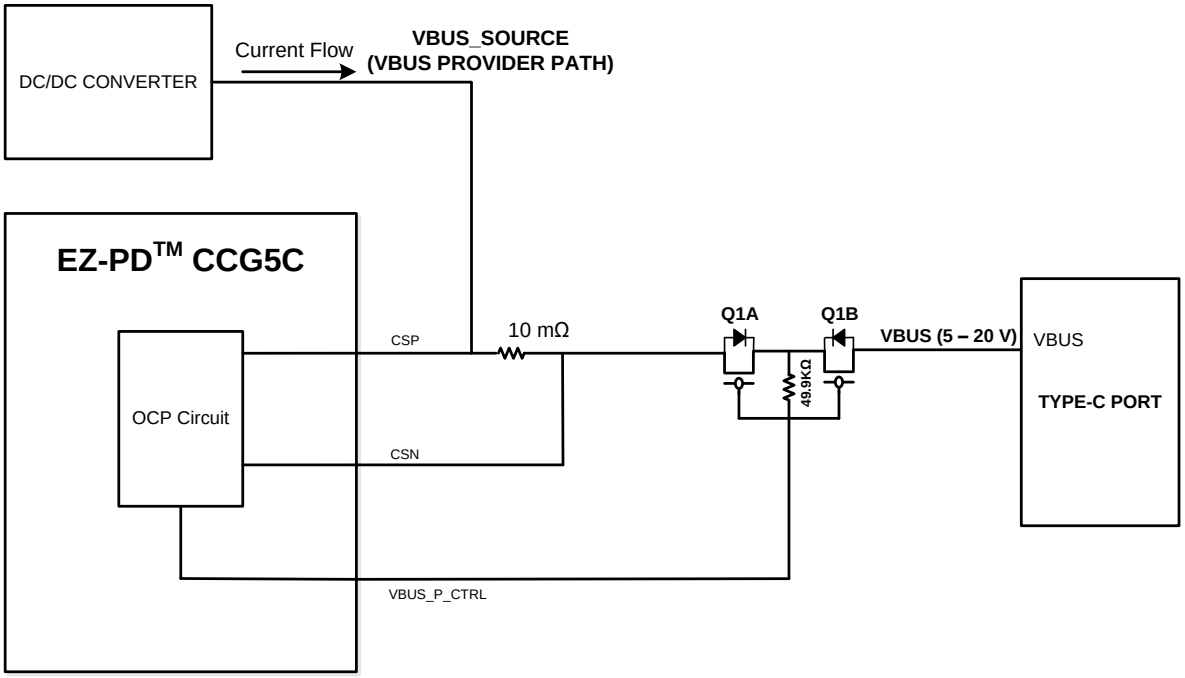
VBUS Voltage (V)	OVP Trip Voltage (V)
5	6
9	10.8
15	18
20	24

The inputs to the comparator are a reference voltage (vref_out) from REFGEN module and either 8% or 10% of the VBUS. Based on the chosen VBUS voltage input to the MUX, the reference value (vref_out[3]) will be programmed. For example, when you choose 8% of VBUS as input to the comparator, then vref_out[3] in the reference generator will be programmed to 0.48 V ((8 * 6) / 100) to detect OVP at 6 V when VBUS voltage is at 5 V. The reference input to the comparator is programmable through Firmware hence the OVP trip voltage is also programmable through Firmware. Any overvoltage event will be detected by the OVP circuit and will be notified via the OVP_TRIP GPIO pin.

7.4.4 Overcurrent Protection (OCP) for VBUS

An OCP circuit is required on VBUS to prevent damage to the system if the VBUS current exceeds the maximum current negotiated by the CCG5C controller. As shown in Figure 25, CCG5C has a built-in OCP circuit; therefore, no external circuitry is required for OCP implementation.

Figure 25. OCP Circuitry

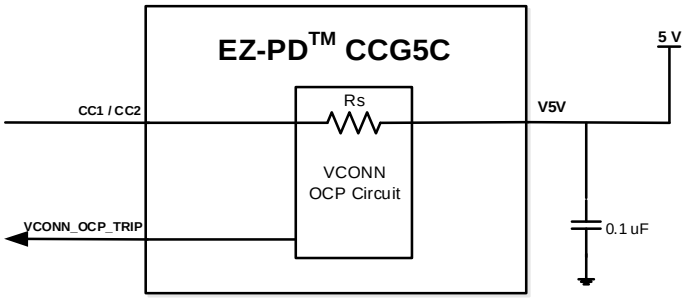


CCG5C has a built-in current sense monitor circuitry and built-in comparator that detect any overcurrent event on VBUS. The VBUS_P_CTRL signal will be triggered in the overcurrent scenario; the CCG5C device turns OFF VBUS by turning OFF the power provider FETs Q1A and Q1B as shown in Figure 25. The CCG5C device also disconnects itself from the Type-C port to shut off VBUS. The value at which OC can trigger is programmable using Firmware.

7.4.5 Overcurrent Protection (OCP) for VCONN

In a notebook design, VCONN supplies power to the electronically marked cable attached to it. An OCP circuit is required on VCONN to prevent damage to the system if the VCONN current exceeds 550 mA. As shown in Figure 26, CCG5C has a built-in VCONN OCP circuit, therefore no external circuitry is required to implement OCP for VCONN in a notebook design using CCG5C.

Figure 26. OCP for VCONN

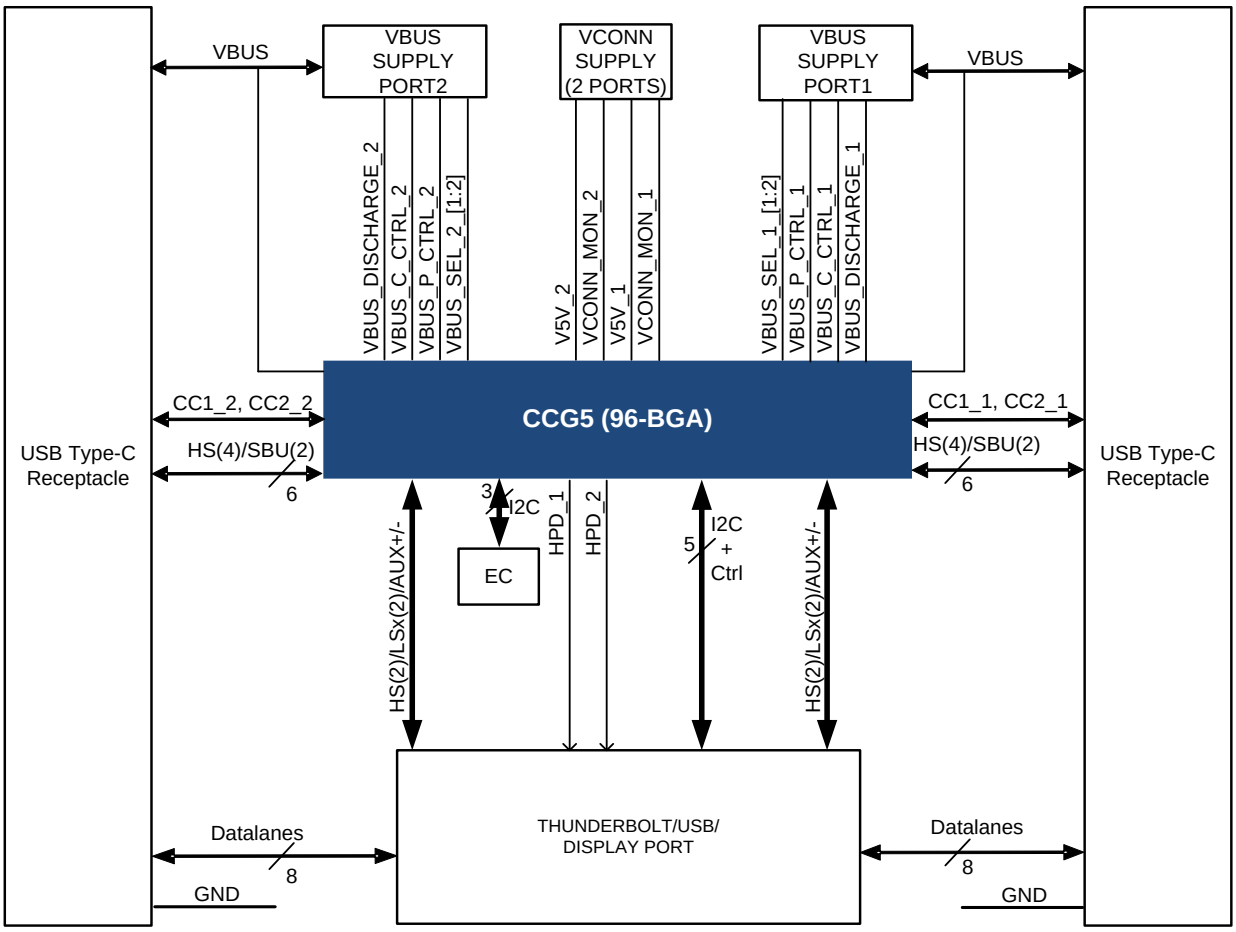


8 Dual Type-C Port DRP Application Using CCG5

A CYPD5225-96BZXIT CCG5 controller is used here as the reference.

CCG5 integrates two Type-C transceivers and facilitates a dual Type-C port notebook design with reduced BOM in comparison with CCG2 and CCG3 family which integrate only one Type-C transceiver. In this application, both Type–C ports can be either power providers or power consumers at the same or different times. Similarly, both Type-C ports can play the role of DFP or DRP at any point of time. Figure 27 shows the logical connections between CCG5 and the components in a notebook design.

Figure 27. Dual Type-C Port Notebook Design Using CCG5



EC - Embedded Controller

The following are the critical sections of the dual Type-C notebook design using CCG5:

- Power Supply Design
- I²C Communication with Embedded Controller
- Dead Battery Charging
- Power Provider or Consumer (DRP) Role
- DisplayPort Connections
- Electrical Design Considerations

8.1 Power Supply Design

Cypress' CCG5 Type-C PD Controller operates with two possible external supply voltages, VBUS or VSYS as referred in Table 14. The VDDIO supply powers the device I/Os as referred in Table 14. VDDD generates 3.3 V from an internal regulator; this can be shorted to VDDIO. VCCD is the output voltage from the core regulator and this pin is intended to connect only a decoupling capacitor. The VCCD pin cannot be used as a voltage source. CCG5 has power supply inputs at V5V_P1 and V5V_P2 pins for providing power to EMCA cables through integrated VCONN FETs. There are two VCONN FETs in CCG5 per Type-C port to power CC1_P1/P2 and CC2_P1/P2 pins. These FETs can provide a minimum of 1.5 W on the CC1 and CC2 pins for EMCA cables.

Figure 28. CCG5 Power Subsystem

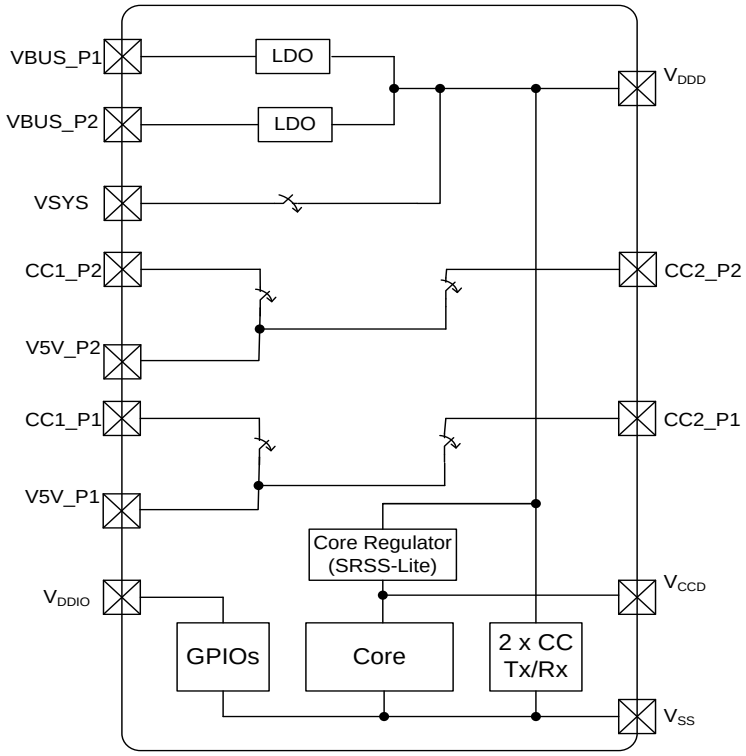


Table 14. CCG Operating Voltage Range

Parameter	Min (V)	Typ (V)	Max (V)
VBUS	4.0	–	21.5
VSYS	3.0	–	5.5
VDDD	3.0	–	5.5
VDDIO	1.71	–	VDDD
V5V_P1	4.85	–	5.5
V5V_P2	4.85	–	5.5

8.1.1 Reset and Clock

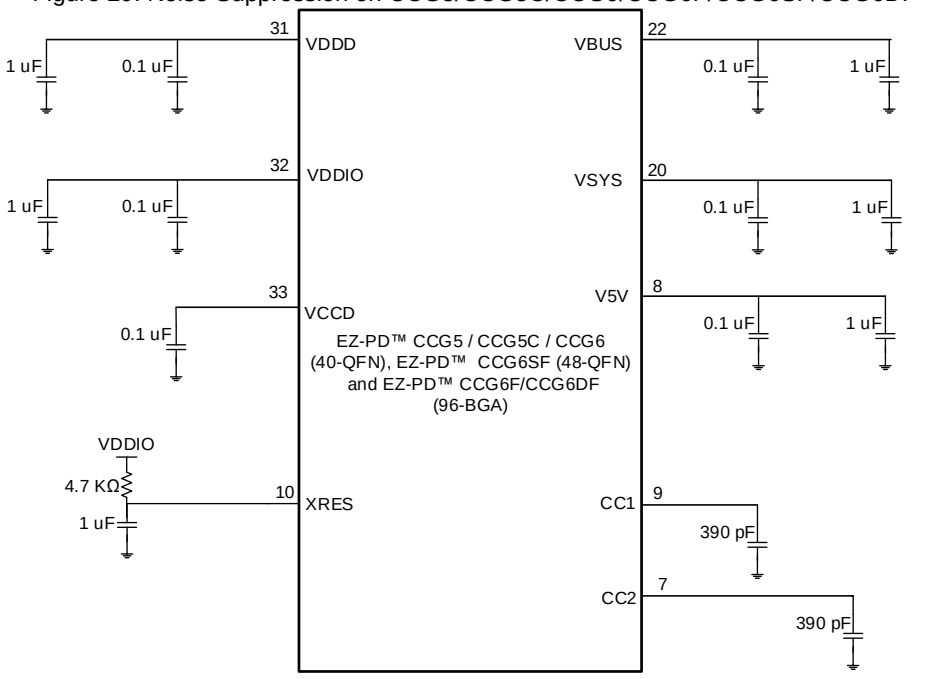
CCG5 supports a power-on-reset (POR) mechanism and it also has an active LOW external reset (XRES) pin. The XRES pin can be used by external devices to reset the CCG5 device. The XRES pin should be held LOW for a minimum of 5 µs to reset the CCG5 device. This XRES pin should be tied through an RC circuit.

CCG5 has integrated clock circuitry; external components such as a crystal or oscillator are not required.

8.1.2 Power supply Noise Suppression

Power supply noise can be suppressed by using decoupling capacitors to power supply pins VBUS, VSYS, VDDD, VDDIO, VCCD, and VCONN pins as shown in Figure 29 . A 390-pF decoupling capacitor should be connected to CC lines (CC1, CC2) to maintain the signal quality at the signaling rate of 300 kHz. Noise suppression diagram shown in Figure 29 is for a single port controller, CCG5.

Figure 29. Noise Suppression on CCG5/CCG5C/CCG6/CCG6F/CCG6SF/CCG6DF[2]



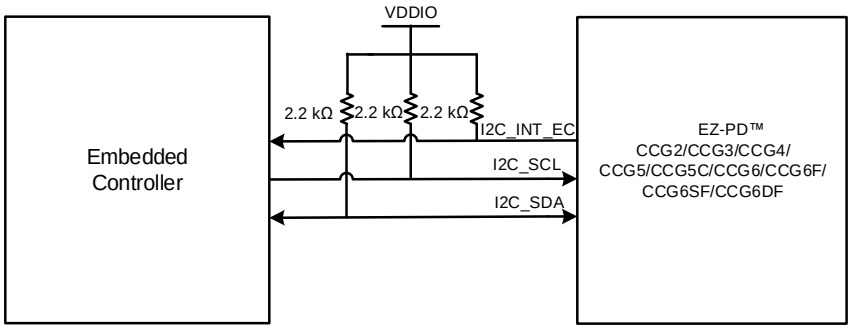
8.2 I²C Communication with Embedded Controller

This section is applicable to CCG2, CCG3, CCG4, CCG5, CCG5C, CCG6, CCG6F, CCG6SF, and CCG6DF devices.

Serial Communication Blocks (SCBs) in CCG2, CCG3, CCG4, CCG5, CCG5C, CCG6F, CCG6SF, and CCG6DF can be reconfigured as I²C (master/slave)/UART/SPI (master/slave). In a typical notebook design, the internal battery's charging or discharging is controlled by the Battery Charger Controller (BCC), which is managed by the Embedded Controller (EC). The CCG2/ CCG3/CCG4/CCG5/CCG5C/CCG6/CCG6F/CCG6SF/CCG6DF device is interfaced with the EC over I²C as shown in Figure 30.

Consider a scenario in which a Type-C port in a notebook can provide 5 V at 3 A to a connected device when the battery is full. If the charge in the battery goes below a threshold level, then the EC communicates with the CCG2/ CCG3/CCG4/CCG5/CCG5C/CCG6/CCG6F/CCG6SF/CCG6DF device over the I²C interface to negotiate the current (for example, 5 V, 900 mA) with the connected device.

Figure 30. Connection Between CCG Device I²C Lines and Embedded Controller



[2] See the CCG6F Datasheet for the ball number.

The SCL and SDA lines are required to be pulled up with a 2.2-kΩ resistor. While any CCG2 device's GPIO can be configured as an I²C interrupt pin, care should be taken to ensure that the application firmware and bootloader utilize the same GPIO as an interrupt pin. Pin#15 of the CCG4, CCG5, CCG5C, and CCG6 and Pin#F8 of the CCG6F devices is a fixed-function I/O, which is configured as an I²C interrupt pin. The application firmware running on the CCG2/CCG3/CCG4/CCG5/CCG5C/CCG6/CCG6F/CCG6SF/CCG6DF device (I²C slave) triggers the interrupt line LOW to indicate the start of a Type-C or PD event (for example, Type-C port connect or disconnect, power role swap from provider to consumer) to the EC (I²C master).

Note: See the respective CCGx datasheet to learn more about the I²C pin numbers for each SCB.

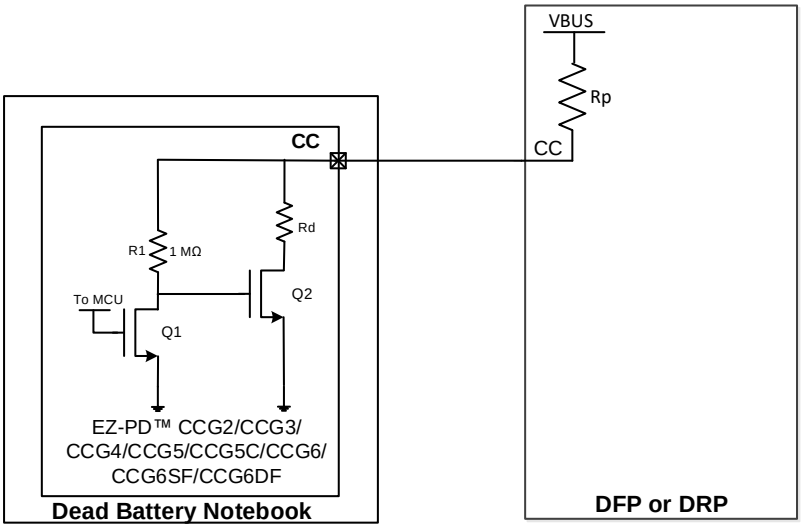
8.3 Dead Battery Charging

This section is applicable to CCG2, CCG3, CCG4, CCG5, CCG5C, CCG6, CCG6F, CCG6SF and CCG6DF devices.

If the battery of a Type-C notebook design using a CCG2/CCG3/CCG4/CCG5/CCG5C/CCG6/CCG6F/CCG6SF/CCG6DF device is completely dead, it can still be charged by connecting a DFP (such as a power adapter) or DRP devices (such as a monitor or self-powered external hard disk) to its Type-C port.

By default, a DFP or DRP presents an Rp resistor. Upon connection, the CC line on the CCG2/CCG3/CCG4/CCG5/CCG5C/CCG6 device in a notebook with a dead battery is pulled HIGH. This turns FET Q2 ON through resistor R1, and the CCG2/CCG3/CCG4/CCG5/CCG5C/CCG6/CCG6F/CCG6SF/CCG6DF device (in the notebook with the dead battery) presents a dead battery Rd resistor on the CC line (CC1 and CC2), as shown in Figure 31.

Figure 31. Dead Battery Charging of Type-C Notebook



By presenting the Rd resistor, a Type-C connection is established between the CCG2/CCG3/CCG4/CCG5/CCG5C/CCG6/ CCG6F/CCG6SF/CCG6DF device (in the notebook with the dead battery) and the DFP or DRP. Now, the notebook with the dead battery is a power consumer and receives a default 5 V on VBUS, which charges the dead battery. FET Q1 is turned OFF once the CCG2/CCG3/CCG4/CCG5/CCG5C/CCG6/CCG6F/CCG6SF/CCG6DF device is powered. After 5 V is available on VBUS, the CCG2/CCG3/CCG4/CCG5/CCG5C/CCG6/CCG6F /CCG6SF/CCG6DF device in the notebook is powered and starts negotiating with the connected DFP or charging UFP for a higher VBUS, depending on the application configuration.

CCG3, CCG4, CCG5, CCG5C, CCG6, CCG6F, CCG6SF, and CCG6DF have integrated dead battery termination resistors (Rd) on both CC1 and CC2 lines. CCG2 has an integrated termination resistor (Rd) on the CC2 line and a dedicated RD1 resistor pin that needs to be shorted with the CC1 line of CCG2. The dead battery Rd resistors are disabled by the application firmware once the device is powered up. CCG2/CCG3/CCG4/CCG5/CCG5C/CCG6/CCG6F /CCG6SF/CCG6DF devices have internal active Rd terminations that are used after the dead battery Rd resistors are disabled.

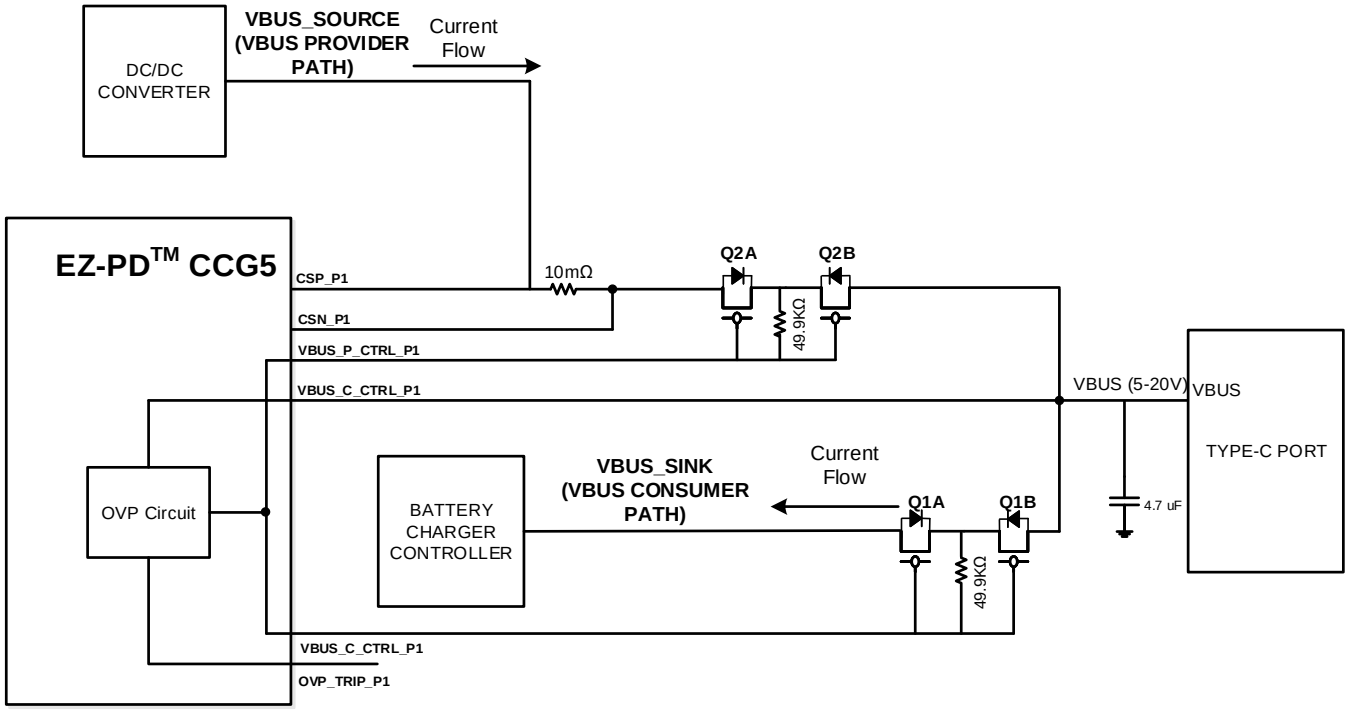
8.4 Power Provider/Consumer Role

This section explains the recommended external hardware circuitry for VBUS control, and overvoltage and overcurrent protection in a notebook design. A notebook design using a CCG5 device is a power provider when running from its internal battery and a power consumer when being charged from a DFP (such as a power adapter) or a DRP (such as a monitor or external, self-powered hard disc).

8.4.1 Control of VBUS Provider Path and VBUS Consumer Path

A Battery Charger Controller (BCC) controls the charging (sinking of VBUS) or discharging (sourcing of VBUS) of the battery. A CCG5 device consists of two I/Os per Type-C port, namely, VBUS_P_CTRL and VBUS_C_CTRL, to control the VBUS provider (sourcing of power) or consumer (sinking of power) path connected to the BCC. Figure 32 shows the recommended implementation to control this VBUS path.

Figure 32. VBUS Provider and Consumer Path Control

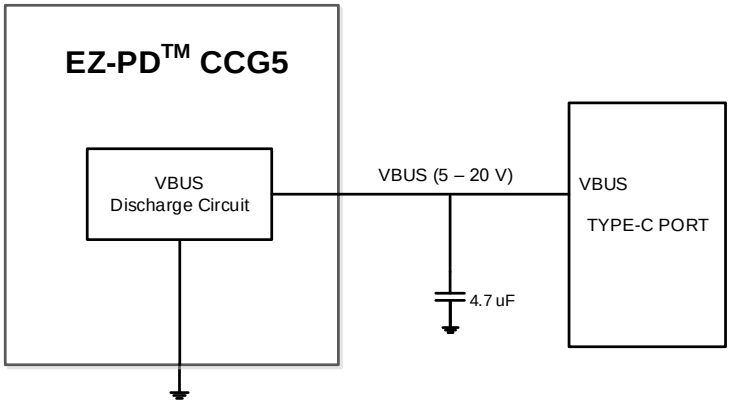


8.4.2 Control of VBUS Discharge Path

This section explains the critical need of the VBUS discharge circuitry. Depending on the connected downstream device, the VBUS voltage varies as illustrated by the following example scenarios:

- Example Scenario 1: A UFP device sinking 100 W of power (20 V, 5 A) is disconnected from a Type-C port, and immediately another UFP device sinking 25 W of power (5 V, 5 A) is connected to the same Type-C port.
- Example Scenario 2: A notebook changes its power role from provider (sourcing 100 W of power) to consumer (sinking 45 W of power).

Figure 33. VBUS Discharge Control Circuitry



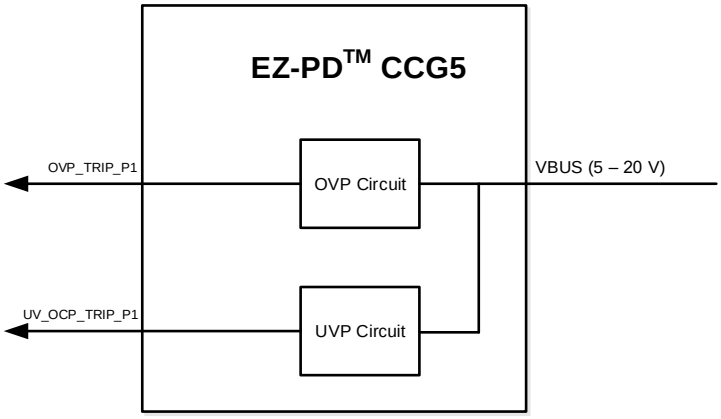
In Scenario 1, the VBUS capacitor shown in Figure 33 may not have discharged fully from the original 20 V when the second UFP device is connected. This could cause an overvoltage on the second UFP device, which requires 5 V on VBUS.

In Scenario 2, a similar overvoltage could occur when the power role is swapped. To prevent this scenario, the CCG5 device provides a built-in VBUS discharge circuit which provides a discharge path for the VBUS capacitor. This avoids overvoltage scenarios like example scenarios 1 and 2.

8.4.3 Overvoltage Protection (OVP) for VBUS

An Overvoltage Protection (OVP) circuit is required on VBUS to prevent damage to the system if VBUS exceeds the maximum voltage negotiated by the CCG5 controller. CCG5 is integrated with a built-in OVP unit and hence no external circuitry is required.

Figure 34. OVP/UVP Circuit



As per the USB PD specification, the maximum voltage at VBUS can be 20 V. Table 15 provides the value of OVP trip voltage (1.2 times V_{BUS}) for possible VBUS voltages.

Table 15. Values of OVP Trip Voltage at Different VBUS Voltages

VBUS Voltage (V)	OVP Trip Voltage (V)
5	6
9	10.8
15	18
20	24

A CCG5 device has a built-in OVP circuit. The built-in resistor divider circuit and comparator compares OVP trip voltage with respective VBUS voltage (shown in Table 15). Any overvoltage event will be detected by the OVP circuit and will be notified via pin OVP_TRIP_P1.

8.4.4 Undervoltage Protection (UVP) for VBUS

An Undervoltage Protection (UVP) circuitry is required on VBUS to detect a Type-C disconnect event when a CCG5-enabled notebook is consuming power from the DFP (such as a power adapter) or charging UFP (such as a monitor or external hard disk) over the Type-C interface.

As shown in Figure 34, CCG5 is integrated with a built-in UVP unit and hence no external circuitry is required.

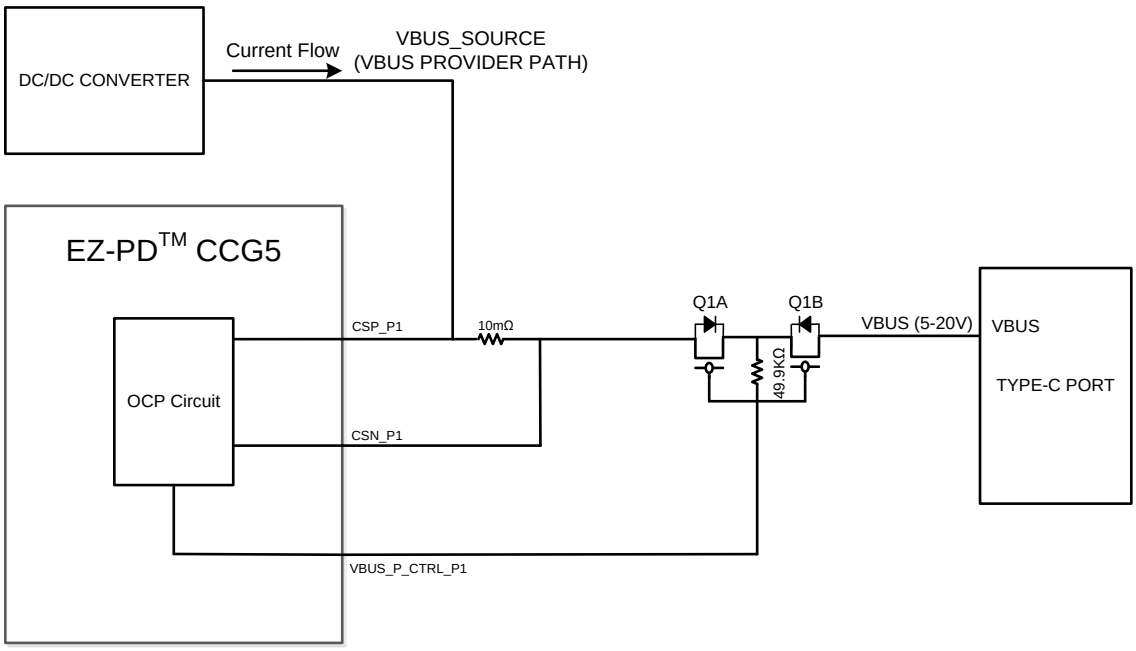
Consider a scenario in which the notebook and the DFP device connected to its Type-C port establish a power contract, and the notebook starts receiving 5 V of VBUS from the DFP. The voltage Vx is derived from VBUS using internal resistor divider circuit (as defined in Table 15), which is the first input to CCG5 device's UVP comparator.

The CCG5 device's firmware has set the VBUS undervoltage detection threshold to 4 V. The value of Vx for 4-V VBUS would be 0.363 V (as defined in Table 17), which is configured by the CCG5 device's firmware as the UVP trip voltage. This UVP trip voltage is the second input to the UVP comparator. The UVP comparator compares this UVP trip voltage (0.363 V) with the Vx voltage for the 5-V VBUS (0.454 V, as listed in Table 17). The output of the UVP circuit is connected to the VBUS_C_CTRL_P1 pin to control the VBUS consumer path as shown in Figure 32 in an undervoltage scenario (if VBUS goes below 4 V), and CCG5 device turns OFF.

8.4.5 Overcurrent Protection (OCP) for VBUS

An Overcurrent Protection (OCP) circuitry is required on VBUS to prevent damage to the system if the VBUS current exceeds the maximum current negotiated by the CCG5 controller. As shown in Figure 35, CCG5 is integrated with a built-in OCP control; therefore, no external circuitry is required for OCP implementation.

Figure 35. OCP Circuitry

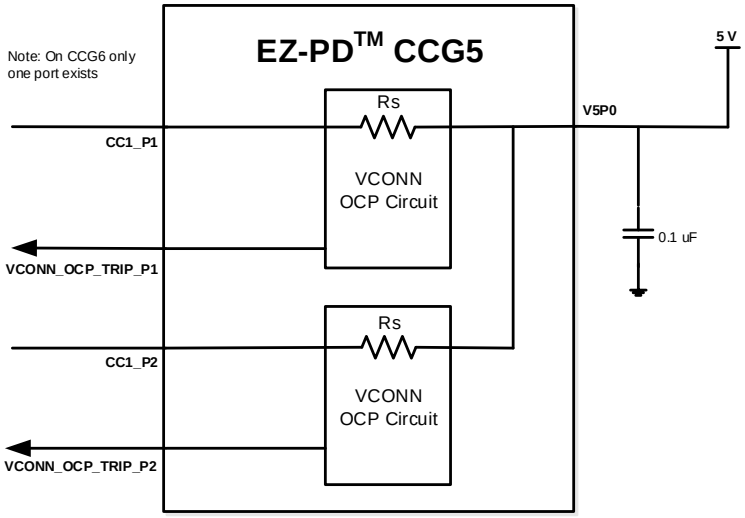


CCG5 has a built-in current sense monitor circuitry and built-in comparator which detect any overcurrent event on VBUS.VBUS_P_CTRL_P1 signal will be triggered in the overcurrent scenario and the CCG5 device turns OFF VBUS by turning OFF the power provider FETs Q1A and Q1B as shown in Figure 35. CCG5 also disconnects itself from the Type-C port to shut off the VBUS.

8.4.6 Overcurrent Protection (OCP) for VCONN

In a notebook design, VCONN supplies power to the electronically marked cable attached to it. VCONN FETs on CC lines can handle a current up to 0.5 A. OCP circuitry is required on VCONN to prevent damage to the system if VCONN current exceeds 0.5 A. As shown in Figure 36, CCG5 is integrated with a built-in VCONN OCP circuit, hence no external circuitry is required to implement OCP for VCONN in a notebook design using CCG5.

Figure 36. OCP for VCONN

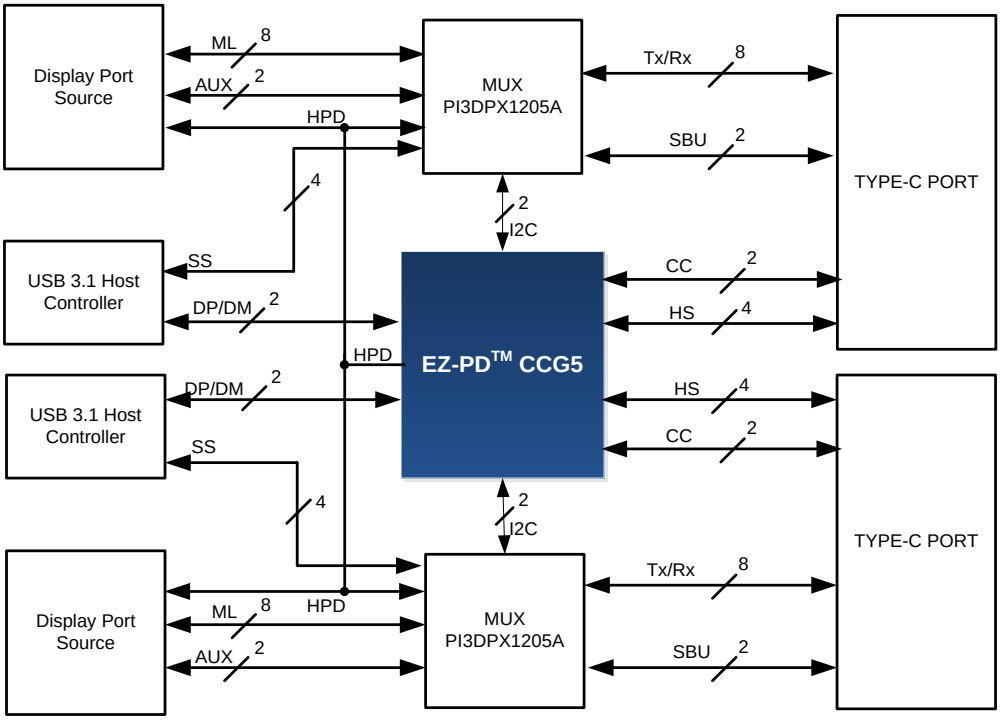


8.5 DisplayPort Connections

Type-C is a versatile connector, which also supports DisplayPort signals by repurposing one of the SuperSpeed lanes and two sideband signals. These repurposed signals act in a new mode, called “alternate mode.” One example of using a Type-C interconnection in alternate mode is DisplayPort. See the VESA specification for more details on DisplayPort Alt Mode on the USB Type-C Standard.

In a Type-C notebook design, a display monitor can be connected directly to the notebook over the Type-C interface using a CCG5 and a display mux controller. Figure 37 shows the connections between CCG5 and two display mux controllers in a notebook design having two USB 3.1 Host controllers and one DisplayPort Source.

Figure 37. CCG5/CCG6DF and Dual Display Mux Controller Connections



1] SS- SuperSpeed Lanes
2] ML- Main Link Lanes
3] AUX- Auxilliary Lines
4] HPD- Hot Plug Detect
5] SBU- Side Band Use
6] HS- High Speed Lines(D+/D-_top and D+/D-_bottom)

Whenever a display monitor is connected to the Type-C port on a notebook, CCG5 discovers that it has a device attached with alternate mode supported. Through PD communication, CCG5 identifies the display monitor's Standard ID (SID) or Vendor ID (VID) (so SVID = SID or VID). The display monitor reports an SVID of 0xFF01 (per the VESA specification), which is assigned to a DisplayPort connection.

CCG5 initiates an alternate mode sequence and asserts the Hot Plug Detect (HPD) signal to the DisplayPort source and display mux controller. The DisplayPort source detects that the display monitor is connected to the notebook. The display monitor can have two or four Main Link (DisplayPort) lanes. The 2-lane Main Link configuration supports a raw bit rate up to 10.8 Gbps, and the 4-lane Main Link configuration supports a raw bit rate up to 21.6 Gbps.

CCG5 checks the DisplayPort status, and if it receives an ACK, CCG5 configures the display mux controller in either 2-lane or 4-lane mode. CCG5 communicates with the display mux controller over the I^2C interface (such as the display mux controller from Pericom, PI3DPX1205A). See the respective mux controller's datasheet for more details.

The display mux controller switches its output lines (TX/RX) between the USB SuperSpeed lanes and the Main Link (DisplayPort) lanes from the DisplayPort source.

Consider a scenario in which a 4-lane display monitor is connected to the notebook, and no other USB 3.0 device is connected. In this case, the display mux controller connects four Main Link (DisplayPort) lanes to the Type-C port, and the display appears on the screen. Now if a USB 3.0 device is connected to the notebook, it enumerates as a USB 2.0 device because all the SuperSpeed lanes on the Type-C port are repurposed as DisplayPort lanes. USB 2.0 enumeration occurs because USB 2.0 (DP/DM) lines are connected from the USB Host controller to the Type-C port through CCG5.

The USB Host controller detects the presence of the SuperSpeed device (enumerated as a USB 2.0 device) and communicates it to the EC. The system may decide to switch from 4-lane to 2-lane display to enable SuperSpeed device enumeration or it may continue to be in 4-lane mode. This is implementation-specific. If the system wants to switch to 2-lane mode, the EC sends a message to CCG5 to reconfigure the display mux controller from 4-lane to 2-lane display mode to enable connection of the USB SuperSpeed lane to the Type-C port. Now, the display appears on the monitor, and the USB 3.0 device is detected as a SuperSpeed device. Note that the display monitor's resolution in the 2-lane mode will be lower than in the 4-lane mode. The Type-C port also receives auxiliary signals from the DisplayPort Source through the display mux controller that carry either the audio signals or the control signals for display.

The recommended part for display mux controller is from Pericom (PI3DPX1205A), which has a built-in re-driver.

8.6 Electrical Design Considerations

See Electrical Design Considerations for more details.

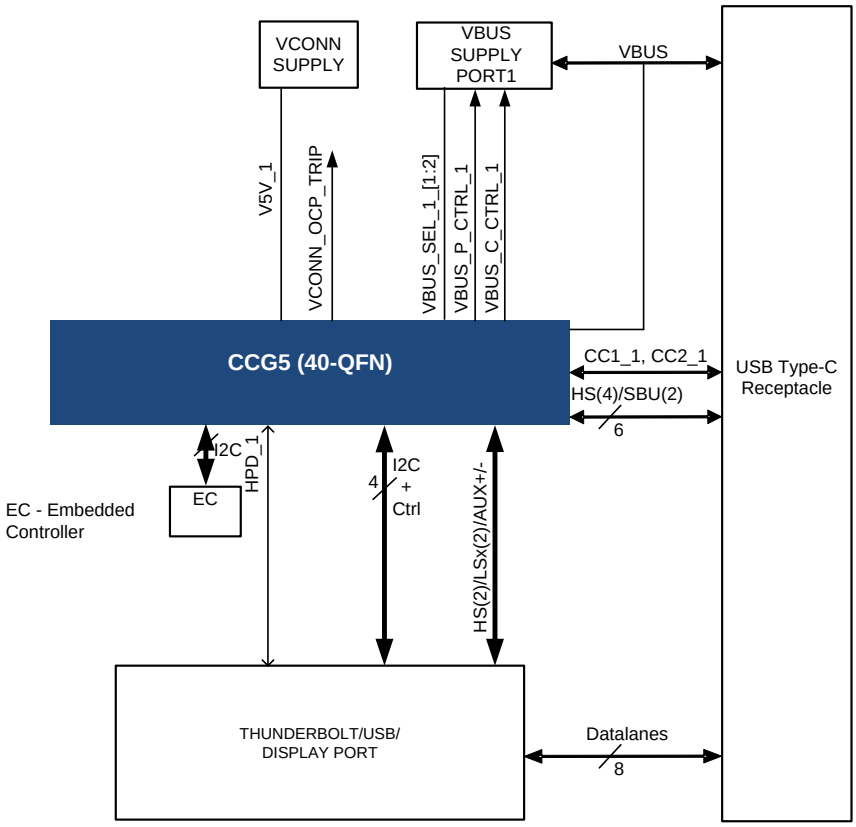
9 Single Type-C Port DRP Application Using CCG5

Note: CCG5 single port part CYPD5125-40LQXIT is NRND. See the CCG5C datasheet for pin-to-pin compatible replacement part.

A CYPD5125-40LQXI CCG5 controller is used here as the reference.

This section describes the design of a typical single Type-C port DRP application, such as a Type-C notebook, using the EZ-PD CCG5 controller. Figure 38 shows the logical connections between CCG5 and components in a notebook. This design is similar to the dual Type-C port application discussed in Dual Type-C Port DRP Application Using CCG6DF.

Figure 38. Single Type-C Port Notebook Design Using CCG5



The following are the critical sections of this Type-C notebook design using CCG5:

- Power Supply Design
- Dead Battery Charging
- Power Provider/Consumer Role
- DisplayPort Connection
- Electrical Design Considerations

9.1 Power Supply Design

See Power Supply Design.

9.2 I²C Communication with Embedded Controller

See I2C Communication with Embedded Controller.

9.3 Dead Battery Charging

See Dead Battery Charging.

9.4 Power Provider/Consumer Role

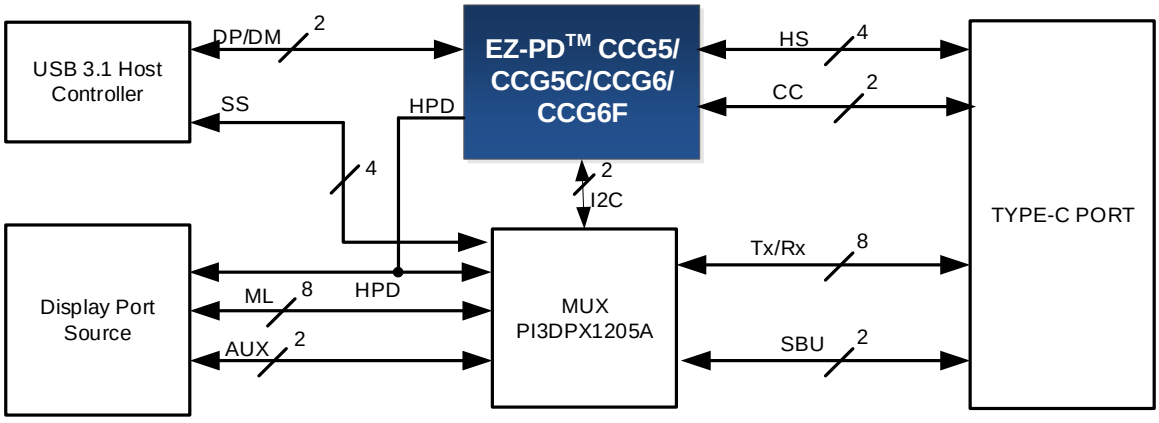
See Power Provider/Consumer Role.

9.5 DisplayPort Connections

Type-C is a versatile connector, which also supports DisplayPort signals by repurposing one of the SuperSpeed lanes and two sideband signals. These repurposed signals act in a new mode, called an “alternate mode.” One example of using a Type-C interconnection in the alternate mode is DisplayPort. See the VESA specification for more details on the DisplayPort Alt Mode on the USB Type-C Standard.

In a Type-C notebook design, a display monitor can be connected directly to the notebook over the Type-C interface using CCG5/CCG5C/CCG6/CCG6F and a display mux controller. Figure 39 shows the connections between CCG5/CCG5C/CCG6/CCG6F and the display mux controller in a notebook design.

Figure 39. CCG5/CCG5C /CCG6/CCG6F/CCG6SF and Display Mux Controller Connections



1] SS- SuperSpeed Lanes
2] ML- Main Link Lanes
3] AUX- Auxilliary Lines
4] HPD- Hot Plug Detect
5] SBU- Side Band Use
6] HS- High Speed Lines(D+/D-_top and D+/D-_bottom)

Whenever a display monitor is connected to the Type-C port on a notebook, the CCG5/CCG5C/CCG6/CCG6F device discovers that it has a device attached with alternate mode supported. Through PD communication, the CCG5/CCG5C/CCG6/CCG6F device identifies the display monitor's Standard ID (SID) or Vendor ID (VID) (so SVID = SID or VID). The display monitor reports an SVID of 0xFF01 (per the Type-C specification), which is assigned to a DisplayPort connection.

The CCG5/CCG5C/CCG6/CCG6F device initiates an alternate mode sequence and asserts the Hot Plug Detect (HPD) signal to the DisplayPort source and display mux controller. The DisplayPort source detects that the display monitor is connected to the notebook. The display monitor can have two or four Main Link (DisplayPort) lanes. The 2-lane Main Link configuration supports a raw bit rate up to 10.8 Gbps, and the 4-lane Main Link configuration supports a raw bit rate up to 21.6 Gbps.

The CCG5/CCG5C/CCG6/CCG6F device checks the DisplayPort status, and if it receives an ACK, the CCG5/CCG5C/CCG6/CCG6F device configures the display mux controller in either 2-lane or 4-lane mode. The CCG5/CCG5C/CCG6/CCG6F device communicates with the display mux controller over an I^2C interface (such as the display mux controller from Pericom, PI3DPX1205A). See the respective mux controller's datasheet for more details.

The display mux controller switches its output lines (TX/RX) between the USB SuperSpeed lanes and the Main Link (DisplayPort) lanes from the DisplayPort source.

Consider a scenario in which a 4-lane display monitor is connected to the notebook, and no other USB 3.0 device is connected. In this case, the display mux controller connects four Main Link (DisplayPort) lanes to the Type-C port, and a display appears on the screen. Now, if a USB 3.0 device is connected to the notebook, it enumerates as a USB 2.0 device because all the SuperSpeed lanes on the Type-C port are repurposed as DisplayPort lanes. USB 2.0 enumeration occurs because USB 2.0 (DP/DM) lines are connected from the USB Host controller to the Type-C port through CCG5/CCG5C/CCG6/CCG6F.

The USB Host controller detects the presence of the SuperSpeed device (enumerated as a USB 2.0 device) and communicates it to the EC. The system may decide to switch from 4-lane to 2-lane mode to enable SuperSpeed device enumeration or it may continue to be in 4-lane mode. This is implementation-specific. If the system wants to switch to 2-lane mode, the EC sends a message to the CCG5/CCG5C/CCG6/CCG6F device to reconfigure the display mux controller from 4-lane to 2-lane display mode to enable connection of the USB SuperSpeed lane to the Type-C port. Now, the display appears on the monitor, and the USB 3.0 device is detected as a SuperSpeed device. Note that the display monitor's resolution in the 2-lane mode will be lower than in the 4-lane mode. The Type-C port also receives auxiliary signals from the DisplayPort source through the display mux controller that carry either the audio signals or the control signals for the display.

The recommended part for display mux controller is from Pericom (PI3DPX1205A), which has a built-in re-driver.

9.6 Electrical Design Considerations

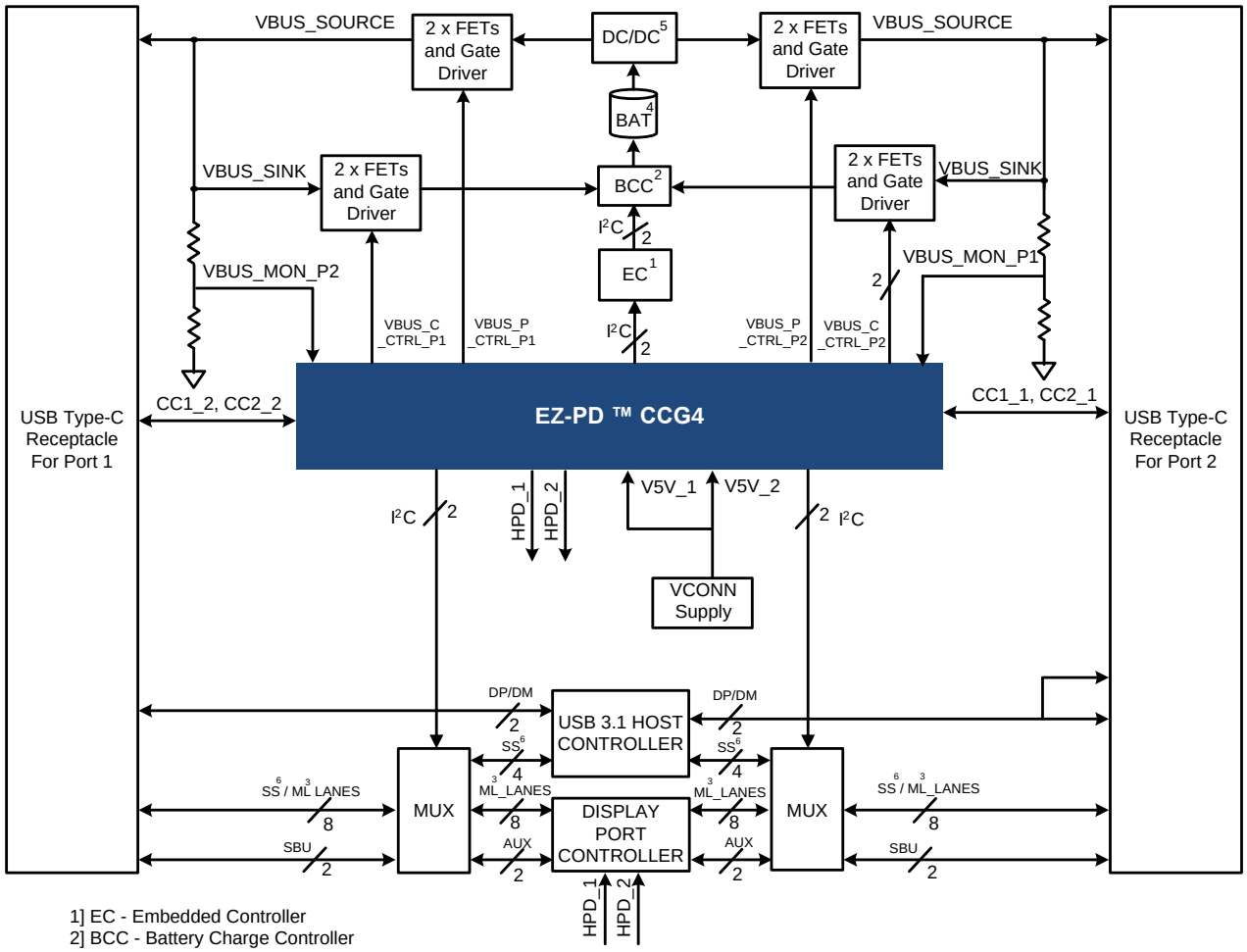
See Electrical Design Considerations.

10 Dual Type-C Port DRP Application Using CCG4

A CYPD4225-40LQXIT CCG4 controller is used here as the reference.

CCG4 integrates two Type-C transceivers and facilitates a dual Type-C port notebook design with a reduced BOM compared to CCG2 and CCG3, which integrate only one Type-C transceiver. In this application, both Type-C ports can be either power providers or power consumers at the same or different times. Similarly, both Type-C ports can play the role of DFP or DRP at any point of time. Figure 40 shows the logical connections between CCG4 and the components in a notebook design.

Figure 40. Dual Type-C Port Notebook Design Using CCG4



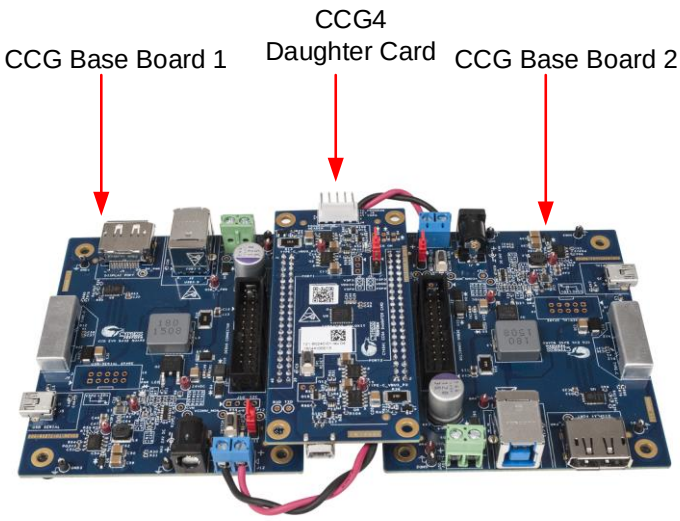
1] EC - Embedded Controller
2] BCC - Battery Charge Controller
3] ML – Main Link
4] BAT – Battery
5] DC/DC – DC to DC Converter
6] SS -- SuperSpeed

The following are the critical sections of the dual Type-C notebook design using CCG4:

- Power Supply Design
- I²C Communication with Embedded Controller
- Dead Battery Charging
- Power Provider or Consumer (DRP) Role
- DisplayPort Connections
- Electrical Design Considerations

Cypress provides the CY4541 EZ-PD CCG4 EVK (Evaluation Kit) to evaluate the dual Type-C notebook design using CCG4 as shown in Figure 41. A notebook or a PC with two USB 3.0 ports and a DisplayPort along with the CY4541 EZ-PD CCG4 EVK is equivalent to a PD-enabled dual Type-C-port notebook. The CY4541 EZ-PD CCG4 EVK consists of two CCG base boards and one CCG4 daughter card. See section 3.1 of the CY4541 EZ-PD CCG4 EVK kit guide for more details on kit architecture.

Figure 41. CY4541 EZ-PD CCG4 EVK



10.1 Power Supply Design

Cypress' Type-C PD Controller CCG4 operates with two supply voltages; the voltage supply VDDD powers the device core and two Type-C transceivers. The VDDIO supply powers the device I/Os as referred in Table 16. CCG4 has an integrated voltage regulator as shown in Figure 42. VCCD is the output voltage from the core regulator and this pin is intended to connect only a decoupling capacitor. The VCCD pin cannot be used as a voltage source. CCG4 has power supply inputs V5V_P1 and V5V_P2 pins for providing power to EMCA cables through integrated VCONN FETs. There are two VCONN FETs in CCG4 per Type-C port to power CC1_P1/P2 and CC2_P1/P2 pins. These FETs can provide a minimum of 1 W on the CC1 and CC2 pins for EMCA cables.

Figure 42. CCG4 Power Subsystem

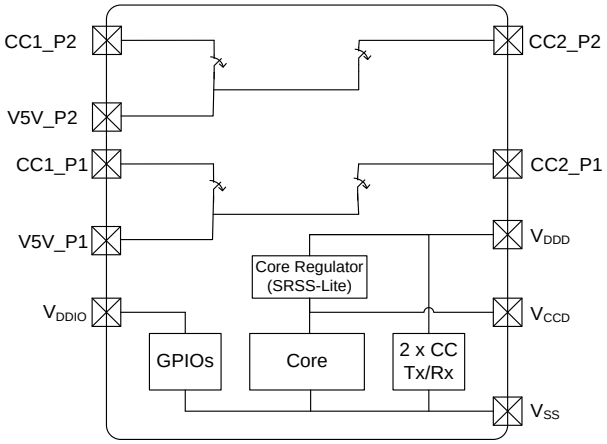


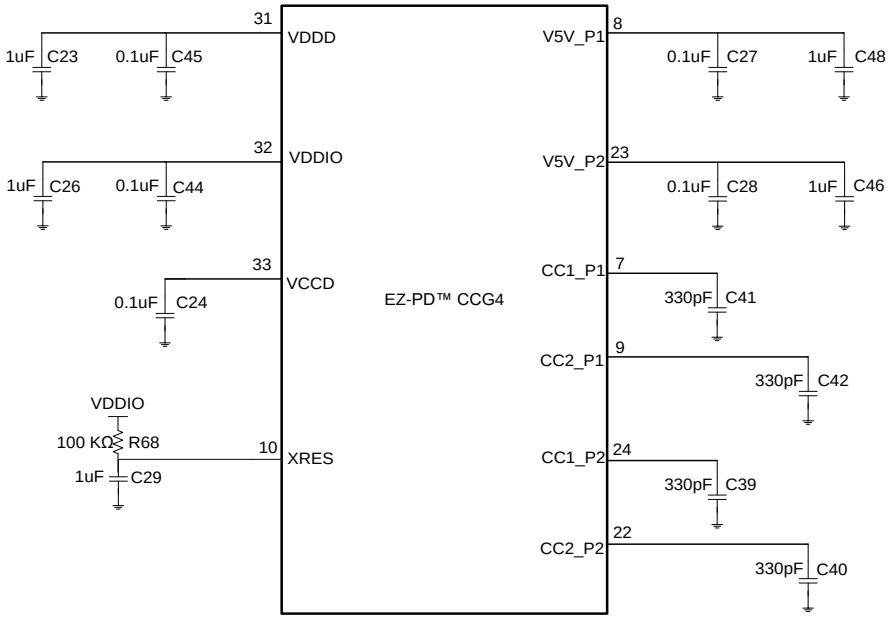
Table 16. CCG4 Operating Voltage Range

Parameter	Min (V)	Typ (V)	Max (V)
VDDD	3	--	5.5
VDDIO	1.71	--	VDDD
V5V_P1	4.85	--	5.5
V5V_P2	4.85	--	5.5

10.1.1 Decoupling Capacitors in Power Subsystem

Power supply noise can be suppressed by using decoupling capacitors to power supply pins VDDD, VDDIO, VCCD, V5V_P1, and V5V_P2 as shown in Figure 43. A 330-pF decoupling capacitor should also be connected to the CC lines (CC1_P1, CC2_P1, CC1_P2, and CC2_P2) to maintain the signal quality at the signaling rate of 300 kHz.

Figure 43. Noise Suppression Using Decoupling Capacitors



10.1.2 Reset and Clock

CCG4 supports a power-on-reset (POR) mechanism and it also has an active LOW external reset (XRES) pin The XRES pin can be used by external devices to reset the CCG4 device. The XRES pin should be held LOW for a minimum of 1 µs to reset the CCG4 device. This XRES pin should be tied through an RC circuit as shown in Figure 43. The recommended values for R and C are 100 kΩ and 1 µF respectively to meet the 1-µs pulse-width requirement,

CCG4 has integrated clock circuitry; external components such as a crystal or oscillator are not required.

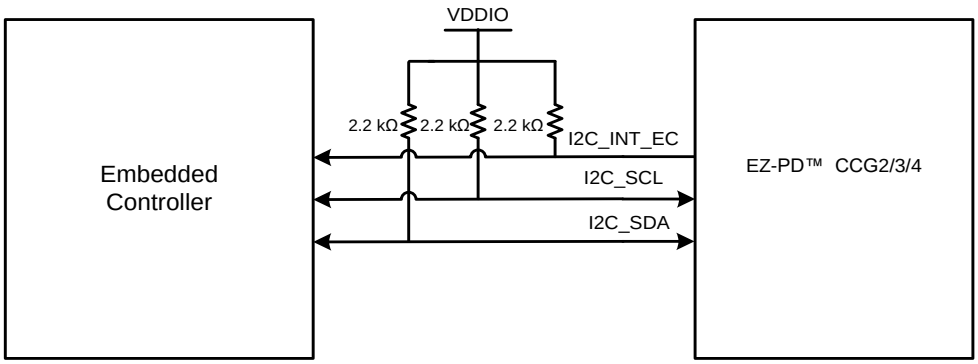
10.2 I²C Communication with Embedded Controller

This section is applicable to CCG2, CCG3, and CCG4 devices.

Serial Communication Blocks (SCBs) in CCG2, CCG3, and CCG4 can be reconfigured as I²C (master/slave)/UART/SPI (master/slave). In a typical notebook design, the internal battery's charging or discharging is controlled by the Battery Charger Controller (BCC), which is managed by the Embedded Controller (EC). The CCG2/CCG3/CCG4 device is interfaced with the EC over I²C as shown in Figure 44.

Consider a scenario in which a Type-C port in a notebook can provide 5 V at 3 A to a connected device when the battery is full. If the charge in the battery goes below a threshold level, then the EC communicates with the CCG2/CCG3/CCG4 device over the I²C interface to negotiate the current (for example, 5 V, 900 mA) with the connected device.

Figure 44. Connection Between CCG Device I²C Lines and Embedded Controller



The SCL and SDA lines are required to be pulled up with a 2.2-kΩ resistor. While any CCG2 device's GPIO can be configured as an I²C interrupt pin, care should be taken to ensure that the application firmware and bootloader utilize the same GPIO as an interrupt pin. Pin#15 of the CCG4 device is a fixed-function I/O, which is configured as an I²C interrupt pin. The application firmware running on the CCG2/CCG3/CCG4 device (I²C slave) triggers the interrupt line LOW to indicate the start of a Type-C or PD event (for example, Type-C port connect or disconnect, power role swap from provider to consumer, and so on) to the EC (I²C master).

In the CY4541 EZ-PD CCG4 EVK, the CCG4 device's I²C lines are present on jumper headers J9 and J10 on the CCG baseboards. See the CY4541 CCG EVK baseboard schematics for details.

Note: See the respective Type-C and PD controller's datasheet to learn more about the I²C pin numbers for each SCB.

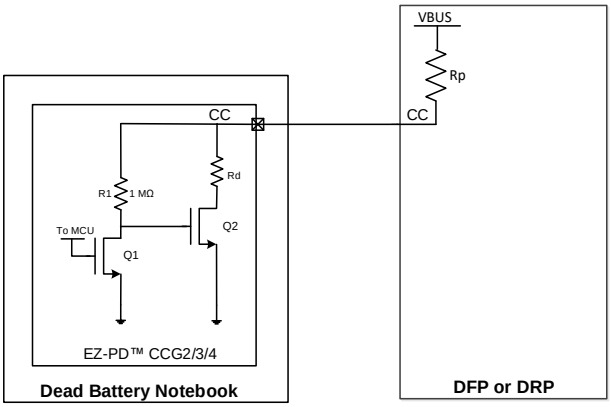
10.3 Dead Battery Charging

This section is applicable to CCG2, CCG3, and CCG4 devices.

If the battery of a Type-C notebook design using a CCG2/CCG3/CCG4 device is completely dead, it can still be charged by connecting a DFP (such as a power adapter) or DRPs (such as a monitor or external hard disk) to its Type-C port.

By default, a DFP or DRP presents an Rp resistor. Upon connection, the CC line on the CCG2/CCG3/CCG4 device in a notebook with a dead battery is pulled HIGH. This turns FET Q2 ON through resistor R1, and the CCG2/CCG3/CCG4 device (in the notebook with the dead battery) presents a dead battery Rd resistor on the CC line (CC1 and CC2), as shown in Figure 45.

Figure 45. Dead Battery Charging of Type-C Notebook

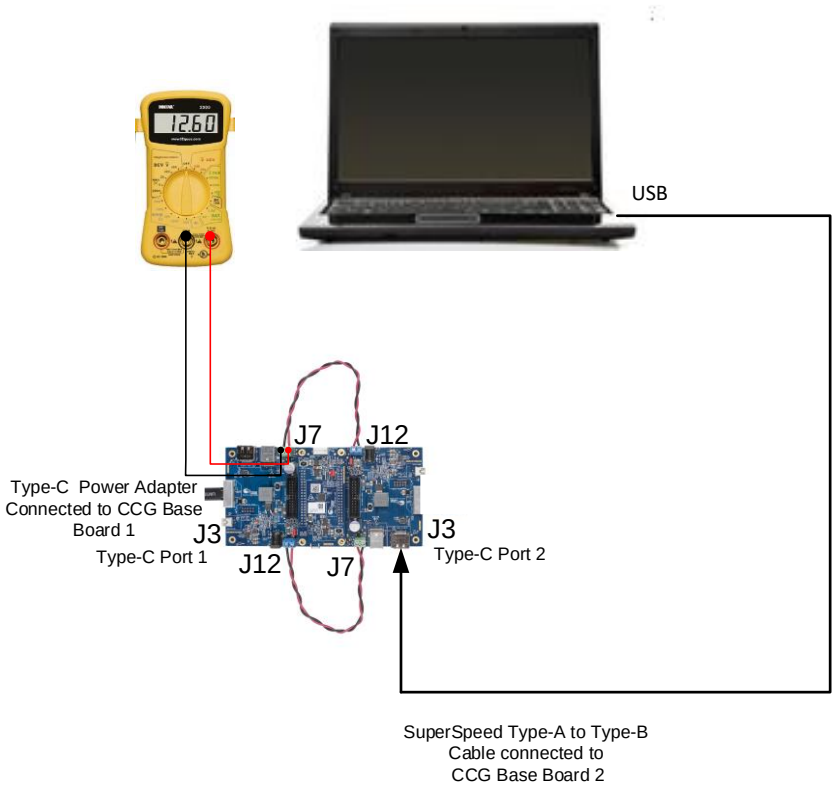


By presenting the Rd resistor, a Type-C connection is established between the CCG2/CCG3/CCG4 device (in the notebook with the dead battery) and the DFP or DRP. Now, the notebook with the dead battery is a power consumer and receives a default 5 V on VBUS, which charges the dead battery. FET Q1 is turned OFF once the CCG2/CCG3/CCG4 device is powered. After 5 V is available on VBUS, the CCG2/CCG3/CCG4 device in the notebook is powered and starts negotiating with the connected DFP or charging UFP for a higher VBUS, depending on the application configuration.

CCG3 and CCG4 have integrated dead battery termination resistors (Rd) on both CC1 and CC2 lines. CCG2 has an integrated termination resistor (Rd) on the CC2 line and a dedicated RD1 resistor pin that needs to be shorted with the CC1 line of CCG2. The dead battery Rd resistors are disabled by the application firmware once the device is powered up. CCG2/CCG3/CCG4 devices have internal active Rd terminations that are used after the dead battery Rd resistors are disabled.

Dead battery charging of CCG4 can be demonstrated by using the CY4541 EZ-PD CCG4 EVK as shown in Figure 46. See Chapter 4 (DRP Kit Operation) of the CY4541 EZ-PD CCG4 EVK kit guide for details on hardware connections of this setup.

Figure 46. Dead Battery Charging Demo Using CY4541 EZ-PD CCG4 EVK



A notebook or a PC with two USB 3.0 ports along with the CY4541 EZ-PD CCG4 EVK is equivalent to a PD-enabled dual Type-C port notebook. Because a DC power adapter is not connected to the EVK, the onboard CCG4 is not powered, which emulates a dual-Type-C notebook with dead battery. CCG4 can be powered by connecting a Type-C power adapter to one of the EVK's Type-C ports as shown in Figure 46. Once CCG4 in the EVK is powered, it establishes a power contract with the Type-C power adapter and starts consuming power. This can be verified by connecting a digital multimeter to the power output header (J7) of the CCG base board (where the Type-C power adapter is connected) to measure the output voltage in the dead-battery charging scenario. This demonstrates that a CCG4-enabled dual Type-C notebook can be charged even from a dead battery condition.

10.4 Power Provider/Consumer Role

This section explains the recommended external hardware circuitry for VBUS control, and overvoltage and overcurrent protection in a notebook design. This applies only to CCG2 and CCG4 devices because CCG3 has integrated gate drivers to control VBUS and a 20-V tolerant VBUS regulator for overvoltage and overcurrent protection.

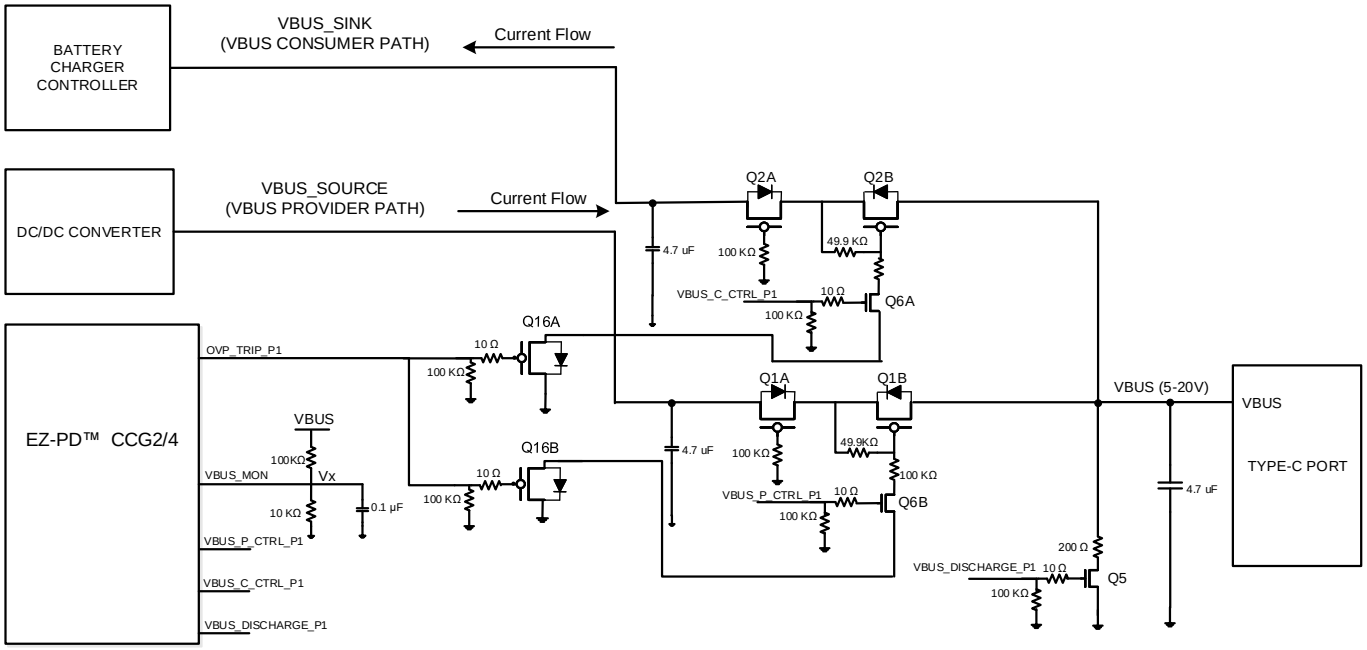
See Power Provider/Consumer Role for CCG3.

A notebook design using a CCG2/CCG4 device is a power provider when running from its internal battery and a power consumer when being charged from a DFP (such as a power adapter) or a DRP (such as a monitor or external, self-powered hard disc).

10.4.1 Control of VBUS Provider Path and VBUS Consumer Path

A Battery Charger Controller (BCC) controls the charging (sinking of VBUS) or discharging (sourcing of VBUS) of the battery. A CCG2/CCG4 device consists of two I/Os per Type-C port, namely, VBUS_P_CTRL and VBUS_C_CTRL, to control the VBUS provider (sourcing of power) or consumer (sinking of power) path connected to the BCC. Figure 47 shows the recommended implementation of FETs to control this VBUS path.

Figure 47. VBUS Provider and Consumer Path Control

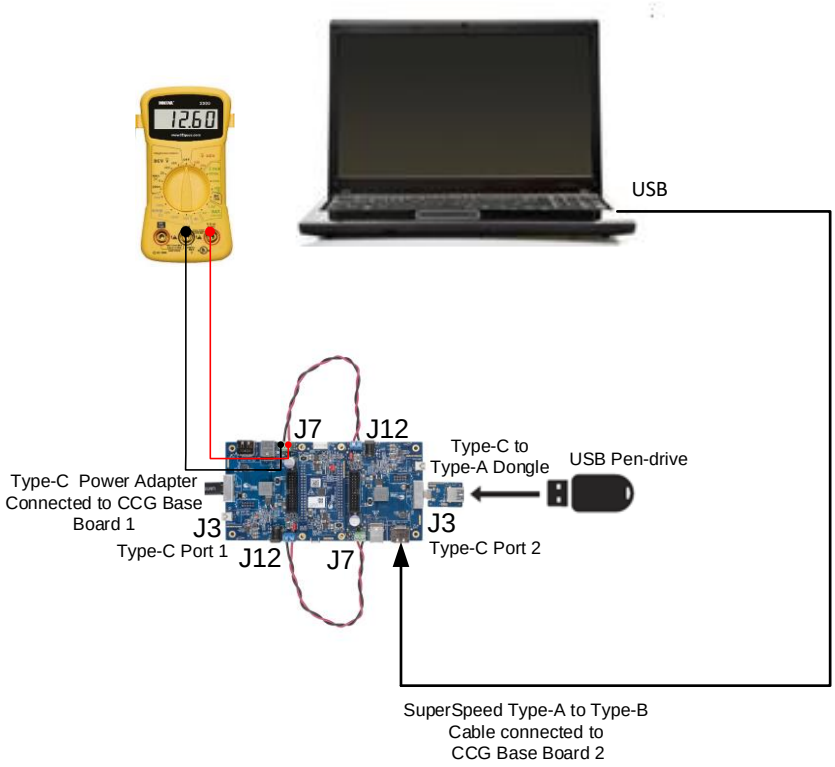


VBUS_C_CTRL and VBUS_P_CTRL are active HIGH pins. As shown in Figure 47, when VBUS_C_CTRL is LOW, FET Q6A turns OFF. This FET controls Q2A and Q2B, and turns them OFF. Thus, a CCG2/CCG4 device will not be able to consume power from the DFP or charging UFP, as its power consumer path is OFF. When VBUS_C_CTRL is HIGH, FET Q6A is ON, which turns ON FETs Q2A and Q2B, and thus the VBUS consumer path is ON.

When the VBUS_P_CTRL pin is HIGH, FETs Q6B, Q1A, and Q1B are ON, and thus the VBUS provider path turns ON. When VBUS_P_CTRL is LOW, FETs Q6B, Q1A, and Q1B are OFF.

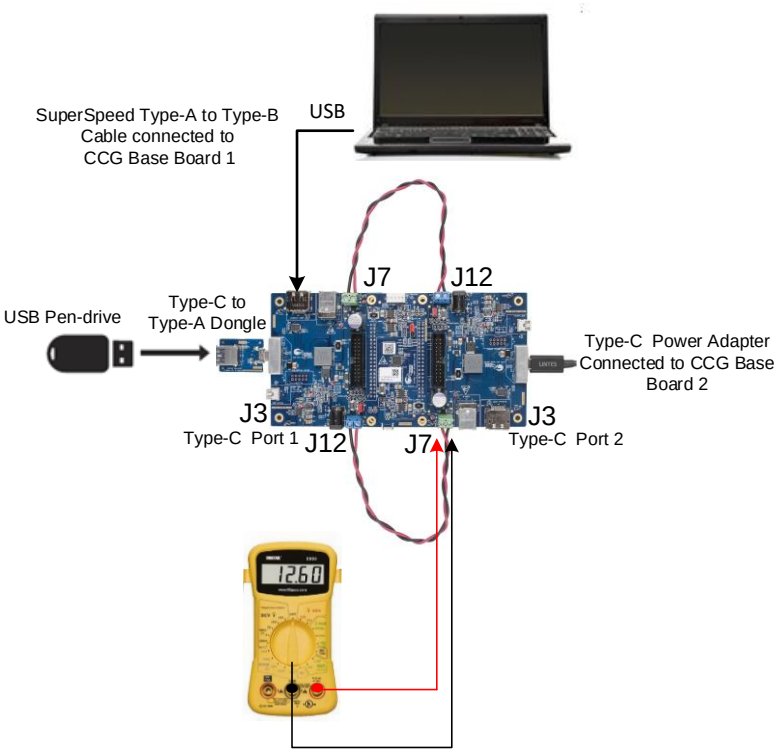
The diodes between the source and drain terminals of FETs Q2A and Q2B turn OFF the VBUS consumer path completely when the VBUS provider path is active. Similarly, the diodes between the source and drain terminals of FETs Q1A and Q1B turn OFF the VBUS provider path completely when the VBUS consumer path is active. This capability of CCG4 to switch the power role from provider to consumer or vice-a-versa can be demonstrated by using the CY4541 EZ-PD CCG4 EVK as shown in Figure 47. The CY4541 EZ-PD CCG4 EVK along with a USB 3.0- enabled notebook or a PC emulates a CCG4-enabled Type-C notebook. See Chapter 4 (DRP Kit Operation) of the CY4541 EZ-PD CCG4 EVK kit guide for details on hardware connections of this setup.

Figure 48. Switching Between Power Provider and Power Consumer Roles of CCG4 Using CY4541 EZ-PD CCG4 EVK (Example 1)



As shown in Figure 48, when the Type-C power adapter is connected to Type-C port 1 of the CY4541 EZ-PD CCG4 EVK, CCG4 starts consuming power from the Type-C power adapter. This can be verified by measuring the voltage on the power output header (J7) of the CCG base board 1 (where the Type-C power adapter is connected) using a digital multimeter. This emulates the charging of a CCG4-enabled Type-C notebook in which the Type-C port 1 of the notebook consumes power from the power adapter to charge its internal battery. However, if a USB pen drive is connected to the Type-C port 2 of the CCG4-enabled Type-C notebook, the CCG4 device provides negotiated power to the connected USB pen drive from the Type-C power adapter. In this scenario, Type-C port 1 of the CCG4-enabled notebook is a power consumer and Type-C port 2 is a power provider.

Figure 49. Switching Between Power Provider and Power Consumer Roles of CCG4 Using CY4541 EZ-PD CCG4 EVK (Example 2)



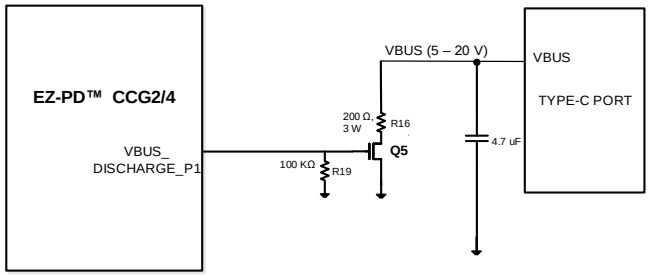
The Type-C power adapter and a USB pen drive can be interchanged between Type-C port 1 and Type-C port 2 as shown in Figure 49. In this scenario, Type-C port 1 of the CCG4-enabled notebook provides power to the USB pen drive and Type-C port 2 consumes power from the Type-C power adapter. In this scenario, Type-C port 1 of the CCG4-enabled notebook is a power provider and Type-C port 2 is a power consumer. This demonstrates that CCG4 can switch its power role from provider to consumer and vice-versa.

10.4.2 Control of VBUS Discharge Path

This section explains the critical need of the VBUS discharge circuitry. Depending on the connected downstream device, the VBUS voltage varies as illustrated by the following example scenarios:

- Example Scenario 1: A UFP device sinking 100 W of power (20 V, 5 A) is disconnected from a Type-C port, and immediately another UFP device sinking 25 W of power (5 V, 5 A) is connected to the same Type-C port.
- Example Scenario 2: A notebook changes its power role from provider (sourcing 100 W of power) to consumer (sinking 45 W of power).

Figure 50. VBUS Discharge Control Circuitry



In Scenario 1, the VBUS capacitor shown in Figure 50 may not have discharged fully from the original 20 V when the second UFP device is connected. This could cause an overvoltage on the second UFP device, which requires 5 V on VBUS.

In Scenario 2, a similar overvoltage could occur when the power role is swapped. To prevent this scenario, the CCG2/CCG4 device provides a discharge path to the VBUS capacitor by triggering the VBUS Discharge pin. VBUS Discharge is an active HIGH signal, which turns ON FET Q5 causing a discharge of the VBUS capacitor through a resistor as shown in Figure 50. It is necessary to use a series resistor (200 Ω) with a minimum 2.5-W power rating, as the power dissipation during VBUS discharge is high.

VBUS discharge circuitry is implemented in CY4541 the CCG4 EVK as shown in Figure 50. See CY4541 EZ-PD CCG4 Daughter Board schematics for details.

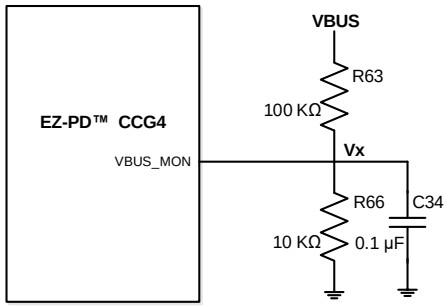
10.4.3 Overvoltage Protection (OVP) for VBUS

Overvoltage Protection (OVP) circuitry is required on VBUS to prevent damage to the system if VBUS exceeds the maximum voltage negotiated by the CCG2/CCG4 controller.

OVP for CCG4:

Figure 51 shows the external circuitry required to monitor the VBUS in a notebook design using CCG4.

Figure 51. OVP/UVP Circuitry



Per the USB PD specification, the maximum voltage at VBUS can be 20 V. Table 17 provides the value of voltage V_X (shown in Figure 51) and OVP trip voltage (1.2 times V_x) for the possible VBUS voltages.

Table 17. Values of Vx Voltage at Different VBUS Voltages

VBUS Voltage (V)	V_X Voltage (V)	OVP Trip Voltage (V)
4	0.363	0.435
5	0.454	0.544
9	0.818	0.981
15	1.363	1.635
20	1.818	2.181

A CCG4 device has a built-in comparator. The VBUS_MON pin is an input to the comparator as shown in Figure 51. CCG4 device's firmware configures the OVP trip voltage for the respective negotiated VBUS voltage (defined in Table 17) as the second input of the comparator. The comparator compares the Vx voltage with OVP trip voltage for the respective VBUS voltage, as shown in Table 17. The capacitor (0.1 µF) on the VBUS_MON pin (Figure 51) acts as a low-pass filter and prevents glitches on the ADC input pin.

Consider a scenario in which the notebook and the DFP device connected to its Type-C port establish a power contract, and the notebook starts receiving 15 V of VBUS from the DFP. The voltage generated at the VBUS_MON pin would be 1.363 V, which is an input to the CCG4 device's comparator. The CCG4 device's firmware sets the OVP trip voltage to 1.635 V for the 15-V VBUS. The comparator compares this OVP trip voltage with the Vx voltage (1.363 V for the 15-V VBUS, as listed in Table 17). The output of the comparator is connected to one of the CCG4 device's fixed-function I/O, which is called the OVP trip pin (OVP_TRIP_P1) as shown in Figure 19. This pin becomes LOW in the overvoltage scenario (if Vx exceeds the OVP trip voltage), and the CCG4 device turns OFF the VBUS consumer path by turning OFF FETs Q2A and Q2B as shown in Figure 47. The CCG4 device also disconnects itself from the Type-C port.

The overvoltage protection feature is implemented in the CY4541 EZ-PD CCG4 EVK as shown in Figure 51. See CY4541 EZ-PD CCG4 EVK Daughter Board schematics for more details.

OVP for CCG2:

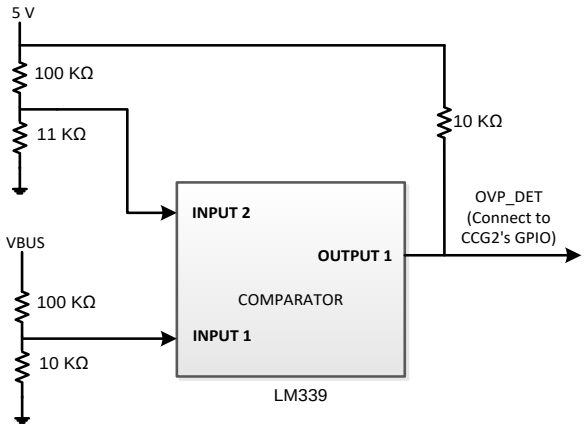
Figure 26 shows the implementation of OVP for the 5-V VBUS using a comparator IC (LM339) for CCG2. Input 1 of the comparator IC is the negotiated VBUS voltage through a resistor divider network. Per the circuit shown in Figure 52, this voltage is 0.454 V for the 5-V VBUS through the resistor divider network. Input 2 of the comparator IC is the OVP trip voltage, which is set based on the overvoltage limit of the system.

For example, a system may have an overvoltage limit of 5.5 V. Accordingly, the resistor divider circuit at input 2 terminal generates 0.5 V for 5.5 V VBUS, which gets compared with the voltage at input 1 terminal (0.454 V for 5 V VBUS) of the comparator IC. The 5 V voltage supply to the resistor divider circuitry at input 2 terminal is an output voltage of the 5 V V_{BAT} regulator in the system. V_{BAT} is the battery voltage, which comes from the internal battery in a notebook. The output of the comparator is connected to one of the CCG2's I/O, which is configurable in FW. See the firmware configuration and programming details on EZ-PD CCG2 Firmware webpage.

This I/O becomes LOW in the overvoltage scenario, and the CCG2 device turns OFF VBUS by turning OFF the power consumer FETs Q2A and Q2B as shown in Figure 47. The CCG2 also disconnects itself from the Type-C port.

The LM339 voltage comparator outputs a logic LOW or high-impedance (logic HIGH with pull-up) based on the input differential polarity. Thus, a 10-kΩ pull-up resistor needs to be connected on output terminal of LM339 comparator IC. See the LM339 datasheet for further details.

Figure 52. External Hardware Required for OVP



10.4.4 Undervoltage Protection (UVP) for VBUS

Undervoltage Protection (UVP) circuitry is required on VBUS to detect a Type-C disconnect event when a CCG2/CCG4-enabled notebook is consuming power from the DFP (such as a power adapter) or charging UFP (such as a monitor or external hard disk) over the Type-C interface.

UVP for CCG4:

Figure 51 shows the external RC circuitry required to implement this feature for VBUS in a notebook design using CCG4 (the same circuit as used for OVP). The voltage generated at the VBUS_MON pin is an input to two built-in CCG4 comparators, which facilitate both UVP and OVP at the same time. The first comparator is used for OVP whereas the second comparator is used for UVP. The CCG4 device's firmware configures the UVP trip voltage as the second input of the UVP comparator. Existing CCG4 FW implements UVP only for 5-V VBUS. The UVP trip voltage for 5-V VBUS is set to 4 V (0.8 times VBUS).

Consider a scenario in which the notebook and the DFP device connected to its Type-C port establish a power contract, and the notebook starts receiving 5 V of VBUS from the DFP. The voltage generated at the VBUS_MON pin would be 0.454 V (Vx, as defined in Table 17), which is the first input to the CCG4 device's UVP comparator. The CCG4 device's firmware has set the VBUS undervoltage detection threshold to 4 V. The value of Vx for 4-V VBUS would be 0.363 V (as defined in Table 17), which is configured by the CCG4 device's firmware as the UVP trip voltage. This UVP trip voltage is the second input to the UVP comparator. The UVP comparator compares this UVP trip voltage (0.363 V) with the Vx voltage for the 5-V VBUS (0.454 V, as listed in Table 17). The output of the comparator is connected to one of the CCG4's device's fixed-function I/Os, which is called the VBUS_C_CTRL_P1 pin as shown in Figure 47. This I/O becomes LOW in the undervoltage scenario (if VBUS goes below 4 V), and the CCG4 device turns OFF the VBUS consumer path by turning OFF FETs Q2A and Q2B as shown in Figure 47. The CCG4 device also disconnects itself from the Type-C port.

The capacitor (0.1 µF) on the VBUS_MON pin (Figure 51) acts as a low-pass filter and prevents glitches on the ADC input pin. The undervoltage detection feature is implemented in the CY4541 EZ-PD CCG4 EVK as shown in Figure 51. See CY4541 EZ-PD CCG4 EVK Daughter Board schematics for more details.

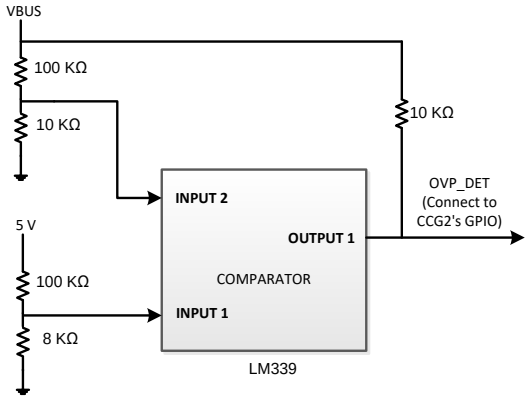
UVP for CCG2:

Figure 53 shows the implementation of UVP using a comparator IC (LM339) for CCG2. Input 2 of the comparator IC is the negotiated Type-C VBUS voltage through a resistor divider network. Existing CCG2 FW implements UVP only for 5-V VBUS. Per the circuit shown in Figure 53, this voltage is 0.45 V for the 5-V VBUS through the resistor divider network. The CCG2 device's firmware has set the VBUS undervoltage detection threshold to 4 V. Input 1 of the comparator IC is the UVP trip voltage, which is 0.3636 V for the 4-V VBUS through a resistor divider network.

The 5-V supply to the resistor divider circuitry at input 2 terminal is an output voltage of the 5-V V_{BAT} regulator in a system. V_{BAT} is the battery voltage, which comes from the internal battery in a notebook design. The comparator IC compares this UVP trip voltage (0.3636 V for the 4-V VBUS) with the voltage at input 2 terminal (0.45 V for the 5-V VBUS). The output of the comparator is connected to one of the CCG2's I/Os, which is configurable in firmware. See the firmware configuration and programming details on EZ-PD CCG2 Firmware webpage. This I/O becomes LOW in the undervoltage scenario, and the CCG2 device turns OFF VBUS by turning OFF power consumer FETs Q2A and Q2B as shown in Figure 47. The CCG2 device also disconnects itself from the Type-C port.

The LM339 voltage comparator outputs a logic LOW or high-impedance (logic HIGH with pull-up) based on the input differential polarity. Thus, a 10-kΩ pull-up resistor needs to be connected on output terminal of the LM339 comparator IC. See the LM339 datasheet for further details.

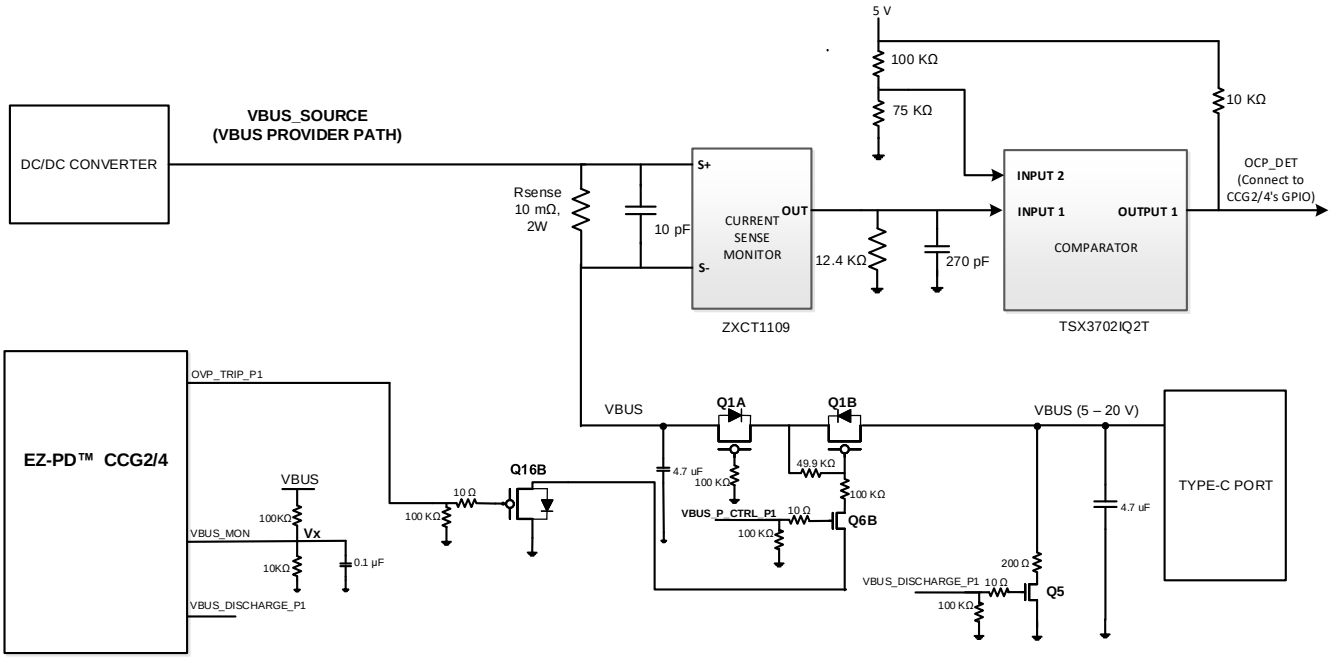
Figure 53. External Hardware Required for UVP



10.4.5 Overcurrent Protection (OCP) for VBUS

Overcurrent protection (OCP) circuitry is required on VBUS to prevent damage to the system if the VBUS current exceeds the maximum current negotiated by the CCG2/CCG4 controller. Figure 54 shows the external components (current sense monitor and comparator) required to implement OCP for VBUS in a notebook design using CCG2/CCG4. See Overcurrent Protection (OCP) for VBUS for OCP implementation in CCG3.

Figure 54. OCP Circuitry



The Rsense resistor connected between the S+ and S- terminals of the current sense monitor IC converts the current through the Rsense resistor into a voltage to be measured by the comparator. The comparator IC compares the output voltage from the current sense monitor IC with the reference voltage set using resistor divider circuitry at input 2 terminal. This reference voltage is set based upon the OCP limit of the system. The circuit shown in Figure 54 has set the OCP to 5.35 A with 100-kΩ and 75-kΩ resistor divider circuitry at input 2 terminal. See the respective datasheet of the comparator to choose the appropriate resistor and capacitor values, which define the reference voltage and OCP current limit. The 5-V supply to the resistor divider circuitry at input 2 terminal is an output voltage of the 5-V V_{BAT} regulator in a system. V_{BAT} is the battery voltage, which comes from the internal battery in a notebook.

The output of the comparator is connected to one of the CCG2/CCG4's I/Os, which is configurable in firmware. For CCG4, this is a fixed-function I/O, which is called OCP_DET_P1. For CCG2, see the firmware configuration and programming details on EZ-PD CCG2 Firmware webpage. This I/O becomes LOW in the overcurrent scenario and the CCG2/CCG4 device turns OFF the VBUS by turning OFF power provider FETs Q1A and Q1B as shown in Figure 47. The CCG2/CCG4 also disconnects itself from the Type-C port.

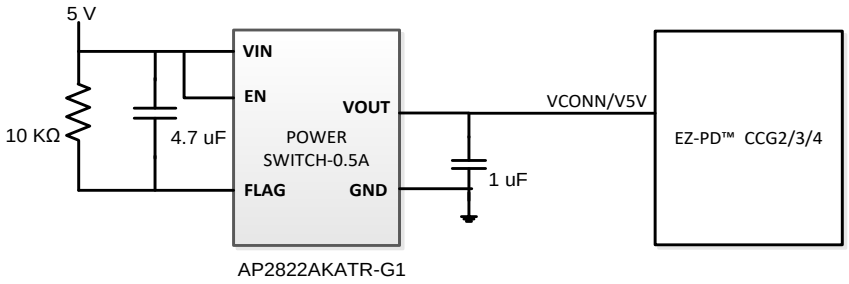
Figure 54 shows a reference schematic of the OCP circuitry using a current sense monitor IC (ZXCT1109) and a comparator (TSX3702IQ2T). The voltage comparator outputs a logic LOW or high-impedance (logic HIGH with pull-up) based on the input differential polarity. Thus, a pull-up resistor needs to be connected on output terminal of the voltage comparator IC. See the datasheet of current sense monitor IC and voltage comparator for further details.

The overcurrent protection feature on the CCG4 daughter card is implemented using current a sense monitor IC (ZXCT1109) and comparator (TSX3702IQ2T) as shown in Figure 54. See the CY4541 EZ-PD CCG4 EVK Daughter Board schematic for more details.

10.4.6 Overcurrent Protection (OCP) for VCONN

In a notebook design, VCONN supplies power to the electronically marked cable attached to it. VCONN FETs on the CC lines can handle a current up to 0.5 A. Overcurrent Protection (OCP) circuitry is required on VCONN to prevent damage to the system if VCONN current exceeds 0.5 A. Figure 55 shows the external components required to implement OCP for VCONN in a notebook design using CCG2/CCG3/CCG4.

Figure 55. OCP for VCONN



The VCONN power switch (AP2822AKATR-G1) has an overcurrent detection limit of 0.5 A. Output of the switch (VOUT) is connected to VCONN of CCG2/CCG3 or V5V_P1 or V5V_P2 of CCG4. The 5-V supply (VIN) to the VCONN power switch is an output voltage of the 5-V V_{BAT} regulator in a system. V_{BAT} is the battery voltage, which comes from the internal battery in a notebook. If VCONN current exceeds the overcurrent detection limit of 0.5 A, VOUT (5 V) power supply is shut down by the power switch, preventing any damage to the system. See the respective datasheet of the power switch to choose the appropriate resistor and capacitor values.

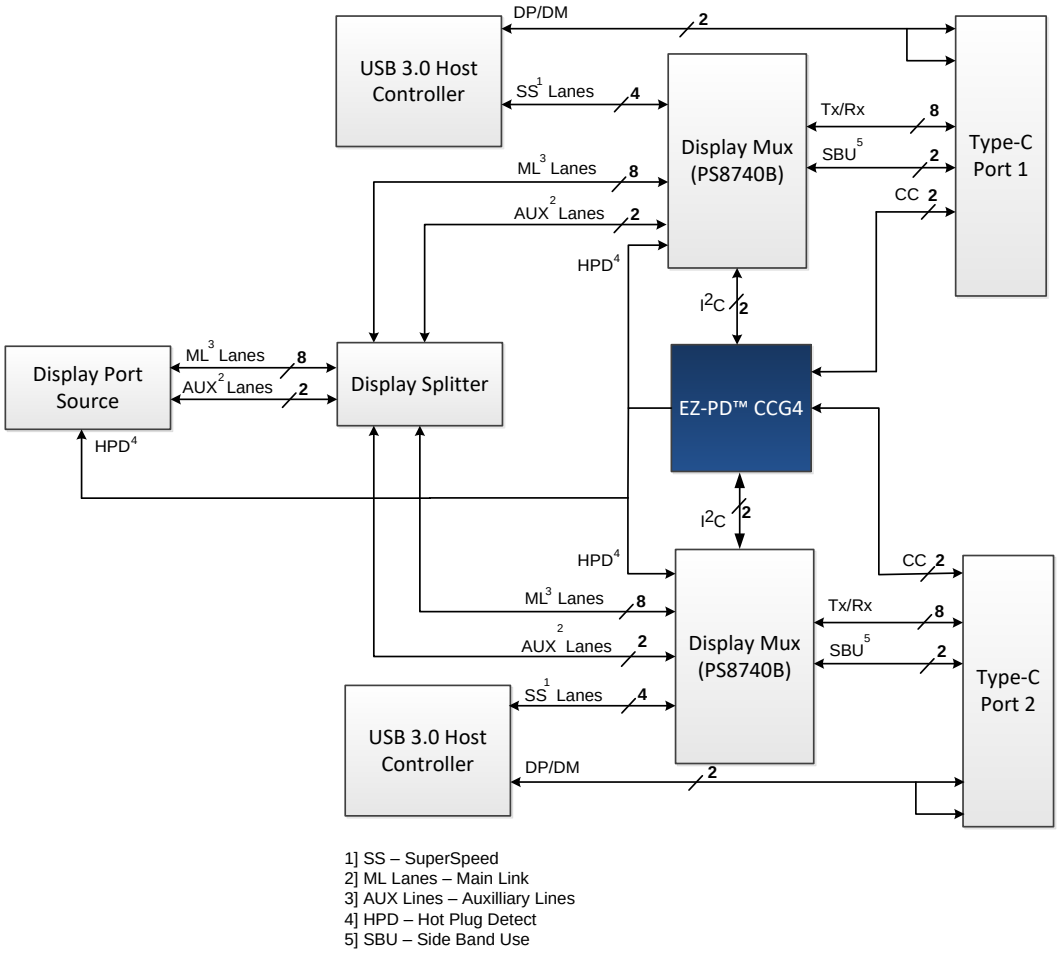
10.5 DisplayPort Connections

This section is applicable only to the dual Type-C port CCG4 controller (CY4225-40LQXIT) for notebook application.

Type-C is a versatile connector, which also supports DisplayPort signals by repurposing one of the SuperSpeed lanes and two sideband signals. These repurposed signals act in a new mode, called “alternate mode.” One example of using a Type-C interconnection in alternate mode is DisplayPort. See the VESA specification for more details on DisplayPort Alt Mode on the USB Type-C Standard.

In a Type-C notebook design, a display monitor can be connected directly to the notebook over the Type-C interface using a CCG4 and a display mux controller. Figure 56 shows the connections between CCG4 and two display mux controllers in a notebook design having two USB 3.0 Host controllers and one DisplayPort Source.

Figure 56. CCG4 and Dual Display Mux Controller Connections



1] SS – SuperSpeed
2] ML Lanes – Main Link
3] AUX Lines – Auxilliary Lines
4] HPD – Hot Plug Detect
5] SBU – Side Band Use

Whenever a display monitor is connected to the Type-C port on a notebook, CCG4 discovers that it has a device attached with alternate mode supported. Through PD communication, CCG4 identifies the display monitor's Standard ID (SID) or Vendor ID (VID) (so SVID = SID or VID). The display monitor reports an SVID of 0xFF01 (per the VESA specification), which is assigned to a DisplayPort connection.

CCG4 initiates an alternate mode sequence and asserts the Hot Plug Detect (HPD) signal to the DisplayPort source and display mux controller. The DisplayPort source detects that the display monitor is connected to the notebook. The display monitor can have two or four Main Link (DisplayPort) lanes. The 2-lane Main Link configuration supports a raw bit rate up to 10.8 Gbps, and the 4-lane Main Link configuration supports a raw bit rate up to 21.6 Gbps.

CCG4 checks the DisplayPort status, and if it receives an ACK, CCG4 configures the display mux controller in either 2-lane or 4-lane mode. CCG4 communicates with the display mux controller either over the I^2C interface (such as the display mux controller from Parade, PS8740B) or over a GPIO interface (such as the display mux controller from Pericom, PI3DBS12412AZHE), depending on the type of display mux controller used in the system. See the respective mux controller's datasheet for more details.

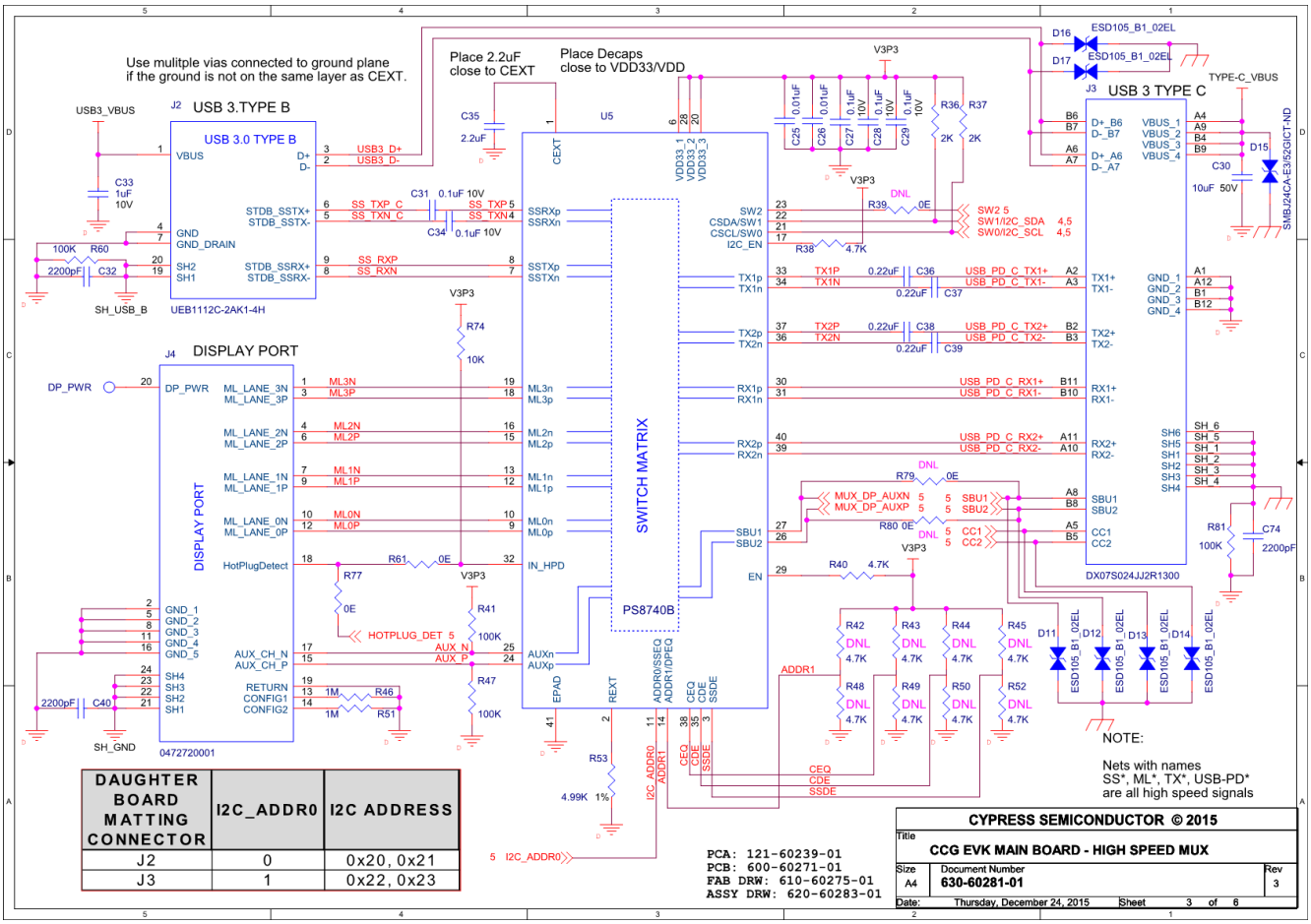
The display mux controller switches its output lines (TX/RX) between the USB SuperSpeed lanes and the Main Link (DisplayPort) lanes from the DisplayPort source.

Consider a scenario in which a 4-lane display monitor is connected to the notebook, and no other USB 3.0 device is connected. In this case, the display mux controller connects four Main Link (DisplayPort) lanes to the Type-C port, and the display appears on the screen. Now, if a USB 3.0 device is connected to the notebook, it enumerates as a USB 2.0 device because all the SuperSpeed lanes on the Type-C port are repurposed as DisplayPort lanes. USB 2.0 enumeration occurs because USB 2.0 (DP/DM) lines are directly connected from the USB Host controller to the Type-C port.

The USB Host controller detects the presence of the SuperSpeed device (enumerated as a USB 2.0 device) and communicates it to the EC. The system may decide to switch from 4-lane to 2-lane display to enable SuperSpeed device enumeration or it may continue to be in 4-lane mode. This is implementation-specific. If the system wants to switch to 2-lane mode, the EC sends a message to CCG4 to reconfigure the display mux controller from 4-lane to 2-lane display mode to enable connection of the USB SuperSpeed lane to the Type-C port. Now, the display appears on the monitor, and the USB 3.0 device is detected as a SuperSpeed device. Note that the display monitor's resolution in the 2-lane mode will be lower than in the 4-lane mode. The Type-C port also receives auxiliary signals from the DisplayPort Source through the display mux controller that carry either the audio signals or the control signals for display.

The recommended part for display mux controller with redriver circuitry is from Parade Technologies (PS8740B), which compensates for the PC board, connector, and cable losses and maintains signal quality by adjusting the gain of the redriver circuitry. See the datasheet of mux controller to learn more about the configuration of controller. Figure 57 shows the connections between Display mux controller, DisplayPort Source, Type-C port and USB host in the CY4541 EZ-PD CCG4 EVK schematic. Refer to the CY4541 CCG EVK Base Board schematics for details.

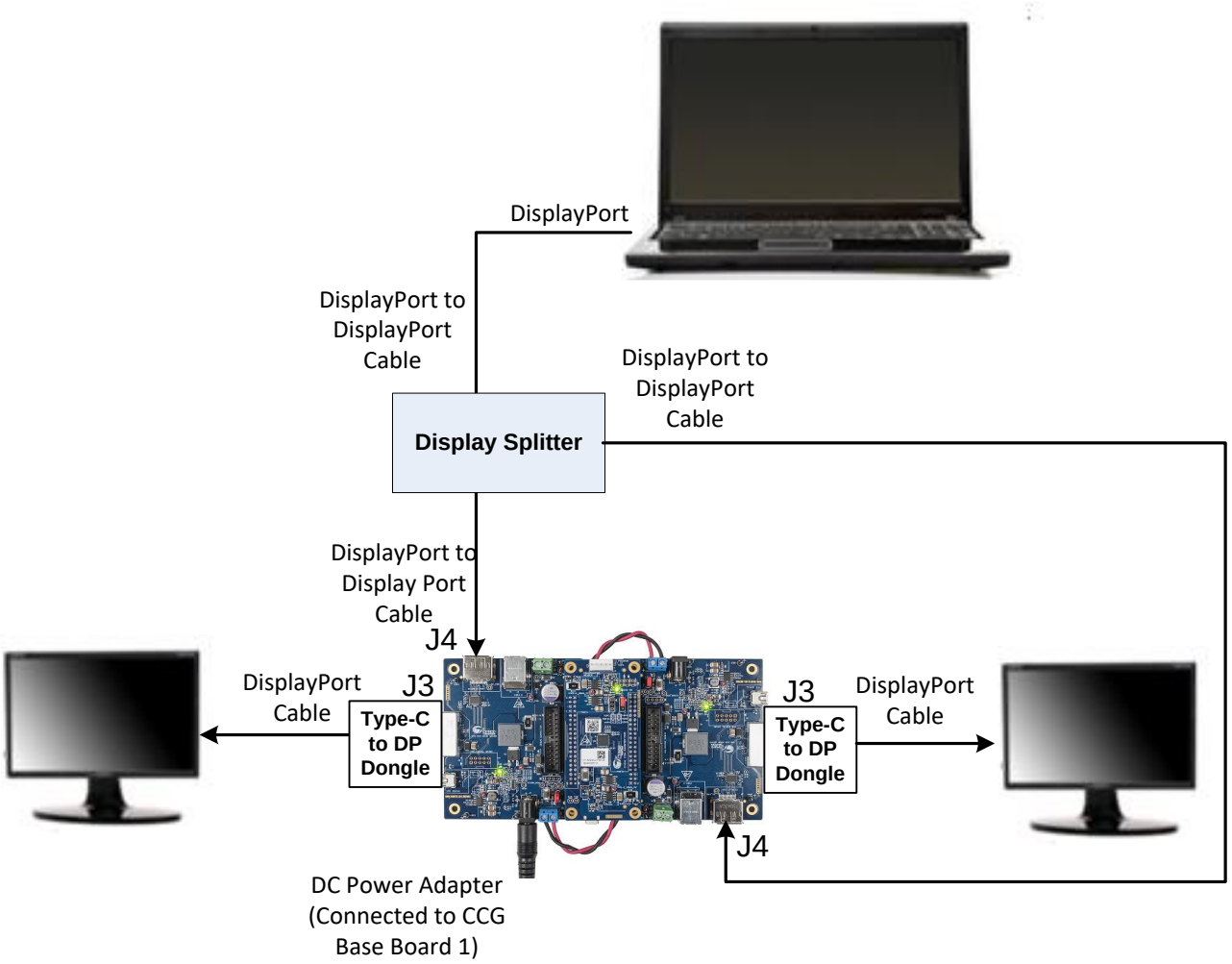
Figure 57. DisplayPort Connections in CY4541 EZ-PD CCG4 EVK Schematic



DAUGHTER BOARD MATTING CONNECTOR	I2C_ADDR0	I2C ADDRESS
J2	0	0x20, 0x21
J3	1	0x22, 0x23

Dual DisplayPort control of CCG4 can be demonstrated by using the CY4541 EZ-PD CCG4 EVK as shown in Figure 58. See Chapter 4 (DRP Kit Operation) of the CY4541 EZ-PD CCG4 EVK kit guide for details on hardware connections of this setup.

Figure 58. Dual DisplayPort Connection Demo Using CY4541 EZ-PD CCG4 EVK



The CY4541 EZ-PD CCG4 EVK along with a USB 3.0- and DisplayPort-enabled notebook or a PC emulates a CCG4-enabled Type-C notebook. In this scenario, the DP splitter receives DisplayPort signals from a notebook or a PC having a DisplayPort interface. A DP splitter performs internal demultiplexing of DisplayPort signals and routes these signals to both the DisplayPorts (J4) of the CCG baseboards as shown in Figure 56. CCG4 delivers DisplayPort video from the host (notebook or PC) to the Display monitors connected to both Type-C port 1 and Type-C port 2 using the onboard display mux controllers and Type-C to DP dongles. This demonstrates the CCG4's capability to control two Display Ports simultaneously. See the CY4541 EZ-PD CCG4 EVK kit guide for recommended Display splitter boards.

10.6 Electrical Design Considerations

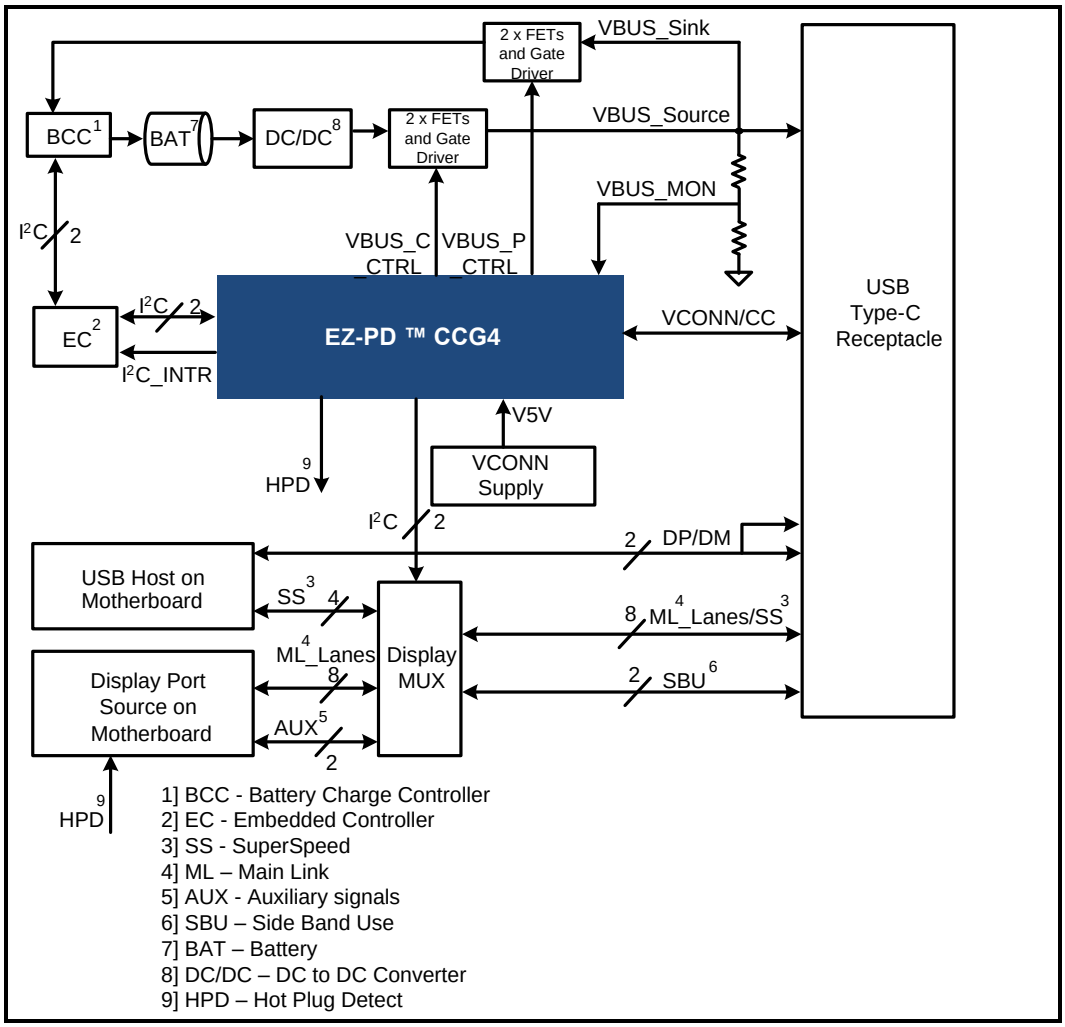
See Electrical Design Considerations for more details.

11 Single Type-C Port DRP Application Using CCG4

A CYPD4125-40LQXIT CCG4 controller is used here as the reference.

This section describes the design of a typical single Type-C port DRP application, such as a Type-C notebook, using the EZ-PD CCG4 controller. Figure 59 shows the logical connections between the CCG4 and the components in a notebook. This design is similar to the dual Type-C port application discussed in Dual Type-C port DRP application using CCG4.

Figure 59. Single Type-C Port Notebook Design Using CCG4



The following are the critical sections of this Type-C notebook design using CCG4 are described below:

- Power Supply Design
- Dead Battery Charging
- Power Provider/Consumer
- DisplayPort Connection
- Electrical Design Considerations

11.1 Power Supply Design

See Power Supply Design.

11.2 I²C Communication with Embedded Controller

See I²C Communication with Embedded Controller.

11.3 Dead Battery Charging

See Dead Battery Charging.

11.4 Power Provider/Consumer Role

See Power Provider/Consumer Role.

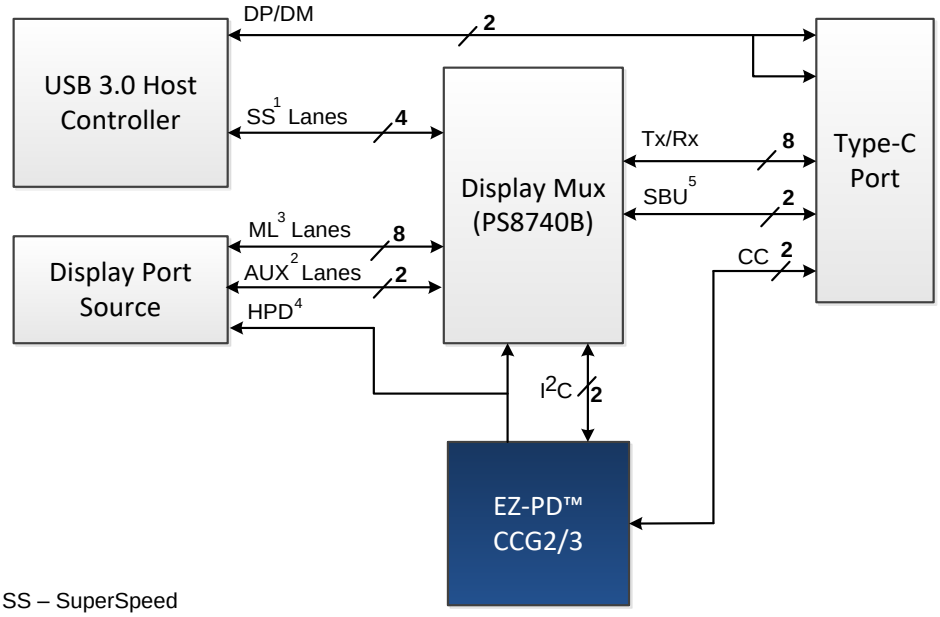
11.5 DisplayPort Connections

This section is applicable to CCG2, CCG3 and CCG4 (only single Type-C port CCG4 controller, CY4125-40LQXIT).

Type-C is a versatile connector, which also supports DisplayPort signals by repurposing one of the SuperSpeed lanes and two sideband signals. These repurposed signals act in a new mode, called an “alternate mode.” One example of using a Type-C interconnection in the alternate mode is DisplayPort. See the VESA specification for more details on the DisplayPort Alt Mode on the USB Type-C Standard.

In a Type-C notebook design, a display monitor can be connected directly to the notebook over the Type-C interface using CCG2/CCG3/CCG4 and a display mux controller. Figure 60 shows the connections between CCG2/CCG3/CCG4 and the display mux controller in a notebook design.

Figure 60. CCG2/CCG3/CCG4 and Display Mux Controller Connections



1] SS – SuperSpeed
2] ML Lanes – Main Link
3] AUX Lines – Auxilliary Lines
4] HPD – Hot Plug Detect
5] SBU – Side Band Use

Whenever a display monitor is connected to the Type-C port on a notebook, the CCG2/CCG3/CCG4device discovers that it has a device attached with alternate mode supported. Through PD communication, the CCG2/CCG3/CCG4 device identifies the display monitor’s Standard ID (SID) or Vendor ID (VID) (so SVID = SID or VID). The display monitor reports an SVID of 0xFF01 (per the Type-C specification), which is assigned to a DisplayPort connection.

The CCG2/CCG3/CCG4 device initiates an alternate mode sequence and asserts the Hot Plug Detect (HPD) signal to the DisplayPort source and display mux controller. The DisplayPort source detects that the display monitor is connected to the notebook. The display monitor can have two or four Main Link (DisplayPort) lanes. The 2-lane Main Link configuration supports a raw bit rate up to 10.8 Gbps, and the 4-lane Main Link configuration supports a raw bit rate up to 21.6 Gbps.

The CCG2/CCG3/CCG4 device checks the DisplayPort status, and if it receives an ACK, the CCG2/CCG3/CCG4 device configures the display mux controller in either 2-lane or 4-lane mode. The CCG2/CCG3/CCG4 device communicates with the display mux controller either over an I^2C interface (such as the display mux controller from Parade, PS8740B) or over a GPIO interface (such as the display mux controller from Pericom, PI3DBS12412AZHE), depending on the type of display mux controller used in the system. See the respective mux controller's datasheet for more details.

The display mux controller switches its output lines (TX/RX) between the USB SuperSpeed lanes and the Main Link (DisplayPort) lanes from the DisplayPort source.

Consider a scenario in which a 4-lane display monitor is connected to the notebook, and no other USB 3.0 device is connected. In this case, the display mux controller connects four Main Link (DisplayPort) lanes to the Type-C port, and a display appears on the screen. Now, if a USB 3.0 device is connected to the notebook, it enumerates as a USB 2.0 device because all the SuperSpeed lanes on the Type-C port are repurposed as DisplayPort lanes. The USB 2.0 enumeration occurs because the USB 2.0 (DP/DM) lines are directly connected from the USB Host controller to the Type-C port.

The USB Host controller detects the presence of the SuperSpeed device (enumerated as a USB 2.0 device) and communicates it to the EC. The system may decide to switch from 4-lane to 2-lane mode to enable SuperSpeed device enumeration or it may continue to be in 4-lane mode. This is implementation-specific. If the system wants to switch to 2-lane mode, the EC sends a message to the CCG2/CCG3/CCG4 device to reconfigure the display mux controller from 4-lane to 2-lane display mode to enable connection of the USB SuperSpeed lane to the Type-C port. Now, the display appears on the monitor, and the USB 3.0 device is detected as a SuperSpeed device. Note that the display monitor's resolution in the 2-lane mode will be lower than in the 4-lane mode. The Type-C port also receives auxiliary signals from the DisplayPort source through the display mux controller that carry either the audio signals or the control signals for the display.

The recommended part for display mux controller with redriver circuitry is from Parade Technologies (PS8740B), which compensates for the PC board, connector, and cable losses and maintains signal quality by adjusting the gain of the redriver circuitry. See the datasheet of mux controller to learn more about the configuration of controller.

11.6 Electrical Design Considerations

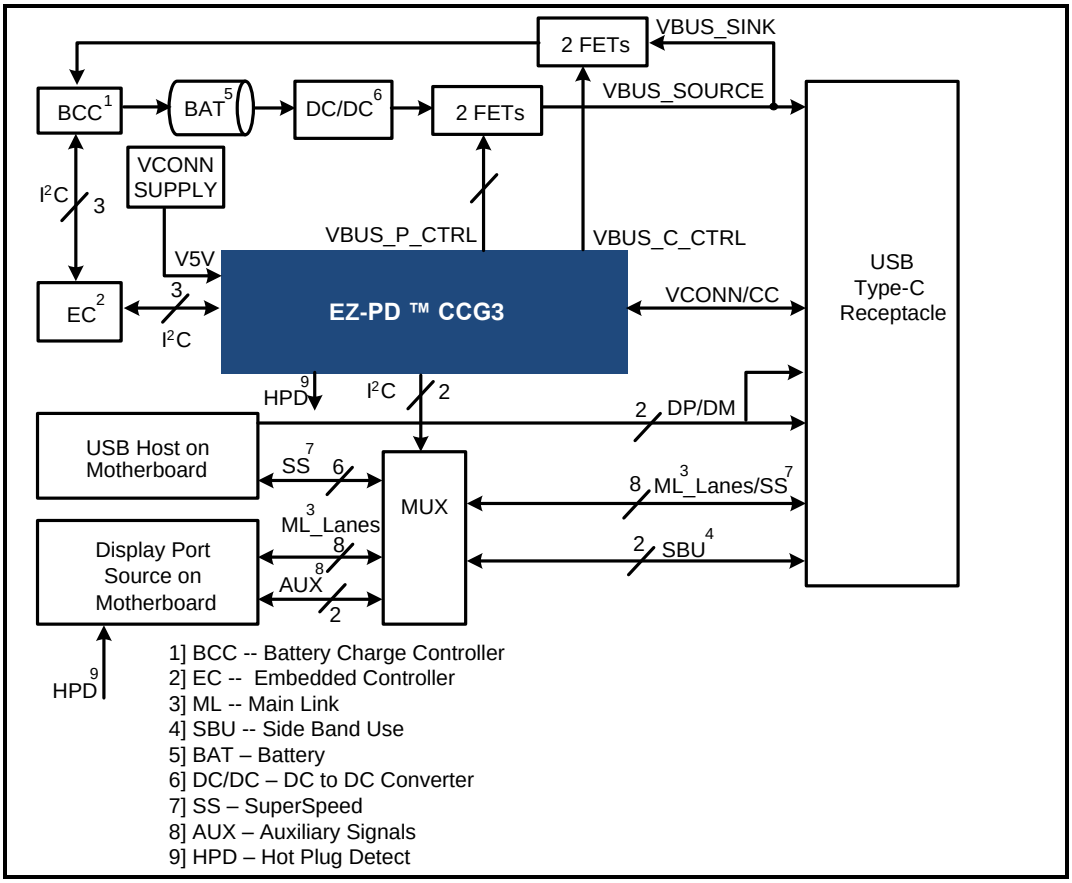
See Electrical Design Considerations.

12 Single Type-C Port DRP Application Using CCG3

A CYPD3125-40LQXIT CCG3 controller is used here as the reference.

CCG3 includes integrated 20-V VBUS NFET/PFET gate drivers, VCONN FETs, VBUS Discharge FETs, OVP, and OCP, which facilitate the single-port Type-C notebook design with a reduced BOM compared to EZ-PD CCG2. Figure 61 shows the logical connections between CCG3 and the components in a notebook design.

Figure 61. Single Type-C Port Notebook Design Using CCG3



The following are the critical sections of this Type-C notebook design using CCG3:

- Power Supply Design
- I²C Communication with Embedded Controller
- Dead Battery Charging
- Power Provider/Consumer Role
- DisplayPort Connection
- Electrical Design Considerations

12.1 Power Supply Design

Cypress' Type-C PD Controller CCG3 operates with two possible external supply voltages, VBUS or VSYS as referred in Table 18. The VBUS supply is regulated inside the chip with a low-dropout regulator (LDO). The chip's internal VDDD rail is intelligently switched between the output of the VBUS regulator and unregulated VSYS. The switched supply, VDDD is either used directly inside some analog blocks or further regulated down to VCCD which powers the majority of the core using regulators as shown in Figure 62. VCCD is the output voltage from the core regulator and this pin is intended to connect only a decoupling capacitor. The VCCD pin cannot be used as a voltage source. CCG3 has the power supply input VCONN pin for providing power to electronically marked cables through integrated VCONN FETs. There is a VCONN FET in CCG3 to power the CC1 and CC2 pins. This FET can provide a maximum of 500-mA current on the CC1 and CC2 pins for EMCA cables.

Figure 62. CCG3 Power Subsystem

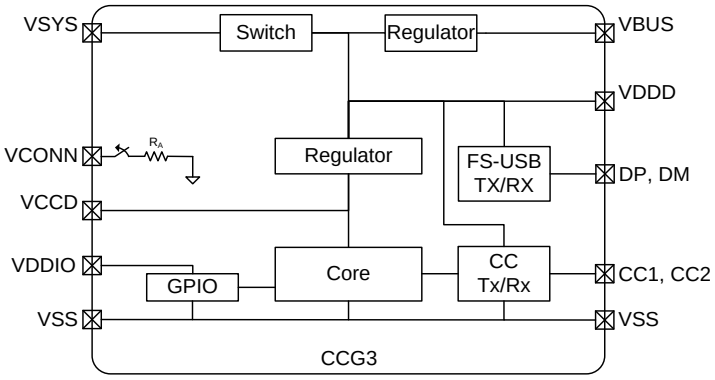


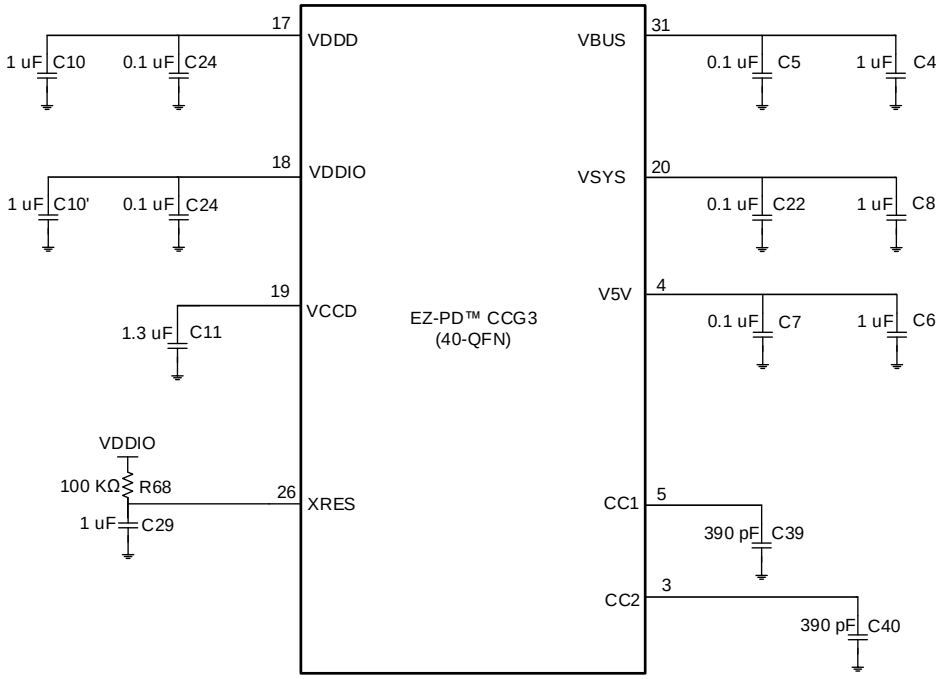
Table 18. CCG3 Operating Voltage Range

Parameter	Min (V)	Typ (V)	Max (V)
VBUS	4	–	21.5
VSYS	4.5	–	5.5
VCONN	2.7	–	5.5
VDDD	2.7		5.5
VDDIO	1.71	1.80	VDDD

12.1.1 Noise Suppression Using Decoupling Capacitors

Power supply noise can be suppressed by using decoupling capacitors to power supply pins VBUS, VSYS, VDDD, VDDIO, VCCD, and VCONN pins as shown in Figure 63. A 390-pF decoupling capacitor should be connected to CC lines (CC1, CC2) to maintain the signal quality at the signaling rate of 300 kHz.

Figure 63. Noise Suppression Using Decoupling Capacitors



12.1.2 Reset and Clock Circuit

CCG3 supports a power-on-reset (POR) mechanism and it also has an active LOW external reset (XRES) pin. The XRES (active LOW) pin can be used by external devices to reset the CCG3. The XRES pin should be held LOW for a minimum of 1us to reset the CCG3. This XRES pin should be tied through an RC circuit as shown in Figure 63 .The recommended values for R and C are 100 kΩ and 1 µF respectively to meet the 1-µs pulse-width requirement.

CCG3 has integrated clock circuitry and any external components such as crystal or oscillator are not required.

12.2 I²C Communication with Embedded Controller

This section is applicable to CCG3. See I²C Communication with Embedded Controller.

12.3 Dead Battery Charging

This section is applicable to CCG3. See Dead Battery Charging.

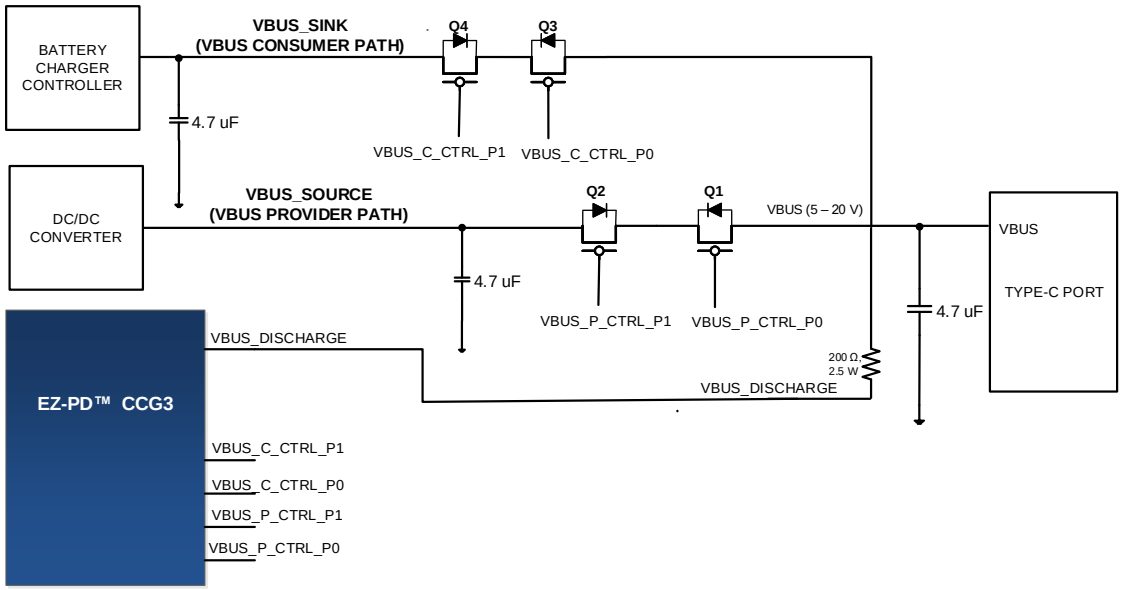
12.4 Power Provider/Consumer Role

This section is applicable to CCG3.

A notebook design using CCG3 (with DRP capabilities) will be a power provider when running from its internal battery and a power consumer when being charged from the DFP (or a charging UFP such as a power adapter, monitor, or any external power provider such as a hard disk).

A BCC controls the charging (sinking of VBUS) or discharging (sourcing of VBUS) of the battery. CCG3 consists of gate drivers and four I/Os, namely VBUS_P_CTRL_P1, VBUS_P_CTRL_P0, VBUS_C_CTRL_P1, and VBUS_C_CTRL_P0, to control the VBUS provider or consumer path connected to the BCC. Figure 64 shows the recommended implementation of FETs to control this VBUS path.

Figure 64. VBUS Provider and Consumer Path Control Circuitry



VBUS_P_CTRL_P1 and VBUS_P_CTRL_P0 are active HIGH pins. FETs Q1 and Q2 turn ON when both the pins are HIGH. This turns ON the VBUS provider path. Similarly, when VBUS_C_CTRL_P1 and VBUS_C_CTRL_P0 are HIGH, FETs Q3 and Q4 turn ON, which turns ON the VBUS consumer path.

The diodes between the source and drain terminals of FETs Q1 and Q2 turn OFF the VBUS provider path completely when the VBUS consumer path is active. Similarly, the diodes between the source and drain terminals of FETs Q3 and Q3 turn OFF the VBUS consumer path completely when the VBUS provider path is active.

12.4.1 Control of VBUS Discharge Path

Depending on the connected downstream device, the VBUS voltage varies, as illustrated by the following example scenarios:

- Example Scenario 1: A UFP device sinking 100 W of power (20 V, 5 A) is disconnected from the Type-C port and immediately another UFP device sinking 25 W of power (5 V, 5 A) is connected to the same Type-C port.
- Example Scenario 2: A notebook changes its power role from provider (sourcing 100 W of power) to consumer (sinking 45 W of power).

In Scenario 1, the VBUS capacitor shown in Figure 64 may not have discharged fully from the original 20 V when the second UFP device was connected. This could cause an overvoltage on the second UFP device, which requires 5 V on VBUS.

In Scenario 2, a similar overvoltage could occur when the power role is swapped. To prevent this scenario, CCG3 provides a discharge path to the VBUS capacitor by triggering the VBUS Discharge pin. VBUS Discharge is an active HIGH signal, which turns ON the integrated VBUS discharge FET in CCG3, causing a discharge of the VBUS capacitor through a resistor, as shown in Figure 64. It is necessary to use a series resistor (200 Ω) with a minimum 2.5-W power rating because the power dissipation during VBUS discharge will be high.

12.4.2 Overvoltage Protection (OVP) for VBUS

CCG3 includes integrated OVP circuits to sense overvoltage conditions on VBUS.

Consider a scenario in which the notebook and the DFP device connected to its Type-C port establish the power contract, and the notebook starts receiving 13 V of VBUS from the DFP. Once the power contract is established for a 13-V VBUS, CCG3 device's firmware configures the OVP trip voltage, which is 1.2 times the negotiated VBUS voltage. If the VBUS voltage exceeds the OVP trip voltage, CCG3 detects the overvoltage at VBUS and turns OFF the VBUS from the external power supply. CCG3 also turns OFF power consumer FETs Q3 and Q4 as shown in Figure 64 and disconnects itself from the Type-C port.

12.4.3 Undervoltage Protection (UVP) for VBUS

Undervoltage Protection (UVP) circuitry is required on VBUS to detect Type-C disconnect events when CCG3-enabled notebook is consuming power from the DFP (such as a power adapter) or charging UFP (such as a monitor or an external hard disk) over Type-C interface. CCG3 includes integrated UVP circuits to sense undervoltage conditions on VBUS.

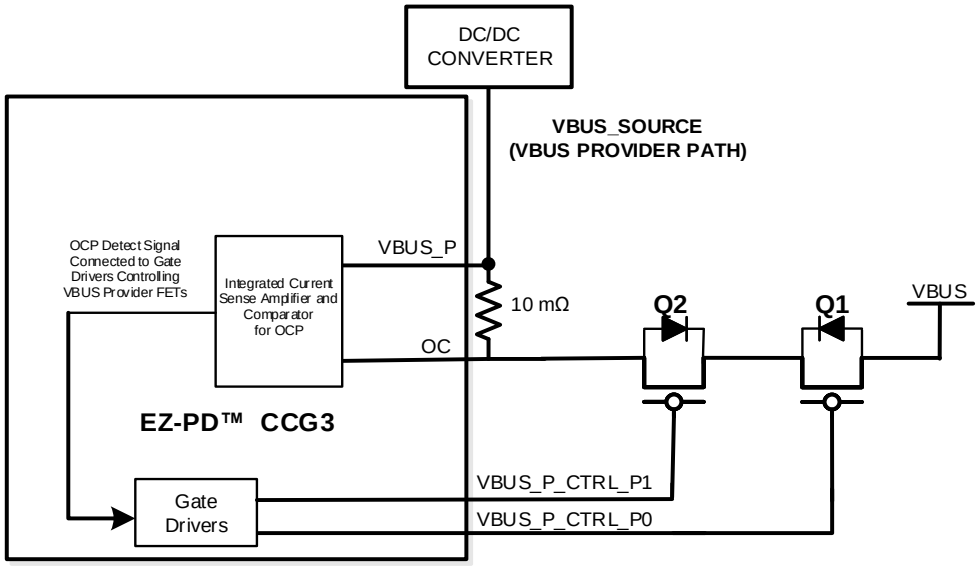
Consider a scenario in which the notebook and the DFP device connected to its Type-C port establish the power contract, and the notebook starts receiving 5 V of VBUS from the DFP. The CCG3 device has set undervoltage detection threshold to 4 V in its firmware. If the VBUS voltage goes below 4 V, then CCG3 detects the undervoltage at VBUS and turns OFF VBUS from the external power supply. CCG3 also turns OFF power consumer FETs Q3 and Q4 as shown in Figure 64 and disconnects itself from the Type-C port.

12.4.4 Overcurrent Protection (OCP) for VBUS

CCG3 includes integrated OCP circuits to sense overcurrent conditions on VBUS. Consider a scenario in which the notebook and the UFP device connected to its Type-C port establish the power contract, and the notebook starts providing 5 A of VBUS current to the UFP. Once the power contract is established for 5 A of VBUS, CCG3 device's firmware configures the OCP trip current, which can be set to 1.2 times the negotiated VBUS current. If the VBUS current exceeds the OCP trip current (for example, due to a hardware fault in the UFP device), CCG3 detects the overcurrent at VBUS and turns OFF the VBUS by turning OFF gate drivers to turn OFF power provider FETs Q1 and Q2. CCG3 also disconnects itself from the Type-C port.

The OC pin is the overcurrent sensor input pin to CCG3. This pin is connected to the VBUS_P pin of CCG3 through a 10-mΩ resistor to sense the input current, as shown in Figure 65.

Figure 65. OCP Circuitry



12.4.5 Overcurrent Protection (OCP) for VCONN

See Overcurrent Protection (OCP) for VCONN.

12.5 DisplayPort Connections

This section is applicable to CCG3. See DisplayPort Connections.

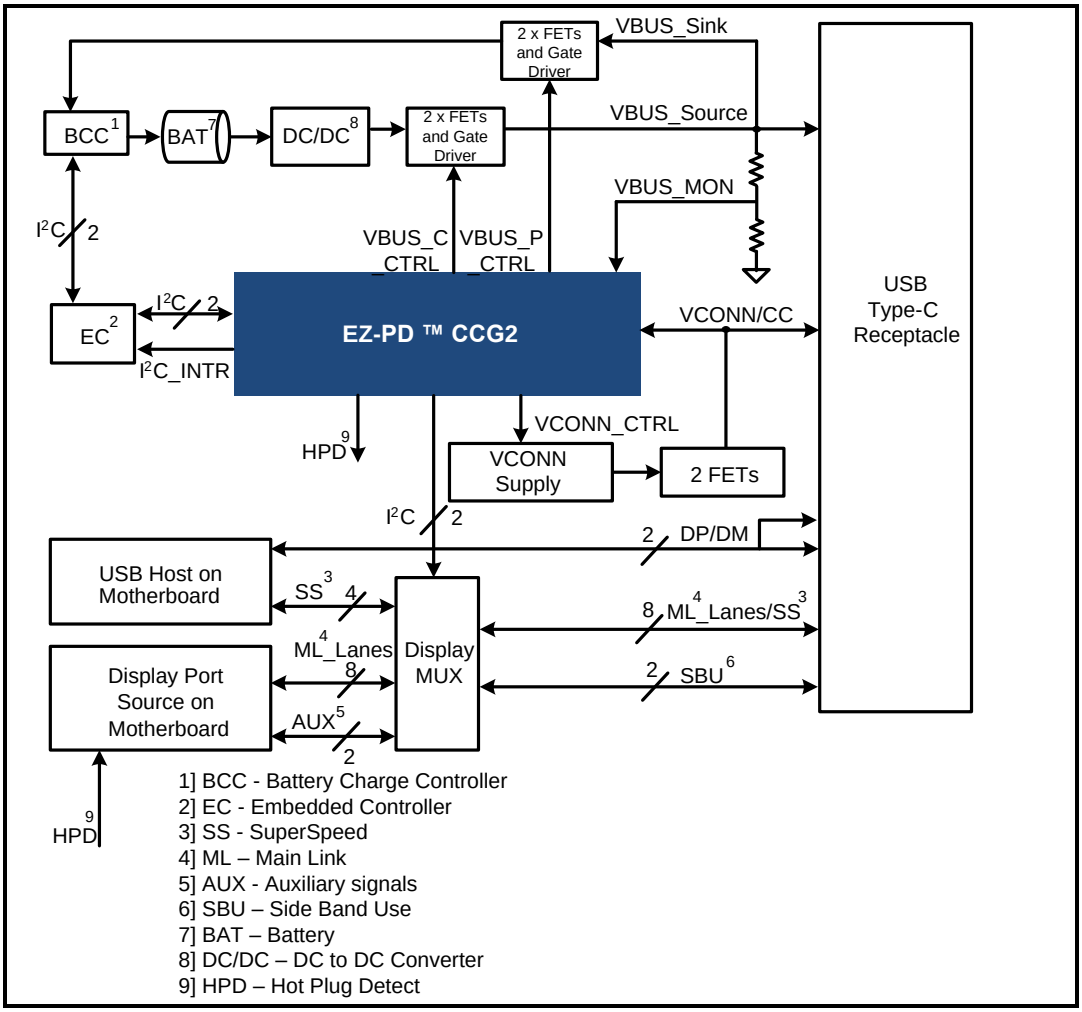
12.6 Electrical Design Considerations

See Electrical Design Considerations.

13 Single Type-C Port DRP Application Using CCG2

This section describes the design of a typical single Type-C port DRP application, such as a Type-C notebook, using CCG2 Type-C PD Controller (CYPD2122-24LQXIT). Figure 66 shows the logical connections between CCG2 and the components in a notebook.

Figure 66. Single Type-C Port Notebook Design Using CCG2



The following are the critical sections of this Type-C notebook design using CCG2:

- Power Supply Design
- I²C Communication with Embedded Controller
- Dead Battery Charging
- Power Provider/Consumer
- DisplayPort Connection
- Electrical Design Considerations

13.1 Power Supply Design

Cypress' Type-C PD Controller CCG2 operates with two supply voltages; the first voltage supply, VDDD, powers the device core and two Type-C transceivers. The other supply, VDDIO, powers the device I/Os as referred in Table 19. CCG2 has an integrated voltage regulator as shown in Figure 67. The core regulator powers the core logic and VCCD is an output of the regulator. The VCCD pin is intended to connect only a decoupling capacitor. It cannot be used as a voltage source. CCG2 has power supply inputs VCONN1 and VCONN2, which can be used as connections to the VCONN pins on a Type-C plug of a cable or VCONN-powered accessory. CCG2 can be used in Electronically Marked Cable Applications (EMCA) with only one or both VCONN pins as power sources.

Figure 67. CCG2 Power Subsystem

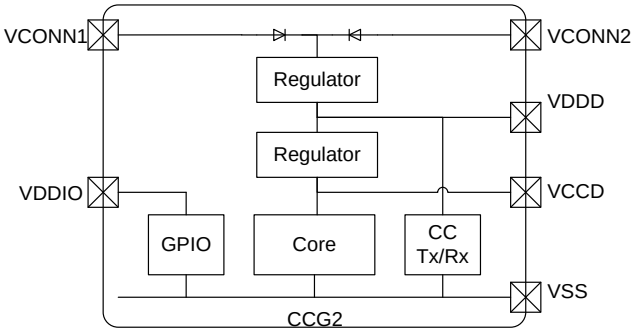


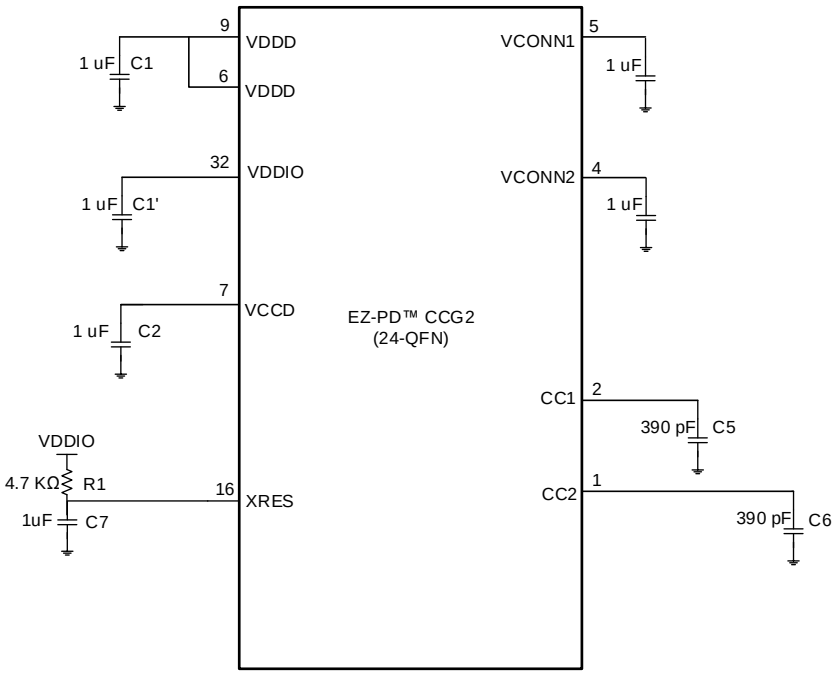
Table 19. CCG2 Operating Voltage Range

Parameter	Min (V)	Typ (V)	Max (V)
VDDD	3	–	5.5
VDDIO	1.71	–	VDDD

13.1.1 Noise Suppression Using Decoupling Capacitors

Power supply noise can be suppressed by using decoupling capacitors to power supply pins VDDD, VDDIO, VCCD, VCONN1, and VCONN2 as shown in Figure 68. A 390-pF decoupling capacitor should be connected to the CC lines (CC1 and CC2) to maintain signal quality at the signaling rate of 300 kHz.

Figure 68. Noise Suppression Using Decoupling Capacitors



13.1.2 Reset and Clock Circuit

CCG2 supports a power-on-reset (POR) mechanism; it also has an active LOW external reset (XRES) pin. The XRES (active LOW) pin can be used by external devices to reset the CCG2 device. The XRES pin should be held LOW for a minimum of 1 µs to reset the CCG2 device. This XRES pin should be tied through an RC circuit as shown in Figure 68. The recommended values for R and C are 100 kΩ and 1 µF respectively to meet the 1-µs pulse-width requirement.

CCG2 has an integrated internal clock; external components such as crystals or oscillators are not required.

13.2 I²C Communication with Embedded Controller

This section is applicable to CCG2. See I²C Communication with Embedded Controller.

13.3 Dead Battery Charging

This section is applicable to CCG2. See Dead Battery Charging.

13.4 Power Provider/Consumer Role

This section is applicable to CCG2. See Power Provider/Consumer Role.

13.5 DisplayPort Connections

This section is applicable to CCG2. See DisplayPort Connections.

13.6 Electrical Design Considerations

See Electrical Design Considerations.

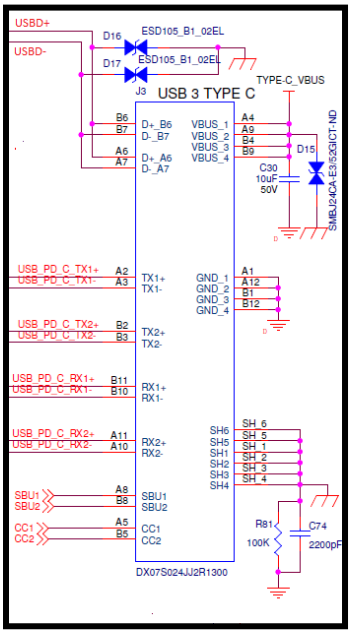
14 Electrical Design Considerations

This section explains PCB design guidelines for routing power signals and USB signals. It provides recommendations for placing components on the board.

14.1.1 ESD and EMI/EMC Protection

Ferrite beads are not mandatory for all Type-C applications but are recommended to be connected between the USB Type-C Connector's Shield and the system's GND pin (in the place of resistor R81), as shown in Figure 69, to prevent the transmission of electrical stress from the Type-C connector to the CCG2/CCG3/CCG4/CCG5/CCG5C/CCG6 /CCG6F/CCG6SF/CCG6DF device.

Figure 69. ESD and EMC Protection



CCG2/CCG4/CCG5/CCG5C/CCG6 has built-in ESD protection of 2 kV on VBUS line whereas CCG3 has on VBUS, USB D+ and USB D- lines. CCG6F has built-in ESD protection of 500 V on TYPE_C_VBUS, PWR_IN, VBUS_P_CTRL and SOURCE pins. ESD protection diodes (D15, D16, and D17) are recommended to be connected to VBUS, USB D+, and USB D- lines for protection above 2 kV as shown in Figure 69. CCG2, CCG3, CCG4, CCG5, CCG5C, CCG6, and CCG6F devices have been tested to work with ESD protection diode model ESD105_B1_02EL. The ESD Diodes meet the requirement of IEC61000-4-2 and low input capacitance. SBU and CC pins supports 1.1 kV and 2.2 kV ESD protection.

14.1.2 Power Domain

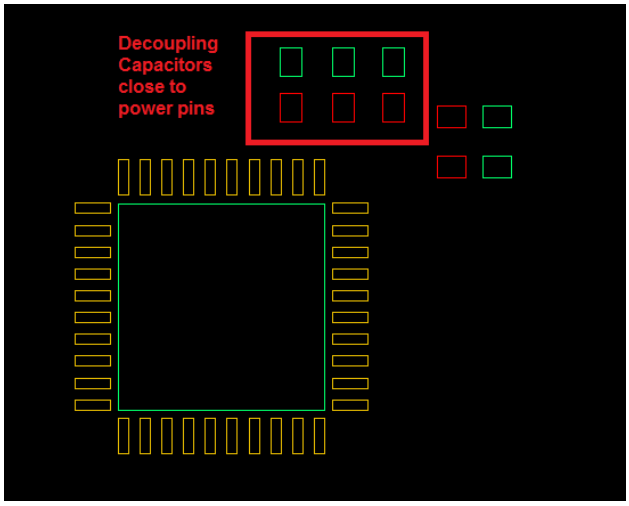
Consider the following while designing the power system network for DRP applications:

- Placement of bulk and decoupling capacitors
- Placement of power and ground planes
- Power domain routing

Placement of Bulk and Decoupling Capacitors

- Place decoupling capacitors close to the power pins of the respective CCG controller for high- and low-frequency noise filtering as shown in Figure 70.
- Place the bulk capacitor, which acts as a local power supply, close to the power supply input and output headers and voltage regulators. Filter power inputs and outputs near the power headers to reduce the electrical noise. Ceramic or tantalum capacitors are recommended; electrolytic capacitors are not suitable for bulk capacitance.

Figure 70. Placement of Bulk and Decoupling Capacitors



Placement of Power and Ground Planes

- Use a high-performance substrate material for PCBs. Per the USB-PD specification, the system may carry current up to 5 A. Thus, it is required to construct PCBs with 2-ounce (oz) copper thickness. Minimum recommended space between copper elements is 8 mil (0.203 mm).
- Use dedicated planes for power and ground. Use of dedicated planes reduces jitter on USB signals and helps minimize the susceptibility to EMI and RFI.
- Use cutouts on the power plane if more than one voltage is required on the board (for example, 2.5 V, 3.3 V, 5.0 V).
- Place the power plane near the ground plane for good planar capacitance. Planar capacitance that exists between the planes acts as a distributed decoupling capacitor for high-frequency noise filtering, thereby reducing the electromagnetic radiation.
- Do not split or cut the ground plane. Splitting it increases the electrical noise and jitter on USB signals. Ground planes should be continuous. A discontinuous ground plane leads to larger inductance due to longer return current paths, which can increase EMI radiation. Also, multiple split grounds can cause increased crosstalk.

Voltage Regulation

The following points must be considered while selecting voltage regulators to reduce electrical emissions and prevent regulation problems during USB suspend:

- Select voltage regulators that have minimum load current less than the board's load current during USB suspend. If the current drawn on the regulator is less than the regulator's minimum load current, then the output voltage may change.

- Place voltage regulators so they straddle split VCC planes; this reduces emissions.

Power Domain Routing

- Power traces should be routed with a minimum of 40 mils trace width to reduce inductance.
- Keep the power traces short.
- Use larger vias (at least 30-mil pad, 15-mil hole) on power traces.
- Make the power trace width the same dimension as the power pad. To connect power pins to the power plane, keep the vias very close to the power pads. This helps in minimizing the stray inductance and IR drop on the line.
- CCG2/CCG3/CCG4/CCG5/CCG5C/CCG6/CCG6F/CCG6SF devices have an EPAD (Exposed PAD), which needs to be soldered onto an exposed ground pad provided in the PCB.
- If a switched-mode power supply is used, power traces should be far away from signal traces to avoid addition of power noise on signal or keep ground traces in between the signal traces.

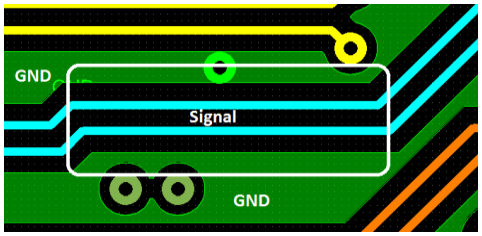
14.1.3 Routing of Type-C (USB Data and CC) Lines

USB SuperSpeed lines from the Host controller are connected to the Type-C port of the notebook through a display multiplexer. Care should be taken while routing USB data and CC lines to achieve good signal quality and reduced emission. Improper layouts lead to poor signal quality especially on the USB signaling, which may lead to enumeration failure of SuperSpeed USB devices connected at Type-C port of the notebook. Follow these guidelines while routing USB data and CC lines during the PCB design phase.

Guidelines for Routing USB Data Lines

- Keep USB SuperSpeed traces as short as possible. Ensure that these traces have a nominal differential characteristic impedance of 90 Ω.
- Match the differential SS pair trace lengths within 0.12 mm (5 mils).
- Match the Hi-Speed (Dp and Dn) signal trace lengths within 1.25 mm (50 mils).
- For CCG5, CCG5C, CCG6, and CCG6F, where USB Hi-Speed signals are routed through internal mux, ensure that the Hi-Speed signals are less than three inches (75 mm) between CCG5, CCG5C, CCG6, CCG6SF, and CCG6DF and the host. Also, maintain trace length less than three inches between CCG5, CCG5C, CCG6, CCG6F, CCG6SF, and CCG6DF and Type-C connector. See the respective device datasheet for more explanation.
- Ensure that the differential pairs (Dp, Dn, SSTxp1, SSTxn1, SSRxp1, and SSRxn1) have a minimum pair-to-pair separation of 0.5 mm.
- Adjust the High-Speed signal trace lengths near the USB receptacle, if necessary.
- Make adjustments for SS Rx signal trace lengths near the USB receptacle. Make adjustments for SS Tx signal trace lengths near the device if necessary.
- Select a grounded coplanar waveguide (CPWG) system as a transmission line method as shown in Figure 71.

Figure 71. PWG Example

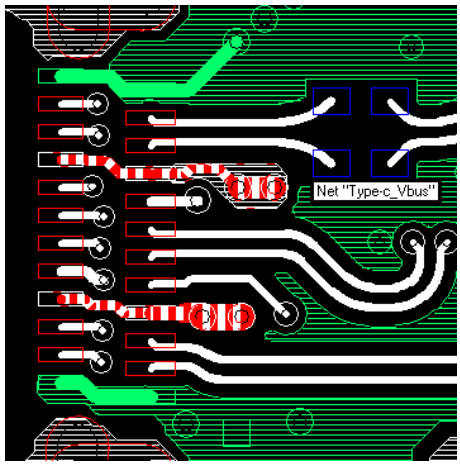


- Minimize the use of vias.

Guidelines for Routing Type-C (VBUS, GND and CC) Lines

- Group the VBUS pins together (all VBUS pins are brought out to the same plane using vias) as shown in Figure 72.

Figure 72. All VBUS Pins are Grouped Together

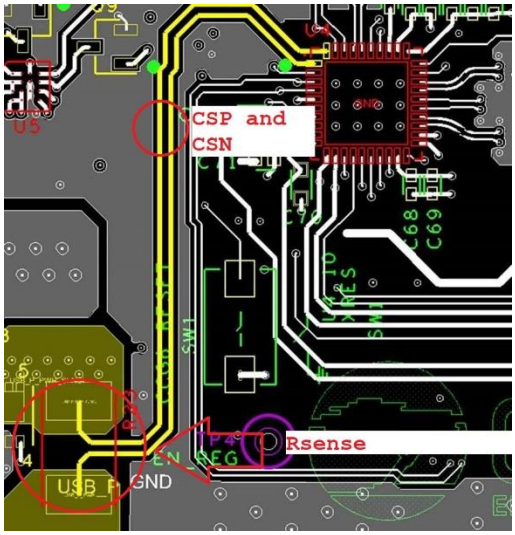


- Similarly, group the GND pins together (all GND pins are brought out to the same plane using vias).
- Place GND plane adjacent and below CC (CC1, CC2) lines. Traces from CC pins must be routed with a minimum of 20 mils trace width for VCONN operation.

14.1.4 Routing of CSP and CSN Lines on CCG5, CCG5C, CCG6, CCG6F, CCG6SF, and CCG6DF Devices

- CSP and CSN must be of shorter length
- The signals must be routed as differential pair to the external Rsense resistor as shown in Figure 73.

Figure 73. Routing of CSP and CSN Traces to Rsense Resistor



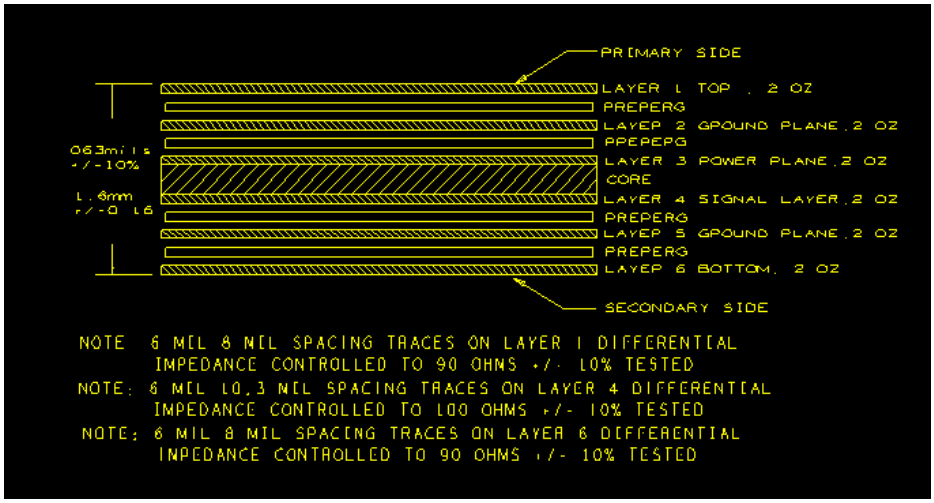
14.1.5 Routing of DisplayPort Lines

- Keep DisplayPort traces (MLLane[3:0] , AUX_CH_N, and AUX_CH_P) as short as possible. Ensure that these traces have a nominal differential characteristic impedance of 90 Ω.
- Match the differential DisplayPort and AUXCH pair trace lengths within 0.12 mm (5 mils).
- Ensure that the differential pairs (MLLane[3:0] , AUX_CH_N and AUX_CH_P) have a minimum pair-to-pair separation of 0.5 mm.

14.1.6 Typical 32-mil, Six-Layer PCB Example for DRP Application

Figure 74 shows the recommended stack up for a standard 32-mil-(0.8 mm) thick PCB. When this stack up is used with two parallel traces, each with a width (W) of 'x' mils and a spacing (S) of 'y' mils., the calculated differential impedance is 90 Ω. Figure 74 shows the values of width (W) and spacing (S) for CY4541 EZ-PD CCG4 EVK's PCBs.

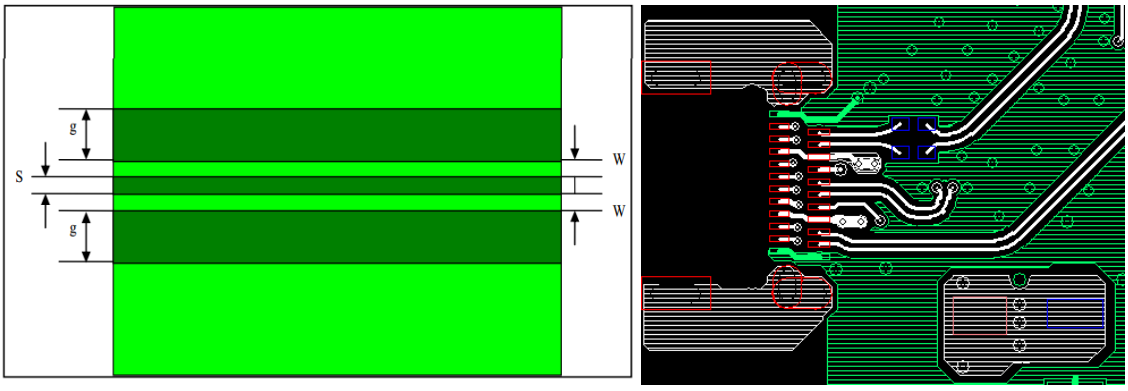
Figure 74. PCB Stack-Up



14.1.7 Impedance Matching

1. Maintain a constant trace width and spacing in differential pairs to avoid impedance mismatches, as shown in Figure 75. Keep minimum 25 mils distance between USB SuperSpeed signals and the adjacent copper pour. Copper pour affects their differential impedance when it is placed too close to USB signals.

Figure 75. Differential Pair Placement in CY4541 EZ-PD CCG4 EVK Layout



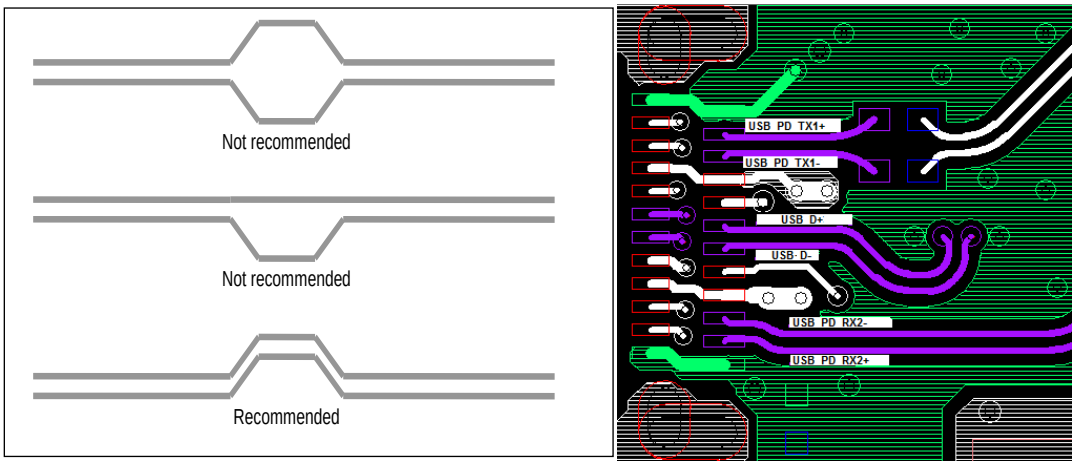
'g' is the minimum gap between the trace and other planes (8 mils)

'W' is the width of the signal trace

'S' is the gap between the differential pair signals

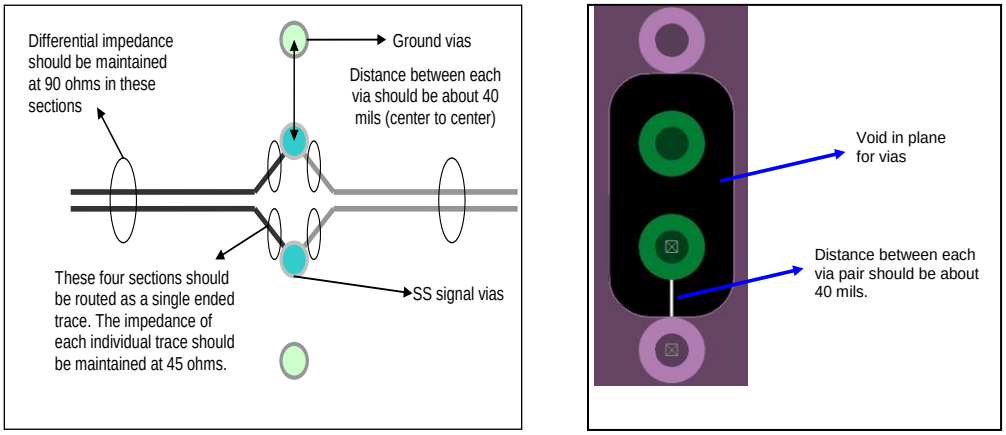
2. Keep the trace length of USB SuperSpeed signals to less than 3 inches (75 mm). A 1.5-inch trace length (25–30 mm) or less is preferred. Match the lengths of USB traces to be within 50 mils (1.25 mm) of each other to avoid skewing the signals and affecting the crossover voltage. Keep minimum 5-mil distance between USB SuperSpeed signals (SSTx+, SSTx-) and other nonstatic traces wherever possible.
3. On USB signal lines, use as few bends as possible. Do not use a 90-degree bend. Use 45-degree or rounded (curved) bends if necessary, as illustrated in Figure 76.

Figure 76. Differential Pair Impedance Matching Techniques in CY4541 EZ-PD CCG4 EVK Layout



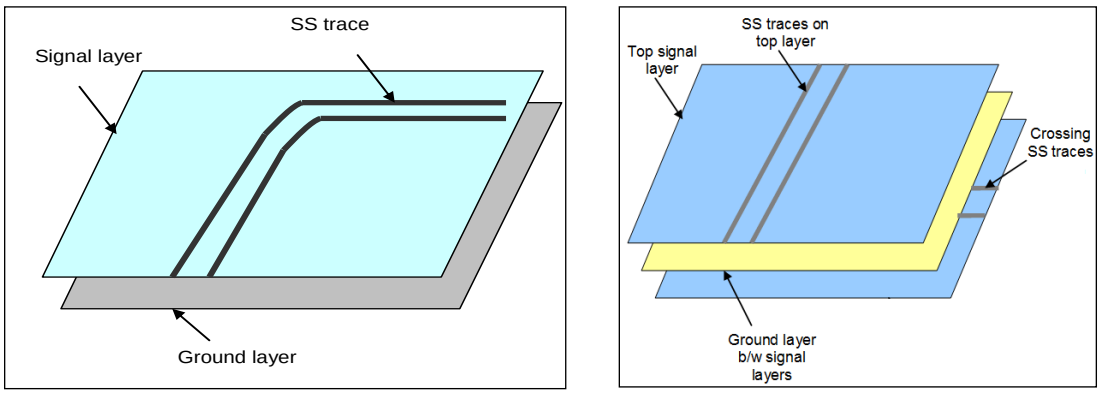
4. SuperSpeed (SS) signals should be routed in a single layer. Vias introduce discontinuities in the signal line and affect the SS signal quality. If you need to route the SS signal to another layer, maintain continuous grounding to ensure uniform impedance throughout. To do so, place ground vias next to signal vias, as shown in Figure 77. The distance between the signal and ground vias should be at least 40 mils. Voids for vias on the SS signal traces should be common for the differential pair. A common void, shown in Figure 77 helps to match the impedance better than separate vias.

Figure 77. Ground Vias and Void Vias Placement for SS Traces



5. All SS signal lines should be routed over an adjacent ground plane layer to provide a good return current path. Splitting the ground plane underneath the SS signals introduces an impedance mismatch, thereby increasing the loop inductance and electrical emissions. Figure 78 shows a recommended solid ground plane under the SS signal.

Figure 78. Solid Ground Plane Under SS Signal



6. Whenever two pairs of USB traces cross each other in different layers, a ground layer should run all the way between the two USB signal layers, as Figure 78 shows.

14.1.8 CAP Recommendation on CSP Pin for CCG6 Notebook Designs

CCG6 has integrated load switch controller which requires capacitance C1 on CSP pin. The capacitance C1 ≥ 50 uF to 100 uF is required for optimal performance of CCG6 during SCP and RCP events.

Figure 79. External Capacitor Requirement on CSP Pin on CCG6 Devices

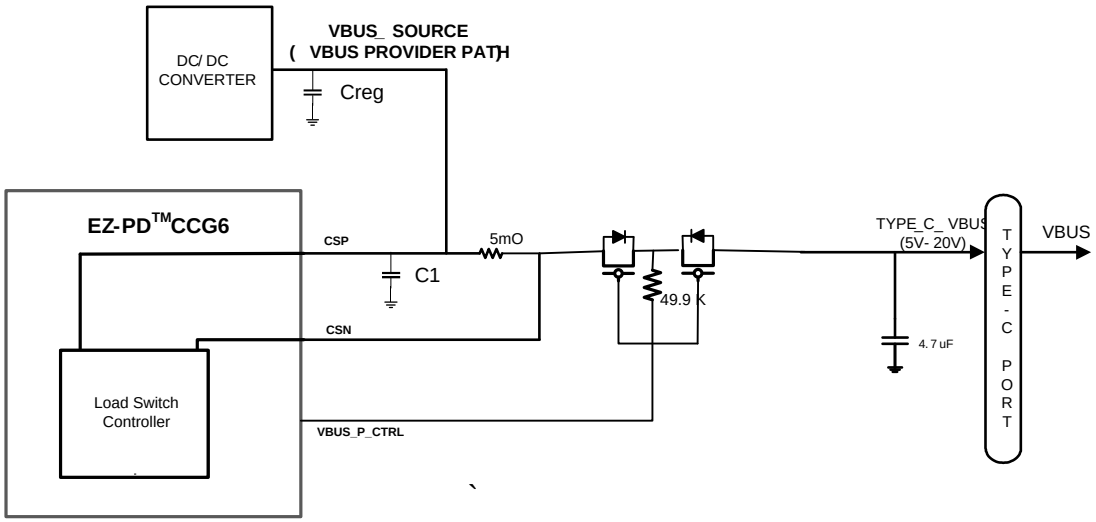


Figure 80. USB_P_PWR when 1-uF Capacitor is used as C1

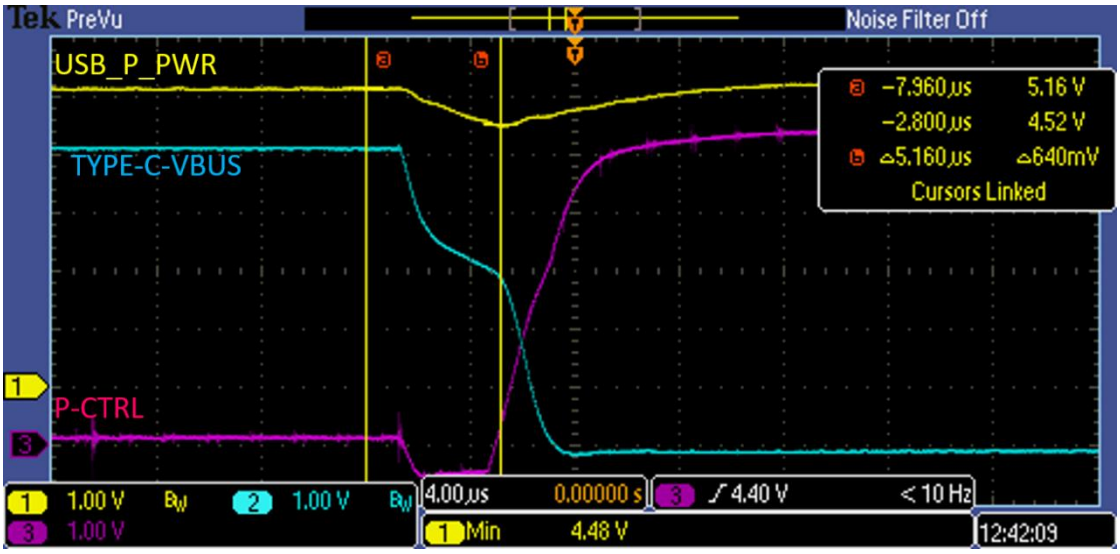
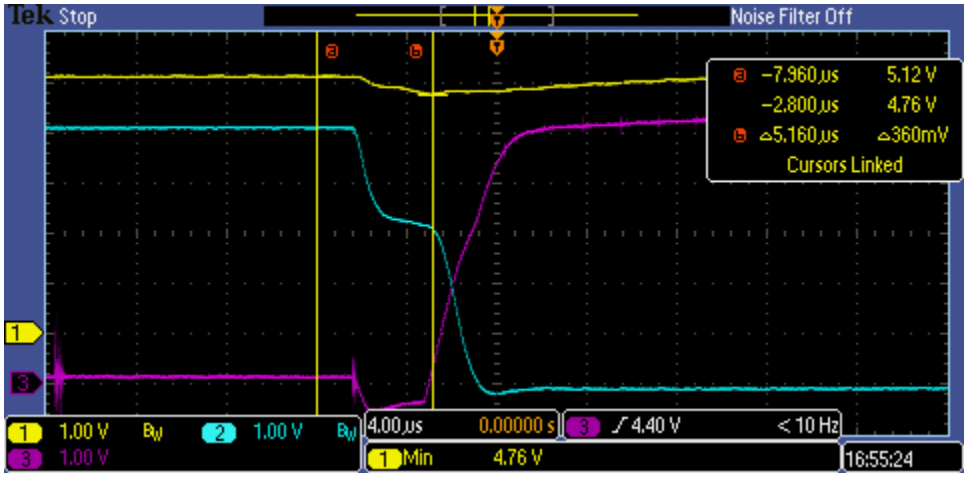


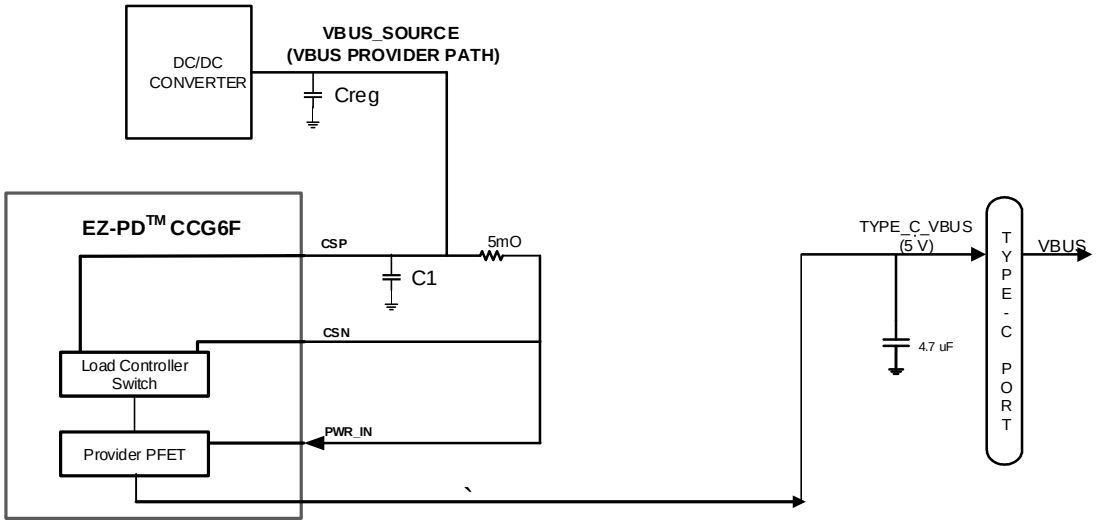
Figure 81: USB_P_PWR when 100-uF Capacitor is used as C1



14.1.9 CAP Recommendation on CSP Pin for CCG6F, CCG6SF, and CCG6DF Notebook Designs

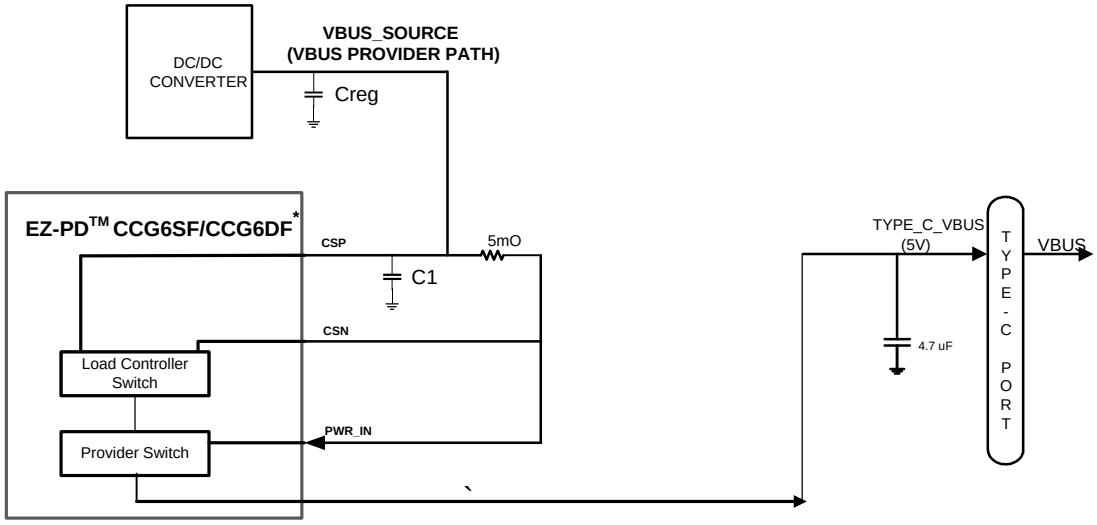
CCG6F has integrated load switch controller which requires capacitance C1 on CSP pin. The capacitance C1 ≥ 50 uF to 100 uF is required for optimal performance of CCG6F during SCP and RCP events.

Figure 82 External Capacitor Requirement on CSP Pin on CCG6F Devices



CCG6SF and CCG6DF have integrated load switch controllers, which require capacitance C1 on CSP pin. CCG6DF has two ports and requires separate external capacitor on each port. The capacitance C1 ≥ 50 uF to 100 uF is required for optimal performance of CCG6F/CCG6SF/CCG6DF during SCP and RCP events.

Figure 83. External Capacitor Requirement on CSP Pin on CCG6SF and CCG6DF Devices



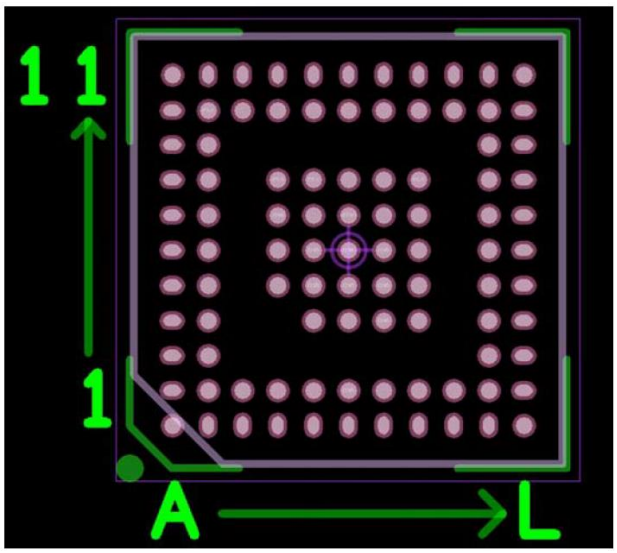
** CCG6DF has two ports, and external capacitor should be connected to both CSP pins separately*

15 Layout Design Guidelines for BGA Packages-CCG6DF

Proper routing and placement help to maintain signal integrity for high-speed signals, improve thermal dissipation and reduce power consumption for CCG6DF. The combination of power and high-speed data signals can be better routed if these design guidelines are followed. It is highly recommended to consult with a PCB manufacturer to verify the manufacturing capabilities to propose the right design guidelines.

Figure 84 shows the CCG6DF 96-BGA device footprint that is recommended. The footprint has oval-shaped pads in specific locations. It is recommended to use oval pads to reduce the manufacturing cost by eliminating a High-Density Interconnector (HDI) board processing. This method allows the PCB designer to route the inner perimeter balls through the top layer. The balls around the perimeter have their pads in an oval shape with the exception of the corner balls.

Figure 84. Top View Standard Footprint (Recommended) for CCG6DF 96-BGA



See the EZ-PD CCG6DF, CCG6SF USB Type-C Port Controller datasheet for complete layout guidelines for CCG6DF 96-BGA controller design.

16 Schematic and Layout Review Checklist

The following is a list of items that are critical for successful Type-C notebook design using Type-C PD controllers. The ideal answer to each of the checklist items below should be “Yes”. Go through this checklist before creating a PCB using the Type-C PD Controller. If a board has already been built and is not behaving as expected, go through this list to verify that all the items are being implemented correctly on the target.

No.	Schematic Checklist	Answer (Yes/No/NA)
1	Are the decoupling capacitors and bulk capacitors connected on power supply and CC pins as shown in Figure 29 for CCG5, CCG5C, CCG6, CCG6F, CCG6SF, and CCG6DF, Figure 43 for CCG4, Figure 63 for CCG3, and Figure 68 for CCG2?	
2	Do the power-on-reset RC components meet the minimum reset time (1 µs) as shown in Figure 29 for CCG5, CCG5C, CCG6F, CCG6SF, and CCG6DF, Figure 43 for CCG4, Figure 63 for CCG3, and Figure 68 for CCG2?	
3	Are the I^2C lines provided with pull-up resistors (2.2 KΩ) as shown in Figure 30 and Figure 44? Is the GPIO for I^2C interrupt pin is same in both bootloader and application firmware?	
4	Is the recommended arrangement of FETs present on VBUS to control power provider and consumer path as shown in Figure 47 for CCG2/CCG4, Figure 53 for CCG3 and Figure 32 for CCG5?	
5	Is the VBUS discharge circuitry present in the design as shown in Figure 50 for CCG2/CCG4?	
6	Is the overvoltage and undervoltage protection circuitry for VBUS present in the design as shown in Figure 51 and Figure 54 for CCG2/CCG4?	
7	Is the overcurrent protection circuitry for VBUS and VCONN present in the design as shown in Figure 55 for CCG2/CCG3/CCG4?	
8	Is the Hot Plug Detect (HPD) signal connected from the Type-C PD controller to the DisplayPort source as shown in Figure 60 for CCG2/CCG3/CCG4 and Figure 37 and Figure 39 for CCG5/CCG5C/CCG6/CCG6F/CCG6SF/CCG6DF?	
9	Are CAP recommendations on CSP pin followed for CCG6 as provided in section 14.1.8, for CCG6F/CCG6SF/CCG6DF as provided in section 14.1.9?	

No.	Layout Checklist	Answer (Yes/No/NA)
1	Are the decoupling capacitors and bulk capacitors placed close to the Type-C PD controller power pins?	
2	Is a 0.1-µF decoupling capacitor placed close to VCCD pin?	
3	Are the vias placed close to the Type-C PD controller power pins?	
4	Are the power traces routed away from the High-Speed (HS) and SuperSpeed (SS) data lines?	
5	Is the capacitor in the RC reset circuitry placed close to the reset pin of the Type-C PD controller?	
6	Has a dedicated and continuous GND plane been used?	
7	Are all VBUS pins on the Type-C connector brought on the same plane using vias?	
8	Are all GND pins on the Type-C connector brought on the same plane using vias?	
9	Is GND present adjacent to and below CC lines?	
10	Do the differential DisplayPort signal lines match in length?	
11	Do the USB SS and HS signal lines match in length?	
12	Are the USB SS and HS signal lines provided with a solid ground plane underneath?	
13	Are the USB traces kept short?	
14	Do the USB traces have minimum bends and no 90-degree bends?	
15	Is it ensured that there are no vias on SS traces?	
16	Are CSP and CSN pins routed as instructed in Section 14.1.4?	

A Cypress Design Resources

Table 20. CCG Design Resources

Design	Available Resources	Where To Find Resources
Hardware	Development Board – Schematic, Board files and documentation	Development Kit (DVK) Schematic Board files available with CY4501 CCG1 DVK (For CCG1) CY4502 CCG2 DVK (For CCG2) CY4502 CCG2 DVK (For CCG2) CY4531 CCG3 EVK (For CCG3) CY4541 CCG4 EVK (For CCG4)
	Hardware design guidelines including recommendations for resistors, decoupling capacitors for power supplies and PCB layout	Application note – AN95599
	IBIS model	IBIS model files
Programming Specification	The programming reference manual gives the information necessary to program the nonvolatile memory of the CYPD1xxx/CYPD2xxx devices.	Programming Specification
	The programming reference manual gives the information necessary to program the nonvolatile memory of the CYPD4xxx and CYPD5xxx devices.	Programming Specification
Code Example	EZ-PD CCG2 firmware examples	Firmware images
	EZ-PD CCG4 firmware examples	Firmware images
Host PC Software	GUI-based Windows application to help configure CCG controllers	EZ-PD Configuration Utility

Table 21. Application Notes and Reference Designs for Type-C PD Controllers

Application	Product Name	Document Link
Designing USB Type-C Products using Cypress CCG1 controllers	EZ-PD CCG1	Application Note
USB Type-C to HDMI/DVI/VGA Adapter design	EZ-PD CCG1	Reference Design
USB Type-C to Display Port solution	EZ-PD CCG1	Reference Design
Electronically marked cable assembly (EMCA) paddle card reference design	EZ-PD CCG1	Reference Design
USB Type-C to legacy USB device cable paddle reference design	EZ-PD CCG1	Reference Design
Designing USB 3.1 Type-C cables using EZ-PD CCG2	EZ-PD CCG2	Application Note
Hardware Design Guidelines for EZ-PD CCG2	EZ-PD CCG2	Application Note
Electronically marked cable assembly (EMCA) paddle card reference design	EZ-PD CCG2	Reference Design
EZ-PD CCG2 USB Type-C to DisplayPort Cable Solution	EZ-PD CCG2	Reference Design
EZ-PD CCG2 USB Type-C to HDMI Adapter Solution	EZ-PD CCG2	Reference Design
EZ-PD CCG2 USB Type-C Monitor/Dock Solution	EZ-PD CCG2	Reference Design
CCG2 18W Power Adapter Reference Design	EZ-PD CCG2	Reference Design
CCG2 20W Power Adapter Reference Design	EZ-PD CCG2	Reference Design
CCG2 24W Power Adapter Reference Design	EZ-PD CCG2	Reference Design
CCG2 60W Car Charger Reference Design	EZ-PD CCG2	Reference Design
CCG2 60W Car Charger Reference Design using Southchip	EZ-PD CCG2	Reference Design
EZ-PD CCG2 USB Type-C Power Bank Solution	EZ-PD CCG2	Reference Design
EZ-PD CCG3 USB Type-C to DisplayPort Cable Solution	EZ-PD CCG3	Reference Design
EZ-PD CCG3 USB Type-C to HDMI Adapter Solution	EZ-PD CCG3	Reference Design
EZ-PD CCG3 USB Type-C Charge-Through Dongle	EZ-PD CCG3	Reference Design
EZ-PD CCG3 USB Type-C Power Bank Solution	EZ-PD CCG3	Reference Design
EZ-PD CCG3-based HDMI over Type-C Cable Reference Design	EZ-PD CCG3	Reference Design
EZ-PD CCG4-based Type-C Monitor/Dock Solution	EZ-PD CCG4	Reference Design
Cypress USB-C Thunderbolt Reference Solution	Cypress PD Controllers	Reference Design

Table 22. Available Collaterals for Type-C PD Controllers

Other Collaterals
CCG1 Datasheet
CCG2 Datasheet
CCG3 Datasheet
CCG4 Datasheet
CCG5 Datasheet
CCG5C Datasheet
CCG6 Datasheet
CCG6F Datasheet
CCG6SF/CCG6DF Datasheet
Knowledge Base Articles for Type-C PD Controllers
Qualification report link for Type-C PD Controllers

Document History

Document Title: AN210403 – Hardware Design Guidelines for DRP Applications Using EZ-PD USB Type-C Controllers

Document Number: 002-10403

Revision	ECN	Submission Date	Description of Change
**	5074748	03/02/2016	New application note
*A	5688186	04/07/2017	Updated logo and copyright
*B	5840865	09/14/2017	Updated sections 1, 3, 10, 11 for CGG5 Added Section 4 and 5 for Dual and single Type-C port DRP application using CCG5 Updated template
*C	6409359	12/13/2018	Added Design Guidelines for CCG5C and CCG6
*D	6504739	03/08/2019	Updated Table 5 Updated section 6.4.4 Updated Figure 16 Updated section 9 (Marked CYPD5125-40LQXI as Not Recommended) Updated sections 14.1.1, 14.1.3, 14.1.4, and 14.1.8
*E	6539269	04/10/2019	Updated sections 1, 3, 4, 8.1.2, and 8.2 Added Section 14.1.9 Updated Table 22
*F	6819884	02/28/2020	Sunset review Added sections 4, 5, and 15 Updated section 14.1.9 Updated cross-references Updated Table 1, Table 6, Table 7, Table 21, and Table 22 Updated Figure 11 to Figure 19 Updated Figure 22 to Figure 26 Updated Figure 29 to Figure 36 Updated Figure 43 to Figure 45 Updated Figure 47, Figure 50, Figure 51, Figure 63, Figure 65, Figure 68, Figure 79Figure 82, and Figure 83

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