

# Datasheet AP6275S

IEEE 802.11ax/ac/a/b/g/n 2x2 WiFi with Bluetooth5.0 Combo Sip Module



## The revision history of the product specification

Version	Purpose	Date	Editor
1.0	Initial Doc	2019/11/29	Aaron



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#### 1. Introduction

#### 1.1 Product Overview

AP6275S is an 802.11ax (WiFi 6) SiP Module, 802.11ax allow Increased capacity, faster speed, better coverage connections, improve the battery life of IoT sensors, and extend the range of Wi-Fi signals. By implementing the new 802.11ax standard with its unique features such as OFDMA, 1024QAM, Target Wake Time (TWT), and spatial reuse, the AP6275S module enables smooth streaming of high-resolution videos, fewer dropped connections and faster connections farther away from the router and in dense environments.

The Wi-Fi and Bluetooth 5.0 functionalities module with seamless roaming capabilities and advanced security. The 802.11 ax sip module can support Multi-User MIMO (MU-MIMO) technology to increase channel capacity when simultaneously servicing multiple devices using the same frequency chunks. Furthermore the included SDIO interface for Wi-Fi, UART/ PCM interface for Bluetooth.

#### 1.2 Product Features

#### 1.2.1 WLAN

- Dual-stream spatial multiplexing up to 1200 Mbps data rate
- 20, 40, 80 MHz channels with optional SGI (1024 QAM modulation)
- TX and RX low-density parity check (LDPC) support for improved range and power efficiency
- Supports standard SDIO v3.0, compatible with SDIO v2.0 HOST interfaces.
- Client MU-MIMO

#### 1.2.2 Bluetooth

- BT host digital interface:
  - HCI UART (up to 4 Mbps)
  - PCM for audio data
- Complies with Bluetooth Core Specification Version 5.0 with provisions for supporting future specifications. With Bluetooth Class 1 or Class2 transmitter operation
- Supports extended synchronous connections (eSCO), for enhanced voice quality by allowing for retransmission of dropped packets



## 2. Specification

## 2.1 General Specification

Standards	IEEE 802.11 ax/ac/a/b/g/n 2T2R Wi-Fi + BT 5.0 Module Bluetooth : BDR \cdot EDR(1Mdps & 2Mdps) \cdot LE(1Mdps) \cdot 2LE(2Mdps)	
Chipset	Broadcom	
Operating Frequency	2.400 GHz ~ 2.4835 GHz (2.4GHz ISM Band) 5.15~5.35GHz \ 5.47~5.725GHz \ 5.725~5.85GHz (5GHz UNII Band) Bluetooth: 2402 MHz ~ 2480 MHz	
Modulation	802.11b : DQPSK \ DBPSK \ CCK  802.11 g/n : OFDM /64-QAM \ 16-QAM \ QPSK \ BPSK  802.11a : OFDM /64-QAM \ 16-QAM \ QPSK \ BPSK  802.11n : OFDM /64-QAM \ 16-QAM \ QPSK \ BPSK  802.11ac : OFDM /256-QAM \ 64-QAM \ 16-QAM \ QPSK \ BPSK  802.11ax : OFDMA /1024-QAM \ 256-QAM \ 64-QAM \ 16-QAM \ QPSK \ BPSK  Bluetooth: GFSK, \(\pi/4\)-DQPSK, 8DPSK	
WiFi Interface	SDIO 3.0 / 2.0	
BT Interface	UART / PCM	
Form Factor	SiP (System in Package) LGA Type	
Antenna	External	
Dimension	L x W : 15 x 13 mm(Typical) , H : 1.55 mm(Maximum)	
Operating temperature	-30°C to 85°C	
Storage temperature	-40°C to 105°C	
Humidity	Operating Humidity 10% to 95% Non-Condensing	
Driver Support	Linux, Android	

Note: The optimal RF performance specified in the data sheet, however, is guaranteed only -10  $^{\circ}$ C to +55  $^{\circ}$ C and 3.2V < VBAT < 3.8V without derating performance.



## 2.2 WiFi 2.4GHz RF Specification

Conditions: VBAT=3.3V; VDDIO=1.8V; Temp:25°C

	Conditions: VBAT=3.3V; VDDIO=1.8V; Temp:25 °C  Output Power, tolerance <u>+</u> 1.5dB						
The transm	sit F\/N/I amalita	-				TF 902 11 ston	ماميط
rne transn	nit EVM quality						uaru 
802.11b	1Mbps	2Mb	•	5.5Mbps		11Mbps	
	19.5	19.5 12 \ 18Mbps		19.5		19.5	40046
	6 \ 9Mbps		•		24Mbps	36Mbps	48Mbps
802.11g	19.5	19.	5		18.5	18.5	18
J	54Mbps						
	18						
	MCS0~2	MC			MCS4	MCS5	MCS6
802.11n	19.5	18.	5		18.5	18	18
20MHz	MCS7						
	17.5						
	HEO~2	HE	3		HE4	HE5	HE6
802.11ax	19.5	18.	5		18.5	18	18
20MHz	HE7	HE	8		HE9	HE10	HE11
	17.5	16.	5		16.5	15	15
	Data rate	Tones	Spec(d	lBm)	Data rate	Tones	Spec(dBm)
	MCS0	26	19	)		26	17.5
		52	19		NACCC	52	17.5
		106	19		MCS6	106	17.5
		256	19	)		256	17.5
		26	18.	5		26	17.5
		52	18.	5		52	17.5
	MCS1-2	106	18.	5	MCS7	106	17.5
		256	18.5			256	17.5
000 44 000 444		26	18	}		26	16.5
802.11ax_20MHz		52	18	}		52	16.5
SISO	MCS3	106	18	}	MCS8	106	16.5
		256	18	}		256	16.5
		26	18			26	16.5
		52	18			52	16.5
	MCS4	106	18		MCS9	106	16.5
		242	18			256	16.5
		26	17.				
		52	17.		MCS10	242	15
	MCS5	106	17.		N.4004.4	2.12	4-
		242	17.		MCS11	242	15

Note: The specifications of RF output power are subject to change to fulfill the safety regulation and requirements in end-user product.



	Sensitivity, tolerance ± 2 dB				
	CCK modulation P	ER ≤ 8% · OFDM	modulation PER ≤	10%	
	Data Rate	Spec.(dBm)			
	1Mbps	-98			
802.11b	2Mbps	-93			
	5.5Mbps	-91			
	11Mbps	-89			
	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)	
002.11~	6Mbps	-93	24Mbps	-85	
802.11g SISO	9Mbps	-92	36Mbps	-82	
3130	12Mbps	-91	48Mbps	-78	
	18Mbps	-88	54Mbps	-76	
	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)	
002.11~	6Mbps	-95	24Mbps	-87	
802.11g MIMO	9Mbps	-94	36Mbps	-84	
IVIIIVIO	12Mbps	-93	48Mbps	-81	
	18Mbps	-90	54Mbps	-78	
	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)	
002 11m 20MII-	MCS0	-93	MCS4	-81.5	
802.11n_20MHz SISO	MCS1	-89	MCS5	-78	
3130	MCS2	-87	MCS6	-76	
	MCS3	-84	MCS7	-76	
	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)	
	MCS0	-93	MCS5	-80	
802.11n_20MHz	MCS1	-92	MCS6	-78	
MIMO	MCS2	-90	MCS7	-76	
	MCS3	-87	MCS8	-72	
	MCS4	-83	MCS15	-73	
	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)	
	MCS0	-93	MCS6	-76	
802.11ax_20MHz SISO	MCS1	-89	MCS7	-76	
	MCS2	-87	MCS8	-72	
	MCS3	-84	MCS9	-70	
	MCS4	-81.5	MCS10	-65	
	MCS5	-79	MCS11	-61.5	
Maximum Input	802.11b : -10 dBr	n	•		
Level	802.11g/n/ax : -2	0 dBm			



## 2.3 WiFi 5GHz RF Specification

Conditions: VBAT=3.3V; VDDIO=1.8V; Temp:25°C

Conditions: VBAT=3.3V; VDDIO=1.8V; Temp:25°C					
<b>-</b> 1		Output Power , to		'th 1555 000 44 -	
The tran	smit EVM quality	& spectrum mask	are compliant v	vith IEEE 802.11 s	tandard
	Frequency (MHz)	6~9Mbps	12~18Mbps	24Mbps	36Mbps
	5150~5350	17	17	16.5	16.5
	5470~5720	17	17	16.5	16.5
802.11a	5725~5845	17	17	16.5	16.5
002.11a	Frequency (MHz)	48Mbps	54Mbps		
	5150~5350	16	16		
	5470~5720	16	16		
	5725~5845	16	16		
	Frequency (MHz)	MCS0~2	MCS3	MCS4	MCS5
	5150~5350	17	16.5	16.5	16
	5470~5720	17	16.5	16.5	16
802.11n	5725~5845	17	16.5	16.5	16
20MHz	Frequency (MHz)	MCS6	MCS7		
	5150~5350	16	15.5		
	5470~5720	16	15.5		
	5725~5845	16	15.5		
	Frequency (MHz)	MCS0~2	MCS3	MCS4	MCS5
	5150~5350	16.5	15.5	15.5	15
	5470~5720	16.5	15.5	15.5	15
802.11n	5725~5845	16.5	15.5	15.5	15
40MHz	Frequency (MHz)	MCS6	MCS7		
	5150~5350	15	14.5		
	5470~5720	15	14.5		
	5725~5845	15	14.5		
	Frequency (MHz)	MCS0~2	MCS3	MCS4	MCS5
	5150~5350	17	16.5	16.5	16
	5470~5720	17	16.5	16.5	16
802.11ac	5725~5845	17	16.5	16.5	16
20MHz	Frequency (MHz)	MCS6	MCS7	MCS8	
	5150~5350	16	14.5	12	
	5470~5720	16	14.5	11	
	5725~5845	16	14.5	11	



	Frequency (MHz)	MCS0~2	MCS3	MCS4	MCS5
	5150~5350	16.5	15.5	15.5	15
	5470~5720	16.5	15.5	15.5	15
802.11ac	5725~5845	16.5	15.5	15.5	15
40MHz	Frequency (MHz)	MCS6	MCS7	MCS8	MCS9
	5150~5350	14	14	13	11
	5470~5720	13	13	13	10
	5725~5845	13	13	13	10
	Frequency (MHz)	MCS0~2	MCS3	MCS4	MCS5
	5150~5350	16	15	15	15
	5470~5720	16	15	15	15
802.11ac	5725~5845	16	15	15	15
80MHz	Frequency (MHz)	MCS6	MCS7	MCS8	MCS9
	5150~5350	14	14	11	11
	5470~5720	13	13	10	10
	5725~5845	13	13	10	10
	Frequency (MHz)	MCS0~2	MCS3	MCS4	MCS5
	5150~5350	17	16.5	16.5	16
	5470~5720	17	16.5	16.5	16
	5725~5845	17	16.5	16.5	16
802.11ax	Frequency (MHz)	MCS6	MCS7	MCS8	MCS9
802.11ax 20MHz	5150~5350	16	14.5	12	12
Ζυίνιπζ	5470~5720	16	14.5	11	11
	5725~5845	16	14.5	11	11
	Frequency (MHz)	MCS10	MCS11		
	5150~5350	10.5	10.5		
	5470~5720	10	10		
	5725~5845	10	10		
	Frequency (MHz)	MCS0~2	MCS3	MCS4	MCS5
	5150~5350	16.5	15.5	15.5	15
	5470~5720	16.5	15.5	15.5	15
802.11ax	5725~5845	16.5	15.5	15.5	15
40MHz	Frequency (MHz)	MCS6	MCS7	MCS8	MCS9
	5150~5350	14	14	13	11
	5470~5720	13	13	13	10
	5725~5845	13	13	13	10



	Frequency (MHz)	MCS10	MCS11		
	5150~5350	9	9		
	5470~5720	8	8		
	5725~5845	8	8		
	Frequency (MHz)	MCS0~2	MCS3	MCS4	MCS5
	5150~5350	16	15	15	15
	5470~5720	16	15	15	15
	5725~5845	16	15	15	15
902.1169	Frequency (MHz)	MCS6	MCS7	MCS8	MCS9
802.11ax 80MHz	5150~5350	14	14	11	11
ουίνιπε	5470~5720	13	13	10	10
	5725~5845	13	13	10	10
	Frequency (MHz)	MCS10	MCS11		
	5150~5350	9	9		
	5470~5720	9	9		
	5725~5845	9	9		

Note: The specifications of RF output power are subject to change to fulfill the safety regulation and requirements in end-user product.

## Sensitivity, tolerance $\pm$ 1.5 dB CCK modulation PER $\leq$ 8% $\cdot$ OFDM modulation PER $\leq$ 10%

	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
802.11a	6Mbps	-90.5	24Mbps	-83
SISO	9Mbps	-90	36Mbps	-80
3130	12Mbps	-88	48Mbps	-75
	18Mbps	-86	54Mbps	-73
	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
802.11a	6Mbps	-92	24Mbps	-86
MIMO	9Mbps	-91	36Mbps	-83
IVIIIVIO	12Mbps	-90	48Mbps	-78
	18Mbps	-89	54Mbps	-77
	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
902 11n 20MHz	MCS0	-90	MCS4	-79
802.11n_20MHz SISO	MCS1	-88	MCS5	-76
3130	MCS2	-86	MCS6	-73
	MCS3	-83	MCS7	-72
	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0	-92	MCS5	-78
802.11n_20MHz	MCS1	-91	MCS6	-76
MIMO	MCS2	-89	MCS7	-75
	MCS3	-86	MCS8	-89
	MCS4	-82	MCS15	-70



	Data Rate	Spac (dDm)	Data Rate	Spac (dDm)
		Spec.(dBm) -88		Spec.(dBm)
802.11n_40MHz	MCS0 MCS1	-86	MCS4 MCS5	-77 -72
SISO				
	MCS2	-83	MCS6	-70
	MCS3	-80	MCS7	-69
	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
000 44 400 411	MCS0	-88	MCS5	-75
802.11n_40MHz	MCS1	-88	MCS6	-73
MIMO	MCS2	-86	MCS7	-72
	MCS3	-83	MCS8	-86
	MCS4	-79	MCS15	-67
	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0	-90	MCS5	-75
802.11ac_20MHz	MCS1	-88	MCS6	-73
SISO	MCS2	-86	MCS7	-70
	MCS3	-83	MCS8	-68
	MCS4	-79		
	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0,NSS=1	-92	MCS6,NSS=1	-76
802.11ac_20MHz	MCS1,NSS=1	-91	MCS7,NSS=1	-75
MIMO	MCS2,NSS=1	-88	MCS8,NSS=1	-72
IVIIIVIO	MCS3,NSS=1	-85	MCS0,NSS=2	-88
	MCS4,NSS=1	-82	MCS8,NSS=2	-65
	MCS5,NSS=1	-77		
	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0	-88	MCS5	-72
802.11ac_40MHz	MCS1	-86	MCS6	-70
SISO	MCS2	-83	MCS7	-69
	MCS3	-80	MCS8	-65
	MCS4	-76	MCS9	-64
	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0,NSS=1	-90	MCS6,NSS=1	-73
000.44 400.411	MCS1,NSS=1	-88	MCS7,NSS=1	-72
802.11ac_40MHz	MCS2,NSS=1	-86	MCS8,NSS=1	-68
MIMO	MCS3,NSS=1	-82	MCS9,NSS=1	-66
	MCS4,NSS=1	-79	MCS0,NSS=2	-86
	MCS5,NSS=1	-77	MCS9,NSS=2	-60
	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0	-85	MCS5	-68
802.11ac 80MHz	MCS1	-82	MCS6	-67
SISO	MCS2	-79	MCS7	-65
	MCS3	-76	MCS8	-62
	MCS4	-73	MCS9	-61
	IVICS4	-/3	IVICS9	-61



	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0,NSS=1	-87	MCS6,NSS=1	-70
	MCS1,NSS=1	-85	MCS7,NSS=1	-68
802.11ac_80MHz	MCS2,NSS=1	-82	MCS8,NSS=1	-66
MIMO	MCS3,NSS=1	-79	MCS9,NSS=1	-63
	MCS4,NSS=1	-76	MCS0,NSS=2	-83
	MCS5,NSS=1	-71	MCS9,NSS=2	-58
	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0	-90	MCS6	-73
002 44 201411-	MCS1	-88	MCS7	-70
802.11ax_20MHz	MCS2	-86	MCS8	-68
SISO	MCS3	-83	MCS9	-64
	MCS4	-79	MCS10	-59
	MCS5	-75	MCS11	-57
	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0	-90	MCS6	-73
802.11ax 40MHz	MCS1	-88	MCS7	-70
SISO	MCS2	-86	MCS8	-68
3130	MCS3	-83	MCS9	-64
	MCS4	-79	MCS10	-60
	MCS5	-75	MCS11	-55
	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0	-90	MCS6	-73
802.11ax 80MHz	MCS1	-88	MCS7	-70
	MCS2	-86	MCS8	-68
3130	MCS3	-83	MCS9	-61
	MCS4	-79	MCS10	-57
	MCS5	-75	MCS11	-53
Maximum Input Level	802.11a/n/ac : -30 c	dBm		



## 2.4 Bluetooth RF Specification

Conditions: VBAT=3.3v ; VDDIO=1.8V ; Temp:25  $^{\circ}\text{C}$ 

RF Specification	RF Specification			
	Output Power, tolerance ± 1.5 dB			
	CL1 (dBm)			
BDR Output Power	8			
EDR Output Power	6			
BLE Output Power	7			
	Sensitivity, tolerance ± 1.5 dB			
Sensitivity @ BER=0.1% for GFSK (1Mbps)	-88 dBm			
Sensitivity @ BER=0.01% for $\pi/4$ -DQPSK (2Mbps)	-91 dBm			
Sensitivity @ BER=0.01% for 8DPSK (3Mbps)	-85 dBm			
Sensitivity @ BER=30.8% for LE (1Mbps)	-90 dBm			
Sensitivity @ BER=30.8% for 2LE (2Mbps)	-91 dBm			
	GFSK (1Mbps):-20dBm			
Maximum Input Level	π/4-DQPSK (2Mbps) :-20dBm			
	8DPSK (3Mbps) :-20dBm			

Note\*: The Bluetooth BDR output power is able to be configured by firmware (hcd file).



## 3. Electrical Characteristics

## **3.1 Absolute Maximum Ratings**

Symbol	Description	Min.	Max.	Unit
VBAT	Input supply Voltage	-0.5	4.5	V
VDDIO	Digital/Bluetooth/SDIO/ I/O Voltage	-0.5	2.07	V

Extreme caution must be exercised to prevent electrostatic discharge (ESD) damage.

Symbol	Condition	Minimum ESD Rating	Unit
ESD_HAND_HBM	Human body model contact discharge per JEDEC EID/JESD22-A114	1	kV
ESD_HAND_CDM	Charged device model contact discharge per JEDEC EIA/JESD22-C101	250	V

## 3.2 Recommended Operating Rating

The module requires two power supplies: VBAT and VDDIO.

Voltage rails	Min.	Тур.	Max.	Unit
VBAT	3.0	3.3	3.8	V
VDDIO	1.68	1.8	1.98	V

VBAT current consumption 1200mA(Peak), when VBAT = 3.3V

The module requires two power supplies: other Digital I/O Pins.

For VDDIO=1.8V	=1.8V Min. Max.		
VIL/VIH	0.35×VDDIO	0.65×VDDIO	V
VOL/VOH output@2mA	0.4	VDDIO-0.4	V



## 3.3 Recommended Operating Conditions and DC Characteristics

Downwater	Complete al		Value			
Parameter	Symbol	Minimum	Typical	Maximum	Unit	
DC supply voltage for VBAT	VBAT	3.2	-	4.8	V	
DC supply voltage for core	VDD	0.81	0.9	0.99	V	
DC supply voltage for RF blocks in chip	VDDRF	0.90	1.0	1.1	V	
DC supply voltage for digital I/O	VDDIO	1.62	1.8	1.98	V	
DC supply voltage for RF switch I/O	VDDIOA VDDIOP PMU_VDDIOA	1.62	1.8	1.98	V	
DC supply voltage for RF switch I/O when supporting 3.3V RF_SW_CTRL pads	- VDDIO RFª	3.13	3.3	3.46	V	
DC supply voltage for RF switch I/O when supporting 1.8V RF_SW_CTRL pads	VDDIO_KF	1.62	1.8	1.98	V	
External TSSI input	TSSI	0.15	-	0.95	V	
Internal POR threshold	Vth_POR	0.4	-	0.7	V	
Other Digital I/O Pins						
For VDDIO = 1.8V						
Input high voltage	VIH	0.65 x VDDIO	-	-	V	
Input low voltage	VIL	-	-	0.4 x VDDIO	V	
Output high Voltage @ 2 mA	VOH	VDDIO - 0.40			V	
Output Low Voltage @ 2 mA	VOL	-	-	0.40	V	
RF Switch Control Output Pins <sup>b</sup>						
For VDDIO_RF = 3.3V						
Output high Voltage @ 2 mA	VOH	TBD	TBD	TBD	V	
Output Low Voltage @ 2 mA	VOL	TBD	TBD	TBD	V	
Input capacitance	C <sub>IN</sub>	TBD	TBD	TBD	pF	

a. The BCM43752 supports either 1.8V or 3.3V RF switch control pads. To select 1.8V, connect RF\_MODE\_HV to ground. To select 3.3V, connect RF\_MODE\_HV to 3.3V.

b. Programmable 2 mA to 16 mA drive strength. Default is 10 mA.

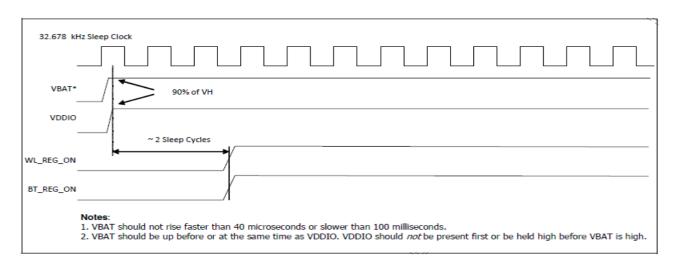


## 4. Host Interface Timing Diagram

#### 4.1 Power-up Sequence Timing Diagram

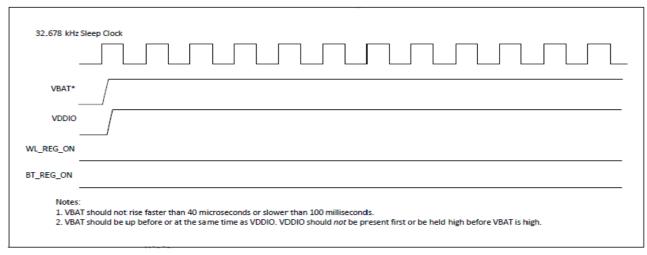
The module has signals that allow the host to control power consumption by enabling or disabling the Bluetooth, WLAN and internal regulator blocks. These signals are described below. Additionally, diagrams are provided to indicate proper sequencing of the signals for carious operating states. The timing value indicated are minimum required values: longer delays are also acceptable.

- WL\_REG\_ON: Used by the PMU to power up or power down the internal regulators used by the WLAN section. When this pin is high, the regulators are enabled and the WLAN section is out of reset. When this pin is low the WLAN section is in reset.
- BT\_REG\_ON: Used by the PMU to power up or power down the internal regulators used by the BT section. Low asserting reset for Bluetooth. This pin has no effect on WLAN and does not control any PMU functions. This pin must be driven high or low (not left floating).

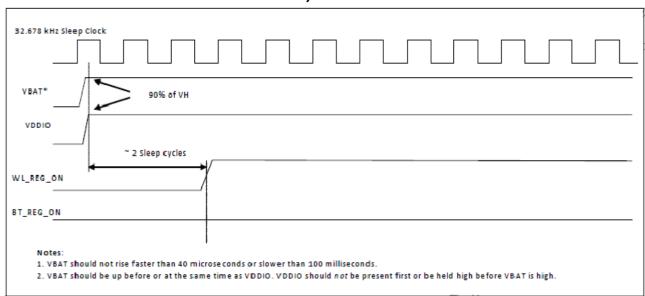


WLAN=ON, Bluetooth=ON

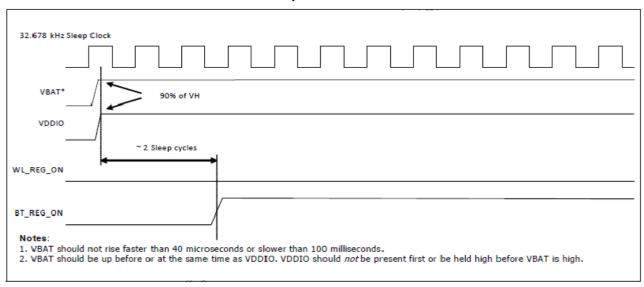




#### WLAN=OFF, Bluetooth=OFF



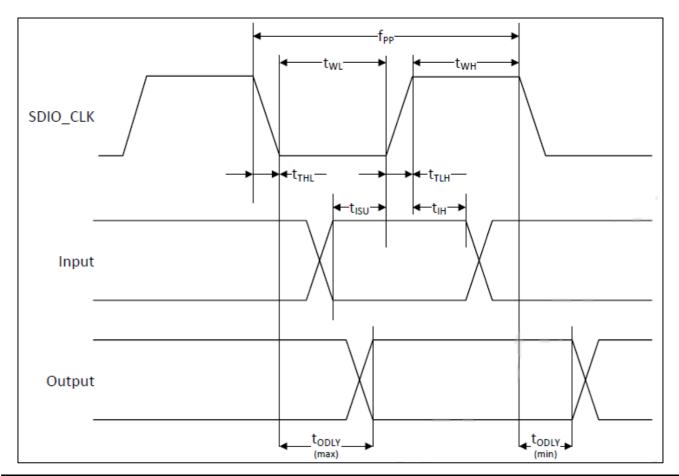
#### WLAN=ON, Bluetooth=OFF



#### WLAN=OFF, Bluetooth=ON



## **4.2 SDIO Default Mode Timing Diagram**

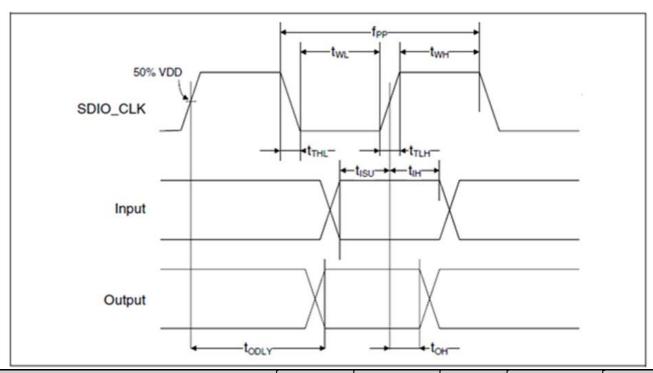


Parameter	Symbol	Minimum	Typical	Maximum	Unit				
SDIO CLK (ALL values are referred to minimum VIH and maximum VIL b)									
Frequency – Data Transfer mode	f <sub>PP</sub>	0	-	25	MHz				
Frequency – Identification mode	f <sub>OD</sub>	0	-	400	kHz				
Clock low time	t <sub>WL</sub>	10	-	-	ns				
Clock high time	t <sub>WH</sub>	10	-	-	ns				
Clock rise time	t <sub>TLH</sub>	-	-	10	ns				
Clock low time	t <sub>THL</sub>	-	-	10	ns				
Inputs: CMD, DAT(referenced to CLK)									
Input setup time	t <sub>ISU</sub>	5	-	-	ns				
Input hold time	t <sub>IH</sub>	5	-	-	ns				
Outputs: CMD, DAT(referenced to CLK)									
Output delay time - Data Transfer mode	t <sub>ODLY</sub>	0	-	14	ns				
Output delay time,- Identification mode	t <sub>ODLY</sub>	0	-	50	ns				

- a. Timing is based on CL ≤ 40 pF load on CMD and Data.
- b. Min. (Vih) =  $0.7 \times VDDIO$  and max. (Vil) =  $0.2 \times VDDIO$



## 4.3 SDIO High Speed Mode Timing Diagram



Parameter	Symbol	Minimum	Typical	Maximum	Unit			
SDIO CLK (ALL values are referred to minimum VIH and maximum VIL <sup>b</sup> )								
Frequency – Data Transfer mode	f <sub>PP</sub>	0	-	50	MHz			
Frequency – Identification mode	f <sub>OD</sub>	0	-	400	kHz			
Clock low time	t <sub>WL</sub>	7	-	-	ns			
Clock high time	twn	7	-	-	ns			
Clock rise time	t <sub>TLH</sub>	-	-	3	ns			
Clock low time	t <sub>THL</sub>	-	-	3	ns			
Inputs: CMD, DAT(referenced to CLK)		•						
Input setup time	t <sub>ISU</sub>	6	-	-	ns			
Input hold time	t <sub>IH</sub>	2	-	-	ns			
Outputs: CMD, DAT(referenced to CLK)								
Output delay time - Data Transfer mode	todly	-	-	14	ns			
Output hold time	tон	2.5	-	-	ns			
Total system capacitance(each line)	C <sub>L</sub>			40	pF			

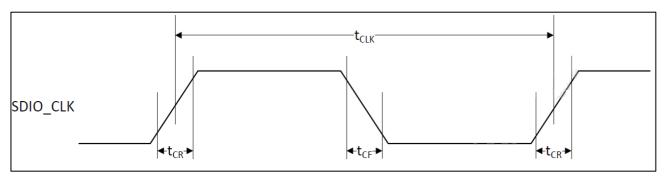
a. Timing is based on CL ≤ 40 pF load on CMD and Data.

b. Min. (Vih) =  $0.7 \times VDDIO$  and max. (Vil) =  $0.2 \times VDDIO$ 



## **4.4 SDIO Bus Timing Specifications in SDR Modes**

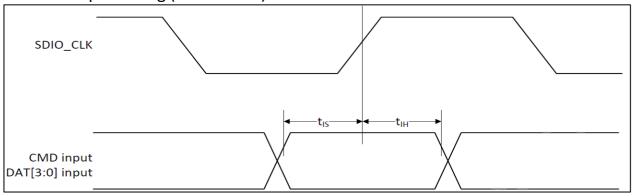
#### Clock timing (SDR Modes)



Parameter	Symbol	Minimum	Maximum	Unit	Comments	
	tclk	40	-	ns	SDR12 mode	
_		20	-	ns	SDR25mode	
		CCLK	10	-	ns	SDR50 mode
		4.8	-	ns	SDR104 mode	
-	t <sub>CR</sub> ,t <sub>CF</sub>	-	0.2 x t <sub>CLK</sub>	ns	$t_{CR}, t_{CF} < 2.00 \text{ ns (max) } @100 \text{MHz},$ $C_{CARD} = 10 \text{ pF}$ $t_{CR}, t_{CF} < 0.96 \text{ ns (max) } @208 \text{MHz},$ $C_{CARD} = 10 \text{ pF}$	
Clock duty	-	30	70	%	-	

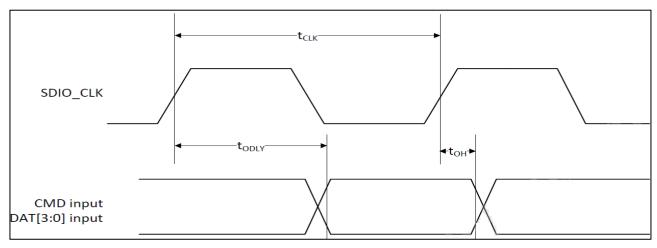


SDIO Bus Input timing (SDR Modes)



Symbol	Minimum	Maximum	Unit	Comments			
SDR104 Mode							
t <sub>IS</sub>	1.4	-	ns	C <sub>CARD</sub> = 10 pF, VCT= 0.975V			
t <sub>IH</sub>	0.80	-	ns	C <sub>CARD</sub> = 5 pF, VCT= 0.975V			
SDR50 Mode							
t <sub>IS</sub>	3.00	-	ns	C <sub>CARD</sub> = 10 pF, VCT= 0.975V			
t <sub>IH</sub>	0.80	-	ns	C <sub>CARD</sub> = 5 pF, VCT= 0.975V			

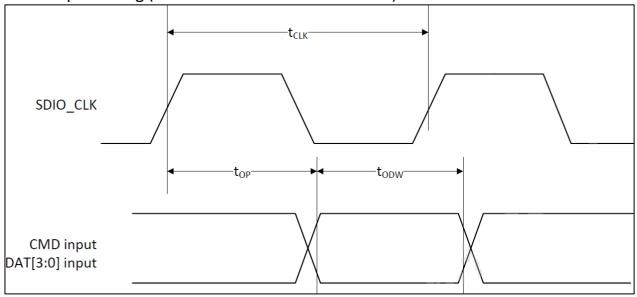
#### SDIO Bus output timing (SDR Modes up to 100MHz)



Symbol	Minimum	Maximum	Unit	Comments
t <sub>ODLY</sub>	-	7.5	ns	$t_{CLK} \ge 10 \text{ ns } C_L = 30 \text{ pF using driver type B for SDR50}$
t <sub>ODLY</sub>	-	14.0	ns	$t_{CLK} \ge 20 \text{ ns } C_L = 40 \text{ pF using for SR12, SDR25}$
t <sub>OH</sub>	1.5	-	ns	Hold time at the t <sub>ODLY</sub> (min) C <sub>L</sub> = 15 pF



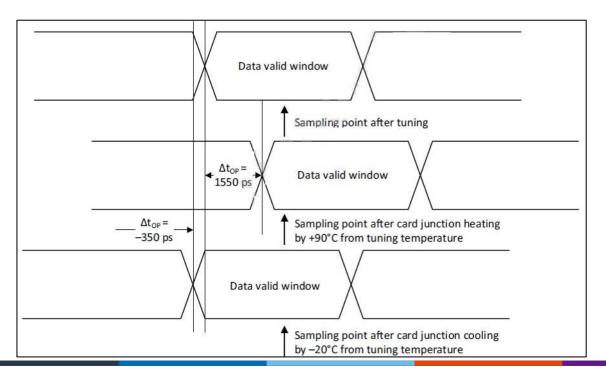
#### Card output timing (SDR Modes 100MHz to 208MHz)



Symbol	Minimum	Maximum	Unit	Comments
top	0	2	UI	Card output phase
$\triangle t_{OP}$	-350	+1550	ps	Delay variation due to temp. change after tuning
$\triangle t_{ODW}$	0.60	-	UI	t <sub>ODW</sub> = 2.88 ns @ 208MHz

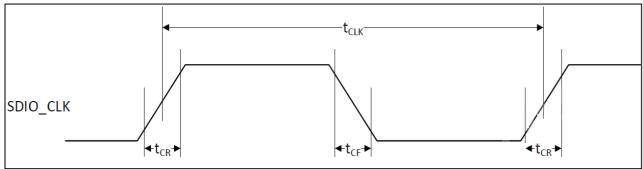
- $\triangle t_{OP}$  = +1550 ps for junction temperature of  $\triangle t_{OP}$  = 90 degrees during operation
- $\triangle t_{OP}$  = -350 ps for junction temperature of  $\triangle t_{OP}$  = -20 degrees during operation
- $\triangle t_{OP}$  = +2600 ps for junction temperature of  $\triangle t_{OP}$  = -20 to +125 degrees during operation

## **△top** Consideration for Variable Data Window (SDR 104 Mode)



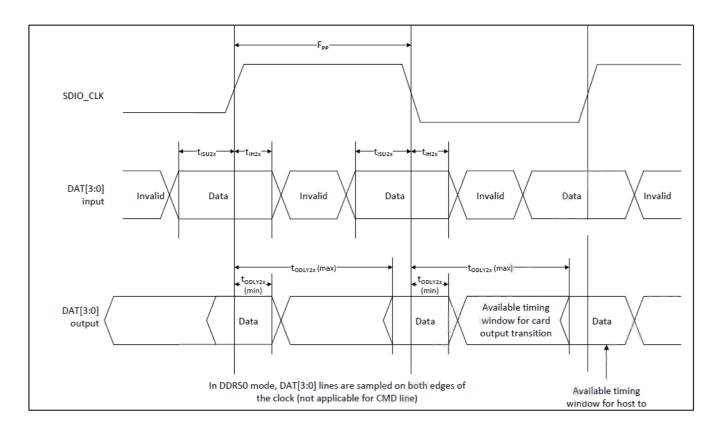


## 4.5 SDIO Bus Timing Specifications in DDR50 Mode



Parameter	Symbol	Minimum	Maximum	Unit	Comments
-	t <sub>CLK</sub>	20	-	ns	DDR50 mode
-	t <sub>CR</sub> ,t <sub>CF</sub>	-	0.2 x t <sub>CLK</sub>	ns	t <sub>CR</sub> ,t <sub>CF</sub> <4.00 ns(max) @ 50MHz C <sub>CARD</sub> = 10 pF
Clock duty	-	45	55	%	-

#### **Data Timing**





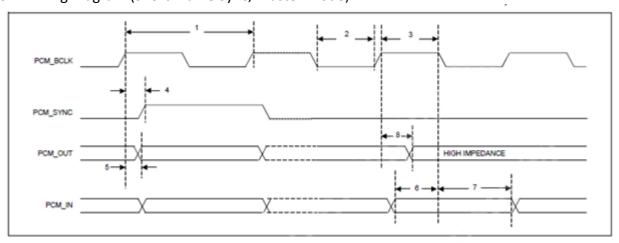
Parameter	Symbol	Minimum	Maximum	Unit	Comments	
Input CMD	<u>'</u>					
Input setup time	t <sub>ISU</sub>	6	-	ns	C <sub>CARD</sub> < 10 pF (1 Card)	
Input hold time	t <sub>IH</sub>	0.8	-	ns	C <sub>CARD</sub> < 10 pF (1 Card)	
Output CMD						
Output delay time	todly	-	13.7	ns	C <sub>CARD</sub> < 30 pF (1 Card)	
Output hold time	tон	1.5	-	ns	C <sub>CARD</sub> < 15 pF (1 Card)	
Input DAT						
Input setup time	t <sub>ISU2x</sub>	3	-	ns	C <sub>CARD</sub> < 10 pF (1 Card)	
Input hold time	t <sub>IH2x</sub>	0.8	-	ns	C <sub>CARD</sub> < 10 pF (1 Card)	
Output DAT	Output DAT					
Output delay time	t <sub>ODLY2x</sub>	-	7.5	ns	C <sub>CARD</sub> < 25 pF (1 Card)	
Output hold time	t <sub>ODLY2x</sub>	1.5	-	ns	C <sub>CARD</sub> < 15 pF (1 Card)	

#### 4.6 PCM Interface Description

The PCM Interface on the AP6275S can connect to linear PCM Codec devices in master or slave mode. In master mode, the AP6275S generates the PCM\_CLK and PCM\_SYNC signals, and in slave mode, these signals are provided by another master on the PCM interface and are inputs to the AP6275S. The configuration of the PCM interface may be adjusted by the host through the use of vendor-specific HCI commands.

#### Short Frame Sync, Master Modem

PCM Timing Diagram (Short Frame Sync, Master Mode)



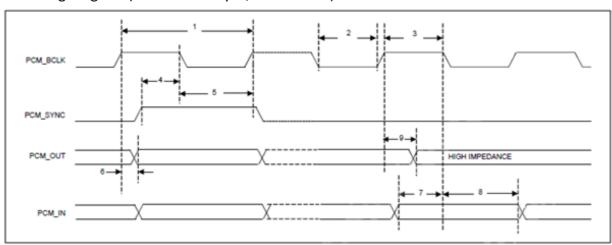


PCM Interface Timing Specifications (Short Frame Sync, Master Mode)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency		-	12	MHz
2	PCM bit clock low	41	-	-	ns
3	PCM bit clock high	41	-	-	ns
4	PCM_SYNC delay	0	-	25	ns
5	PCM_OUT delay	0	-	25	ns
6	PCM_IN setup	8	-	-	ns
7	PCM_IN hold	8	-	-	ns
0	Delay from rising edge of PCM_BCLK during	0		25	
8	last bit period to PCM_OUT becoming high impedance	0	-	25	ns

#### Short Frame Sync, Slave Mode

PCM Timing Diagram (Short Frame Sync, Slave Mode)



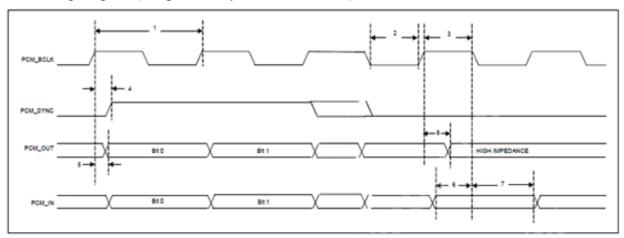
PCM Interface Timing Specifications (Short Frame Sync, Slave Mode)

Reference			Typical	Maximum	Unit
1	PCM bit clock frequency		-	12	MHz
2	PCM bit clock low	41	-	-	ns
3	PCM bit clock high	41	-	-	ns
4	PCM_SYNC setup	8	-	-	ns
5	PCM_SYNC hold	8	-	-	ns
6	PCM_OUT delay	0	-	25	ns
7	PCM_IN setup	8	-	-	ns
8	PCM_IN hold	8	-	-	ns
9	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	-	25	ns



#### Long Frame Sync, Master Mode

PCM Timing Diagram (Long Frame Sync, Master Mode)



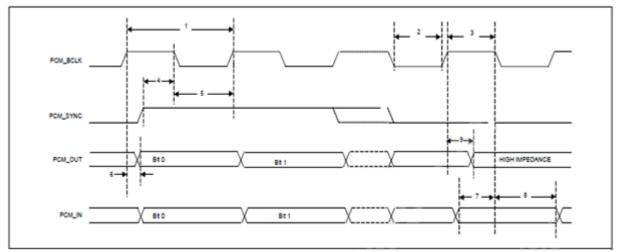
PCM Interface Timing Specifications (Long Frame Sync, Master Mode)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency		-	12	MHz
2	PCM bit clock low	41	-	-	ns
3	PCM bit clock high	41	-	-	ns
4	PCM_SYNC delay	0	-	25	ns
5	PCM_OUT delay	0	-	25	ns
6	PCM_IN setup	8	-	-	ns
7	PCM_IN hold	8	-	-	ns
8	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	-	25	ns



#### Long Frame Sync, Slave Mode

PCM Timing Diagram (Long Frame Sync, Slave Mode)



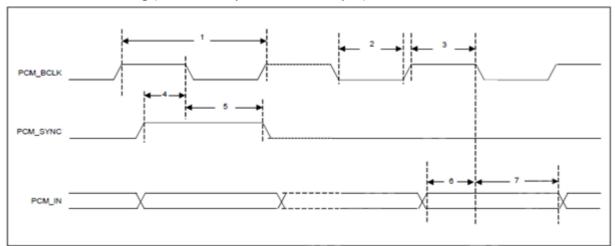
#### PCM Interface Timing Specifications (Long Frame Sync, Slave Mode)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency		-	12	MHz
2	PCM bit clock low	41	-	-	ns
3	PCM bit clock high	41	-	-	ns
4	PCM_SYNC setup	8	-	-	ns
5	PCM_SYNC hold	8	-	-	ns
6	PCM_OUT delay	0	-	25	ns
7	PCM_IN setup	8	-	-	ns
8	PCM_IN hold	8	-	-	ns
9	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	-	25	ns



#### Short Frame Sync, Burst Mode

PCM Burst Mode Timing (Receive Only, Short Frame Sync)

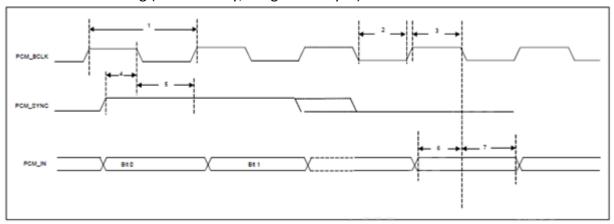


PCM Burst Mode (Receive Only, Short Frame Sync)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	-	-	24	MHz
2	PCM bit clock low	20.8	-	-	ns
3	PCM bit clock high	20.8	-	-	ns
4	PCM_SYNC setup	8	-	-	ns
5	PCM_SYNC hold	8	-	-	ns
6	PCM_IN setup	8	-	-	ns
7	PCM_IN hold	8	-	-	ns

#### Long Frame Sync, Burst Mode

PCM Burst Mode Timing (Receive Only, Long Frame Sync)





PCM Burst Mode	(Receive Only,	Long Frame Sync)
----------------	----------------	------------------

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	-	-	24	MHz
2	PCM bit clock low	20.8	-	-	ns
3	PCM bit clock high	20.8	-	-	ns
4	PCM_SYNC setup	8	-	-	ns
5	PCM_SYNC hold	8	-	-	ns
6	PCM_IN setup	8	-	-	ns
7	PCM_IN hold	8	-	-	ns

#### 4.7 UART Interface Description

The UART is a standard 4-wire interface (RX, TX, RTS, and CTS) with adjustable baud rates from 9600 bps to 4.0 Mbps. The interface features an automatic baud rate detection capability that returns a baud rate selection. Alternatively, the baud rate may be selected through a vendor-specific UART HCI command.

UART has a 1040-byte receive FIFO and a 1040-byte transmit FIFO to support EDR. Access to the FIFOs is conducted through the AHB interface through either DMA or the CPU. The UART supports the Bluetooth 5.0 UART HCI specification: H4, a custom Extended H4, and H5. The default baud rate is 115.2 Kbaud.

The UART supports the 3-wire H5 UART transport, as described in the Bluetooth specification (Three-wire UART Transport Layer). Compared to H4, the H5 UART transport reduces the number of signal lines required by eliminating the CTS and RTS signals.

The UART can perform XON/XOFF flow control and includes hardware support for the Serial Line Input Protocol (SLIP). It can also perform wake-on activity. For example, activity on the RX or CTS inputs can wake the chip from a sleep state.

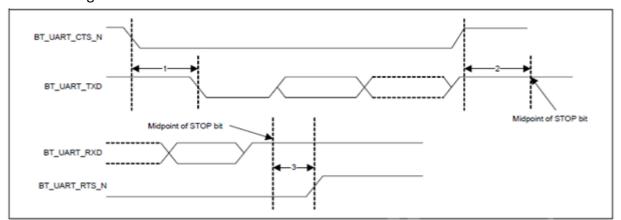
Normally, the UART baud rate is set by a configuration record downloaded after device reset, or by automatic baud rate detection, and the host does not need to adjust the baud rate. Support for changing the baud rate during normal HCI UART operation is included through a vendor-specific command that allows the host to adjust the contents of the baud rate registers. The UARTs operate correctly with the host UART as long as the combined baud rate error of the two devices is within ±2%.



#### **Example of Common Baud Rates**

Desired Rate	Actual Rate	Error(%)
4000000	4000000	0.00
3692000	3692308	0.01
3000000	3000000	0.00
2000000	2000000	0.00
1500000	1500000	0.00
1444444	1454544	0.70
921600	923077	0.16
460800	461538	0.16
230400	230796	0.17
115200	115385	0.16
57600	57692	0.16
38400	38400	0.00
28800	28846	0.16
19200	19200	0.00
14400	14423	0.16
9600	9600	0.00

#### **UART Timing**



#### **UART Timing Specifications**

Ref	Characteristics	Min.	Тур.	Max.	Unit
1	Delay time, BT_UART_CTS_N low BT_UART_TXD valid	1	1	1.5	Bit periods
2	Setup time, BT_UART_CTS_N high before midpoint of stop bit	ı	ı	0.5	Bit periods
3	Delay time, midpoint of stop bit BT_UART_RTS_N high	1	1	0.5	Bit periods



## **5. Power Consumption**

## **5.1 WLAN**

#### ■ 2.4GHz:

Test Mode	DUT Status	VBAT (3.3V)	VDDIO (1.8V)
802.11b	Continue TX(SISO)	365.95	4.52
11Mbps	Continue RX(SISO)	43.49	0.759
802.11b	Continue TX(SISO)	398.83	4.855
1Mbps	Continue RX(SISO)	41.08	0.743
	Continue TX (SISO)	211.9	3.46
802.11g	Continue RX(SISO)	43.63	0.759
54Mbps	Continue TX HT20(MIMO)	464.06	6.12
	Continue RX HT20 (MIMO)	52.54	0.846
	Continue TX (SISO)	313.86	4.6
802.11g	Continue RX(SISO)	42.17	0.753
6Mbps	Continue TX HT20(MIMO)	755.46	8.71
	Continue RX HT20 (MIMO)	50.65	0.84
	Continue TX (SISO)	197.58	3.44
802.11gn	Continue RX(SISO)	45.67	0.824
MCS7 HT-20	Continue TX HT20(MIMO)	299.014	5.97
	Continue RX HT20 (MIMO)	52.93	0.903
	Continue TX (SISO)	325.81	4.63
802.11gn	Continue RX(SISO)	43.42	0.803
MCS0 HT-20	Continue TX HT20(MIMO)	787.19	8.32
	Continue RX HT20 (MIMO)	51.51	0.901
	Continue TX (SISO)	345.6	4.43
802.11ax	Continue RX(SISO)	38.0	0.69
HE0 HE-20	Continue TX HT20(MIMO)	935.09	7.98
	Continue RX HT20 (MIMO)	42.5	0.791
	Continue TX (SISO)	160.8	3
802.11ax	Continue RX(SISO)	38.41	0.7
HE11 HE-20	Continue TX HT20(MIMO)	316.82	5.23
	Continue RX HT20 (MIMO)	42.4	0.791

(Unit: mA)



#### ■ 5GHz:

Test Mode	DUT Status	VBAT (3.3V)	VDDIO (1.8V)
	Continue TX (SISO)	257.35	3.48
802.11a	Continue RX(SISO)	53.13	0.793
54Mbps	Continue TX (MIMO)	410.00	6.09
	Continue RX(MIMO)	67.49	0.876
	Continue TX HT20(SISO)	248.27	3.42
802.11an	Continue RX HT20 (SISO)	53.09	0.793
MCS7_HT20	Continue TX HT20 (MIMO)	370.8	5.96
	Continue RX HT20 (MIMO)	67.33	0.876
	Continue TX HT40(SISO)	191.86	2.92
802.11an	Continue RX HT40 (SISO)	58.5	0.803
MCS7_HT40	Continue TX HT40 (MIMO)	313.21	5.04
	Continue RX HT40 (MIMO)	73.38	1.24
	Continue TX HT20(SISO)	222.76	3.29
802.11ac	Continue RX HT20 (SISO)	53.66	0.795
MCS8_VHT20	Continue TX HT20 (MIMO)	360.94	5.77
	Continue RX HT20 (MIMO)	68.12	0.879
	Continue TX HT40(SISO)	172.29	2.79
802.11ac	Continue RX HT40 (SISO)	59.3	0.805
MCS9_VHT40	Continue TX HT40 (MIMO)	278.54	4.79
	Continue RX HT40 (MIMO)	74.52	1.239
	Continue TX HT80(SISO)	155.27	2.84
802.11ac	Continue RX HT80 (SISO)	68.44	1.14
MCS9_VHT80	Continue TX HT80 (MIMO)	259.99	4.56
	Continue RX HT80 (MIMO)	86.47	1.21
	Continue TX (SISO)	318.9	4.43
802.11ax	Continue RX(SISO)	51.6	0.69
HE0 BW=20	Continue TX HE20(MIMO)	619.99	8.29
	Continue RX HE20 (MIMO)	67.33	0.77
802.11ax	Continue TX (SISO)	180	3.02
HE11 BW=20	Continue RX(SISO)	45.4	0.66



	Continue TX HE20(MIMO)	334.3	5.23
	Continue RX HE20 (MIMO)	65.3	0.76
802.11ax HE0 BW=40	Continue TX (SISO)	307.3	4.44
	Continue RX(SISO)	57	0.707
	Continue TX HE40(MIMO)	592.6	7.78
	Continue RX HE40 (MIMO)	75.32	0.797
	Continue TX (SISO)	166.3	2.98
802.11ax	Continue RX(SISO)	56.6	0.7
HE11 BW=40	Continue TX HE40(MIMO)	294.8	4.96
	Continue RX HE40 (MIMO)	71.9	0.792
	Continue TX (SISO)	314.35	4.08
802.11ax	Continue RX(SISO)	66.07	1.03
MCSO HE-80	HE-80 Continue TX HE80(MIMO)		7.03
	Continue RX HE80 (MIMO)	86.48	1.1
802.11ax MCS11 HE11-80	Continue TX (SISO)	173.2	2.92
	Continue RX(SISO)	60.75	1.04
	Continue TX HE80(MIMO)	291.4	4.56
	Continue RX HE80 (MIMO)	84.01	1.11

(Unit: mA)

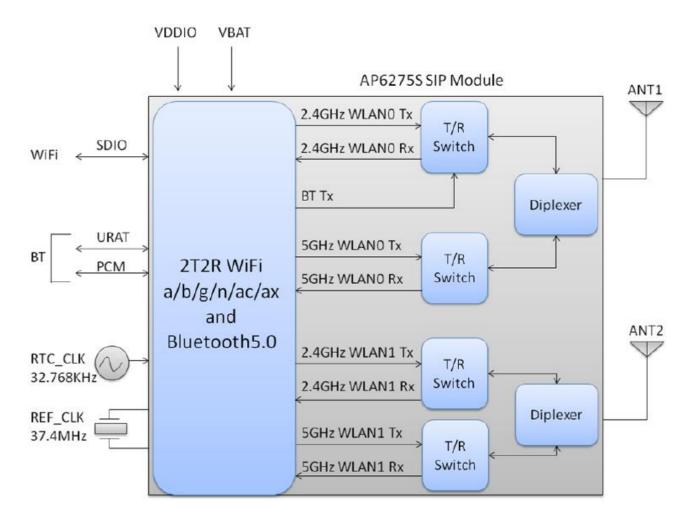
## 5.2 Bluetooth

Test Mode	DUT Status	VBAT (3.3V)	VDDIO (1.8V)
Bluetooth Mode	Continue TX	10.4	0.16
	Continue RX	9.4	0.16

(Unit: mA)



## 6. Block Diagram

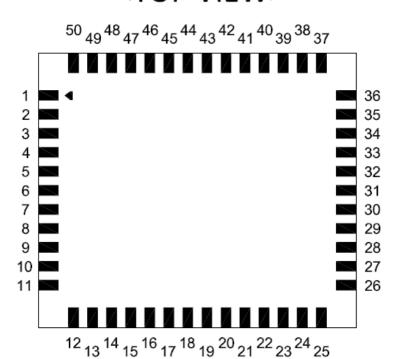




## 7. Pin Definition

#### 7.1 Pin Outline

## <TOP VIEW>



#### 7.2 Pin Table

NO	Name	Туре	Description
1	GND	_	Ground connections
2	WL_ANT0	I/O	RF I/O port0
3	GND	_	Ground connections
4	GND	_	Ground connections
5	GND	_	Ground connections
6	GND	_	Ground connections
7	GND	_	Ground connections
8	GND	_	Ground connections
9	WL_ANT1	I/O	RF I/O port1
10	GND	_	Ground connections
11	GND	_	Ground connections
12	NC	_	Floating (Don't connected to ground)
13	XTAL_IN	0	External Crystal in/ Single clock source in
14	XTAL_OUT	I	External Crystal out
15	WL_REG_ON	I	Low asserting reset for WiFi core

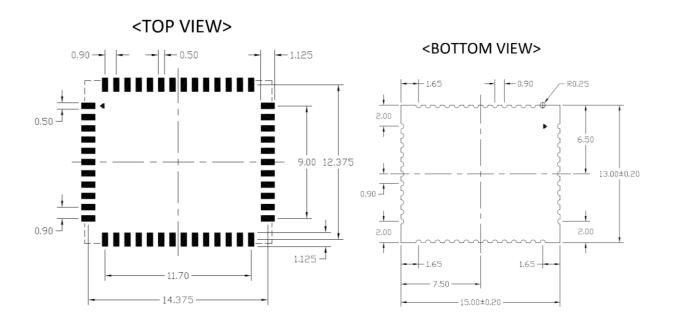


16	WL_HOST_WAKE/WL_GPIO_0	0	WLAN to wake-up HOST and WL_GPIO_0
17	SDIO_DATA_CMD	I/O	SDIO command line
18	SDIO_DATA_CLK	I/O	SDIO clock line
19	SDIO_DATA_3	I/O	SDIO data line 3
20	SDIO_DATA_2	I/O	SDIO data line 2
21	SDIO_DATA_0	I/O	SDIO data line 0
22	SDIO_DATA_1	I/O	SDIO data line 1
23	GND	_	Ground connections
24	NC	_	Floating (Don't connected to ground)
25	CBUCK_0P9	ı	Internal Buck voltage generation pin
26	CSR_VLX	0	Internal Buck voltage generation pin
27	GND	_	Ground connections
28	ASR_VLX	0	Internal Analog Buck voltage generation pin
29	ABUCK_1P12	ı	Internal Analog Buck voltage generation pin
30	GND	_	Ground connections
31	LPO	1	External Low Power Clock input (32.768KHz)
32	GND	_	Ground connections
33	WL_GPIO_10	I/O	WL_GPIO_10
34	VDDIO	Р	I/O Voltage supply input
35	WL_GPIO_11	I/O	WL_GPIO_11
36	VBAT	Р	Main power voltage source input
37	NC	_	Floating (Don't connected to ground)
38	BT_REG_ON	I	Low asserting reset for Bluetooth core
39	GND	_	Ground connections
40	BT_UART_TXD	0	Bluetooth UART interface
41	BT_UART_RXD	I	Bluetooth UART interface
42	BT_UART_RTS_N	0	Bluetooth UART interface
43	BT_UART_CTS_N	I	Bluetooth UART interface
44	BT_PCM_CLK	I/O	BT PCM clock; can be master(output) and slave(input)
45	BT_PCM_SYNC	I/O	BT PCM Sync signal; ; can be master(output) and slave(input)
46	BT_PCM_IN	1	BT PCM Data input
47	BT_PCM_OUT	0	BT PCM Data output
48	NC		NC
49	BT_WAKE	ļ	HOST wake-up Bluetooth device
50	BT_HOST_WAKE	0	Bluetooth device to wake-up HOST



## 8. Mechanical Specifications

## **8.1 Module Dimensions**

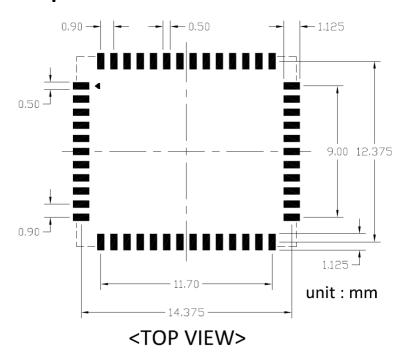




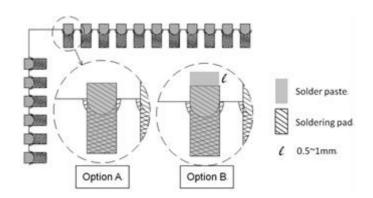
Note, X = 1.55mm



## 8.2 PCB Footprint



Solder paste layer design is generally the same as recommended footprint
If soldering quality with good wetting on upright side is essential for PQC, how to optimize the
aperture design in the stencil to adjust the amount of solder paste would be crucial.
In addition, a kind of stencil design with stepped thickness in partial area would be
considered if the thickness of stencil is about 0.1mm or thinner. Please optimize the stencil
design by manufacture engineer or contact SparkLAN FAE for assistance.





## 9. External clock reference

External LPO signal characteristics

Parameter	Specification	Units
Nominal input frequency	32.76	kHz
Frequency accuracy	+/-25	ppm
Duty cycle	30 -	%
Input signal amplitude	1.8±0.09	V
Signal type	Square-wave or sine-	-
Input impedance	>100k <5	Ω pF
Clock jitter (integrated over 300Hz – 15KHz)	<1	Hz
Output high voltage	0.7Vio - Vio	V

#### External 37.4MHz X'TAL characteristics

Parameter	Specification	Units
Nominal input frequency – F0	37.4	MHz
Frequency Tolerance - Δ F / F 0	+/- 5	ppm
(At 25°C +/- 3°C)		
Operation Temperature Range - Topr	-40 ~ + 85	°C
Freq. Stability(over operating temperature) - TC	+/- 10	ppm
Ref. to 25°C		
Load capacitance - CL	18	pF
Equivalent Series Resistance – ESR	Max. 60	Ω
Drive Level - DL	Typ. 50, Max. 100	uW
Insulation resistance – IR	Min. 500	MΩ
At 100Vdc		



#### 9.1 SDIO Interface Description

The module supports SDIO version 3.0 for all 1.8V 4-bit UHSI speeds: SDR50 (100 Mbps), SDR104 (208MHz) and DDR50 (50MHz, dual rates) in addition to the 3.3V default speed(25MHz) and high speed (50 MHz). It has the ability to stop the SDIO clock and map the interrupt signal into a GPIO pin. This 'out-of-band' interrupt signal notifies the host when the WLAN device wants to turn on the SDIO interface. The ability to force the control of the gated clocks from within the WLAN chip is also provided.

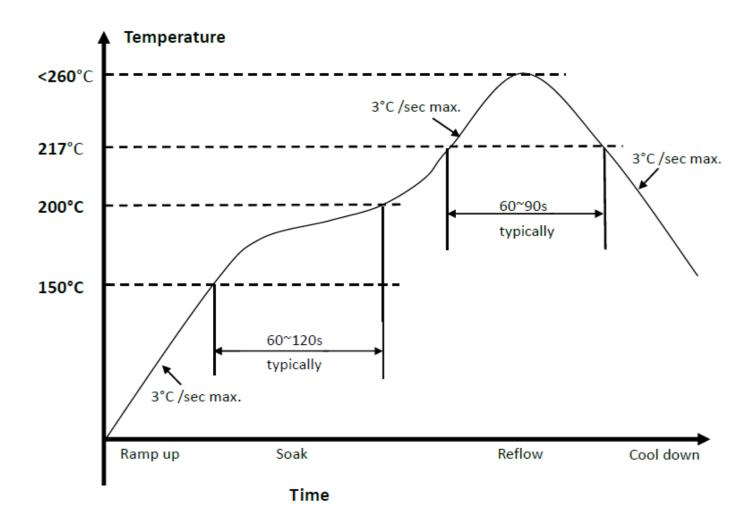
- Function 0 Standard SDIO function (Max BlockSize / ByteCount = 32B)
- Function 1 Backplane Function to access the internal System On Chip (SOC) address space (Max BlockSize / ByteCount = 64B)
- Function 2 WLAN Function for efficient WLAN packet transfer through DMA (Max BlockSize/ByteCount=512B)

#### **SDIO Pin Description**

SD 4-Bit Mode		
DATA0	Data Line 0	
DATA1	Data Line 1 or Interrupt	
DATA2	Data Line 2 or Read Wait	
DATA3	Data Line 3	
CLK	Clock	
CMD	Command Line	



## 10. Recommended Reflow Profile



- 1. Referred to IPC/JEDEC standard
- 2. Peak Temperature: <260°C
- 3. Cycle of Reflow: 2 times max.
- 4. Adding Nitrogen (N2) to implement 2000ppm or less of oxygen concentration during reflow process is recommended.
- 5. If the shelf time is exceeded, be sure baking step to remove the moisture from the component



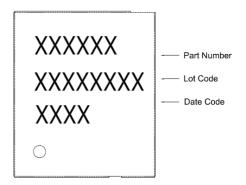
## 10.1 Caution for SMT Preparation

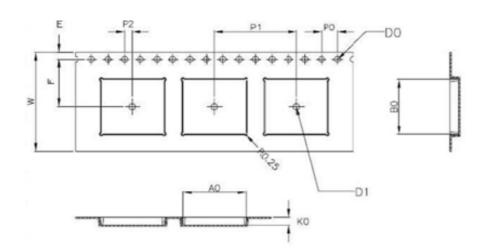
Moisture Sensitivity Level: 4

- 1. Calculated shelf life in sealed bag: 12 months at <40 $^{\circ}$ C and <90% relative humidity (RH).
- 2. Peak package body temperature: 250°℃.
- 3. After bag was opened, devices that will be subjected to reflow solder or other high temperature process must be
  - a) Mounted within: 72 hours of factory conditions  $\leq 30^{\circ}$ C/60%RH or
  - b) Stored per J-STD-033
- 4. Devices require bake before mounting, if:
  - a) Humidity Indicator Card reads> 10% for level 2a 5a devices or >60% for level 2 devices when read at 23+5  $^{\circ}\mathrm{C}$
  - b) 3a or 3b are not met.
- 5. If baking is required, refer to IPC/JEDEC J-STD-033 for bake procedure.



## 11. Package Information

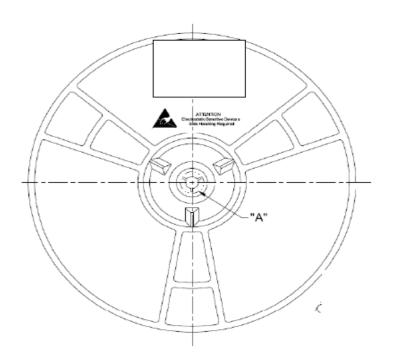


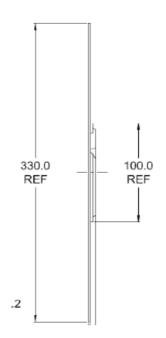


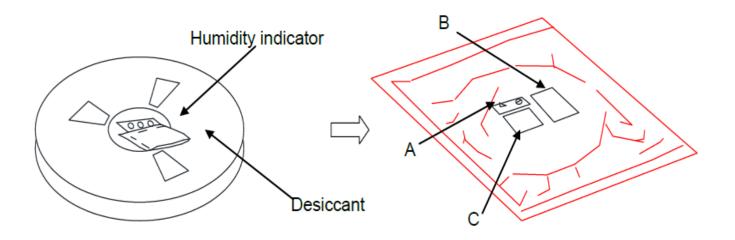
W	24.00±0.30		
A0	15.30±0.10		
В0	13.30±0.10		
КО	2.00±0.10		
Е	1.75±0.10		
F	11.50±0.10		
P0	4.00±0.10		
P1	20.00±0.10		
P2	2.00±0.10		
D0	1.50 +0.10 -0.00		
D1	¢ 1.50MIN		

- 1. 10 sprocket hole pitch cumulative tolerance ±0.20.
- 2. Carrier camber is within 1 mm in 250 mm.
- 3. Material: Black Conductive Polystyrene Alloy.
- 4. All dimensions meet EIA-481-D requirements.
- 5. Thickness: 0.30±0.05mm.
- 6. Component load per 13"reel: 1000 pcs

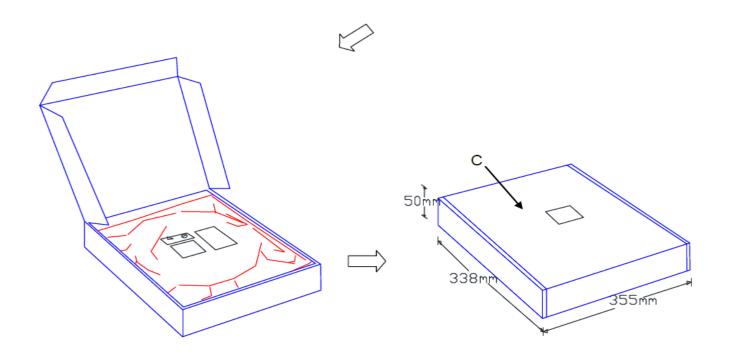


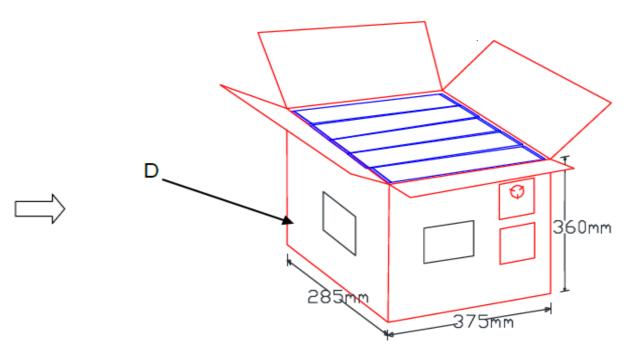












Note: 1 tape reel = 1 box = 1,000pcs 1 Carton = 5 box = 5,000pcs



## **12.** Ordering Information

Product Name	Part Number	Description
AP6275S	R9701A20001	11ax/ac/a/b/g/n 2T2R WiFi + BT5.0 Combo Sip Module