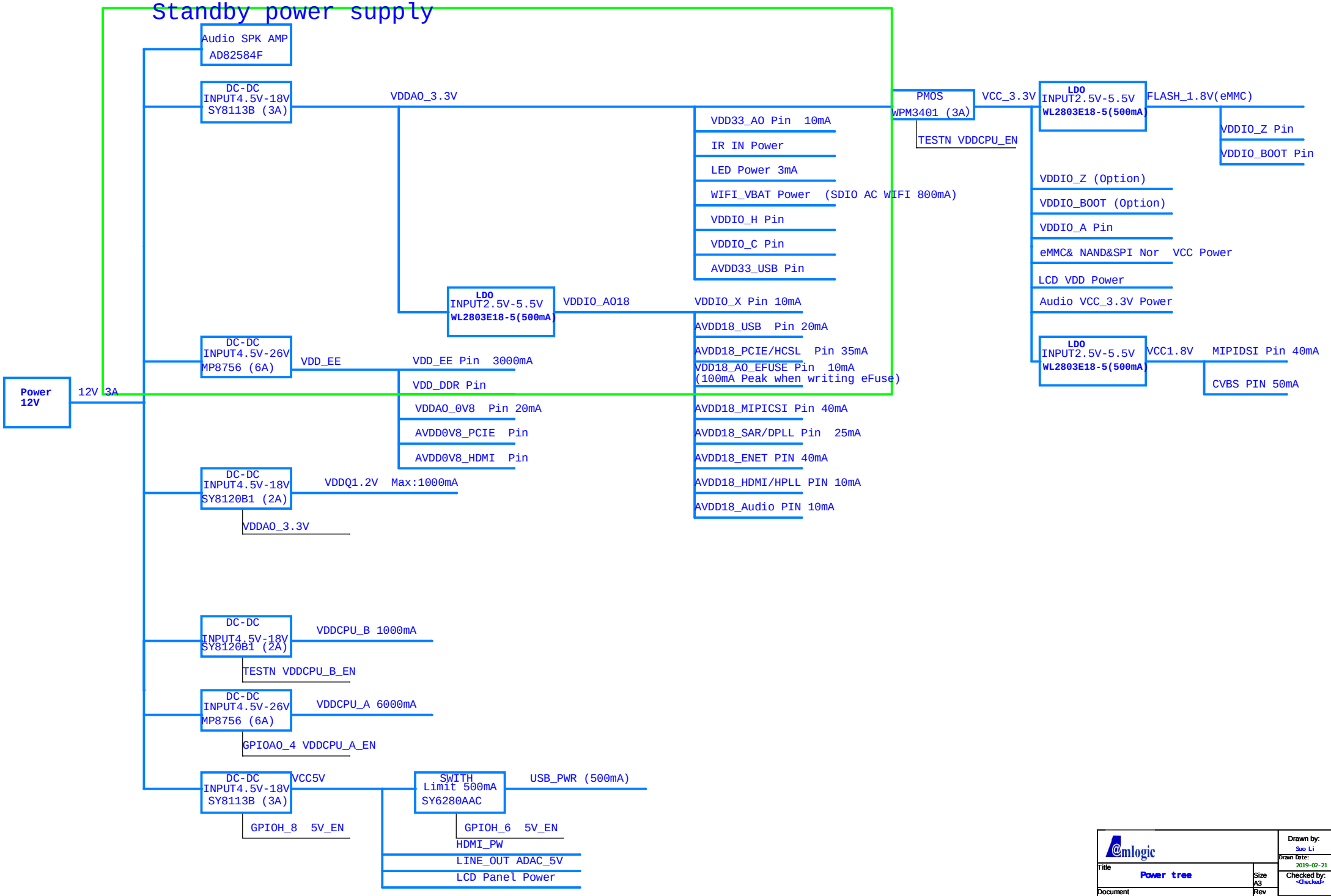
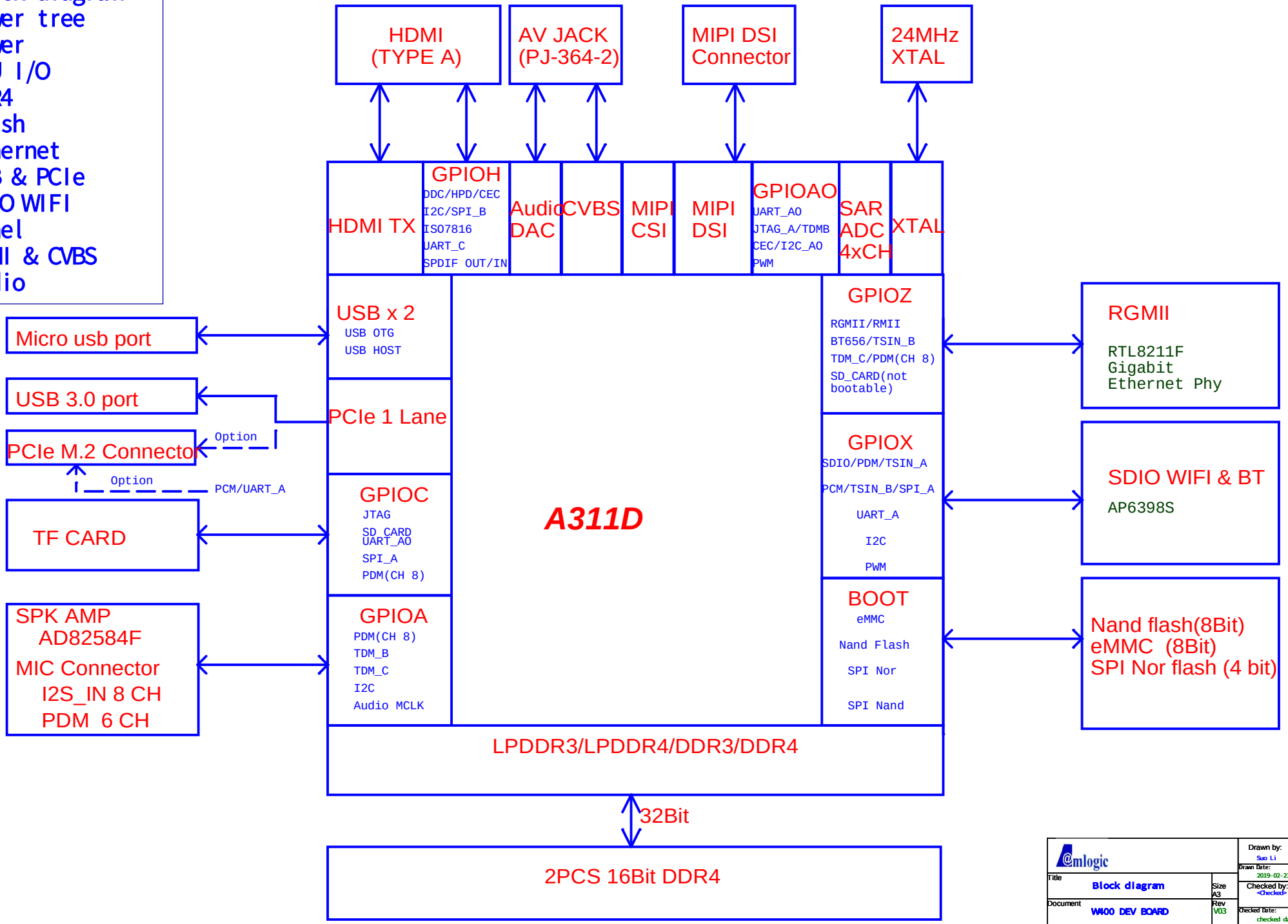
Standby power supply



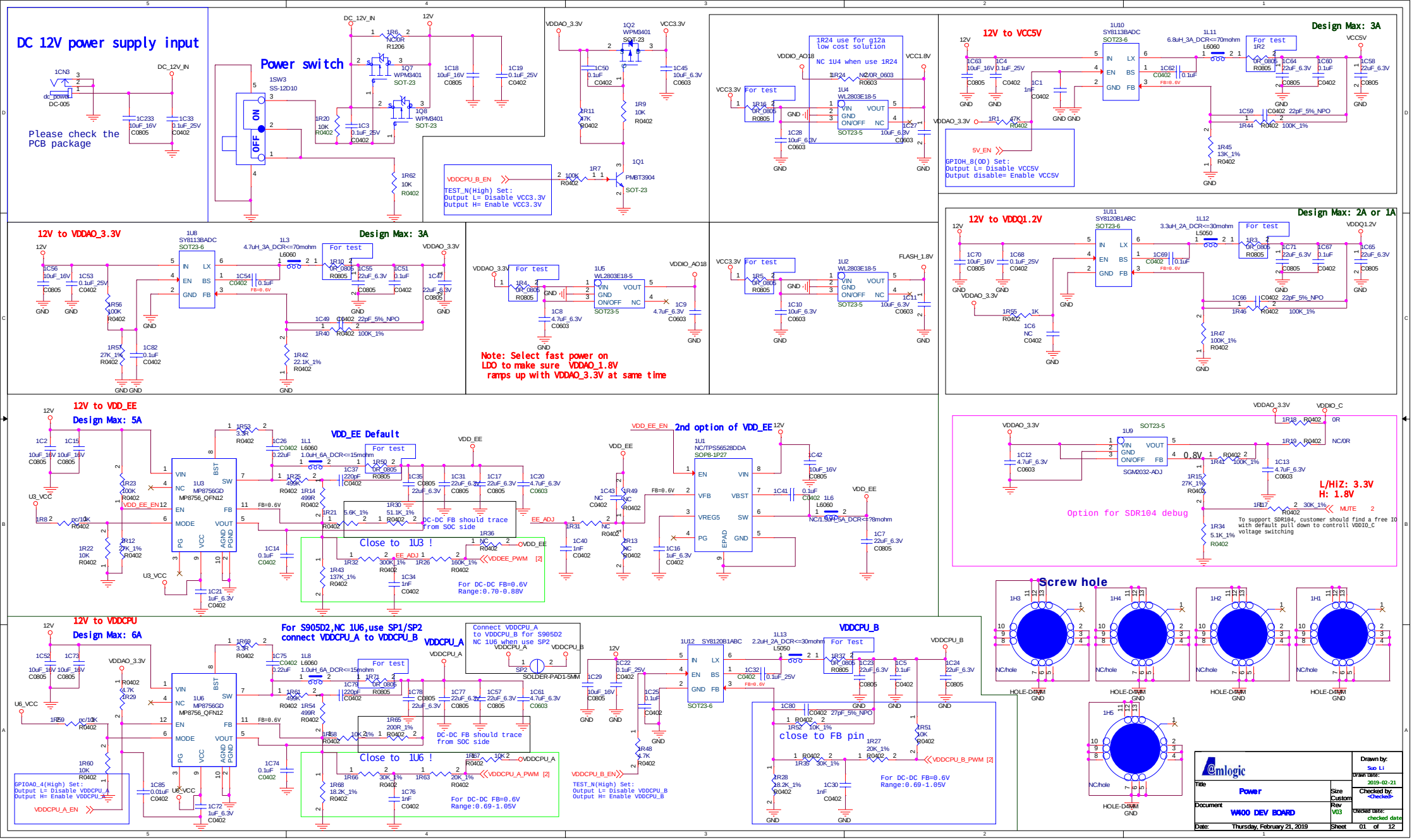
Amlogic		Drawn by: Suo Li
Title: Power tree	Size: A3	Drawn Date: 2019-02-21
Document: W400 DEV BOARD	Rev: V03	Checked by: <Checked>
Date: Thursday, February 21, 2019	Sheet: 00 of 12	Checked Date: checked date

A311D Diagram

PAGE INDEX



Amlogic			Drawn by: Suo Li
Title: Block diagram		Size: A3	Drawn Date: 2019-02-21
Document: W400 DEV BOARD		Rev: V03	Checked by: <Checked>
Date: Thursday, February 21, 2019	Sheet: 00 of 12		Checked Date: checked date


DC 12V power supply input
Please check the PCB package
Power switch
ON
OFF
VDDCPU_B_EN
TEST_N(High) Set:
Output L= Disable VCC3.3V
Output H= Enable VCC3.3V
1R24 use for g12a low cost solution
NC 1U4 when use 1R24
12V to VCC5V
Design Max: 3A
5V_EN
GPIOH_8(OD) Set:
Output L= Disable VCC5V
Output disable= Enable VCC5V
12V to VDDAO_3.3V
Design Max: 3A
12V to VDDQ1.2V
Design Max: 2A or 1A
Note: Select fast power on LDO to make sure VDDAO_1.8V ramps up with VDDAO_3.3V at same time
12V to VDD_EE
Design Max: 5A
VDD_EE Default
2nd option of VDD_EE
Close to 1U3 !
DC-DC FB should trace from SOC side
For DC-DC FB=0.6V Range:0.70-0.88V
Option for SDR104 debug
To support SDR104, customer should find a free IO with default pull down to controll VDDIO_C voltage switching
L/HiZ: 3.3V
H: 1.8V
Screw hole
12V to VDDCPU
Design Max: 6A
For S905D2,NC 1U6,use SP1/SP2 connect VDDCPU_A to VDDCPU_B
VDDCPU_A
VDDCPU_B
Close to 1U6 !
close to FB pin
GPIOAO_4(High) Set:
Output L= Disable VDDCPU_A
Output H= Enable VDDCPU_A
VDDCPU_A_EN
TEST_N(High) Set:
Output L= Disable VDDCPU_B
Output H= Enable VDDCPU_B
For DC-DC FB=0.6V Range:0.69-1.05V
Amlogic
Title: Power
Document: WH00 DEV BOARD
Size: Custom
Rev: V03
Drawn by: Suo Li
Drawn date: 2019-02-21
Checked by: <checked>
Checked date: checked date
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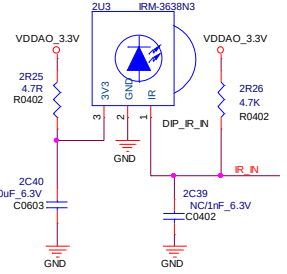
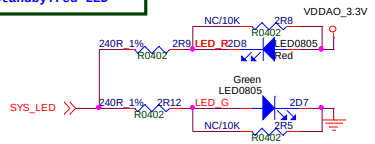
Sheet 01 of 12

Remote control receiver

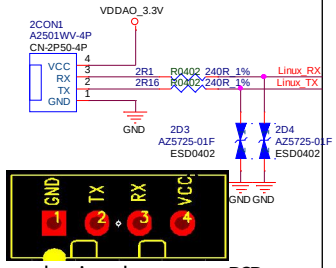


System LED

Logic	LED function
SYS_LED=1	System running: green LED
SYS_LED=0	Standby:red LED

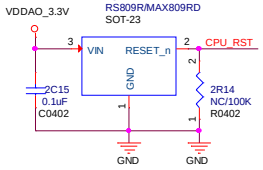


For linux debug

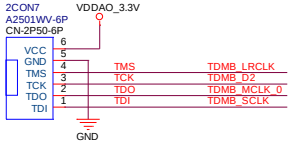


mark signal name on PCB

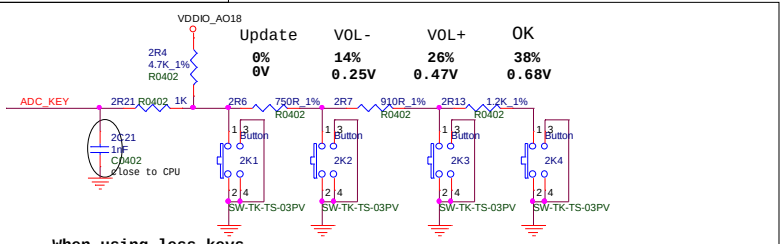
CPU reset



ARM JTAG Debug



mark signal name on PCB

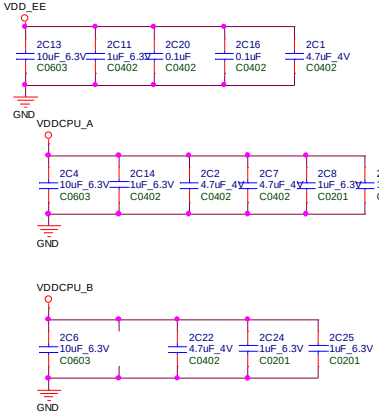


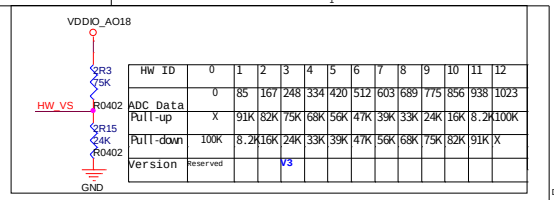
When using less keys, delete right side buttons. Only the left key works when multiple keys pressed key like "OK", and other special keys should be placed to the right side

Please follow below resistor value

Key	1	2	3	4	5	6	7	8
Value	0%	14%	26%	38%	50%	62%	75%	87%
Resister		750R 1%	910R 1%	1.2K 1%	1.8K 1%	3K 1%	6.2K 1%	18K 1%

Pull-up: 4.7K 1% max 8 ADC keys

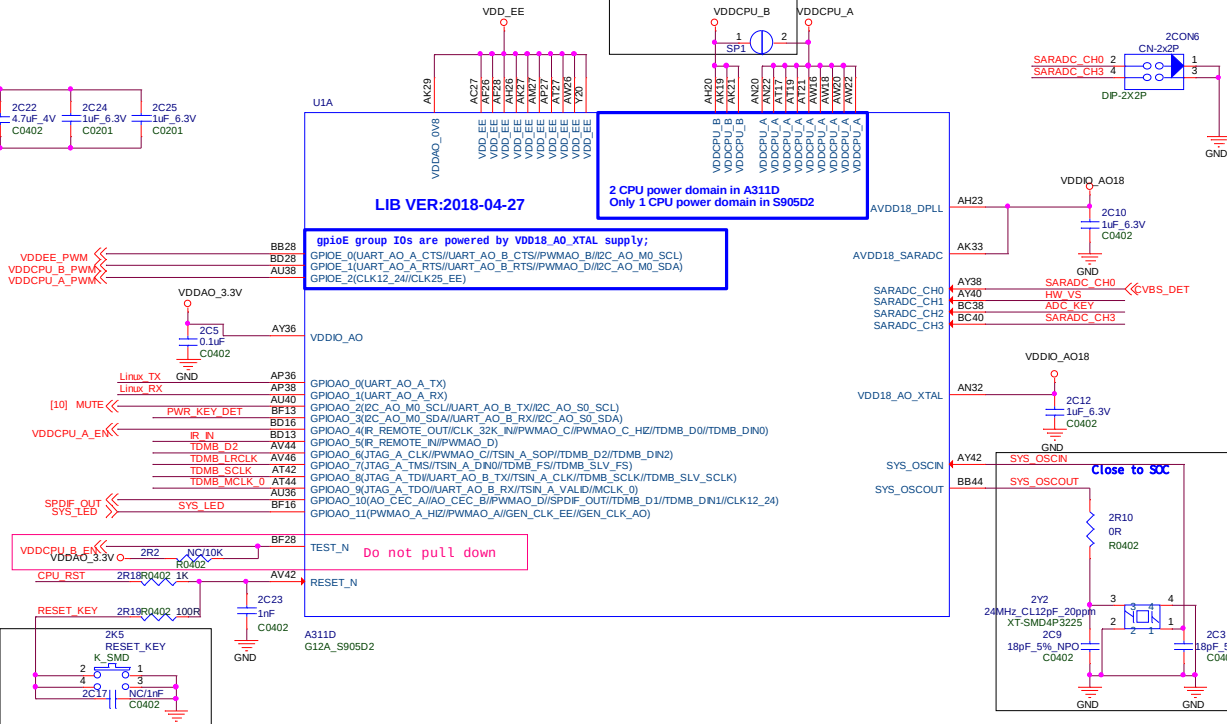




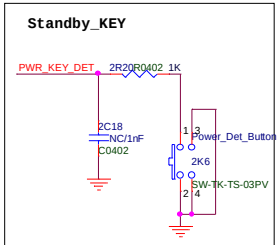
HW ID	0	1	2	3	4	5	6	7	8	9	10	11	12
ADC Data	0	85	167	248	334	420	512	603	689	775	856	938	1023
Pull-up	X	91K	82K	75K	68K	56K	47K	39K	33K	24K	16K	8.2K	100K
Pull-down	100K	8.2K	16K	24K	33K	39K	47K	56K	68K	75K	82K	91K	X
Version	Reserved			V3									

Connect VDDCPU_A to VDDCPU_B for S905D2

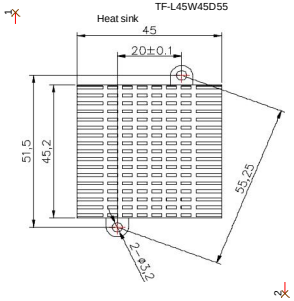
NC 1U6 when use SP1



Standby_KEY



Heat sink



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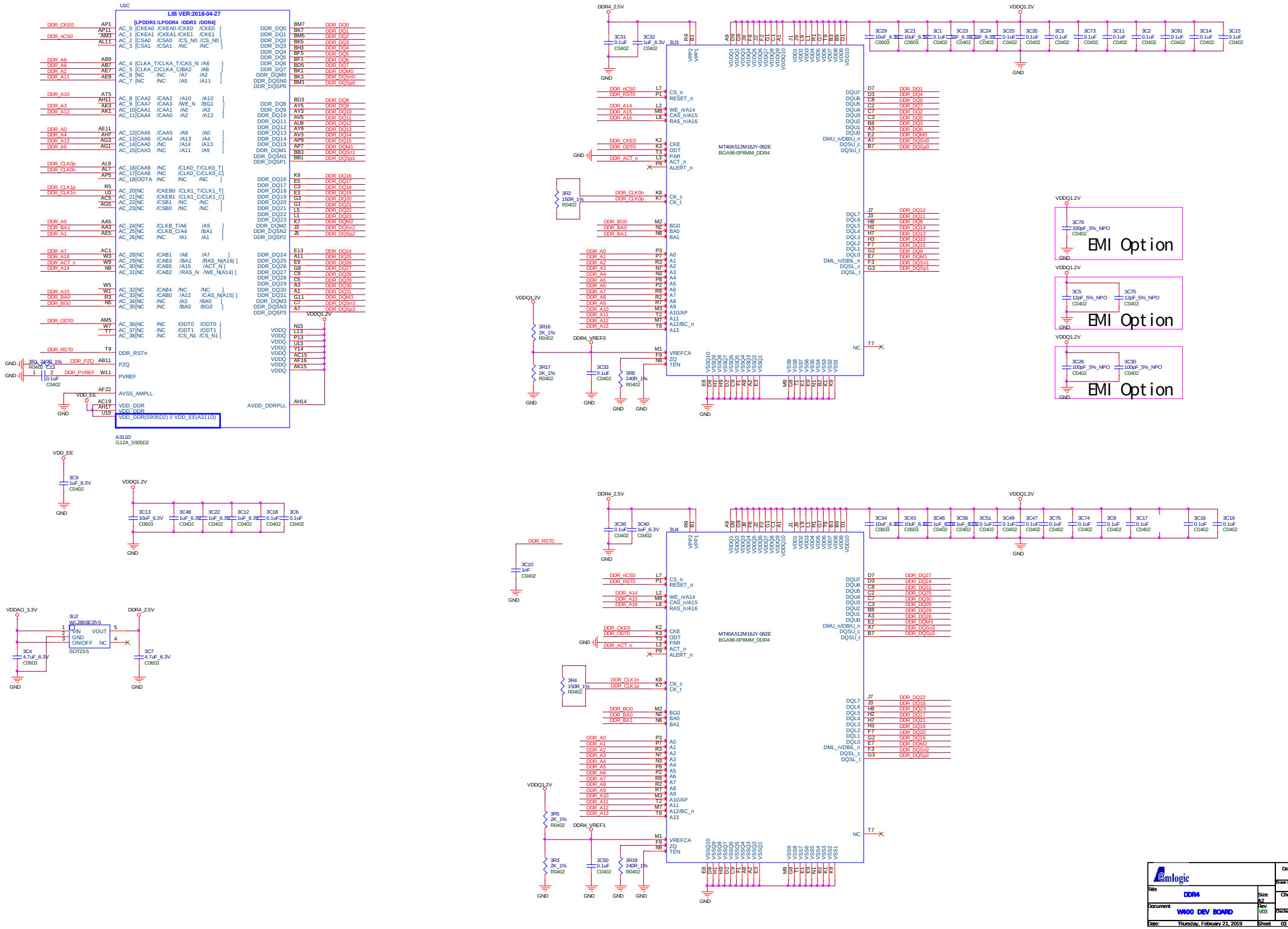
Title	CPU I/O	Drawn Date:	2019-02-21
		Size	Custom
		Checked by:	<Checked>
Document	W400 DEV BOARD	Rev	V03
		Checked Date:	checked date
Date:	Thursday, February 21, 2019	Sheet	02 of 12


U1C
LIB VER:2018-04-27
[LPDDR3 /LPDDR4 /DDR3 /DDR4]
A311D
G12A_S905D2
VDD_DDR(S905D2) // VDD_EE(A311D)
MT40A512M16JY-062E
BGA96-0P8MM_DDR4
DDR4_VREF0
DDR4_VREF1
DDR4_2.5V
VDDQ1.2V
VDD_EE
VDDAO_3.3V
EMI Option
WL2803E25-5
SOT23-5
Amlogic
DDR4
W400 DEV BOARD
Thursday, February 21, 2019

eMMC/iNAND

PCB Decal:169pin balls type(BGA)

VCC = 2.7 -3.6V

4U7A
eMMC_FLASH
BGA169-INAND

eMMC V5.1

Do not route over RFU & VFS pins

4U7B
eMMC_FLASH
BGA169-INAND

eMMC V5.1

eMMC NC PIN FOR ALLEGRO

U1B

LIB VER:2018-04-27

VDDIO_BOOT
BOOT_0(EMMC_D0)
BOOT_1(EMMC_D1)
BOOT_2(EMMC_D2)
BOOT_3(EMMC_D3//NOR_HOLD)
BOOT_4(EMMC_D4//NOR_D)
BOOT_5(EMMC_D5//NOR_Q)
BOOT_6(EMMC_D6//NOR_C)
BOOT_7(EMMC_D7//NOR_WP)
BOOT_8(EMMC_CLK//NAND_WEN_CLK)
BOOT_9(NAND_ALE)
BOOT_10(EMMC_CMD//NAND_CLE)
BOOT_11(NAND_CE0)
eMMC reset GIPO BOOT_12(NAND_REN_WR)
BOOT_13(EMMC_NAND_DQS)
BOOT_14(NAND_RB0//NOR_CS)
BOOT_15(NAND_CE1)

A311D
G12A_S905D2

Note:
Nand flash: 4C1=NC
eMMC: Reserved 4C1=1nF for esd

SPI Nor flash

4U8
NC
SOIC-8-150MIL

SPI Flash:4R3/4R12 NC
NO SPI Flash:4R3/4R12 ON

Nand(TSOP)

4U1 NC/NAND-FLASH TSOP-48

Normal // Micron ONFI // Toshiba

Close to nand VCC pin
Close to 4CON1

Power on config

BOOT_4[NAND_D4]: 0= SPI NAND Boot first
BOOT_5[NAND_D5]: 0= USB Boot first
BOOT_6[NAND_D6]: 0= SPI NOR Boot first

Close to branch ponit

When using daughter, these resistors NC

4CON1

DC3_1P27_2X13P_SMT
DC3_1P27_2X13P_SMT-M

Fool proof design for 4CON1
Place on the opposite of 4CON1 assemble

eMMC/NAND daughter board config

	4R21	4R29	4R25	4R24
eMMC	0R	NC	NC	NC
Nand	NC	0R	0R	0R

Title	Flash
Size	A3
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Checked by:	<Checked>
Checked Date:	checked date

U1G

LIB VER:2018-04-27

ENET_TXP
ENET_TXN
ENET_RXP
ENET_RXN
ENET_ATP
ENET_EXTRES
AVSS_ENETPLL
AVDD18_ENET
VDDIO_Z

GPIOZ_0(ETH_MDIO//ISO7816_CLK//BT656_A_VS//I2C_EE_M0_SDA)
GPIOZ_1(ETH_MDC//ISO7816_DATA//BT656_A_HS//I2C_EE_M0_SCL)
GPIOZ_2(ETH_RGMII_RX_CLK//TSIN_B_VALID//TDMC_D0//TDMC_DIN0//PDM_DIN0//SDCARD_D0)
GPIOZ_3(ETH_RX_DV//TSIN_B_SOP//BT656_A_CLK//TDMC_D1//TDMC_DIN1//PDM_DIN1//SDCARD_D1)
GPIOZ_4(ETH_RXD0//TSIN_B_DIN0//BT656_A_DIN0//TDMC_D2//TDMC_DIN2//PDM_DIN2//SDCARD_D2)
GPIOZ_5(ETH_RXD1//TSIN_B_CLK//BT656_A_DIN1//TDMC_D3//TDMC_DIN3//PDM_DIN3//SDCARD_D3)
GPIOZ_6(ETH_RXD2_RGMII//TSIN_B_FAIL//BT656_A_DIN2//TDMC_FS//TDMC_SLV_FS//PDM_DCLK//SDCARD_CLK)
GPIOZ_7(ETH_RXD3_RGMII//TSIN_B_DIN1//BT656_A_DIN3//TDMC_SCLK//TDMC_SLV_SCLK//I2C_EE_M0_SDA//SDCARD_CMD)

CARD port on GPIOZ is not bootable

GPIOZ_8(ETH_RGMII_TX_CLK //TSIN_B_DIN2//BT656_A_DIN4//MCLK_1//I2C_EE_M0_SCL)
GPIOZ_9(ETH_TXEN //TSIN_B_DIN3//BT656_A_DIN5)
GPIOZ_10(ETH_TXD0 //TSIN_B_DIN4//BT656_A_DIN6)
GPIOZ_11(ETH_TXD1 //TSIN_B_DIN5//BT656_A_DIN7)
GPIOZ_12(ETH_TXD2_RGMII//TSIN_B_DIN6)
GPIOZ_13(ETH_TXD3_RGMII//TSIN_B_DIN7//GEN_CLK_EE)

GPIOZ_14 (OD3.3V) (ETH_LINK_LED//I2C_EE_M2_SDA)
GPIOZ_15 (OD3.3V) (ETH_ACT_LED//I2C_EE_M2_SCL)

G12A_S905D2
A311D

CT_VCC

5T17 H1601CG TS8121C

TD+ TCT TD- NC0 NC1 RD+ RCT RD-
TX+ TX- TCM NC3 NC2 RX+ RX- RCM

MDI_TP MDI_TN MDI_RP MDI_RN

5J1 RJ45-LED-LYRG RJ45LED-LY-RG

Left-Yellow Right-Green

ETH LED

5D13 Yellow LED0805
5D12 Green LED0805

RJ45_VCC VCC3.3V

RGMII_RST# RGMII_INT

Internal 100M with LED: 5R46-47 -> 510ohm
1000M ETH: 5R46-47 -> NC

	5R28-29/5R33/5R35 5R49	5R30-31/5R32/5R34 5R50
GRMII/DVP/TSIN	0R	NC
LCD/TOUCH	NC	0R

	5R36-38/5R42-43	5R39-41/5R44-45 /5R55/5R53
GRMII/DVP/TSIN	0R	NC
Mipi CSI camera	NC	0R

5U2 AZ1513-04S SOT23-6

MDI-RP MDI-TN MDI-RN MDI-TP

5U1 RTL8211F-CG QFN40-PT04-S65mm

RGMII (10/100/1000Mbps)

Decouple pin 21
Decouple pins 3, 8, 38
Decouple pins 11,40

5Y2 25MHz_CL12pF_20ppm XT-SMD4P3225

GXTAL_O GXTAL_IN CLKOUT

LED2_CFG_LDO1 LED1_CFG_LDO0 LED0_CFG_EXT INTB_PMEB

RXCLK_PHYAD1 RXCTL_PHYAD2 RXD0_RXDLY RXD1_TXDLY RXD2_PLLOFF RXD3_PHYAD0

Data from MAC to PHY

TXCLK TXEN TXD0 TXD1 TXD2 TXD3 MDIO MDC PHY_RST

5J3 G11T1001 T-24P-PT50mil Transformer

MDI-BI_DAP_TXP MDI-BI_DAN_TXN MDI-BI_DBP_RXP MDI-BI_DBN_RXN MDI-BI_DCP MDI-BI_DCN MDI-BI_DDP MDI-BI_DDN

The transformer center tap must be short together

5J2 RJ45_Tab-Down-With-LED RJ45_TAB-DOWN-8P

PCB No.

BI_DAP_TXP BI_DAN_TXN BI_DBP_RXP BI_DCP BI_DCN BI_DBN_RXN BI_DDP BI_DDN

Left-Green Right-Yellow

LED1_CFG_LDO0 LED2_CFG_LDO1

Internal 100M with LED: 5R82 -> 0ohm , 5R81-> NC
1000M ETH: 5R82 -> NC, 5R81-> 0ohm

When use 5CON3, component of this part should NC

GRMII/DVP/TSIN debug

5CON3 A2005WV-N-2X13P_Debug CN-2P00-2X13P-L

Close to PHY

Phy address 3'b001(default)

PLL Mode(Enable/Disable)

Pull-up to disable PLL @ ALDPS mode.

TXC/RXC Delay config

Pull-up for additional 2ns delay to TXC/RXC for data latching

External 1.8V(default)

ETH_VDDIO(DVDD_RG) Voltage config

ETH_VDDIO	
USE External 3.3V	5R59->4.7K , 5R15->4.7K , 5R69-> NC
USE External 1.8V(default)	5R59->4.7K , 5R15->4.7K , 5R69-> 4.7K

LED Settings

Pin name	Logical	LED IO active&Link/blinking(TX/RX)	
LED1/CFG_LDO0	1'b0	LED[1] H	100Mbps
LED2/CFG_LDO1	1'b1	LED[2] L	1000Mbps

Amlogic	Drawn by: Suo Li
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limit 500mA output current

GPIOH_6(down) Set:
Output L= Disable USB Power
Output H= Enable USB Power

Need to check pacakge
A425-720490-001

USB differential signal impedance : 90 ohm

Layout stack

Should close to branch ponit

USB 3.0 :6C8/6C13/6R11/6R12 should placed
6C20/6C27/6R10/6R9 should NC

PCIe :6C8/6C13/6R11/6R12 should NC
6C20/6C27/6R10/6R9 should placed

SD card

Close to CPU

Close to SD card

When use SDIO WIFI,6R16/67,6RN1/RN2 NC
When use PCIe WIFI,6R16/67,6RN1/RN2 placed

Title	USB & PCIe
Size	C
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Checked by:	<Checker>
Checked Date:	checked date

AMPAK WIFI: 7R3 0R,7R1 NC
PCIe WIFI and RTL WIFI: 7R3 NC,7R1 0R

VDDIO_X
VDDAO_3.3V
VDDIO_AO18
NC/0R R0402 7R1
0R R0402 7R3
U1F
7C6 0.1uF C0402
7C1 1uF_6.3V C0402
GND

LIB VER:2018-04-27

VDDIO_X BF25

GPIOX_0(SDIO_D0//PDM_DIN0//TSIN_A_DIN0) BM32 WIFI_SD_D0
GPIOX_1(SDIO_D1//PDM_DIN1//TSIN_A_SOP) BK32 WIFI_SD_D1
GPIOX_2(SDIO_D2//PDM_DIN2//TSIN_A_VALID) BK34 WIFI_SD_D2
GPIOX_3(SDIO_D3//PDM_DIN3//TSIN_A_CLK//PWM_D) BH34 WIFI_SD_D3
GPIOX_4(SDIO_CLK//PDM_DCLK) BM36 7R11 0R R0402 WIFI_SD_CLK
GPIOX_5(SDIO_CMD//MCLK_1//PWM_C) BK38 WIFI_SD_CMD

GPIOX_6(PWM_A//UART_EE_B_TX//PWM_D) BK40 WIFI_PWREN → WIFI_PWREN
GPIOX_7(PWM_F//UART_EE_B_RX//PWM_B) BH40 WIFI_WAKE_HOST → WIFI_WAKE_HOST

GPIOX_8(TDMA_D1//TDMA_DIN1//TSIN_B_SOP//SPI_A_MOSI//ISO7816_CLK//PWM_C) BB34 BTPCM_DIN → BTPCM_DIN [7]
GPIOX_9(TDMA_D0//TDMA_DIN0//TSIN_B_VALID//SPI_A_MISO//ISO7816_DATA) BD34 BTPCM_DOUT → BTPCM_DOUT [7]
GPIOX_10(TDMA_FS//TDMA_SLV_FS//TSIN_B_DIN0//SPI_A_SS0//I2C_EE_M1_SDA) BD31 BTPCM_SYNC → BTPCM_SYNC [7]
GPIOX_11(TDMA_SCLK//TDMA_SLV_SCLK//TSIN_B_CLK//SPI_A_SCLK//I2C_EE_M1_SCL) BF34 BTPCM_CLK → BTPCM_CLK [7]
GPIOX_12(UART_EE_A_TX) BK28 BTUART_A_TX → BTUART_A_TX [7]
GPIOX_13(UART_EE_A_RX) BH30 BTUART_A_RX → BTUART_A_RX [7]
GPIOX_14(UART_EE_A_CTS) BH28 BTUART_A_CTS_N → BTUART_A_CTS_N [7]
GPIOX_15(UART_EE_A_RTS) BK26 BTUART_A_RTS_N → BTUART_A_RTS_N [7]

GPIOX_16(PWM_E) BK30 WIFI_32K → WIFI_32K [7]
GPIOX_17(I2C_EE_M2_SDA) BF31 BT_EN → BT_EN [7]
GPIOX_18(I2C_EE_M2_SCL) BM24 BT_WAKE_HOST → BT_WAKE_HOST
GPIOX_19(PWM_B//WORLD_SYNC//GEN_CLK_EE) BH26 HOST_WAKE_BT

G12A_S905D2
A311D

AP6398S WIFI+BT

50 ohm impedance RF trace

WiFi ANT

7J2 I-PEX_RF-CON J-MS-156
G1 G2 G3 FEED 4 2 1 3
WIFI_ANTA
7C19 0R C0402
7C20 NC C0402
7C26 NC C0402
GND

WiFi/BT ANT

7C46 0R C0402
WIFI_ANTC
7C50 NC C0402
7C32 NC C0402
7J5 I-PEX_RF-CON J-MS-156
FEED G1 G2 G3 4 2 1 3
GND

7Y1
Part Name = TZ0606A
37.4MHz_12pF_10ppm
Y-SMD4P3225
WXTAL_IN
WXTAL_OUT 7R26 22R R0402
7C31 12pF_5%_NPO C0402
7C10 12pF_5%_NPO C0402
GND

SDIO WIFI 7R6 placed
PCIe WIFI 7R6 NC

WIFI_WAKE_HOST 7R6 R0402 22R
7C37 NC/6.8pF_5%_NPO C0402

7U4
AP6398S
LIB VER:2017-11-23

12	NC4	BT_HOST_WAKE	50 22R R0402 7R2 BT_WAKE_HOST
13	XTAL_OUT	BT_WAKE	49 22R R0402 7R5 HOST_WAKE_BT
14	XTAL_IN	BT_ANT(AP6359S/AP6398SR3)/MODE SEL(AP6356S)	48
15	WL_REG_ON	GND(AP6359S/AP6398SR3)/NC	47
16	WL_HOST_WAKE	NC3	46
17	SDIO_DATA_CMD	NC2	45
18	SDIO_DATA_CLK	NC1	44
19	SDIO_DATA_3	UART_CTS_N	43
20	SDIO_DATA_2	UART_RTS_N	42
21	SDIO_DATA_0	UART_RXD	41
22	SDIO_DATA_1	UART_TXD	40
23	GND8	GND1	39
24	NC/SDIO_VSEL(AP6359SA/AP6359S/AP6398S/AP6398SR3)	BT_REG_ON	38
25	VIN_LDO	NC5	37

WIFI_WAKE_HOST
WIFI_SD_CMD
WIFI_SD_CLK
WIFI_SD_D3
WIFI_SD_D2
WIFI_SD_D0
WIFI_SD_D1
WIFI_PWREN

RN0402: 7RN1 4x0R → BTUART_A_RTS_N, BTUART_A_CTS_N, BTUART_A_TX, BTUART_A_RX
BT_EN

VDDIO_X
7R32 10K R0402
7R31 NC/10K R0402
WIFI_SD_D0
WIFI_SD_CMD

7R4 NC/10K R0402
GND

When SDIO Voltage level = 1.8V, 7R4 NC
When SDIO Voltage level = 3.3V, 7R4 placed
When use PCIe WIFI, 7R4 placed

BT ANT option

VDDIO_X
7R25 NC/10K R0402
7C3 0R C0402
BT_ANTA
7C4 NC C0402
7C2 NC C0402
7J1 NC/I-PEX_RF-CON J-MS-156
FEED G1 G2 G3 4 2 1 3
GND

Close to WIFI pin 36

WIFI_VBAT
VDDAO_3.3V
7R30 0R_0603 R0603
7C5 10uF_6.3V C0603
7C41 10uF_6.3V C0603
7C40 0.1uF C0402
GND

AP_WIFI2X2_13X15
VIN_LDO_OUT PCM_SYNC PCM_IN PCM_OUT PCM_CLK LPO GND12 NC/PCIE_REFCLK_N VDDIO NC/PCIE_REFCLK_P VBAT
26 27 28 29 30 31 32 33 34 35 36

7L1 2 4.7uH_1A_DCR80mohm L3030
WIFI_VBAT
VDDIO_X
7C49 4.7uF_6.3V C0603
7C48 0.1uF C0402
GND

BTPCM_SYNC 5
BTPCM_DOUT 6
BTPCM_DIN 7
BTPCM_CLK 8
WIFI_32K 7R47 100R R0402
4x0R 7RN2 R0402
GND GND

When use SDIO WIFI, 7R2/5/47,7RN1/2 placed
When use PCIe WIFI, 7R2/5/47,7RN1/2 NC

When use SDIO WIFI, 7R83/84/86 NC
When use PCIe WIFI, 7R83/84/86 placed

WIFI_PWREN 7R83 R0402 22R → PCIE_WIFI_EN [7]
WIFI_WAKE_HOST 7R84 R0402 22R → PCIE_RST_L 7
HOST_WAKE_BT 7R86 R0402 22R → PCIE_WAKEn

Amlogic	Drawn by: Suo Li
Title: SDIO WIFI	Drawn Date: 2019-02-21
Size: A3	Checked by: <Checked>
Document: W400 DEV BOARD	Rev: V03
Date: Thursday, February 21, 2019	Checked Date: checked date
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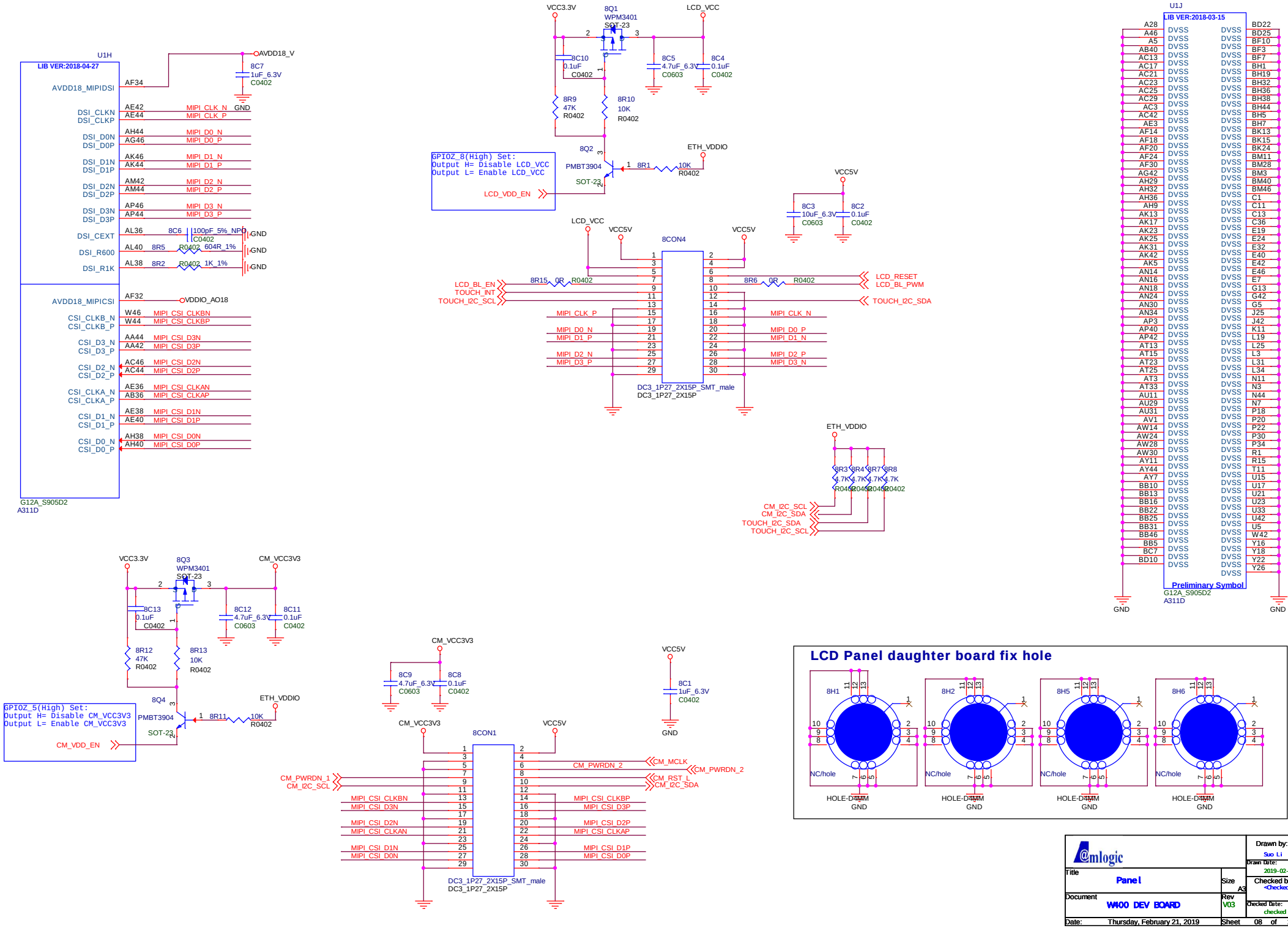
U1H
LIB VER:2018-04-27
AVDD18_MIPIDSI
AF34
AVDD18_V
8C7
1uF_6.3V
C0402
DSI_CLKN
DSI_CLKP
AE42
AE44
MIPI_CLK_N
MIPI_CLK_P
GND
DSI_D0N
DSI_D0P
AH44
AG46
MIPI_D0_N
MIPI_D0_P
DSI_D1N
DSI_D1P
AK46
AK44
MIPI_D1_N
MIPI_D1_P
DSI_D2N
DSI_D2P
AM42
AM44
MIPI_D2_N
MIPI_D2_P
DSI_D3N
DSI_D3P
AP46
AP44
MIPI_D3_N
MIPI_D3_P
DSI_CEXT
AL36
8C6
100pF_5%_NPO
C0402
DSI_R600
AL40
8R5
R0402_604R_1%
DSI_R1K
AL38
8R2
R0402_1K_1%
AVDD18_MIPICSI
AF32
VDDIO_AO18
CSI_CLKB_N
CSI_CLKB_P
W46
W44
MIPI_CSI_CLKBN
MIPI_CSI_CLKBP
CSI_D3_N
CSI_D3_P
AA44
AA42
MIPI_CSI_D3N
MIPI_CSI_D3P
CSI_D2_N
CSI_D2_P
AC46
AC44
MIPI_CSI_D2N
MIPI_CSI_D2P
CSI_CLKA_N
CSI_CLKA_P
AE36
AB36
MIPI_CSI_CLKAN
MIPI_CSI_CLKAP
CSI_D1_N
CSI_D1_P
AE38
AE40
MIPI_CSI_D1N
MIPI_CSI_D1P
CSI_D0_N
CSI_D0_P
AH38
AH40
MIPI_CSI_D0N
MIPI_CSI_D0P
G12A_S905D2
A311D
VCC3.3V
8Q1
WPM3401
SOT-23
LCD_VCC
8C10
0.1uF
C0402
8C5
4.7uF_6.3V
C0603
8C4
0.1uF
C0402
8R9
47K
R0402
8R10
10K
R0402
8Q2
PMBT3904
SOT-23
ETH_VDDIO
8R1
10K
R0402
GPIOZ_8(High) Set:
Output H= Disable LCD_VCC
Output L= Enable LCD_VCC
LCD_VDD_EN
VCC5V
8C3
10uF_6.3V
C0603
8C2
0.1uF
C0402
LCD_VCC
VCC5V
8CON4
VCC5V
8R15
0R
R0402
LCD_BL_EN
TOUCH_INT
TOUCH_I2C_SCL
8R6
0R
R0402
LCD_RESET
LCD_BL_PWM
TOUCH_I2C_SDA
MIPI_CLK_P
MIPI_CLK_N
MIPI_D0_N
MIPI_D1_P
MIPI_D0_P
MIPI_D1_N
MIPI_D2_N
MIPI_D3_P
MIPI_D2_P
MIPI_D3_N
DC3_1P27_2X15P_SMT_male
DC3_1P27_2X15P
ETH_VDDIO
8R3
8R4
8R7
8R8
4.7K
R0402
CM_I2C_SCL
CM_I2C_SDA
TOUCH_I2C_SDA
TOUCH_I2C_SCL
U1J
LIB VER:2018-03-15
DVSS
Preliminary Symbol
G12A_S905D2
A311D
GND
VCC3.3V
8Q3
WPM3401
SOT-23
CM_VCC3V3
8C13
0.1uF
C0402
8C12
4.7uF_6.3V
C0603
8C11
0.1uF
C0402
8R12
47K
R0402
8R13
10K
R0402
8Q4
PMBT3904
SOT-23
ETH_VDDIO
8R11
10K
R0402
GPIOZ_5(High) Set:
Output H= Disable CM_VCC3V3
Output L= Enable CM_VCC3V3
CM_VDD_EN
CM_VCC3V3
8C9
4.7uF_6.3V
C0603
8C8
0.1uF
C0402
VCC5V
8C1
1uF_6.3V
C0402
GND
CM_VCC3V3
8CON1
VCC5V
CM_PWRDN_1
CM_I2C_SCL
CM_PWRDN_2
CM_MCLK
CM_RST_L
CM_I2C_SDA
MIPI_CSI_CLKBN
MIPI_CSI_D3N
MIPI_CSI_D2N
MIPI_CSI_CLKAN
MIPI_CSI_D1N
MIPI_CSI_D0N
MIPI_CSI_CLKBP
MIPI_CSI_D3P
MIPI_CSI_D2P
MIPI_CSI_CLKAP
MIPI_CSI_D1P
MIPI_CSI_D0P
DC3_1P27_2X15P_SMT_male
DC3_1P27_2X15P
LCD Panel daughter board fix hole
8H1
8H2
8H5
8H6
NC/hole
HOLE-D4MM
GND
Amlogic
Drawn by:
Suo Li
Drawn Date:
2019-02-21
Checked by:
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Title
Panel
Size
A3
Document
W400 DEV BOARD
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V03
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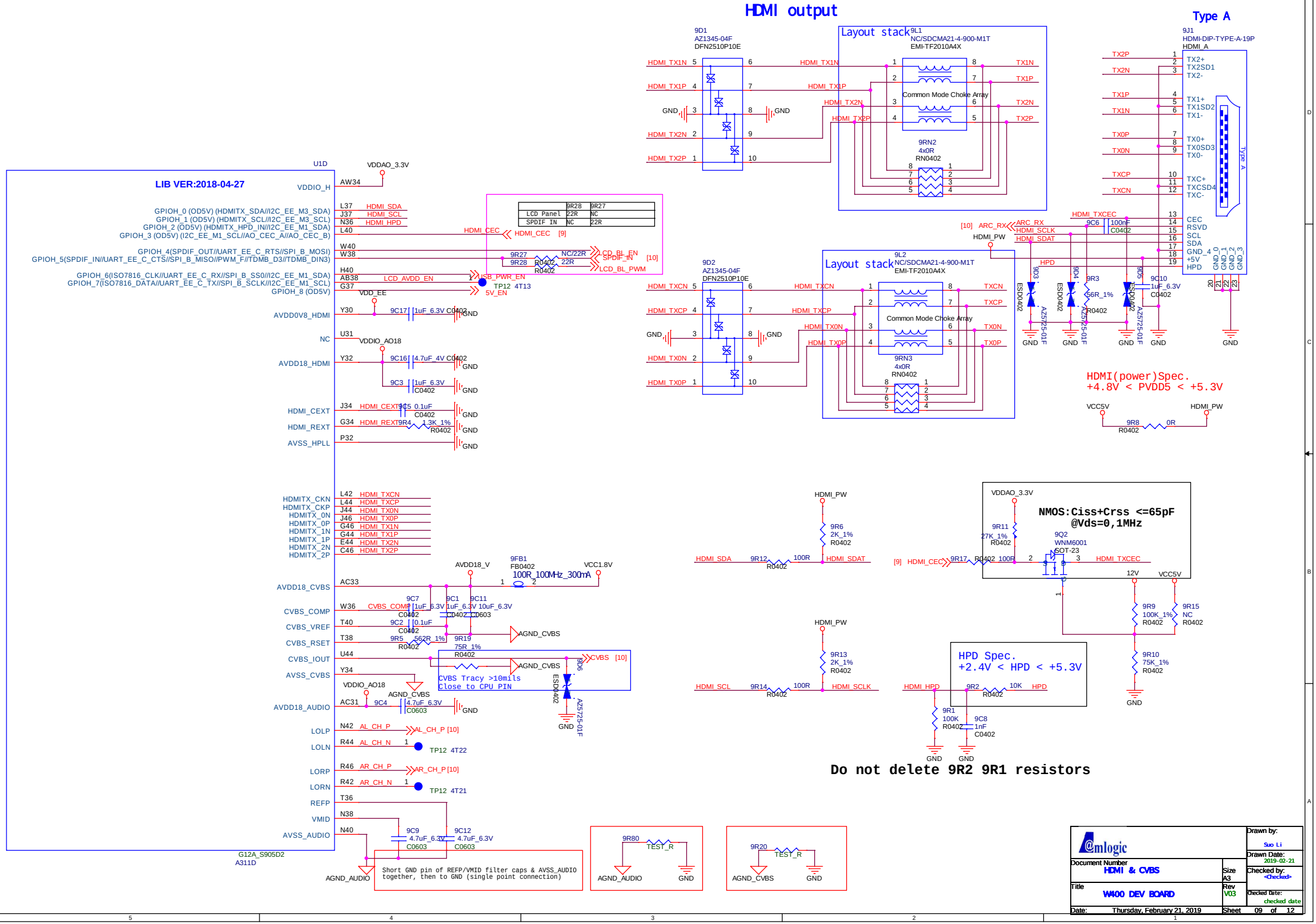
HDMI output



	9R28	9R27
LCD Panel	22R	NC
SPDIF IN	NC	22R

Drawn by:	Suo Li	
Drawn Date:	2019-02-21	
Checked by:	<Checked>	
Checked Date:	checked date	
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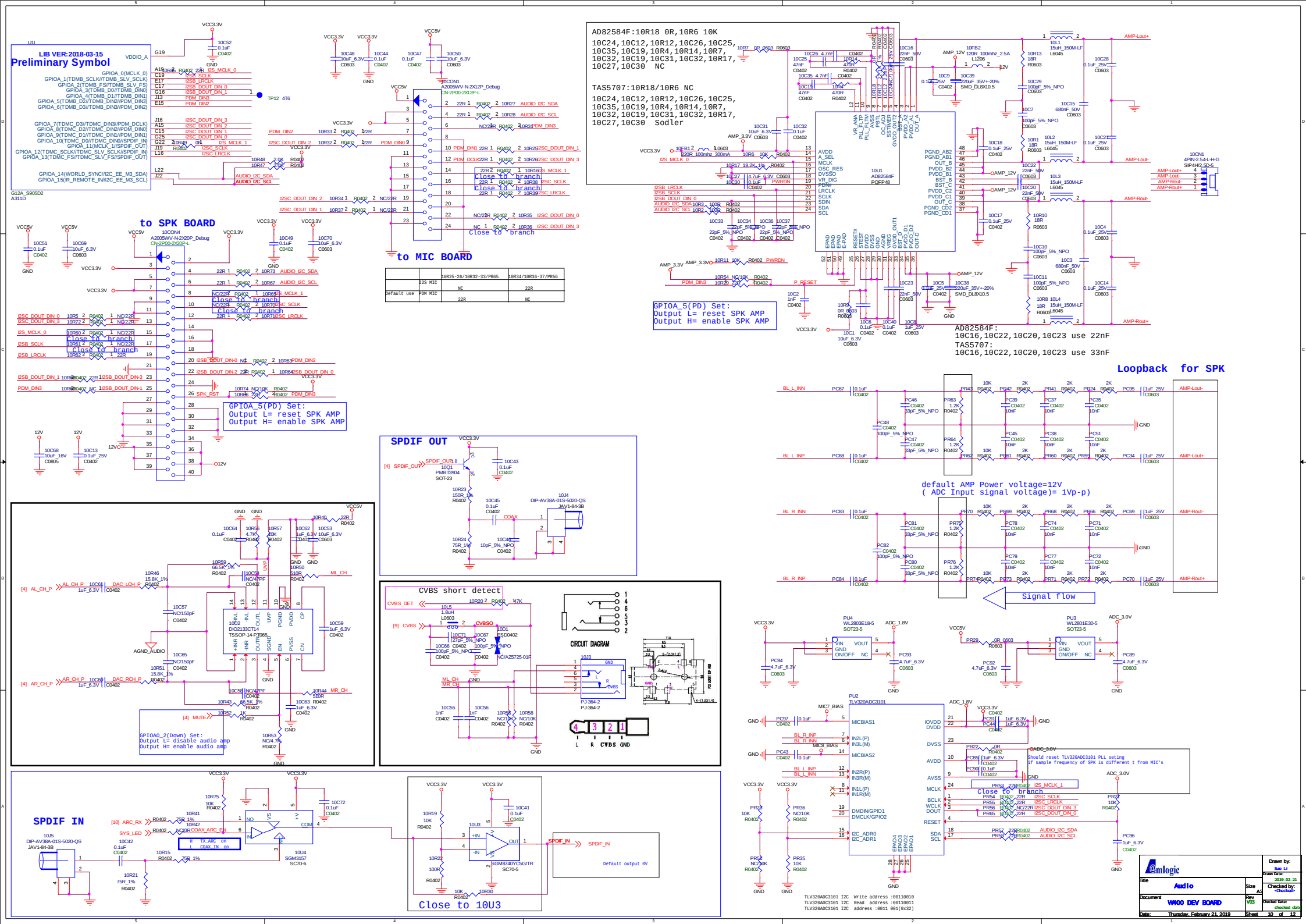
LIB VER:2018-03-15
Preliminary Symbol
U1I
VDDIO_A
GPIOA_0(MCLK_0)
GPIOA_1(TDMB_SCLK//TDMB_SLV_SCLK)
GPIOA_2(TDMB_FS//TDMB_SLV_FS)
GPIOA_3(TDMB_DO//TDMB_DIN0)
GPIOA_4(TDMB_DI//TDMB_DIN1)
GPIOA_5(TDMB_D2//TDMB_DIN2//PDM_DIN3)
GPIOA_6(TDMB_D3//TDMB_DIN3//PDM_DIN2)
GPIOA_7(TDMC_D3//TDMC_DIN3//PDM_DCLK)
GPIOA_8(TDMC_D2//TDMC_DIN2//PDM_DIN0)
GPIOA_9(TDMC_D1//TDMC_DIN1//PDM_DIN1)
GPIOA_10(TDMC_D0//TDMC_DIN0//SPDIF_IN)
GPIOA_11(MCLK_1//SPDIF_OUT)
GPIOA_12(TDMC_SCLK//TDMC_SLV_SCLK//SPDIF_IN)
GPIOA_13(TDMC_FS//TDMC_SLV_FS//SPDIF_OUT)
GPIOA_14(WORLD_SYNC//I2C_EE_M3_SDA)
GPIOA_15(IR_REMOTE_IN//I2C_EE_M3_SCL)
G12A_S905D2
A311D
I2S_MCLK_0
I2SC_SCLK
I2SC_DOUT_DIN_3
I2SC_DOUT_DIN_2
I2SC_DOUT_DIN_1
I2SC_DOUT_DIN_0
I2SC_MCLK_1
I2SC_SCLK
I2SC_LRCLK
PDM_DIN3
PDM_DIN2
AUDIO_I2C_SDA
AUDIO_I2C_SCL
TP12 4T6
to SPK BOARD
to MIC BOARD
Close to branch
GPIOA_5(PD) Set:
Output L= reset SPK AMP
Output H= enable SPK AMP
AD82584F:10R18 0R,10R6 10K
10C24,10C12,10R12,10C26,10C25,
10C35,10C19,10R4,10R14,10R7,
10C32,10C19,10C31,10C32,10R17,
10C27,10C30 NC
TAS5707:10R18/10R6 NC
10C24,10C12,10R12,10C26,10C25,
10C35,10C19,10R4,10R14,10R7,
10C32,10C19,10C31,10C32,10R17,
10C27,10C30 Sodler
AD82584F:
10C16,10C22,10C20,10C23 use 22nF
TAS5707:
10C16,10C22,10C20,10C23 use 33nF
Loopback for SPK
default AMP Power voltage=12V
(ADC Input signal voltage)= 1Vp-p)
Signal flow
SPDIF OUT
CVBS short detect
SPDIF IN
Close to 10U3
Default output 0V
GPIOAO_2(Down) Set:
Output L= disable audio amp
Output H= enable audio amp
TLV320ADC3101 I2C Write address :00110010
TLV320ADC3101 I2C Read address :00110011
TLV320ADC3101 I2C address :0011 001(0x32)
Should reset TLV320ADC3101 PLL seting
if sample frequency of SPK is different t from MIC's
Amlogic
Drawn by: Suo Li
Drawn date: 2019-02-21
Checked by: <Checker>
Checked date: checked date
Title: Audio
Size: A2
Document: W400 DEV BOARD
Rev: V03
Date: Thursday, February 21, 2019
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