Design and Analysis of 4-2 Compressor for Arithmetic Application

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ABSTRACT

Imprecise computing is an attractive model for digital processing at nano metric scales. Inexact computing is particularly interesting for computer arithmetic designs. This work deals about the design and analysis of two new inaccurate 4-2 compressors for utilization in a multiplier. These designs rely on different features of compression, such that imprecision in computation is measured by the error rate and the so-called normalized error distance can meet with respect to circuit-based figures of merit of a design in terms of number of transistors, delay and power consumption. The proposed approximate compressors are proposed and analyzed in Dadda multiplier. Extensive simulation results are provided and an application of the approximate multipliers to image processing is presented. The results proposed designs shows that reduced power dissipation, delay and transistor count.

Keywords: Compressor, Dadda multiplier and Inexact computing.

1. INTRODUCTION

Commonly used multimedia applications have Digital Signal Processing (DSP) blocks as their backbone. Most of these DSP blocks implement the image and video processing algorithms, where the ultimate output is either an image or a video for human consumption [1].

The limited perception of human vision allows the outputs of these algorithms to be numerically approximate rather than accurate. This relaxation on numerical exactness provides some freedom to carry out imprecise or approximate computation. The freedom can be taken advantage of to come up with low-power designs at different levels of design abstraction, viz. logic, architecture, and algorithm.

Methodologies for inexact computing rely on the feature that many applications can tolerate some loss of precision and therefore, the solution can tolerate some degree of uncertainty. However, inexact computing applications are mostly implemented using digital binary logic circuits, thus operating with a high degree of predictability and precision. A framework based on a precise and specific implementation can still be used with a methodology that intrinsically has a lower degree of precision and an increasing uncertainty in operation [4].

Addition and multiplication are widely used operations in computer arithmetic for addition full-adder cells have been extensively analyzed for approximate computing. The paradigm of inexact computation relies on relaxing fully precise and completely deterministic building blocks such as a full adder when for example, implementing the bio-inspired systems. This allows nature inspired computation to redirect the existing design process of digital circuits and systems by taking advantage of a decrease in complexity and cost with possibly a potential increase in performance and power efficiency.

2. EXACT COMPRESSOR

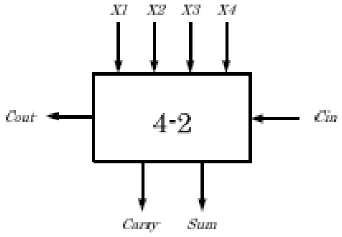

Fig.1. General Structure of 4-2 compressor

The following equation gives the outputs of 4-2 compressor, which table 1 show its truth table. The common implementation of a 4-2 compressor is accomplished by utilizing two full adders are shown in Fig. 3.3.

$$\text{Sum} = x1 \oplus x2 \oplus x3 \oplus x4 \oplus c_{in} \ldots\ldots (1)$$

$$C_{out} = (x1 \oplus x2)\, x3 + (x1 \oplus x2)\,`\, x1 \ldots (2)$$

$$\text{Carry} = (x1 \oplus x2 \oplus x3 \oplus x4)\, c_{in} + (x1 \oplus x2 \oplus x3 \oplus x4)\,`\, x4 \ldots\ldots (3)$$

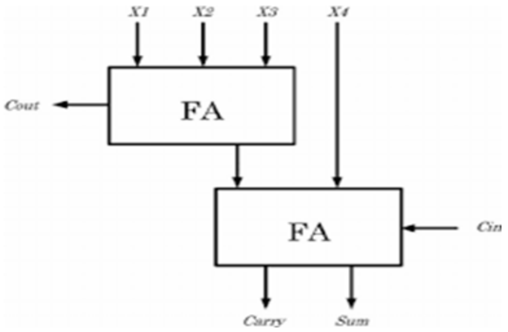

Fig.2. Implementation of 4-2 compressor

This design is not efficient because it produces at least 17 incorrect output of 32 possible combination that is error rate of this exact compressor design is above 53%.

Table 1: Truth table of exact 4-2 compressor

C_{in}	X4	X3	X2	X1	C_{out}	Carry	Sum
0	0	0	0	0	0	0	0
0	0	0	0	1	0	0	1
0	0	0	1	0	0	0	1
0	0	0	1	1	1	0	0
0	0	1	0	0	0	0	1
0	0	1	0	1	1	0	0
0	0	1	1	0	1	0	0
0	0	1	1	1	1	0	1
0	1	0	0	0	0	0	1
0	1	0	0	1	0	1	0
0	1	0	1	0	0	1	0
0	1	0	1	1	1	0	1
0	1	1	0	0	0	1	0
0	1	1	0	1	1	0	1
0	1	1	1	0	1	0	1
0	1	1	1	1	1	1	0
1	0	0	0	0	0	0	1
1	0	0	0	1	0	1	0
1	0	0	1	0	0	1	0
1	0	0	1	1	1	0	1
1	0	1	0	0	0	1	0
1	0	1	0	1	1	0	1
1	0	1	1	0	1	0	1
1	0	1	1	1	1	1	0
1	1	0	0	0	0	1	0
1	1	0	0	1	0	1	1
1	1	0	1	0	0	1	1
1	1	0	1	1	1	1	0
1	1	1	0	0	0	1	1
1	1	1	0	1	1	1	0
1	1	1	1	0	1	1	0
1	1	1	1	1	1	1	1

3. PROPOSED COMPRESSOR

3.1. Design 1

In Design 1, the carry is simplified to c_{in} by changing the value of the other 8 outputs.

$\text{Carry}` = C_{in}$………………………………......... (4)

$\text{Sum}` = c_{in`}\,((x1 \oplus x2)`+(x3 \oplus x4)`)$……... (5)

$C_{out}` = ((x1\ x2)`+(x3\ x4)`)$………….......... (6)

Eqs. (4) - (6) are the logic expressions for the outputs of the first design of the approximate 4-2 compressor proposed in this manuscript. The gate level structure of the first proposed design (Fig.3) shows that the critical path of this compressor has still a delay of 3Δ, so it is the same as for the exact compressor of Fig.2.

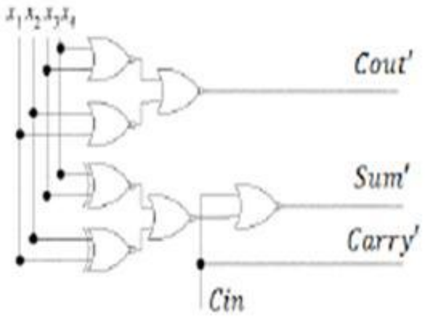

Fig.3. Gate level implementation of design 1

Table 2: Truth table of design 1 compressor

Cin	X4	X3	X2	X1	Cout	Carry	Sum
0	0	0	0	0	0	0	1
0	0	0	0	1	0	0	1
0	0	0	1	0	0	0	1
0	0	0	1	1	0	0	1
0	0	1	0	0	0	0	1
0	0	1	0	1	1	0	0
0	0	1	1	0	1	0	0
0	0	1	1	1	1	0	1
0	1	0	0	0	0	0	1
0	1	0	0	1	1	0	0
0	1	0	1	0	1	0	0
0	1	0	1	1	1	0	1
0	1	1	0	0	0	0	1
0	1	1	0	1	1	0	1
0	1	1	1	0	1	0	1
0	1	1	1	1	1	0	1
1	0	0	0	0	0	1	0
1	0	0	0	1	0	1	0
1	0	0	1	0	0	1	0
1	0	0	1	1	0	1	0
1	0	1	0	0	0	1	0
1	0	1	0	1	1	1	0
1	0	1	1	0	1	1	0
1	0	1	1	1	1	1	0
1	1	0	0	0	0	1	0
1	1	0	0	1	1	1	0
1	1	0	1	0	1	1	0
1	1	0	1	1	1	1	0
1	1	1	0	0	0	1	0
1	1	1	0	1	1	1	0
1	1	1	1	0	1	1	0
1	1	1	1	1	1	1	0

However; the propagation delay through the gates of this design is lower than the one for the exact compressor. Therefore, the critical path delay in the proposed design is lower than in the exact design and moreover, the total number of gates in the proposed design is significantly less than exact compressor.

As shown in Table 1, the carry output in an exact compressor has the same value of the input c_{in} in 24 out of 32 states. Therefore, an approximate design must consider this feature. Table 2 shows the truth table of the first proposed approximate compressor. The proposed design 1 has 12 incorrect outputs out of 32 outputs thus yielding an error rate of 37.5%. This is less than the error rate using the best [2] approximate full-adder cell.

3.2 Design 2

A second design of an approximate compressor is proposed to further increase performance as well as reducing the error rate can be ignored in the hardware design.

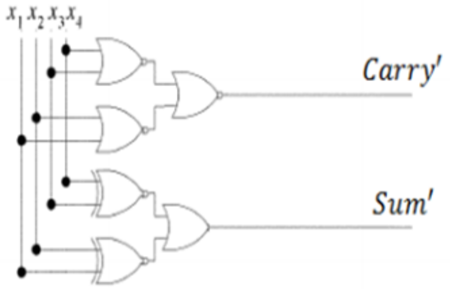

Fig.4. Gate level implementation of design-2

In this new design, carry uses the right hand side of (3) and c_{out} is always equal to c_{in}; since c_{in} is zero in the first stage, c_{out} and c_{in} will be zero in all stages. So, c_{in} and c_{out} can be ignored in the hardware design.

$$\text{Sum}` = ((x1 \oplus x2)` + (x3 \oplus x4)`) \ldots\ldots\ldots\ldots\ldots (7)$$

$$\text{Carry}` = ((x1x2)` + (x3x4)`)` \ldots\ldots\ldots\ldots\ldots (8)$$

Table 3: Truth Table of Design-2

X4	X3	X2	X1	Carry’	Sum'
0	0	0	0	0	1
0	0	0	1	0	1
0	0	1	0	0	1
0	0	1	1	0	1
0	1	0	0	0	1
0	1	0	1	1	0
0	1	1	0	1	0
0	1	1	1	1	1
1	0	0	0	0	1
1	0	0	1	1	0
1	0	1	0	1	0
1	0	1	1	1	1
1	1	0	0	0	1
1	1	0	1	1	1
1	1	1	0	1	1
1	1	1	1	1	1

Fig.4. Shows the gate level implementation of design 2 compressor and the expressions below describe its outputs. The delay of the critical path of this approximate design is 2Δ, so it is 1Δ less than the previous designs; moreover, a further reduction in the number of gates is accomplished

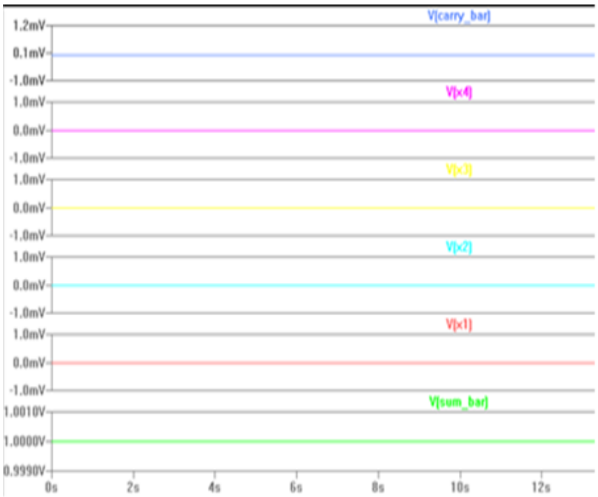

Fig.5. Output waveform of design-2

4. DADDA MULTIPLIER

A multiplier using such a compression scheme is normally referred to as a Dadda multiplier.

In this multipliers least reduction at each stage [4]. The maximum height of consist of three stages.

In the first stage, partial product each stage is determined by working back from final stage matrix is formed.

In the second stage, partial product matrix is reduced to a height of two products.

In the final stage, this consists of two rows of partial products are combined using of each stage should be in the order 2, 3, carry propagation adder. Dadda multiplier less number of half adders are required than the Wallace multiplier.

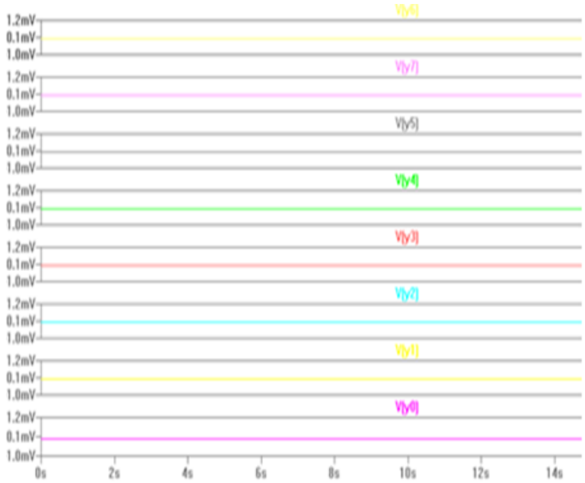

Fig.6. Output waveform of Dadda multiplier

5. RESULT ANALYSIS

The below Table 4 shows that design 2 4-2 compressor is better than other compressor because of its reduced transistor count and power dissipation.

Table 4: Analysis of compressor

COMPRESSOR	POWER DISSIPATION (µW)	TRANSISTOR COUNT
Exact design	0.016140	82
Design1	0.010332	44
Design 2	0.010096	42

Table 5: Analysis of multiplier

MULTIPLIER	POWER DISSIPATION (mW)	DELAY
Exact design	9.6566	1.25ns
Design1	5.8186	1.42ns
Design 2	5.5080	84.3ps

The above Table 5 shows that design 2 multiplier is better than other multiplier because of its reduced delay and power dissipation.

6. CONCLUSION

The compressors are utilized in the reduction module of four approximate multipliers. The approximate compressors show a significant reduction in transistor count, power consumption and delay compared with an exact design. In terms of transistor count, the first design has a 46% improvement, while the second design has a 49% improvement. In terms of power dissipation, the first design has a 57% improvement and the second design has a 60% improvement over CMOS implementation at feature sizes of 32 nm. In terms of delay, the second design has a 44% improvement compared to the exact compressor and 35% improvement compared to the first design on average at CMOS feature sizes of 32 nm. The proposed multipliers show a significant improvement in terms of power consumption and transistor count compared to an exact multiplier.

REFERENCES

[1] Chang C., Gu J. and Zhang M. (2004), ‘Ultra Low-Voltage Low- Power CMOS 4-2 and 5-2 Compressors for Fast Arithmetic Circuits’, *IEEE Transactions on Circuits & Systems*, Vol. 51, No. 10, pp. 1985-1997.

[2] Cheemalavagu S., Kormas P., Palme K.V., Akgul B.E.S. and Chakrapani L.N. (2005), ‘A probabilistic CMOS switch and its realization by exploiting noise’, *in Proc. SOC , Perth, Western Australia.*

[3] Gu J., and Chang C.H., (2003), ‘Ultra Low-voltage, low-power 4-2 compressor for high speed multiplications’, *in Proc. 36th IEEE Int. Symp. Circuits Systems, Bangkok, Thailand.*

[4] Gupta V., Mohapatra D., Park S.P., Raghu Nathan A. and Roy K. (Aug 2011), ‘IMPACT: Imprecise adders for low-power Approximate Computing’, *Low Power Electronics and Design (ISLPED) International Symposium.*

[5] King J.E. and Swartz lander E. (1998), ‘Data dependent truncated scheme for parallel multiplication,’ *in Proceedings of the Thirty First Alomar Conference on Signals and Systems*, pp. 1178–1182.

[6] Kulkarni P., Gupta P. and Ercegovac S.(2011) , ‘Trading accuracy for power in a multiplier architecture’, *Journal of Low Power Electronics*, Vol. 7, No. 4, pp. 490--501.

[7] Liang J., Han J. and Lombardi F.(2013) ,‘New Metrics for the Reliability of Approximate and Probabilistic Adders’, *IEEE Transactions on Computers* ,Vol. 63, No. 9, pp. 1760 – 1771.

[8] Mahanadi H.R., Hamada A., Fakhraie S.M. and Lucas C. (2010), ‘Bio-Inspired Imprecise Computational Blocks for Efficient VLSI Implementation of Soft-Computing Applications’, *IEEE Transactions on Circuits and Systems I:Regular Papers*, Vol. 57, No. 4, pp. 850-862.

[9] Margala M. and Durdle N.G. (1999), ‘Low-power low-voltage 4-2 compressors for VLSI applications,’ *in Proc. IEEE Alessandro Volta Memorial Workshop Low-Power Design*, pp. 84–90.

[10] Mustafa K., Vojin G. and Oklobdzij S. (2010), ‘Energy efficient implementation of parallel CMOS multipliers with improved compressors.’ *Proc. of the 16th ACM/IEEE international symposium on Low power electronics and design- ACM.*