Junzhuo Zhou
个人网站：junzhuo.me email: zhou@junzhuo.me/zhoujz2018@mail.sustech.edu.cn

Education

山东省实验中学
2018 高考成绩 657/750,省内 TOP 0.2%（2k/700k）

Southern University of Science and Technology
(2022 QS #13 Mainland China) Bachelor of Engineering in Microelectronics Science and Engineering; GPA: 3.7/4.0, 89.1/100 Rand 22/60
Expected Summer 2022
Courses: Analog Circuits, Digital Circuits, Embedded System and Microcomputer Principle, System-on-a-Chip Design, Advanced Integrated Circuit Design: Microprocessor, MEMS, Engineering Electromagnetics
Advisor: Dr. Hao Yu

Skills

Languages:	Verilog, Chisel3, SpinalHDL, Python, MATLAB, Java, Shell, LabView
Software:	DesignComplier, PrimeTime, VCS, Virtuoso, Quartus, ModelSim, Silvaco, SolidWorks, AutoCAD, Docker

Reseach Interests

IC Design (Integration Circuit Design)
1. Configurabale Computation (MAC Level), Multi-Precision Computation, NAS-Base.
2.Matrix-Matrix Multiplication (MXM) Architecture for HPC, Systolic Architecture with Pipeline Implement.
3.Parametric IC design based on SpinalHDL/Chisel. RTL-level floating-point algorithm verification methodology based on Scala and Verilator.

Publications

1. A Systolic Vector Accelerator for Multi-Precision Floating-Point High-Performance Computing, (**pending**)
International Conference on Artificial Intelligence Circuits and Systems (AICAS 2022)
Junzhuo Zhou, Boyu Li, Kai Li, Zhengke Yang, Junyi Luo, Wei Mao and Hao Yu∗

2.A Precision-Scalable Energy-Efficient Bit-Split-and-Combination Vector Systolic Accelerator for NAS-Optimized DNNs on Edge, (**pending**)
2022 Design, Automation and Test in Europe Conference (DATE 2022)

Kai Li, **Junzhuo Zhou**, Yuhang Wang, Junyi Luo, Zhengke Yang, Shuxin Yang, Wei Mao, Mingqiang Huang and Hao Yu ∗

3.An Energy-Efficient Bit-Split-and-Combination Systolic Accelerator for NAS-Based Multi-Precision Convolution Neural Networks,
27th Asia and South Pacific Design Automation Conference (ASP-DAC 2022)
Liuyao Dai, Quan Cheng, Yuhang Wang, Gengbin Huang, **Junzhuo Zhou**, Kai Li, Wei Mao, Hao Yu ∗

4.A Fast Method for Steady-State Memristor Crossbar Array Circuit Simulation,
2021 IEEE International Conference on Integrated Circuits Technologies and Applications (ICTA 2021)
Rui Xie, Mingyang Song, **Junzhuo Zhou**, Jie Mei, Quan Chen ∗

Patents

1. A Fixed-Point Multiply-Accumulate Unit and its Methodology for Multi-Precision Neural Networks Computation (Pending), CN 202110178992.7:
一种适用于混合精度神经网络的定点乘加运算单元及方法 (Pending),
Xianglong Wang, Yuhang Wang, **Junzhuo Zhou**, Gang Shi, Kai Li, Wei Mao, Fengwei An, Hao Yu*

2. A Computing-In-Memory Architecture Systolic Array for Multi-Precision Neural Networks Computation (Pending), CN 202110988635.7:
一种适用于多精度神经网络的存算一体架构脉动阵列设计方法 (Pending),
Dingbang Liu, Haoxiang Zhou, Yuliang Han, **Junzhuo Zhou**, Gengbin Huang, Changhai Man, Ao Shen, Wei Mao, Hao Yu*

Projects

A 3D Systolic Vector Accelerator for Floating-Point Matrix-Matrix Multiplication Computation:
1. Use SpinalHDL for parameterization RTL implementation and Floating-Point operations verification, the evaluation was performed on the DesignComplier and PrimeTime tools;
2. 3D dataflow means the systolic-flow, pipeline-flow and stationary are perpendicular to each other, so they will not affect each other, and the implementation of the pipeline will not affect the systolic.

A CNN Acceleration Based on Eyeriss and Implemented on Chisel3:
1. Use Chisel3 for RTL implementation and verification, realizing a parameterization design;
2. The PE internal pipeline and parallel multiplication module are added to the original architecture to improve the speed of data execution;
3. The project won the second prize of 2021 School of Microelectronics Innovation Competition.

A Parallel Optimization Design for Demosaicing on DE-1 FPGA – Controlled by RISC-V CPU:

1. Crafted parallel demosaic algorithm, with median filtering and gamma correction, implement RISC-V cpu as controller;
2. Seven-stages pipeline to process 5×5-pixel data with parallel design, reducing liner-buffer consumption by 40% compared to traditional 3x3-pixel architecture with serial design;
3. Deployed on DE1 FPGA and camera with LCD screen display.

An Area-Delay Optimized 4×4-bits Array Multiplier in 180nm CMOS Technology Node Based on Virtuoso:
1. A 4 × 4 array multiplier of 180nm technique on Virtuoso of Cadence with the area of 769 μm^2 and delay of 1.05ns;
2. Designed with layered structure and organized locating and wiring.

An Innovative Single-Threaded Automatic Target Detection System Based on Raspberry Pi:
1. Utilized Wiring-Pi API to configure on-board interface;
2. Designed the technique of logical value with dichotomous approximation;
3. Utilized the AutoCAD software design a Electromagnetic gun shell implementing the algorithm.

Honors and Awards

First Class of the Admission Scholarship	Sep. 2018
30000 CHY	< 5%
Third Class of the Merit Student Scholarship	Sep. 2019
1500 CHY	< 20%
Second Class of the Merit Student Scholarship	Sep. 2020
3000 CHY	< 20%

EXPERIENCE

Student Volunteer for IEEE Circuits and Systems Society Shanghai and Shenzhen Joint Workshop 2021 (CASS SSJW 2021)

参加深圳当地潜水俱乐部组织的净海小分队(OCEAN CLEANING SQUAD)等潜水活动

南方科技大学致诚书院学长团成员 带领新生开展班会和团建
(SUSTech Zhicheng College