

EDUCATION

- Southern University of Science and Technology, BENG** China
 2022 QS #13 Mainland China Expected Summer 2022
GPA: 3.67/4.0, 88.83/100, Rank 24/60
Core Courses: Analog Circuits, Digital Circuits, Embedded System and Microcomputer Principle, SoC Design,
 Advanced Integrated Circuit Design: Microprocessor, Engineering Electromagnetic
Advisor: Dr. Hao Yu
- Shandong Experimental High School** China
National College Entrance Examination: 657/750 Sep. 2015—June 2018
TOP 0.2% (2k/700k)

PUBLICATIONS

- A Precision-Scalable Energy-Efficient Bit-Split-and-Combination Vector Systolic Accelerator for NAS-Optimized DNNs on Edge:**
DATE'22
 Kai Li, [Junzhuo Zhou](#), Yuhang Wang, Junyi Luo, Zhengke Yang, Shuxin Yang, Wei Mao, Mingqiang Huang and Hao Yu*
- An Energy-Efficient Bit-Split-and-Combination Systolic Accelerator for NAS-Based Multi-Precision Convolution Neural Networks:**
ASP-DAC'22
 Liuyao Dai, Quan Cheng, Yuhang Wang, Gengbin Huang, [Junzhuo Zhou](#), Kai Li, Wei Mao, Hao Yu*
- A Fast Method for Steady-State Memristor Crossbar Array Circuit Simulation:**
ICTA'21
 Rui Xie, Mingyang Song, [Junzhuo Zhou](#), Jie Mei, Quan Chen*

PATENTS

- A Fixed-Point Multiply-Accumulate Unit and its Methodology for Multi-Precision Neural Networks Computation, CN202110178992.7:**
 Xianglong Wang, Yuhang Wang, [Junzhuo Zhou](#), Gang Shi, Kai Li, Wei Mao, Fengwei An, Hao Yu
- A Computing-In-Memory Architecture Systolic Array for Multi-Precision Neural Networks Computation, CN202110988635.7:**
 Dingbang Liu, Haoxiang Zhou, Yuliang Han, [Junzhuo Zhou](#), Gengbin Huang, Changhai Man, Ao Shen, Wei Mao, Hao Yu

COMMUNITY SERVICES

- Volunteer** June 2021
 IEEE Circuits and Systems Society Shanghai and Shenzhen Joint Workshop Shenzhen
 - Created posters for the workshop:
 - Helped scheduling and workshop agenda:
- Volunteer** Sep. 2019—Present
 Diver of Ocean Cleaning Squad, Forever Young International Diving Club Shenzhen
 - Dived to collect garbage and junks in the ocean:
 - Educated community members on environmental protection:
- Upperclassmen Service Group** Sep. 2019—Present
 Zhicheng College, Southern University of Science and Technology SUSTech
 - Organized activities for freshmen:
 - Oriented freshmen to campus life:

HONORS AND AWARDS

- First Class of the Admissions Scholarship** Sep. 2018
 30000 CHY < 3%
- Third Class of the Merit Student Scholarship** Sep. 2019
 1500 CHY < 20%
- Second Class of the Merit Student Scholarship** Sep. 2020
 3000 CHY < 7%

SKILLS

- Languages:** Verilog, Python, C, MATLAB, Java, Scala, Bash, TCL, Chisel, LabView, Swift
- Software:** DesignCompiler, PrimeTime, VCS, MemoryComplier, Virtuoso, Quartus, ModelSim, Vivado, Docker

RESEARCH INTERESTS

- **IC Design**

- *Integration Circuit Design*

- **High Performance Computing Architecture:**
 1. Matrix-Matrix Multiplication (MXM) Architecture for HPC;
 2. Vektored-Systolic Architecture with Pipeline Implement.
- **Configurable Computation:**
 1. Multi-Precision MAC for Fix-Point & Floating-Point;
 2. NAS-Base;
 3. Obtained a Fund of **10,000 CHY**.
- **Parametric IC design:**
 1. RTL-level is based on SpinalHDL/Chisel;
 2. Verification methodology based on Scala and Verilator, floating-point algorithm.

PROJECTS

- **A 3D Systolic Vector Accelerator for Floating-Point Matrix-Matrix Multiplication Computation:**
 1. Use SpinalHDL for parameterization RTL implementation and Floating-Point operations verification, the evaluation was performed on the DesignCompiler and PrimeTime tools;
 2. 3D dataflow means the systolic-flow, pipeline-flow, and stationary are perpendicular to each other, so they will not affect each other, and the implementation of the pipeline will not affect the systolic.
- **A CNN Acceleration Based on Eyeriss and Implemented on Chisel3:**
 1. Use Chisel3 for RTL implementation and verification, realizing a parameterization design;
 2. The PE internal pipeline and parallel multiplication module are added to the original architecture to improve the speed of data execution;
 3. The project was the runner-up of the 2021 School of Microelectronics Innovation Competition.
- **A Parallel Optimization Design for Demosaicing on DE-1 FPGA, Controlled by RISC-V CPU:**
 1. Crafted parallel demosaic algorithm, with median filtering and gamma correction, implemented RISC-V cpu as controller;
 2. Seven-stages pipeline to process 5×5-pixel data with parallel design, reducing liner-buffer consumption by 40%, compared to traditional 3x3-pixel architecture with serial design;
 3. Deployed on DE1 FPGA and camera with LCD screen display.
- **An Area-Delay Optimized 4×4-bits Array Multiplier in 180nm CMOS Technology Node Based on Virtuoso:**
 1. A 4×4 array multiplier of 180nm technique on Virtuoso of Cadence with the area of $769 \mu\text{m}^2$ and delay of 1.05ns;
 2. Designed with layered structure and organized locating and wiring.
- **An Innovative Single-Threaded Automatic Target Detection System Based on Raspberry-Pi:**
 1. Utilized Wiring-Pi API to configure on-board interface;
 2. Designed the technique of logical value with dichotomous approximation;
 3. Utilized the AutoCAD software to design an Electromagnetic gun shell implementing the algorithm.