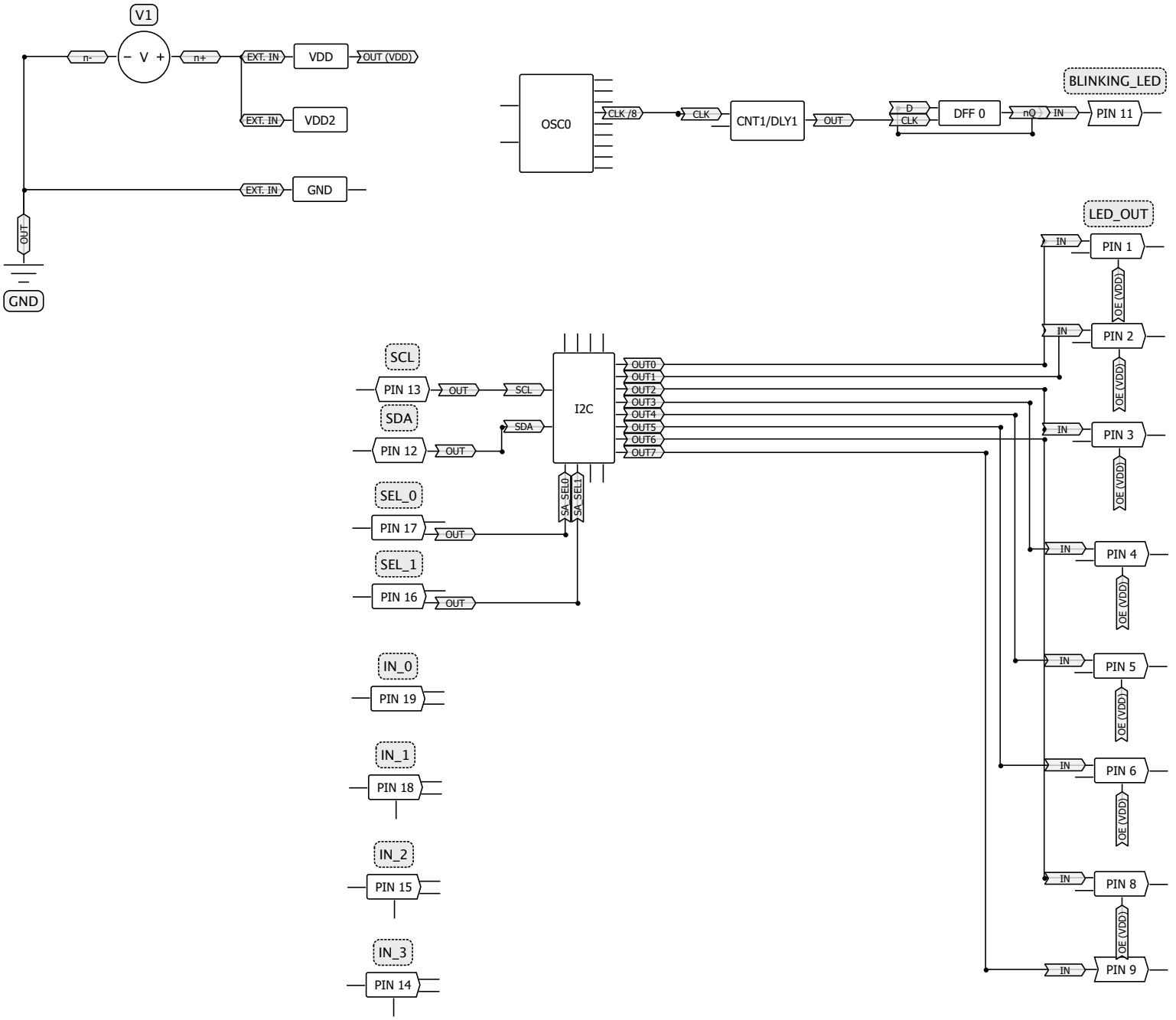
V1
n-
V
n+
EXT. IN
VDD
OUT (VDD)
EXT. IN
VDD2
EXT. IN
GND
OUT
GND
OSC0
CLK /8
CLK
CNT1/DLY1
OUT
D
CLK
DFF 0
nQ
IN
PIN 11
BLINKING_LED
LED_OUT
IN
PIN 1
OE (VDD)
IN
PIN 2
OE (VDD)
IN
PIN 3
OE (VDD)
IN
PIN 4
OE (VDD)
IN
PIN 5
OE (VDD)
IN
PIN 6
OE (VDD)
IN
PIN 8
OE (VDD)
IN
PIN 9
SCL
PIN 13
OUT
SCL
SDA
PIN 12
OUT
SDA
I2C
OUT0
OUT1
OUT2
OUT3
OUT4
OUT5
OUT6
OUT7
SA_SEL0
SA_SEL1
SEL_0
PIN 17
OUT
SEL_1
PIN 16
OUT
IN_0
PIN 19
IN_1
PIN 18
IN_2
PIN 15
IN_3
PIN 14

VDD (PIN 20)

Property	*Value*
Min. value (V)	3.30
Typ. value (V)	3.30
Max. value (V)	3.30

PIN 19 (IO0)
Label: "IN_0"

Property	*Value*
I/O selection	Digital input
In mode	Digital in with Schmitt trigger
Out mode	None
Resistor	Pull Up
Resistor value	10K

PIN 18 (IO1)
Label: "IN_1"

Property	*Value*
I/O selection	Digital input
In mode	Digital in with Schmitt trigger
Out mode	None
Resistor	Pull Down
Resistor value	10K

PIN 17 (IO2)
Label: "SEL_0"

Property	*Value*
I/O selection	Digital input
In mode	Digital in without Schmitt trigger
Out mode	None
Resistor	Pull Up
Resistor value	10K

PIN 16 (IO3)
Label: "SEL_1"

Property	*Value*
I/O selection	Digital input
In mode	Digital in without Schmitt trigger
Out mode	None
Resistor	Pull Up
Resistor value	10K

PIN 15 (IO4)
Label: "IN_2"

Property	*Value*
I/O selection	Digital input
In mode	Digital in with Schmitt trigger
Out mode	None
Resistor	Pull Up
Resistor value	10K

PIN 14 (IO5)
Label: "IN_3"

Property	*Value*
I/O selection	Digital input
In mode	Digital in with Schmitt trigger
Out mode	None
Resistor	Pull Up
Resistor value	10K

PIN 13 (SCL)
Label: "SCL"

Property	*Value*
I/O selection	Digital input
In mode	Digital in without Schmitt trigger
Out mode	None

PIN 12 (SDA)
Label: "SDA"

Property	*Value*
I/O selection	Digital input
In mode	Digital in without Schmitt trigger
Out mode	None

PIN 11 (IO6)
Label: "BLINKING_LED"

Property	*Value*
I/O selection	Digital output
In mode	None
Out mode	2x push pull

PIN 9 (IO7)

Property	*Value*
I/O selection	Digital output
In mode	None
Out mode	1x push pull

PIN 8 (IO8)

Property	*Value*
I/O selection	Digital output
In mode	None
Out mode	1x push pull

VDD2 (PIN 7)

Property	*Value*
Min. value (V)	3.30
Typ. value (V)	3.30
Max. value (V)	3.30

PIN 6 (IO9)

Property	*Value*
I/O selection	Digital output
In mode	None
Out mode	1x push pull

PIN 5 (IO10)

Property	*Value*
I/O selection	Digital output
In mode	None
Out mode	1x push pull

PIN 4 (IO11)

Property	*Value*
I/O selection	Digital output
In mode	None
Out mode	1x push pull

PIN 3 (IO12)

Property	*Value*
I/O selection	Digital output
In mode	None
Out mode	1x push pull

PIN 2 (IO13)

Property	*Value*
I/O selection	Digital output
In mode	None
Out mode	1x push pull

PIN 1 (IO14) Label: "LED_OUT"

Property	*Value*
I/O selection	Digital output
In mode	None
Out mode	1x push pull
100uA pullup on input	Disable

2-bit LUT0/DFF/LATCH0

Property	*Value*
Type	DFF / LATCH
Mode	DFF
Initial polarity	Low
Q output polarity	Inverted (nQ)

MF1 (3-bit LUT7, DFF/LATCH10, 8-bit CNT1/DLY1)

8-bit CNT1/DLY1 (MF1)

Property	*Value*
Mode	Reset counter
Counter data	60
Output period (typical)	238.281 ms
Edge mode select	Rising
DLY IN init. value	Bypass the initial
Output polarity	Non-inverted (OUT)
Mode signal SYNC	Bypass
Clock source	OSC0 /8
Clock frequency	256 Hz

OSC0

Property	*Value*
Control pin mode	Power down
OSC power mode	Force Power On
Clock selector	OSC
'OSC0' frequency	2.048 kHz
'CLK' predivider by	1
'OUT0' second divider by	1
'OUT1' second divider by	1

I2C

Property	*Value*
IO Latching	Enable
Mode selection	Standard/fast mode
Control code, bin	0100
Control byte, read/ write	0x41 / 0x40
Device address, dec/ hex	32 / 0x20
PIN 19 (IO0) output expander select	From matrix
PIN 14 (IO5) output expander select	From matrix
PIN 11 (IO6) output expander select	From matrix
PIN 6 (IO9) output expander select	From matrix
Virtual OUT0	0
Virtual OUT1	0
Virtual OUT2	0
Virtual OUT3	0
Virtual OUT4	0
Virtual OUT5	0
Virtual OUT6	0
Virtual OUT7	0
PIN 19 (IO0) OUT	0
PIN 14 (IO5) OUT	0
PIN 11 (IO6) OUT	0
PIN 6 (IO9) OUT	0
Control code selection	<table><tr><td>#3</td><td>#2</td><td>#1</td><td>#0</td></tr><tr><td>0</td><td>1</td><td>PIN 16</td><td>PIN 17</td></tr></table>

External Components

V1	
Property	*Value*
Element	Voltage Source
Pre-start delay	0s
Internal capacitance	100nF
Internal resistance	10Ohm
Pre-start state	Low
Type	DC
DC Voltage	3.3V
Ramp rise time	1ms

Project Specs			
	Min.	*Typ.*	*Max.*
VDD (V):	3.30	3.30	3.30
VDD2 (V):	3.30	3.30	3.30
Temperature (°C):	25.00	25.00	25.00

General Settings	
GPIO quick charge	Disable
Pattern ID	1
2k Register lock status	Unlocked
2k NVM lock status	Unlocked
Emulated EEPROM lock status	Unlocked
Protect entire lock configuration	Disable

I2C Probing

Probe pins			
Pin	*Signal name*	*Register*	*In use*
GND (PIN 10) -> OUT		HEX: 0x74`b0 DEC: 116`b0	+
PIN 19 (IO0) -> OUT		HEX: 0x74`b1 DEC: 116`b1	-
PIN 18 (IO1) -> OUT		HEX: 0x74`b2 DEC: 116`b2	-
PIN 17 (IO2) -> OUT	SA_SEL0	HEX: 0x74`b3 DEC: 116`b3	-
PIN 16 (IO3) -> OUT	SA_SEL1	HEX: 0x74`b4 DEC: 116`b4	-
PIN 15 (IO4) -> OUT		HEX: 0x74`b5 DEC: 116`b5	-
PIN 14 (IO5) -> OUT		HEX: 0x74`b6 DEC: 116`b6	-
PIN 8 (IO8) -> OUT		HEX: 0x74`b7 DEC: 116`b7	-
PIN 6 (IO9) -> OUT		HEX: 0x75`b0 DEC: 117`b0	-
PIN 5 (IO10) -> OUT		HEX: 0x75`b1 DEC: 117`b1	-
PIN 4 (IO11) -> OUT		HEX: 0x75`b2 DEC: 117`b2	-
PIN 3 (IO12) -> OUT		HEX: 0x75`b3 DEC: 117`b3	-
PIN 2 (IO13) -> OUT		HEX: 0x75`b4 DEC: 117`b4	-
PIN 1 (IO14) -> OUT		HEX: 0x75`b5 DEC: 117`b5	-
2-bit LUT0/DFF/ LATCH0 -> nQ	NET3	HEX: 0x75`b6 DEC: 117`b6	+
2-bit LUT1/DFF/ LATCH1 -> OUT		HEX: 0x75`b7 DEC: 117`b7	-
2-bit LUT2/DFF/ LATCH2 -> OUT		HEX: 0x76`b0 DEC: 118`b0	-
2-bit LUT3/PGEN -> OUT		HEX: 0x76`b1 DEC: 118`b1	-

Probe pins			
3-bit LUT0/DFF/ LATCH3 -> OUT		HEX: 0x76`b2 DEC: 118`b2	-
3-bit LUT1/DFF/ LATCH4 -> OUT		HEX: 0x76`b3 DEC: 118`b3	-
3-bit LUT2/DFF/ LATCH5 -> OUT		HEX: 0x76`b4 DEC: 118`b4	-
3-bit LUT3/DFF/ LATCH6 -> OUT		HEX: 0x76`b5 DEC: 118`b5	-
3-bit LUT4/DFF/ LATCH7 -> OUT		HEX: 0x76`b6 DEC: 118`b6	-
3-bit LUT5/DFF/ LATCH8 -> OUT		HEX: 0x76`b7 DEC: 118`b7	-
3-bit LUT6/Pipe Delay/Ripple Counter -> OUT		HEX: 0x77`b0 DEC: 119`b0	-
3-bit LUT6/Pipe Delay/Ripple Counter -> Q1		HEX: 0x77`b1 DEC: 119`b1	-
3-bit LUT6/Pipe Delay/Ripple Counter -> Q2		HEX: 0x77`b2 DEC: 119`b2	-
FILTER/EDGE DET -> OUT		HEX: 0x77`b3 DEC: 119`b3	-
P DLY -> OUT		HEX: 0x77`b4 DEC: 119`b4	-
8-bit CNT1/DLY1 (MF1) -> OUT	NET4	HEX: 0x77`b5 DEC: 119`b5	+
OSC1 -> OUT0		HEX: 0x77`b6 DEC: 119`b6	-
OSC0 -> OUT0		HEX: 0x77`b7 DEC: 119`b7	-
OSC2 -> OUT		HEX: 0x78`b0 DEC: 120`b0	-
8-bit CNT2/DLY2 (MF2) -> OUT		HEX: 0x78`b1 DEC: 120`b1	-
8-bit CNT3/DLY3 (MF3) -> OUT		HEX: 0x78`b2 DEC: 120`b2	-
8-bit CNT4/DLY4 (MF4) -> OUT		HEX: 0x78`b3 DEC: 120`b3	-
8-bit CNT5/DLY5		HEX:	-

Probe pins			
(MF5) -> OUT		0x78`b4 DEC: 120`b4	
8-bit CNT6/DLY6 (MF6) -> OUT		HEX: 0x78`b5 DEC: 120`b5	-
8-bit CNT7/DLY7 (MF7) -> OUT		HEX: 0x78`b6 DEC: 120`b6	-
4-bit LUT0 (MF0) -> OUT		HEX: 0x78`b7 DEC: 120`b7	-
3-bit LUT7 (MF1) -> OUT		HEX: 0x79`b0 DEC: 121`b0	-
3-bit LUT8 (MF2) -> OUT		HEX: 0x79`b1 DEC: 121`b1	-
3-bit LUT9 (MF3) -> OUT		HEX: 0x79`b2 DEC: 121`b2	-
3-bit LUT10 (MF4) -> OUT		HEX: 0x79`b3 DEC: 121`b3	-
3-bit LUT11 (MF5) -> OUT		HEX: 0x79`b4 DEC: 121`b4	-
3-bit LUT12 (MF6) -> OUT		HEX: 0x79`b5 DEC: 121`b5	-
3-bit LUT13 (MF7) -> OUT		HEX: 0x79`b6 DEC: 121`b6	-
16-bit CNT0/DLY0/ FSM0 (MF0) -> OUT		HEX: 0x79`b7 DEC: 121`b7	-
I2C -> OUT7	NET13	HEX: 0x7A`b0 DEC: 122`b0	+
I2C -> OUT6	NET12	HEX: 0x7A`b1 DEC: 122`b1	+
I2C -> OUT5	NET11	HEX: 0x7A`b2 DEC: 122`b2	+
I2C -> OUT4	NET10	HEX: 0x7A`b3 DEC: 122`b3	+
I2C -> OUT3	NET9	HEX: 0x7A`b4 DEC: 122`b4	+
I2C -> OUT2	NET8	HEX: 0x7A`b5 DEC: 122`b5	+
I2C -> OUT1	NET7	HEX: 0x7A`b6	+

Probe pins			
		DEC: 122`b6	
I2C -> OUT0	NET5	HEX: 0x7A`b7 DEC: 122`b7	+
A CMP0H -> OUT		HEX: 0x7B`b0 DEC: 123`b0	-
A CMP1H -> OUT		HEX: 0x7B`b1 DEC: 123`b1	-
A CMP2L -> OUT		HEX: 0x7B`b2 DEC: 123`b2	-
A CMP3L -> OUT		HEX: 0x7B`b3 DEC: 123`b3	-
OSC1 -> OUT1		HEX: 0x7B`b4 DEC: 123`b4	-
OSC0 -> OUT1		HEX: 0x7B`b5 DEC: 123`b5	-
POR -> OUT		HEX: 0x7B`b6 DEC: 123`b6	-
VDD (PIN 20) -> OUT	VDD	HEX: 0x7B`b7 DEC: 123`b7	-

Macrocells		
Macrocell	*Property*	*Register*
16-bit CNT0/DLY0/ FSM0 (MF0)	Counted Data	HEX: 0x7C, 0x7D DEC: 124, 125
8-bit CNT2/DLY2 (MF2)	Counted Data	HEX: 0x7E DEC: 126
8-bit CNT4/DLY4 (MF4)	Counted Data	HEX: 0x7F DEC: 127