# LED drive controller / keyboard scan ASIC TM1650

### Characterization

Features

LED TM1650 is a kind of keyboard scan interface (light emitting diode display) dedicated drive control circuit. Internal integrated MCU Digital input and output control interface, data latches, LED driver, keyboard scanning, brightness adjustment circuit. TM1650 stable performance, quality The amount of reliable, strong anti-jamming capability, suitable for long-term applications 24 hours of continuous work.

$\Box$ two display modes: $\times$ 4-bit and 8 of paragraph $7 \times 4 \%$
segment drive current is greater than 25mA, bit driver current is greater than 150mA
□ provide 8 brightness control
$\square$ keyboard scan: 7 × 4bit internal integration transistor drive
☐ high-speed two-wire serial interface
☐ Built-in clock oscillator circuit
☐ Built-in power-on reset circuit

☐ Support 2.8V-5.5V power supply voltage

□ provide DIP16 and SOP16 package

Field of application:

 $\ \square$  household products such as set-top boxes, air conditioning, DVD / VCD and other display drivers.

Internal structure diagram

# LED drive controller / keyboard scan ASIC TM1650

### Pinning information

# Pin Function

port		I/O	Constitut description
name	Pin	170	function descriptor
DIG1	1	O	Dan LED driver output 1 / keyboard scan output 1
DIG2	5	O	LED drive output Dan 2/2 keyboard scan output
DIG3	6	O	Dan LED drive output 3 / keyboard scan output 3
DIG4	7	O	Dan LED drive output 4/4 keyboard scan output
SCL	2	I	Data input terminal
SDA	3	I	A clock input
A / KI1	8	O/I	LED segment driver output A / key scan input KI1
B / KI2	9	O/I	LED segment driver output B / key scan input KI2
C/KI3	11	O/I	LED segment driver outputs C / key scan input KI3
D / KI4	12	O/I	LED segment driver output D / key scan input KI4
E / KI5	13	O/I	LED segment driver outputs E / key scan input KI5
F / KI6	14	O/I	LED segment driver output F / key scan input KI6
G / KI7	Fifteen	O/I	LED segment driver output G $/$ key scan input KI7
DP / KP	16	O	Segment LED output DP / keyboard flag output KP
GND	4	-	Logically
VDD	10	-	Logic Supply

In the dry season or drying environment, prone to static electricity, electrostatic discharge can damage integrated circuits, microelectronic recommon. All appropriate preventive measures integrated circuit, if improper operation and soldering, ESD may cause damage or performance degradation, the normal work.

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Protocol

TM1650 2-wire serial transmission protocol.

1: The start signal (START) / end signal (STOP) Start signal: Keep SCL is "1" level, SDA from "1" jump "0", that is the start signal,

As (Figure 3) A section;

End signal: Keep SCL is "1" level, SDA from "0" jump "1", that is the end of the signal,

As (Figure 3) E segment;

2: ACK signal

If this communication is normal, the chip after the falling edge of the eighth clock serial communication, TM1650 initiative SDA low. Until inspection Measured to the rising edge of SCL, SDA released as an input, such as (Figure 3) D segment (in terms of chips).

3: Write "1" and write "0."

Writing "1": Keep SDA is "1" level, SCL from "0" to jump to "1", from "1" to move to the "0", it is considered to be written to "1" As (Figure 3) B segment.

Writing "0": Keep SDA "0" level, SCL from "0" to jump to "1", from "1" to move to the "0", then that is written to "0" As (Figure 3) C segment.

image 3)

### 4: a byte of data transmission format

A byte data transmission format shown in Figure 4, the data is sent MSB first, LSB last. Microprocessor data via a two-wire bus Communication interfaces and TM1650, when the input data when SCL is high, SDA signal must remain unchanged; only on SCL The clock signal is low, the signal on to change the SDA. Start condition data input is SCL is high, SDA changes from high Low; end condition is SCL is high, SDA from low to high.

Figure 4)

#### 5: Read the key data timing

When reading data, SCL falling edge, the data from the TM1650 SDA pin output.

Command: sends a read command buttons. Key data: read keyboard scan codes.

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Keyboard scan codes:

TM1650 corresponding to keyboard scan codes:

Addressing	DIG4	DIG3	DIG2	DIG1
A / KI1	47H	46H	45H	44H
B / KI2	4FH	4EH	4DH	4CH
C / KI3	57H	56H	55H	54H
D / KI4	5FH	5EH	5DH	5CH
E / KI5	67H	66H	65H	64H
F / KI6	6FH	6EH	6DH	6CH
G/KI7	77H	76H	75H	74H

Note: When reading the key, DIG and KI series 2K resistor. It does not support the key combination.

#### 1, the data command

Explanation	B0	B1	B2	В3	B4	B5	B6	В7
Mode command	0	0	0	1	0	0	1	0
Kev data read command	1	×	×	1	0	0	1	0

Note: The play is  $1 \times bit$  can be 0, 0 is written recommendations. The other is to be a fixed value.

# 2, the display command

MSE	3				]	LSB	1	
B7 E	36 B5	B4 I	33 B2	2 B1 E	30 function			Explanation
×	0	0	0		××			8 brightness
×	0	0	1		××			A brightness
×	0	1	0		××			2 Brightness
×	0	1	1		××		Daialtanana	3 Brightness
×	1	0	0		××		Brightness settings	4 brightness
×	1	0	1		××			5 brightness
×	1	1	0		××			6 brightness
×	1	1	1		××			7 brightness
×				0	××		7/0	8 segment display
×				1	××		7/8 segment display co	7-segment display
×					$\times \times 0$		0 / 60   1	Off Display
×					$\times \times 1$		On / off the display po	Open display

Note: The play is  $1 \times \text{bit can be } 0$ , 0 is written recommendations.

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### Memory Address:

The register stores transferred from an external device via the serial interface to the TM1650 data of 4-byte units, respectively, with chip A / KIDP / KP and DIG pins are connected to the corresponding LED lights allocated as follows:

Write LED display data, the address from high to low, from the high to the low-byte of data from the operation display.

A/KI1	B/KI2	C / KI3 E	) / KI4	E / KI5	F/KI6	G/KI7	DP / KP	
	xxHL (le	ow nibble)	)		xxHU	(high nibbl	e)	
B0	B1	B2	В3	B4	B5	B6	B7	
	68	HL			68	BHU		DIG1
	6A	HL			64	AHU		DIG2
	6C	CHL		6CHU I				
	6E	EHL			61	EHU		DIG4

### 1: Memory address command:

MSB							LSB	
В7	B6	B5	B4	В3	B2	B1	В0	Memory address
0	1	1	0	1	0	0	0	68H
0	1	1	0	1	0	1	0	6AH
0	1	1	0	1	1	0	0	6CH
0	1	1	0	1	1	1	0	6EH

NOTE: This command is used to set the address register display.

2: write data to the memory address timing:

ADDRESS: TM1650 write to memory address DATA: TM1650 to write data to be displayed.

A complete write display timing

Command1: Data Command: 48H.

Command2: open display, the display brightness level.

ADDRESS: Memory address. DATA: The display data.

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### Absolute maximum ratings) (2)

	parameter	range	unit
VDD	Logic Supply Voltage	-0.5  To + 7.0	V
VIN	Logic input voltage range SDA, SCL	$-0.5 \sim VDD + 0.5V$	V
Topr	Operating temperature range	-40 ~ + 85	$^{\circ}$
Tstg	Storage temperature range	<b>-</b> 55 ∼ + 125	°C
ECD	Human Body Model (HBM)	3000	V
VIN Topr	Machine model (MM)	200	V

(1) in the table above these levels, the chip under conditions of prolonged use, may cause permanent damage to the device can reduce device reliability.

Nevering in any condition, the chip parameters exceed these limits work.

(2) All voltage values are with respect to network testing.

Recommended operating conditions

	parameter	Test Conditions	Min	TM1650 Typical v	alu <b>M</b> ax	unit
VDD	voltage	-	2.8	5.0	7.0	V
VIH	High-level input volta	ige -	0.7VDD	-	VDD	V
VIL	Low level input volta	ge -	0	-	0.3VDD	V
TA	Operating temperatur	re range	-40		+85	℃
TJ	Operating junction to	emperature range	-40		+125	℃

Electrical Characteristics

(At VDD = 3.0V5.5V and -40 °C + VDD = 5.0V and TA = +25 °C) unless otherwise stated

	parameter	Test Conditions		TM1650		unit	
<b>F</b>			Min Typ. Max.				
VDD	Voltage Voltage		2.8	5.0	7.0	V	
IDD	Supply Current		0.2		150	mA	
$IC_{\mathbf{c}}$	Quiescent Current	SCL, SDA, KP is hig	gh	0.2		mA	

VIL	Low level input voltage			2.8		V
VIH	High-level input voltage			2.8		V
VOH	High-level output voltag	ge	VDD-0.4		VDD	V
VOL	Low-level output voltage	e			0.3	V
VOLdig	DIG pin low output voltage	$I_{D\bar{IG}}^{-200mA}$	-		1.3	V
VOLdig	DIG pin low output voltage	$I_{D\bar{I}G}^{=-100\text{mA}}$			0.9	V
VOHdig	DIG pin high output voltage	I <sub>DIG</sub> 5mA	forty five			V
VOLki	KI pin low output voltage	$I_{KI} = -20 \text{mA}$			0.2	V
VOLki	KI pin low output voltage	I <sub>K</sub> 20mA			0.5	V
IDN1	KI pin down current	$V_{KI} = 5.0V$		85		mA
VR	Power-on reset default voltage	e threshold limits		2.5		V

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Internal timing parameters (test conditions:  $Ta = 25 \,^{\circ}\text{C}$ , VDD = 5V)

parameter	symbol	Least	typical	maximum	unit
Power-generation detection reset time	TPR	10	30	60	ms
Display scan period	TP		7		ms
Keyboard scanning interval, the key response time	TKS		40		ms

yboard scanning interval, the key response time TKS 40 ms

Note: This table is built-in clock cycle timing parameters multiples, with the built-in clock frequency reduces the power supply voltage is reduced.

Interface Timing Parameters (test conditions:  $Ta = 25 \,^{\circ}\text{C}$ , VDD = 5V)

parameter	symbol	Minimum Ty	pical Maximur	nunit		
SDA falling edge of the start-up time signal	TSSTA	100		ns		
SDA falling edge of the start signal hold time	THSTA	100		ns		
SDA rising time of the signal to stop the establishmE6Sc00		100		ns		
SDA rising time of the signal to stop holding	THST0	100		ns		
Low-level width SCL clock signal	TCLOW	100		ns		
High-level width SCL clock signal	TCHIG	100		ns		
SDA SCL rising edge of the input data set-up tin	40		ns			
SDA SCL rising edge of the input data retention	10		ns			
SDA output data valid delay the falling edge of SCITAA		2		ns		
SDA output data is invalid delay the falling edge	2		ns			
The average data transfer rate	Rate		4M	bps		
Note: This table unit of measurem@ntThetrisak@nmamoskecoredical value can not indicate infinity.						

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Typical Application Circuit

TM1650 drive common cathode LED screen wiring diagram:

### Remarks:

- Chip filter capacitor in the layout should be as close to the TM1650 when the pin is placed to enhance the filtering effect. 1)
- 2) Chip power and ground network when you try to widen the width of the wire.
- 3) Due to voltage drop blue digital tube is about 3.0V, so the TM1650 power supply should be selected 5.0V.

All specs and applications shown above subject to change without prior notice.

(Above circuit and specifications are for reference only, as the company be amended, without notice.

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Revision History

version issue date Amendment Introduction

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