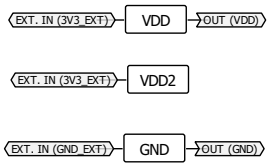
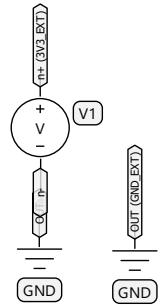
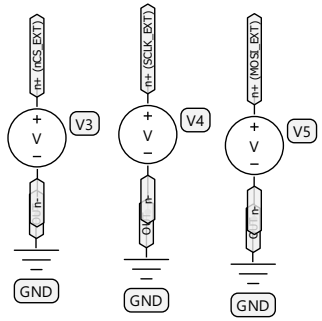
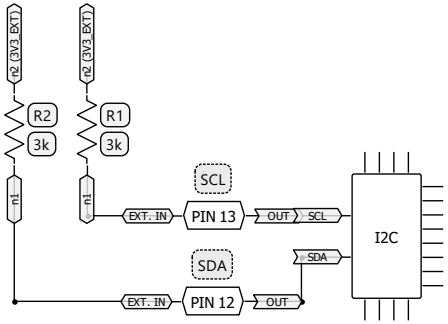
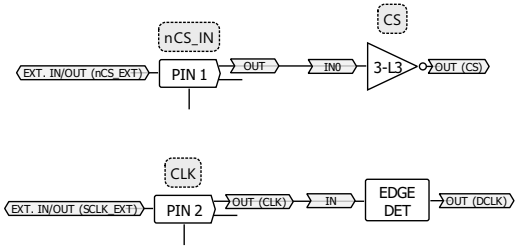
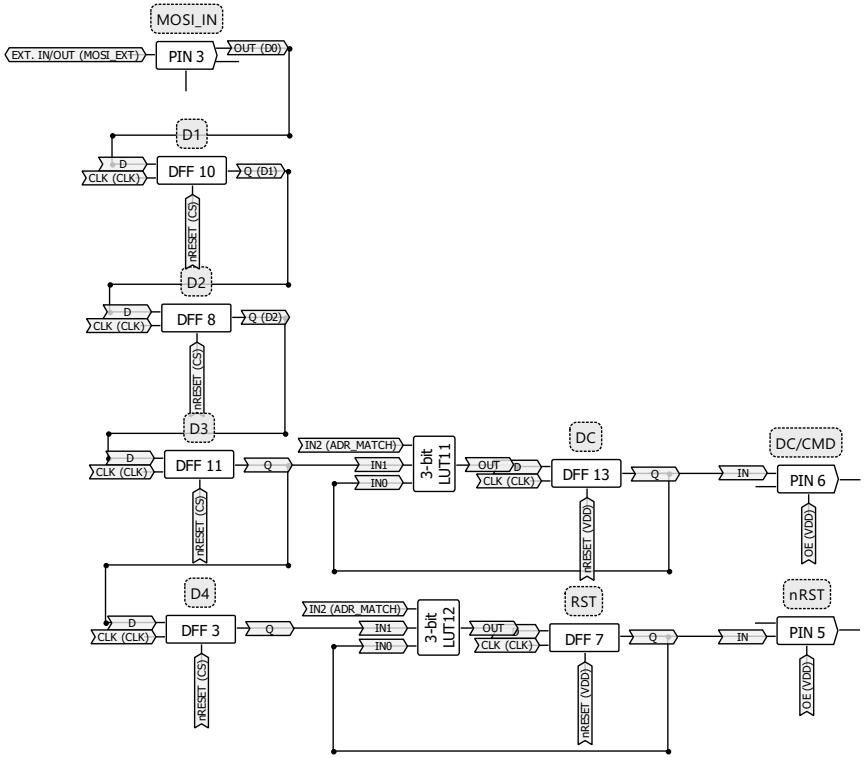

EXT. IN (3V3_EXT)
VDD
OUT (VDD)
EXT. IN (3V3_EXT)
VDD2
EXT. IN (GND_EXT)
GND
OUT (GND)

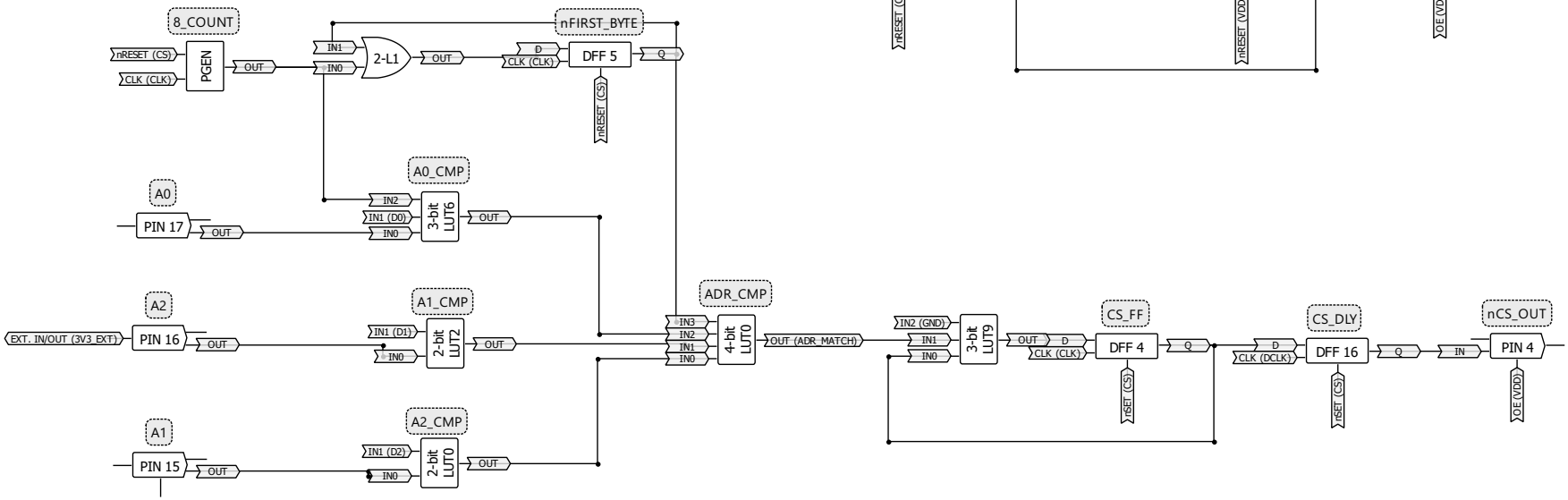

n+ (3V3_EXT)
V1
n-
OUT (GND_EXT)
GND
GND


n+ (nCS_EXT)
V3
n-
n+ (SCLK_EXT)
V4
n-
n+ (MOSI_EXT)
V5
n-
GND
GND
GND


n2 (3V3_EXT)
n2 (3V3_EXT)
R2
3k
R1
3k
n1
n1
SCL
EXT. IN
PIN 13
OUT
SCL
I2C
SDA
SDA
EXT. IN
PIN 12
OUT


nCS_IN
EXT. IN/OUT (nCS_EXT)
PIN 1
OUT
IN0
3-L3
CS
OUT (CS)
CLK
EXT. IN/OUT (SCLK_EXT)
PIN 2
OUT (CLK)
IN
EDGE DET
OUT (DCLK)


MOSI_IN
EXT. IN/OUT (MOSI_EXT)
PIN 3
OUT (D0)
D1
D
CLK (CLK)
DFF 10
Q (D1)
nRESET (CS)
D2
DFF 8
Q (D2)
D3
DFF 11
IN2 (ADR_MATCH)
IN1
IN0
3-bit LUT11
DC
DFF 13
DC/CMD
PIN 6
OE (VDD)
D4
DFF 3
3-bit LUT12
RST
DFF 7
nRST
PIN 5


8_COUNT
nRESET (CS)
CLK (CLK)
PGEN
OUT
IN1
IN0
2-L1
nFIRST_BYTE
DFF 5
A0
PIN 17
A0_CMP
IN2
IN1 (D0)
3-bit LUT6
A2
EXT. IN/OUT (3V3_EXT)
PIN 16
A1_CMP
IN1 (D1)
2-bit LUT2
A1
PIN 15
A2_CMP
IN1 (D2)
2-bit LUT0
ADR_CMP
IN3
IN2
IN1
IN0
4-bit LUT0
OUT (ADR_MATCH)
IN2 (GND)
3-bit LUT9
CS_FF
DFF 4
nSET (CS)
CS_DLY
CLK (DCLK)
DFF 16
nCS_OUT
PIN 4

VDD (PIN 20)

Property	*Value*
Min. value (V)	3.10
Typ. value (V)	3.30
Max. value (V)	3.40

PIN 17 (IO2)
Label: "A0"

Property	*Value*
I/O selection	Digital input
In mode	Digital in with Schmitt trigger
Out mode	None
Resistor	Pull Down
Resistor value	10K

PIN 16 (IO3)
Label: "A2"

Property	*Value*
I/O selection	Digital input
In mode	Digital in with Schmitt trigger
Out mode	None
Resistor	Pull Down
Resistor value	10K

PIN 15 (IO4)
Label: "A1"

Property	*Value*
I/O selection	Digital input
In mode	Digital in with Schmitt trigger
Out mode	None
Resistor	Pull Down
Resistor value	10K

PIN 13 (SCL)
Label: "SCL"

Property	*Value*
I/O selection	Digital input
In mode	Digital in without Schmitt trigger
Out mode	None

PIN 12 (SDA)
Label: "SDA"

Property	*Value*
I/O selection	Digital input
In mode	Digital in without Schmitt trigger
Out mode	None

VDD2 (PIN 7)

Property	*Value*
Min. value (V)	3.10
Typ. value (V)	3.30
Max. value (V)	3.40

PIN 6 (IO9)
Label: "DC/CMD"

Property	*Value*
I/O selection	Digital output
In mode	None
Out mode	1x push pull

PIN 5 (IO10)
Label: "nRST"

Property	*Value*
I/O selection	Digital output
In mode	None
Out mode	1x push pull

PIN 4 (IO11)
Label: "nCS_OUT"

Property	*Value*
I/O selection	Digital output
In mode	None
Out mode	1x push pull

PIN 3 (IO12)
Label: "MOSI_IN"

Property	*Value*
I/O selection	Digital input
In mode	Digital in with Schmitt trigger
Out mode	None
Resistor	Pull Down
Resistor value	100K

PIN 2 (IO13)
Label: "CLK"

Property	*Value*
I/O selection	Digital input
In mode	Digital in with Schmitt trigger
Out mode	None
Resistor	Pull Down
Resistor value	100K

PIN 1 (IO14)
Label: "nCS_IN"

Property	*Value*
I/O selection	Digital input
In mode	Digital in with Schmitt trigger
Out mode	None
Resistor	Pull Up
Resistor value	100K
100uA pullup on input	Disable

FILTER/EDGE DET

Property	Value
Type	EDGE DET
Mode	Falling edge detector
Output polarity	Non-inverted (OUT)

2-bit LUT0/DFF/LATCH0
Label: "A2_CMP"

IN1	IN0	OUT
0	0	1
0	1	0
1	0	0
1	1	1

Property	Value
Type	LUT
Standard gates	NXOR

2-bit LUT1/DFF/LATCH1

IN1	IN0	OUT
0	0	0
0	1	1
1	0	1
1	1	1

Property	Value
Type	LUT
Standard gates	OR

2-bit LUT2/DFF/LATCH2
Label: "A1_CMP"

IN1	IN0	OUT
0	0	1
0	1	0
1	0	0
1	1	1

Property	Value
Type	LUT
Standard gates	NXOR

2-bit LUT3/PGEN
Label: "8_COUNT"

Property	Value
Type	PGEN
Bit range	6 : 0
Pattern	0000001

3-bit LUT0/DFF/LATCH3
Label: "D4"

Property	Value
Type	DFF / LATCH
Mode	DFF
Second Q select	Q of first DFF
nSET/nRESET option	nRESET
Initial polarity	Low
Q output polarity	Non-inverted (Q)

3-bit LUT1/DFF/LATCH4
Label: "CS_FF"

Property	Value
Type	DFF / LATCH
Mode	DFF
nSET/nRESET option	nSET
Initial polarity	High
Q output polarity	Non-inverted (Q)

3-bit LUT2/DFF/LATCH5
Label: "nFIRST_BYTE"

Property	Value
Type	DFF / LATCH
Mode	DFF
nSET/nRESET option	nRESET
Initial polarity	Low
Q output polarity	Non-inverted (Q)

3-bit LUT3/DFF/LATCH6
Label: "CS"

IN0	OUT
0	1
1	0

Property	Value
Type	LUT
Standard gates	Inverter

3-bit LUT4/DFF/LATCH7
Label: "RST"

Property	Value
Type	DFF / LATCH
Mode	DFF
nSET/nRESET option	nRESET
Initial polarity	Low
Q output polarity	Non-inverted (Q)

3-bit LUT5/DFF/LATCH8
Label: "D2"

Property	*Value*
Type	DFF / LATCH
Mode	DFF
nSET/nRESET option	nRESET
Initial polarity	Low
Q output polarity	Non-inverted (Q)

3-bit LUT6/Pipe Delay/Ripple Counter
Label: "A0_CMP"

IN2	*IN1*	*IN0*	*OUT*
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

Property	*Value*
Type	LUT
Standard gates	Defined by user

MF0 (4-bit LUT0, DFF/LATCH9, WS Ctrl, 16-bit CNT0/DLY0/FSM0)

4-bit LUT0 (MF0)
Label: "ADR_CMP"

IN3	*IN2*	*IN1*	*IN0*	*OUT*
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

Property	*Value*
Standard gates	Defined by user

MF1 (3-bit LUT7, DFF/LATCH10, 8-bit CNT1/DLY1)

DFF/LATCH10 (MF1)
Label: "D1"

Property	*Value*
Mode	DFF
nSET/nRESET option	nRESET
Initial polarity	Low
Q output polarity	Non-inverted (Q)

MF2 (3-bit LUT8, DFF/LATCH11, 8-bit CNT2/DLY2)

DFF/LATCH11 (MF2)
Label: "D3"

Property	*Value*
Mode	DFF
nSET/nRESET option	nRESET
Initial polarity	Low
Q output polarity	Non-inverted (Q)

MF3 (3-bit LUT9, DFF/LATCH12, 8-bit CNT3/DLY3)

3-bit LUT9 (MF3)

IN2	*IN1*	*IN0*	*OUT*
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	0

Property	*Value*
Standard gates	Defined by user

MF4 (3-bit LUT10, DFF/LATCH13, 8-bit CNT4/DLY4)

DFF/LATCH13 (MF4)
Label: "DC"

Property	*Value*
Mode	DFF
nSET/nRESET option	nRESET
Initial polarity	Low
Q output polarity	Non-inverted (Q)

MF5 (3-bit LUT11, DFF/LATCH14, 8-bit CNT5/DLY5)

3-bit LUT11 (MF5)

IN2	*IN1*	*IN0*	*OUT*
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

Property	*Value*
Standard gates	Defined by user

MF6 (3-bit LUT12, DFF/LATCH15, 8-bit CNT6/DLY6)

3-bit LUT12 (MF6)

IN2	*IN1*	*IN0*	*OUT*
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

Property	*Value*
Standard gates	Defined by user

MF7 (3-bit LUT13, DFF/LATCH16, 8-bit CNT7/DLY7)

DFF/LATCH16 (MF7)
Label: "CS_DLY"

Property	*Value*
Mode	DFF
nSET/nRESET option	nSET
Initial polarity	High
Q output polarity	Non-inverted (Q)

I2C

Property	*Value*
IO Latching	Enable
Mode selection	Standard/fast mode
Control code, bin	0001
Control byte, read/write	0x11 / 0x10
Device address, dec/hex	8 / 0x08
PIN 19 (IO0) output expander select	From matrix
PIN 14 (IO5) output expander select	From matrix
PIN 11 (IO6) output expander select	From matrix
PIN 6 (IO9) output expander select	From matrix
Virtual OUT0	0
Virtual OUT1	0
Virtual OUT2	0
Virtual OUT3	0
Virtual OUT4	0
Virtual OUT5	0
Virtual OUT6	0
Virtual OUT7	0
PIN 19 (IO0) OUT	0
PIN 14 (IO5) OUT	0
PIN 11 (IO6) OUT	0
PIN 6 (IO9) OUT	0
Control code selection	#3 #2 #1 #0 0 0 0 1

External Components

R1

Property	*Value*
Element	Resistor
Resistance	3kOhm

R2

Property	*Value*
Element	Resistor
Resistance	3kOhm

V1

Property	*Value*
Element	Voltage Source
Pre-start delay	0s
Internal capacitance	100nF
Internal resistance	10Ohm
Pre-start state	Low
Type	DC
DC Voltage	3.3V
Ramp rise time	1ms

V3

Property	*Value*
Element	Voltage Source
Pre-start delay	0s
Repeat state	One-shot
Pre-start state	Start point (V0)
End state	Pre-start state
Type	Logic pattern
Mode	Normal
Umax	3.3V
Umin	0V
Levels adjustment	Standard
Rise time	1µs
Fall time	1µs

V3 Pattern Points

Duration	*Voltage*
5ms	3.3V
9ms	0V

V4

Property	*Value*
Element	Voltage Source
Pre-start delay	5.25ms
Repeat state	One-shot
Pre-start state	Low
End state	Keep last state
Type	Logic pattern
Mode	Normal
Umax	3.3V
Umin	0V
Levels adjustment	Standard
Rise time	1µs
Fall time	1µs

V4 Pattern Points

Duration	*Voltage*
250µs	3.3V
250µs	0V
250µs	3.3V
250µs	0V
250µs	3.3V
250µs	0V
250µs	3.3V
250µs	0V
250µs	3.3V
250µs	0V
250µs	3.3V
250µs	0V
250µs	3.3V
250µs	0V
250µs	3.3V
250µs	0V
250µs	3.3V
250µs	0V
250µs	3.3V
250µs	0V
250µs	3.3V
250µs	0V
250µs	3.3V
250µs	0V
250µs	3.3V
250µs	0V
250µs	3.3V
250µs	0V
250µs	3.3V
250µs	0V

V5	
Property	*Value*
Element	Voltage Source
Pre-start delay	5ms
Repeat state	One-shot
Pre-start state	Low
End state	Pre-start state
Type	Logic pattern
Mode	Normal
Umax	3.3V
Umin	0V
Levels adjustment	Standard
Rise time	1µs
Fall time	1µs

V5 Pattern Points	
Duration	*Voltage*
500µs	3.3V
500µs	0V
500µs	0V
500µs	3.3V
500µs	3.3V
500µs	0V
500µs	3.3V
500µs	0V
500µs	0V
500µs	3.3V
500µs	3.3V
500µs	3.3V
500µs	0V
500µs	3.3V
500µs	3.3V

Project Specs			
	Min.	*Typ.*	*Max.*
VDD (V):	3.10	3.30	3.40
VDD2 (V):	3.10	3.30	3.40
Temperature (°C):	25.00	25.00	25.00

General Settings	
GPIO quick charge	Disable
Pattern ID	1
2k Register lock status	Unlocked
2k NVM lock status	Unlocked
Emulated EEPROM lock status	Unlocked
Protect entire lock configuration	Disable

I2C Probing

Probe pins			
Pin	*Signal name*	*Register*	*In use*
GND (PIN 10) -> OUT	GND	HEX: 0x74`b0 DEC: 116`b0	+
PIN 19 (IO0) -> OUT		HEX: 0x74`b1 DEC: 116`b1	-
PIN 18 (IO1) -> OUT		HEX: 0x74`b2 DEC: 116`b2	-
PIN 17 (IO2) -> OUT	NET21	HEX: 0x74`b3 DEC: 116`b3	+
PIN 16 (IO3) -> OUT	NET14	HEX: 0x74`b4 DEC: 116`b4	+
PIN 15 (IO4) -> OUT	NET26	HEX: 0x74`b5 DEC: 116`b5	+
PIN 14 (IO5) -> OUT		HEX: 0x74`b6 DEC: 116`b6	-
PIN 8 (IO8) -> OUT		HEX: 0x74`b7 DEC: 116`b7	-
PIN 6 (IO9) -> OUT		HEX: 0x75`b0 DEC: 117`b0	-
PIN 5 (IO10) -> OUT		HEX: 0x75`b1 DEC: 117`b1	-
PIN 4 (IO11) -> OUT		HEX: 0x75`b2 DEC: 117`b2	-
PIN 3 (IO12) -> OUT	D0	HEX: 0x75`b3 DEC: 117`b3	+
PIN 2 (IO13) -> OUT	CLK	HEX: 0x75`b4 DEC: 117`b4	+
PIN 1 (IO14) -> OUT	NET13	HEX: 0x75`b5 DEC: 117`b5	+
2-bit LUT0/DFF/ LATCH0 -> OUT	NET17	HEX: 0x75`b6 DEC: 117`b6	+
2-bit LUT1/DFF/ LATCH1 -> OUT	NET22	HEX: 0x75`b7 DEC: 117`b7	+

Probe pins			
2-bit LUT2/DFF/ LATCH2 -> OUT	NET16	HEX: 0x76`b0 DEC: 118`b0	+
2-bit LUT3/PGEN -> OUT	NET28	HEX: 0x76`b1 DEC: 118`b1	+
3-bit LUT0/DFF/ LATCH3 -> Q	NET35	HEX: 0x76`b2 DEC: 118`b2	+
3-bit LUT1/DFF/ LATCH4 -> Q	nCS_OUT	HEX: 0x76`b3 DEC: 118`b3	+
3-bit LUT2/DFF/ LATCH5 -> Q	NET29	HEX: 0x76`b4 DEC: 118`b4	+
3-bit LUT3/DFF/ LATCH6 -> OUT	CS	HEX: 0x76`b5 DEC: 118`b5	+
3-bit LUT4/DFF/ LATCH7 -> Q	NET34	HEX: 0x76`b6 DEC: 118`b6	+
3-bit LUT5/DFF/ LATCH8 -> Q	D2	HEX: 0x76`b7 DEC: 118`b7	+
3-bit LUT6/Pipe Delay/Ripple Counter -> OUT	NET23	HEX: 0x77`b0 DEC: 119`b0	+
3-bit LUT6/Pipe Delay/Ripple Counter -> Q1		HEX: 0x77`b1 DEC: 119`b1	-
3-bit LUT6/Pipe Delay/Ripple Counter -> Q2		HEX: 0x77`b2 DEC: 119`b2	-
FILTER/EDGE DET -> OUT	DCLK	HEX: 0x77`b3 DEC: 119`b3	+
P DLY -> OUT		HEX: 0x77`b4 DEC: 119`b4	-
8-bit CNT1/DLY1 (MF1) -> OUT		HEX: 0x77`b5 DEC: 119`b5	-
OSC1 -> OUT0		HEX: 0x77`b6 DEC: 119`b6	-
OSC0 -> OUT0		HEX: 0x77`b7	-

Probe pins			
		DEC: 119`b7	
OSC2 -> OUT		HEX: 0x78`b0 DEC: 120`b0	-
8-bit CNT2/DLY2 (MF2) -> OUT		HEX: 0x78`b1 DEC: 120`b1	-
8-bit CNT3/DLY3 (MF3) -> OUT		HEX: 0x78`b2 DEC: 120`b2	-
8-bit CNT4/DLY4 (MF4) -> OUT		HEX: 0x78`b3 DEC: 120`b3	-
8-bit CNT5/DLY5 (MF5) -> OUT		HEX: 0x78`b4 DEC: 120`b4	-
8-bit CNT6/DLY6 (MF6) -> OUT		HEX: 0x78`b5 DEC: 120`b5	-
8-bit CNT7/DLY7 (MF7) -> OUT		HEX: 0x78`b6 DEC: 120`b6	-
4-bit LUT0 (MF0) -> OUT	ADR_MATCH	HEX: 0x78`b7 DEC: 120`b7	+
DFF/LATCH10 (MF1) -> Q	D1	HEX: 0x79`b0 DEC: 121`b0	+
DFF/LATCH11 (MF2) -> Q	D3	HEX: 0x79`b1 DEC: 121`b1	+
3-bit LUT9 (MF3) -> OUT	NET31	HEX: 0x79`b2 DEC: 121`b2	+
DFF/LATCH13 (MF4) -> Q	NET33	HEX: 0x79`b3 DEC: 121`b3	+
3-bit LUT11 (MF5) -> OUT	NET25	HEX: 0x79`b4 DEC: 121`b4	+
3-bit LUT12 (MF6) -> OUT	NET32	HEX: 0x79`b5 DEC: 121`b5	+
DFF/LATCH16 (MF7) -> Q	NET36	HEX: 0x79`b6 DEC: 121`b6	+
16-bit CNT0/DLY0/ FSM0 (MF0) -> OUT		HEX: 0x79`b7 DEC: 121`b7	-

Probe pins			
I2C -> OUT7		HEX: 0x7A`b0 DEC: 122`b0	-
I2C -> OUT6		HEX: 0x7A`b1 DEC: 122`b1	-
I2C -> OUT5		HEX: 0x7A`b2 DEC: 122`b2	-
I2C -> OUT4		HEX: 0x7A`b3 DEC: 122`b3	-
I2C -> OUT3		HEX: 0x7A`b4 DEC: 122`b4	-
I2C -> OUT2		HEX: 0x7A`b5 DEC: 122`b5	-
I2C -> OUT1		HEX: 0x7A`b6 DEC: 122`b6	-
I2C -> OUT0		HEX: 0x7A`b7 DEC: 122`b7	-
A CMP0H -> OUT		HEX: 0x7B`b0 DEC: 123`b0	-
A CMP1H -> OUT		HEX: 0x7B`b1 DEC: 123`b1	-
A CMP2L -> OUT		HEX: 0x7B`b2 DEC: 123`b2	-
A CMP3L -> OUT		HEX: 0x7B`b3 DEC: 123`b3	-
OSC1 -> OUT1		HEX: 0x7B`b4 DEC: 123`b4	-
OSC0 -> OUT1		HEX: 0x7B`b5 DEC: 123`b5	-
POR -> OUT		HEX: 0x7B`b6 DEC: 123`b6	-
VDD (PIN 20) -> OUT	VDD	HEX: 0x7B`b7 DEC: 123`b7	+

Macrocells		
Macrocell	*Property*	*Register*
16-bit CNT0/DLY0/FSM0 (MF0)	Counted Data	HEX: 0x7C, 0x7D DEC: 124, 125
8-bit CNT2/DLY2 (MF2)	Counted Data	HEX: 0x7E DEC: 126
8-bit CNT4/DLY4 (MF4)	Counted Data	HEX: 0x7F DEC: 127