

ECEE 5623 RT Embedded Systems

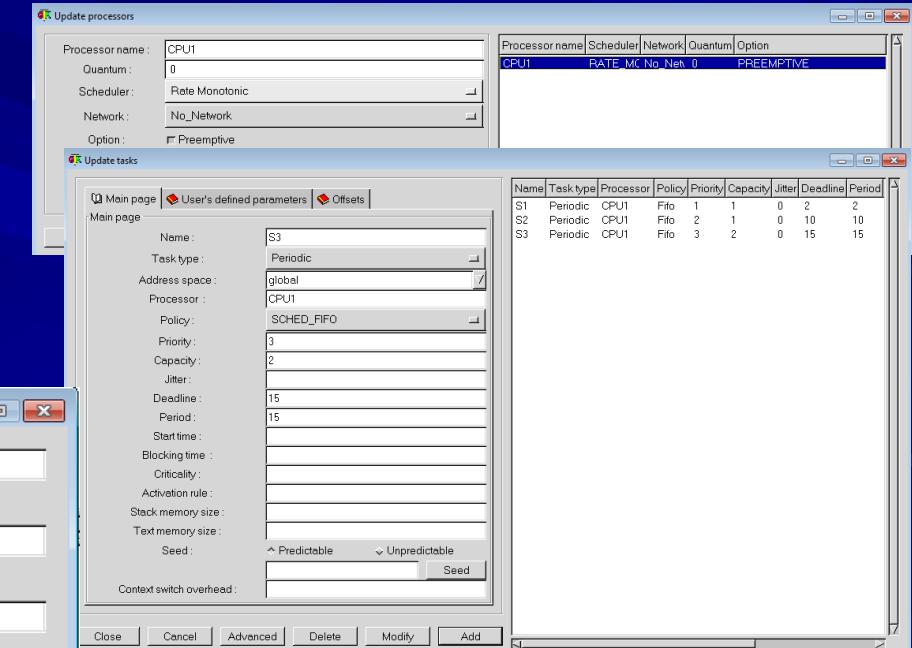
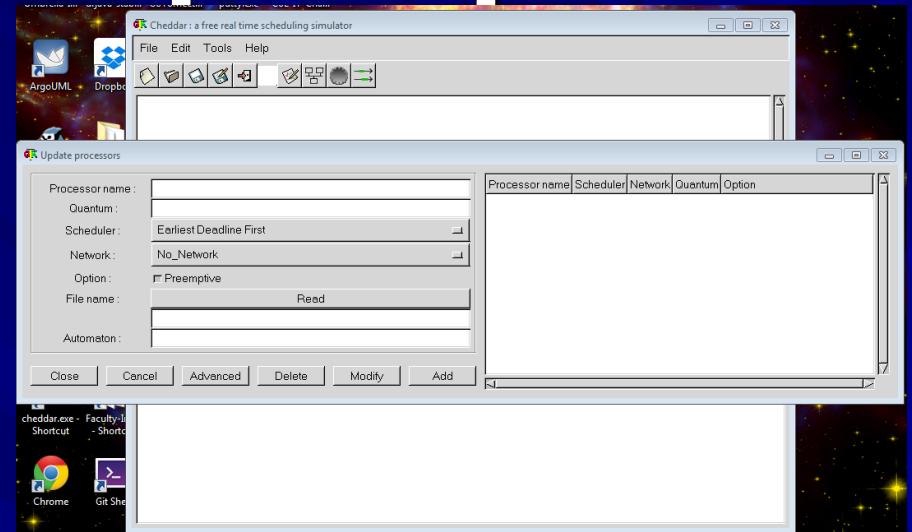
*Lecture – RM Analysis Examples with
Cheddar*

Using Cheddar [Basics]

■ Download for Windows
[[here](#)] or Canvas Files

■ Use “Edit” to Start

1. Start with Update Processors
2. Add it
3. Update Address Spaces, Add it
4. Update Tasks, Add $S_1 \dots S_n$
5. Note Cheddar Runs over LCM



Newer Versions of the Tool

■ Cheddar 2.1 for Windows [on Canvas]

- [Examples-2.1](#) for RTEs
- Download of [Cheddar-2.1 for win32](#)

Use Windows
Cheddar 3.1
Version

■ Cheddar 3.0 for Windows [on Canvas]

- [Examples-3.0](#) for RTEs [Tested and ported from 2.1]
- Cheddar 3.0 User's Guide - [Here](#)

■ Cheddar 3.1 for Windows [[Download](#) or Canvas]

- [Examples-3.1](#) for RTEs [Tested and ported from 3.0]
- Cheddar 3.1 User's Guide - [Here](#)

■ Cheddar 3.1 for Linux [[Download](#)]

- Run on Linux systems [I have not tested yet]

■ Local copy - <http://ecee.colorado.edu/~ecen5623/design/Cheddar-tools/>

Cheddar 3.1 is Latest (2019)

■ Cheddar 3.1 has a new “look and feel”

■ Load an XML Example

■ Hit the Gray Start Button (it is NOT grayed out)

■ QUICK START document

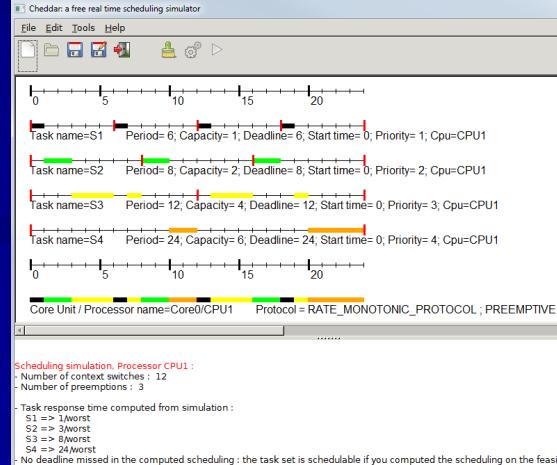
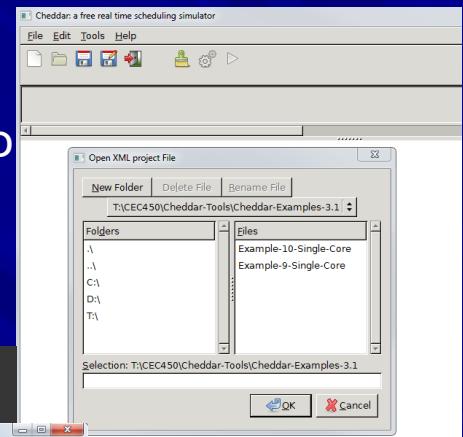
Name	Date modified	Type	Size
glade_files	10/3/2018 10:30 AM	File folder	
project_examples	10/3/2018 10:30 AM	File folder	
aadl2aadl.exe	10/9/2017 2:59 AM	Application	18,196 KB
aadl2xml.exe	10/9/2017 2:59 AM	Application	19,276 KB
AUTHORS.txt	7/19/2017 8:06 AM	Text Document	1 KB
BUGS_TO_FIX.pdf	10/9/2017 2:11 AM	Adobe Acrobat D...	71 KB
ChangesLog.pdf	10/9/2017 2:11 AM	Adobe Acrobat D...	98 KB
cheddar.exe	10/9/2017 2:59 AM	Application	22,053 KB

#1 - Run

#2 - Browse to Example



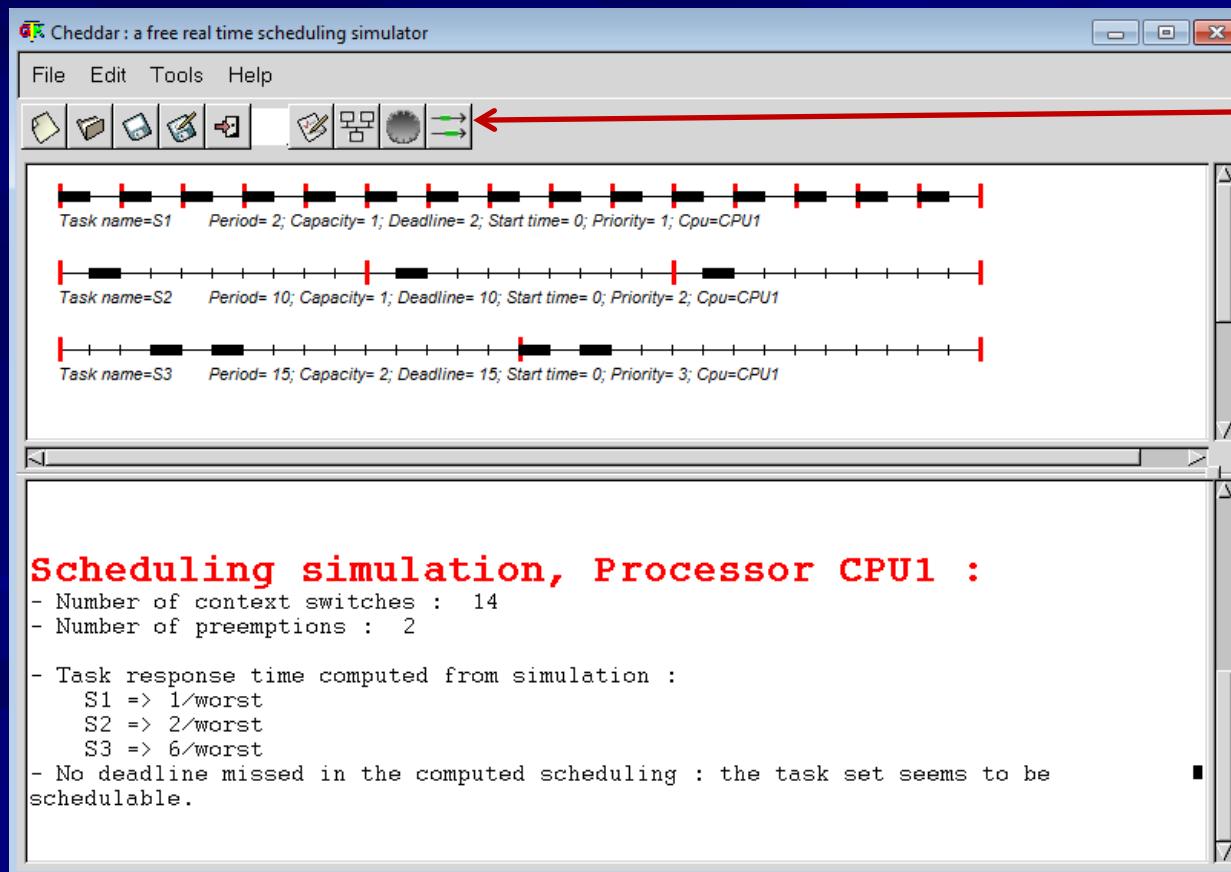
#3 - Hit Play and OK



#4 - Review analysis and change parameters and re-run as needed

Simulation 2.1

- Hit Simulation button to Start
- Calculates LCM, Runs, Produces Timing Diagram and Summary

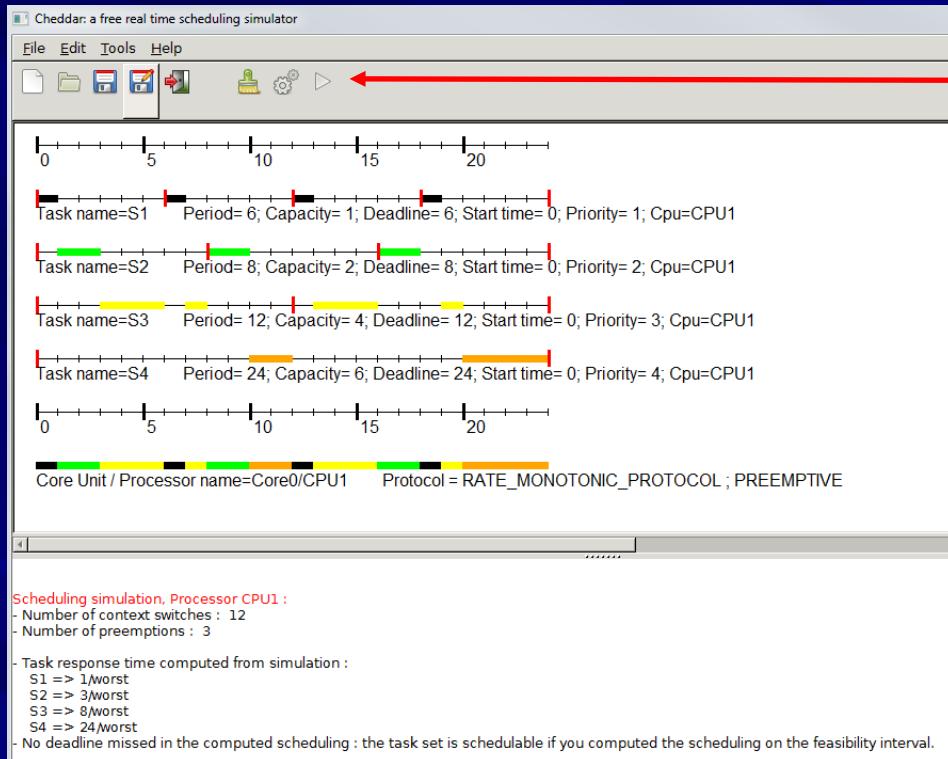


Simulation Button

Timing Diagram

Summary – Note the conclusion “seems”

Simulation 3.1



Simulation button in 3.1

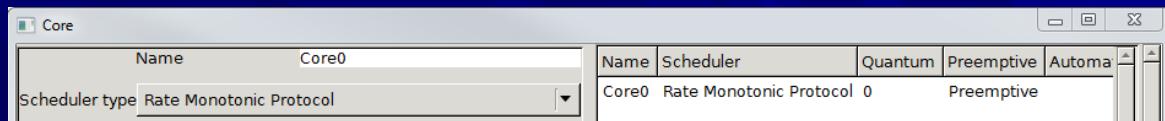
- Simulation button looks like grayed out arrow
 - Load an XML configuration and hit it anyway!
 - E.g. Example-9, with LCM=24 - Check match

v3.1 - Building up a new XML file for Ex 9

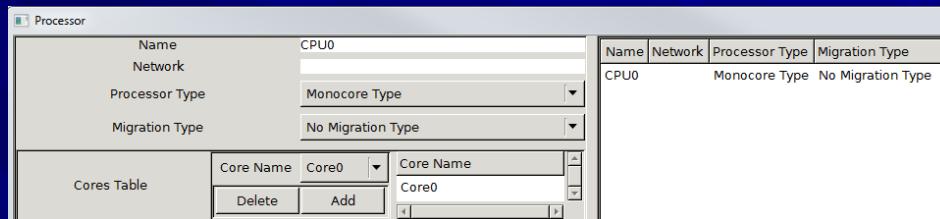
File New, Use "Edit" to Start

1. Hardware, Core, Add it
2. Hardware, Processor, Select Core from above, Add it
3. Software, Address Space, Add it
4. Software, Tasks, Add S₁...S_n
5. Run it!
6. Compare
7. Note Cheddar Runs over LCM

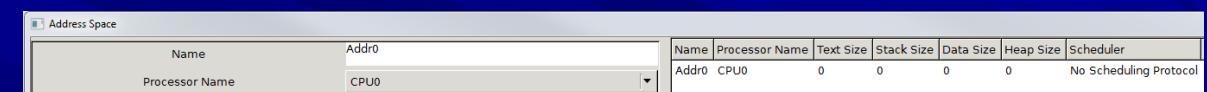
Select Hardware, Software or Deployment



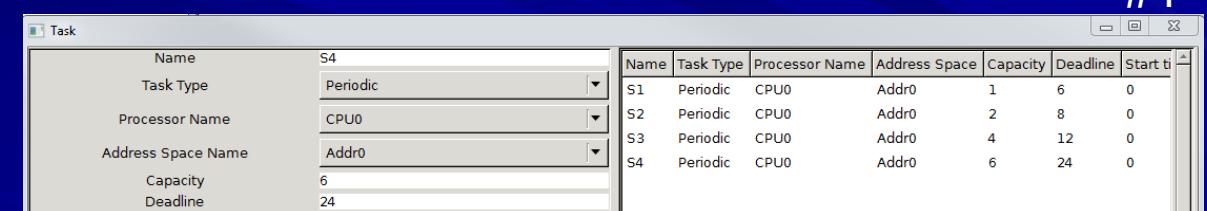
#1



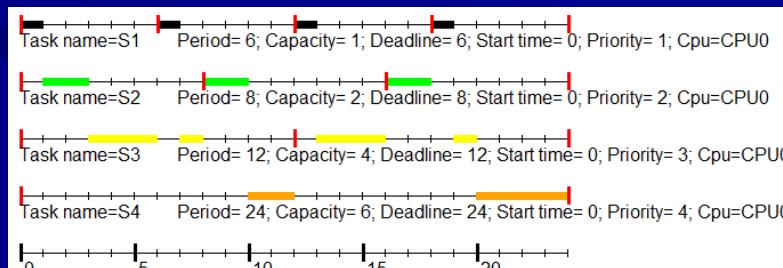
#2



#3



#4



#5

Feasibility Test

- Hit Feasibility button to Test
- For RM Policy, Cheddar Uses the RM LUB
- For All Policies, Cheddar Provides Worst-Case Analysis

Scheduling feasibility, Processor CPU1 :

1) Feasibility test based on the processor utilization factor :

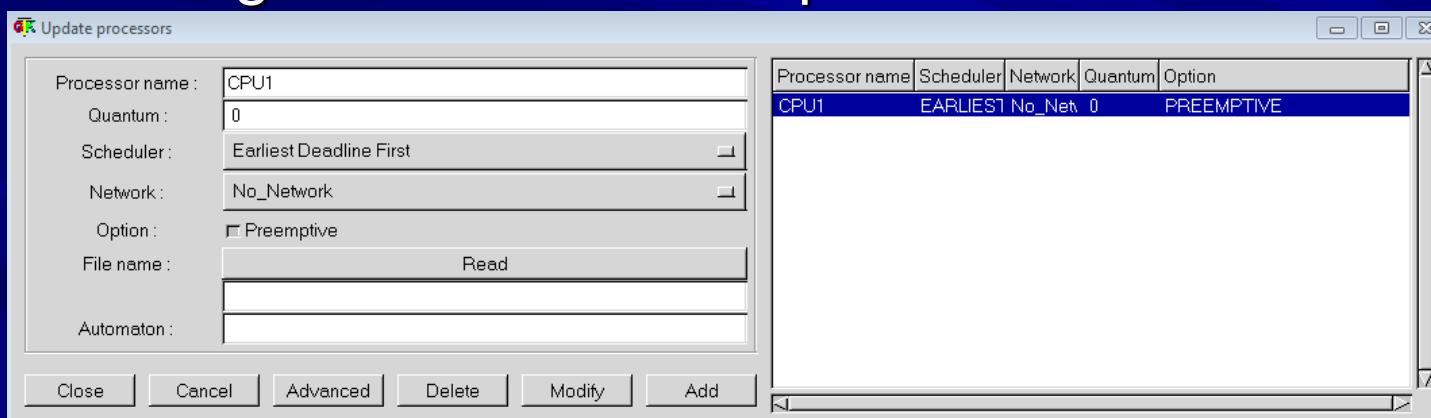
- The base period is 30 (see [18], page 5).
- 8 units of time are unused in the base period.
- Processor utilization factor with deadline is 0.73333 (see [1], page 6).
- Processor utilization factor with period is 0.73333 (see [1], page 6).
- In the preemptive case, with RM, the task set is schedulable because the processor utilization factor 0.73333 is equal or less than 0.77976 (see [1], page 16, theorem 8).

2) Feasibility test based on worst case task response time :

- Bound on task response time : (see [2], page 3, equation 4).
 - S3 => 6
 - S2 => 2
 - S1 => 1
- All task deadlines will be met : the task set is schedulable.

RM Policy Example

- Change with “Edit” and Update Processors to EDF



Run Again with EDF to Compare

- Priorities are Dynamic, So Just Change Processor Scheduler Policy, Re-Run Simulation and Feasibility

Scheduling feasibility, Processor CPU1 :

1) Feasibility test based on the processor utilization factor :

- The base period is 30 (see [18], page 5).
- 8 units of time are unused in the base period.
- Processor utilization factor with deadline is 0.73333 (see [1], page 6).
- Processor utilization factor with period is 0.73333 (see [1], page 6).
- In the preemptive case, with EDF, the task set is schedulable because the processor utilization factor 0.73333 is equal or less than 1.00000 (see [1], page 8, theorem 2).

2) Feasibility test based on worst case task response time :

- Bound on task response time :

S1 => 1
S2 => 8
S3 => 13

- All task deadlines will be met : the task set is schedulable.

Note EDF

Scheduling feasibility, Processor CPU1 :

1) Feasibility test based on the processor utilization factor :

- The base period is 30 (see [18], page 5).
- 8 units of time are unused in the base period.
- Processor utilization factor with deadline is 0.73333 (see [1], page 6).
- Processor utilization factor with period is 0.73333 (see [1], page 6).
- In the preemptive case, with LLF, the task set is schedulable because the processor utilization factor 0.73333 is equal or less than 1.00000 (see [7]).

2) Feasibility test based on worst case task response time :

- Bound on task response time :

S1 => 1
S2 => 8
S3 => 13

- All task deadlines will be met : the task set is schedulable.

Note LLF

Example-0 Timing Diagram

■ RM, EDF, LLF Succeed, 73.33% CPU Utilization

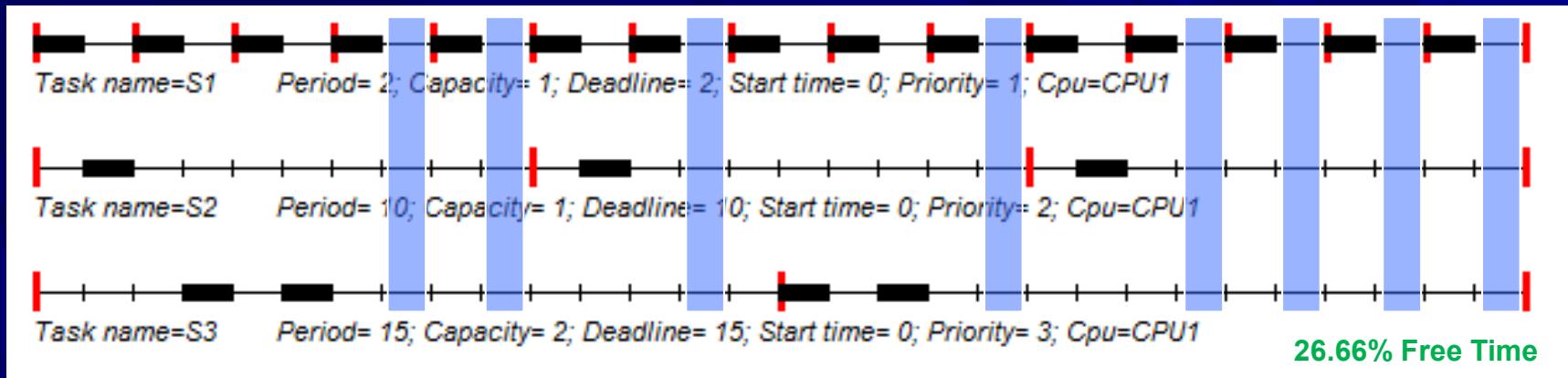
Example 0	T1	2	C1	1	U1	0.5	LCM =	30														
	T2	10	C2	1	U2	0.1																
	T3	15	C3	2	U3	0.133	Utot =	0.733														
RM Schedule	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15							
S1																						
S2																						
S3																						
EDF Schedule																						
S1																						
S2																						
S3																						
TTD																						
S1	2	X	2	X	2	X	2	X	2	X	2	X	2	X	2	X	2	X	2	X	2	
S2	10	9	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	
S3	15	14	13	12	11	10	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	

Scheduling simulation, Processor CPU1 :

- Number of context switches : 14
- Number of preemptions : 2
- Task response time computed from simulation :
 - S1 => 1/worst
 - S2 => 2/worst
 - S3 => 6/worst
- No deadline missed in the computed scheduling : the task set seems to be schedulable.

Example-0 Cheddar RTSS

■ Download Cheddar RT Analyzer, Example-0 XML



Scheduling feasibility, Processor CPU1 :

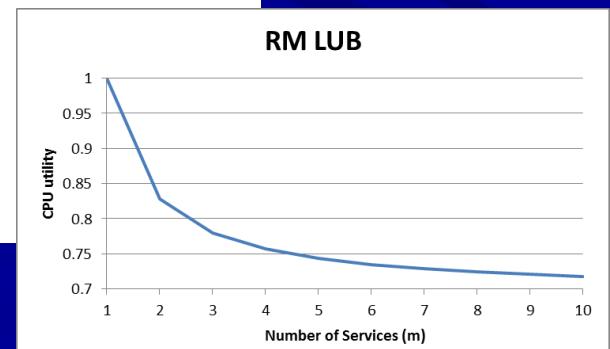
1) Feasibility test based on the processor utilization factor :

- The base period is 30 (see [18], page 5).
- 8 units of time are unused in the base period.
- Processor utilization factor with deadline is 0.73333 (see [1], page 6).
- Processor utilization factor with period is 0.73333 (see [1], page 6).
- In the preemptive case, with RM, the task set is schedulable because the processor utilization factor 0.73333 is equal or less than 0.77976 (see [1], page 16, theorem 8).

2) Feasibility test based on worst case task response time :

- Bound on task response time : (see [2], page 3, equation 4).
S3 => 6
S2 => 2
S1 => 1
- All task deadlines will be met : the task set is schedulable.

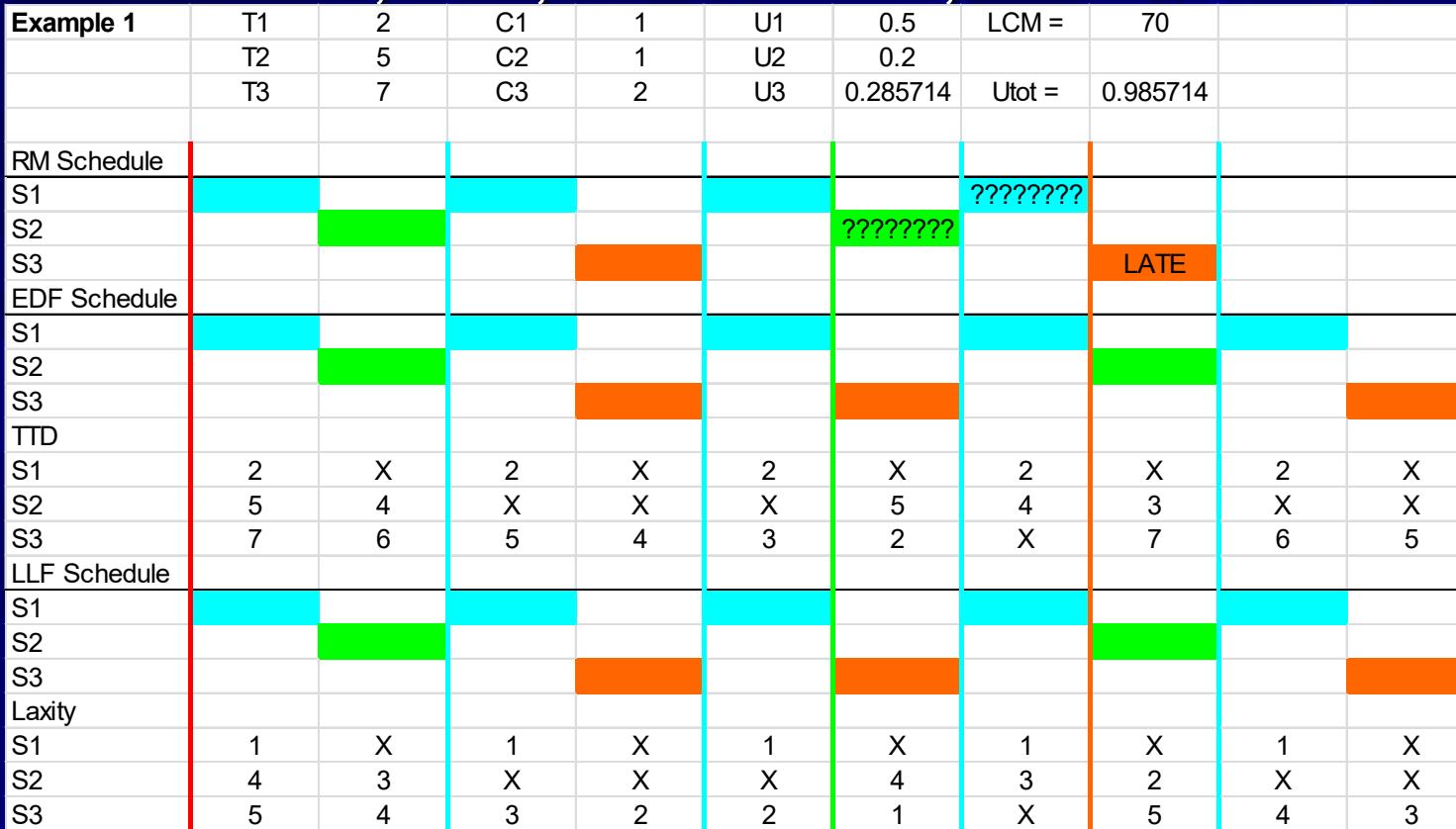
$$U = \sum_{i=1}^m (C_i / T_i) \leq m(2^{\frac{1}{m}} - 1)$$



Cheddar Simulates over LCM (Hyperperiod)

Example-1 Timing Diagram

■ RM FAILS, EDF, LLF Succeed, 98.57% CPU Utilization



Scheduling simulation, Processor CPU1 :

- Number of context switches : 68
- Number of preemptions : 10
- Task response time computed from simulation :
 - S1 => 1/worst
 - S2 => 2/worst
 - S3 => 8/worst , missed its deadline (deadline = 7 ; completion time = 8)
- Some task deadlines will be missed : the task set is not schedulable.

Example-1 Cheddar RTSS

■ RM Not Feasible by LUB or by Inspection over LCM

Scheduling feasibility, Processor CPU1 :

1) Feasibility test based on the processor utilization factor :

- The base period is 70 (see [18], page 5).
- 1 units of time are unused in the base period.
- Processor utilization factor with deadline is 0.98571 (see [1], page 6).
- Processor utilization factor with period is 0.98571 (see [1], page 6).
- In the preemptive case, with RM, we can not prove that the task set is schedulable is more than 0.77976 (see [1], page 16, theorem 8).

2) Feasibility test based on worst case task response time :

- Bound on task response time : (see [2], page 3, equation 4).
 - S3 => 8, missed its deadline (deadline = 7)
 - S2 => 2
 - S1 => 1
- Some task deadlines will be missed : the task set is not schedulable.

■ EDF?

Scheduling feasibility, Processor CPU1 :

1) Feasibility test based on the processor utilization factor :

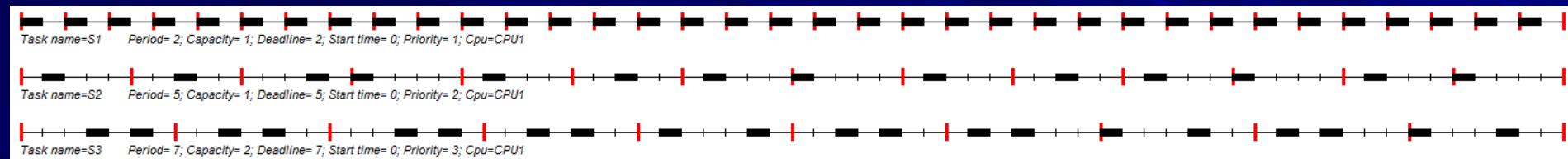
- The base period is 70 (see [18], page 5).
- 1 units of time are unused in the base period.
- Processor utilization factor with deadline is 0.98571 (see [1], page 6).
- Processor utilization factor with period is 0.98571 (see [1], page 6).
- In the preemptive case, with EDF, the task set is schedulable because the processor utilization factor 0.98571 is equal or less 1.00000 (see [1], page 8, theorem 2).

2) Feasibility test based on worst case task response time :

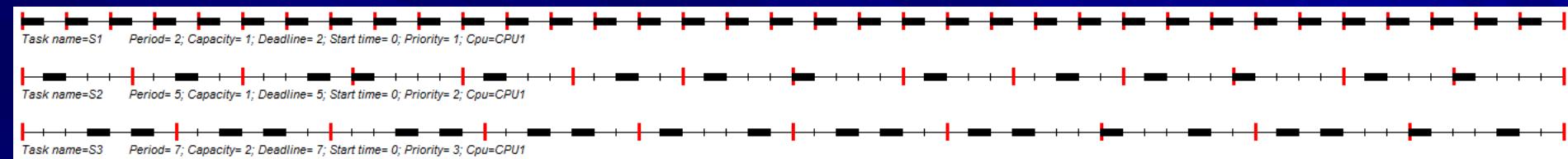
- Bound on task response time :
 - S1 => 1
 - S2 => 4
 - S3 => 6
- All task deadlines will be met : the task set is schedulable.

Example-1 Cheddar RTSS

■ EDF Simulation over LCM of 70



■ LLF Simulation over LCM of 70



■ Worst Case Feasibility Test

- Fixed Priority (RM Policy) FAILS LUB and WC Feasibility Test (Scheduling Point or Completion Test)
- Dynamic Priority Succeeds by Two Methods

Example 9 – RM Policy

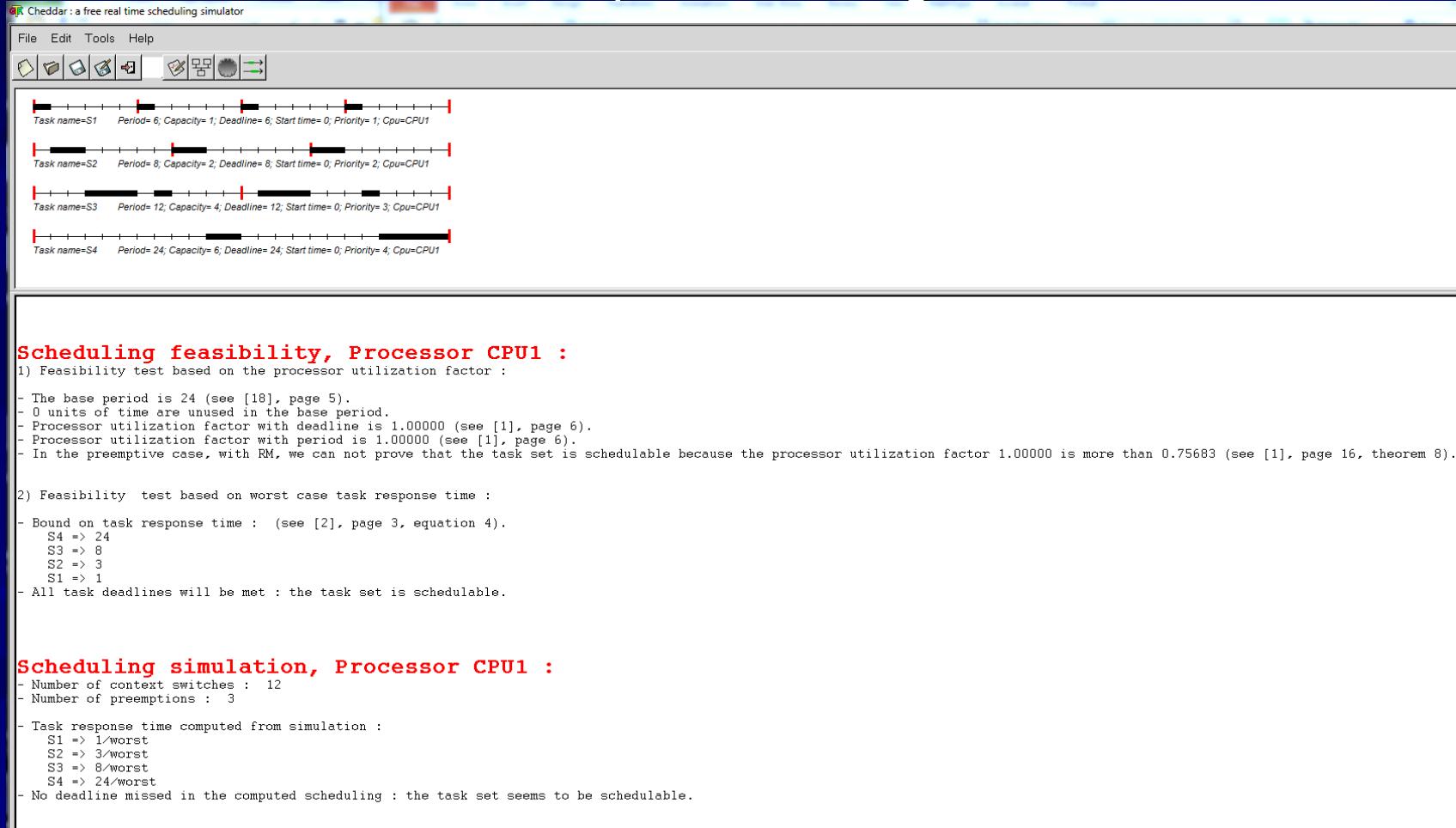
■ Harmonic Services with 100% CPU Utilization

■ Preemptions – 3 in Total:

- @6 S1 preempts S3
 - @12 S1 preempts S4
 - @16 S2 preempts S3

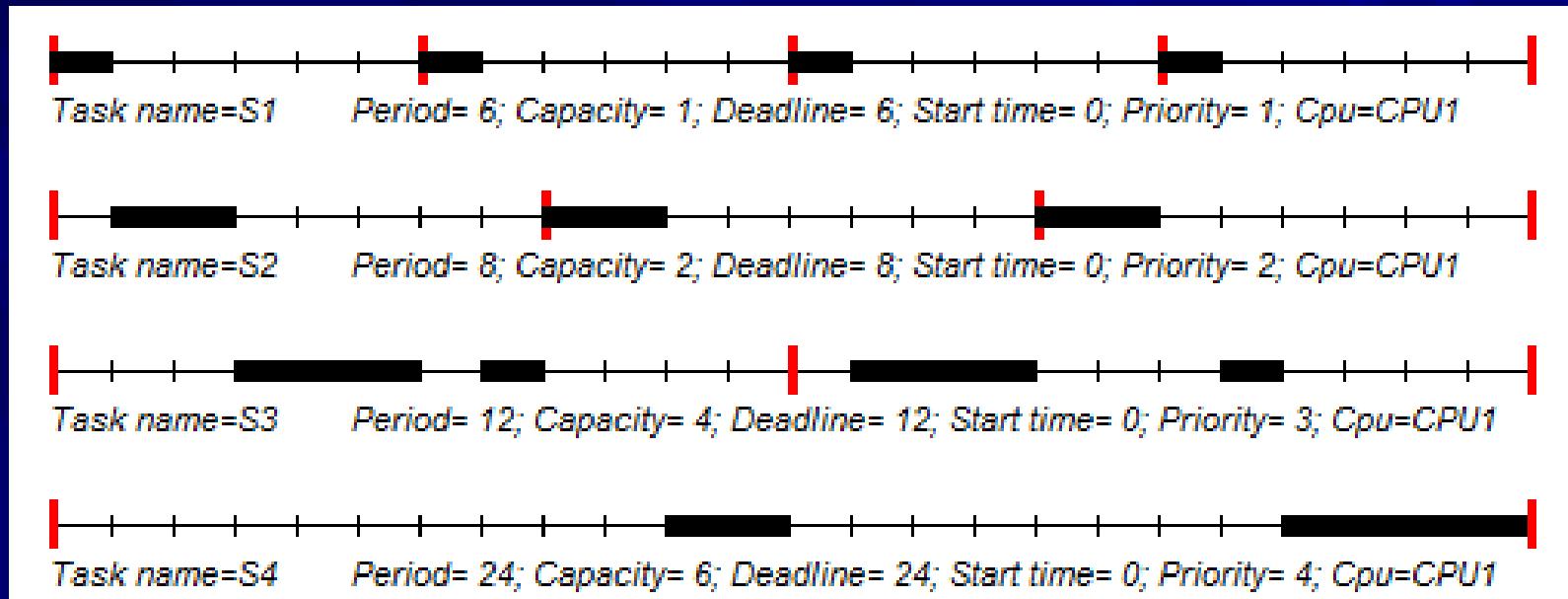
Example 9 – Cheddar RM WC Analysis and Simulation

- Run WC analysis
- Run Simulation to Graph over Longest T or LCM



Example 9 – RM Simulation

- Automates Hand Simulation
- Simpler Modification for Multiple CPUs, Policies, etc.



Example 9 – EDF Simulation

- No Difference from RM in Simulation
- Ties Could Be Broken Randomly [Most Often Favor Highest Frequency – Same as RM]
- Worst-Case Analysis However Shows “task set is schedulable”

Scheduling feasibility, Processor CPU1 :

1) Feasibility test based on the processor utilization factor :

- The base period is 24 (see [18], page 5).
- 0 units of time are unused in the base period.
- Processor utilization factor with deadline is 1.00000 (see [1], page 6).
- Processor utilization factor with period is 1.00000 (see [1], page 6).
- In the preemptive case, with EDF, the task set is schedulable because the processor utilization factor 1.00000 is equal or less than 1.00000 (see [1], page 8, theorem 2).

2) Feasibility test based on worst case task response time :

- Bound on task response time :

S1 => 6
S2 => 8
S3 => 12
S4 => 24

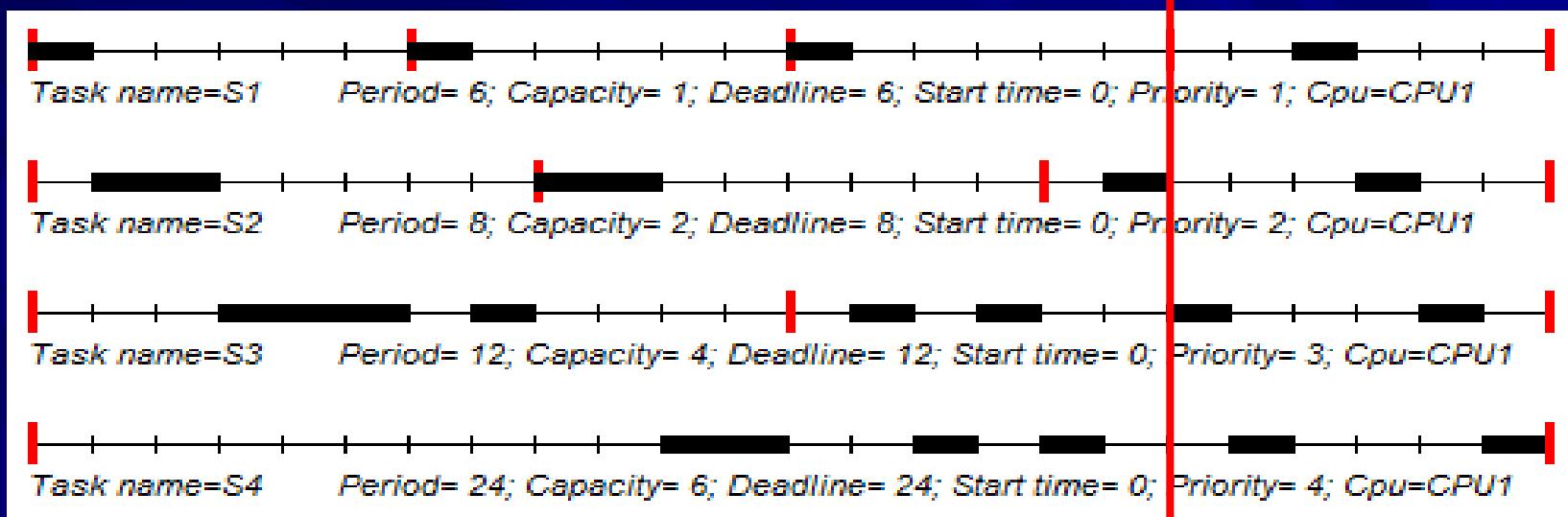
- All task deadlines will be met : the task set is schedulable.

TTD metric for dispatch results in “ties”, noted in red

EDF Schedule																									
		S1	S2	S3	S4																				
TTD		6	X	X	X	X	X	X	X	6	X	X	X	X	X	X	X	X	X	X	6	X	X	X	
S1		6	7	6	9	8	7	6	5	8	7	10	9	11	10	9	8	7	6	5	4	3	2	1	
S2		8	7	6	9	8	7	6	5	8	7	10	9	11	10	9	8	7	6	5	4	3	2	1	
S3		12	11	10	9	8	7	6	5	12	11	10	9	8	7	6	5	4	3	2	1				
S4		24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1

Example 9 – LLF Simulation

- LLF Hand Sim Tedious (Laxity = TTD – Time_to_go)
 - Much Different than RM or EDF
 - Assume Ties Favor Highest Frequency Service? - YES



LLF Schedule 2																				
S1																				
S2																				
S3																				
S4																				
Laxity																				
S1	5	X	X	X	X	X	5	X	X	X	X	5	X	X	X	X	X	X	X	
S2	6	5	5	X	X	X	X	X	6	6	X	X	X	X	X	X	6	5	5	4
S3	8	7	6	5	5	5	5	4	X	X	X	X	8	7	7	6	6	5	4	4
S4	18	17	16	15	14	13	12	11	10	9	8	8	8	7	6	6	5	5	4	3

Review Remaining Examples

- http://ecee.colorado.edu/~ecen5623/ecen/linuxrt_papers/Timing_Diagrams_Updated_2019
- As Noted in Liu and Layland, Static Priority Policy May Not be Feasible in Cases where Dynamic Priority Policy is Feasible
- Are Feasibility and Safety Synonymous?
- Is it Wise to have Zero Margin?
- Have We Accounted for Context Switch Overhead and ISR Latency?

Cheddar References

- Help, Scheduling References
- References Used to Build Cheddar – [Here](#)
- General References - [Here](#)

Scheduling references	
[1]	Preemptive and Non-Preemptive Real Time Uni-Processor Scheduling. L. George, N. Rivierre and M. Spuri INRIA Research Report number 2966. September 1996.
[2]	Holistic Schedulability Analysis for Distributed Hard Real-Time Systems. K. Tindell and J. Clark Microprocessing and Microprogramming 40:117-134. 1994.
[3]	Priority Inheritance Protocols : An Approach to Real Time Synchronization. L. Sha, R. Rajkumar and J.P. Lehoczky IEEE Transactions on computers, 39(9):1175-1185. 1990.
[4]	About Bounds of Buffers Shared by Periodic Tasks : the IRMA project. J. Legrand, F. Singhoff, L Nana, L. Marce, F. Dupont and H. Hafidi
[5]	L. Marce, F. Dupont and H. Hafidi In the 15th IEEE Euromicro, WIP Real Time Systems Conference, 2003.
[6]	Scheduling dependant tasks with Different Arrival Times to Meet Deadlines. J. Blazewicz In. Gelende H. Beilner (eds), Modeling and Performance Evaluation of Computer Systems,. Amsterdam 1976
[7]	Dynamic Scheduling of Real Time Tasks Under Precedence Constraints. H. Chetto, M. Silly and T. Bouchentouf RTS International Journal of Time Critical Computing Systems. 2(3):181-194, September 1990.
	Scheduling Algorithms for multi-Programming in a hard-real-time environment. C. L. Liu and J. W. Layland Journal of the ACM, 20 (1):46--61,1973.