CSE 306 Assignment 1
A1
Group 5

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1 Introduction

A processor unit implements the operations in a digital system or a digital computer. It is comprised of a number of registers and the digital functions implementing arithmetic, logic, shift and transfer micro-operations. A Central Processing Unit or CPU is basically the processor unit combined with a control unit.

An operation may be implemented in a processor unit either with a single micro-operation or with a sequence of micro-operations. The digital function that implements the micro-operations on the information stored in processor registers is called an Arithmetic Logic Unit or ALU. The control routes the source information from registers into the inputs of ALU. Then the ALU performs a given operation as specified by the control.

An ALU is a multi-operation, combinational-logic digital function that can perform a set of basic arithmetic and logic operations. It has a number of selection lines to select a particular operation (arithmetic or logic) in the unit. The selection lines are decoded within the ALU so that k selection variables can specify up to 2k distinct operations.

The main component of an ALU is a parallel binary adder. A parallel adder is comprised of a number of full adders connected in cascade. By controlling the data inputs to the parallel adder, it is possible to obtain different types of arithmetic operations. It is also possible to obtain different logic operations by controlling those data inputs and the carry inputs to the cascaded Full Adders.

The steps involved in the design of an ALU are as follows:

- Designing the arithmetic section independent of the logic section.
- Determining the logic operations obtained from the arithmetic circuit in step 1, assuming that the input carries to all stages are 0.
- Modifying the arithmetic circuit to obtain the required logic operations.

2 Problem Specification with assigned instructions

Design an ALU for the following function specification

C_{in} S_2	S_1	S_0	Function
0	0	0	Add
0	1	0	Transfer A
1	0	0	Add with carry
1	1	0	Increment A
x	0	1	OR
x	1	1	Complement A

3 Truth Table and Required k-maps

C_{in} S_2	S_1	S_0	Function	X	Y	Z
0	0	0	$A + B$	A	B	0
0	1	0	A	A	0	0
1	0	0	$A + B + 1$	A	B	1
1	1	0	$A + 1$	A	0	1
x	0	1	$A \vee B$	$A \vee B$	0	0
x	1	1	$\overline{A}$	A	1	0

S_1S_0 \ A_iB_i	00	01	11	10
00	0	0	1	1
01	0	1	1	1
11	0	0	1	1
10	0	0	1	1

$$X_i = A_i + \overline{S_1} S_0 B_i$$

B_i \ S_1S_0	00	01	11	10
0	0	0	1	0
1	1	0	1	0

$$Y_i = \overline{S_1}\ \overline{S_0}\ B_i + S_1 S_0$$

C_i \ S_1S_0	00	01	11	10
0	0	0	0	0
1	1	0	0	1

$$Z_i = \overline{S_0} C_i$$

4 Block Diagram

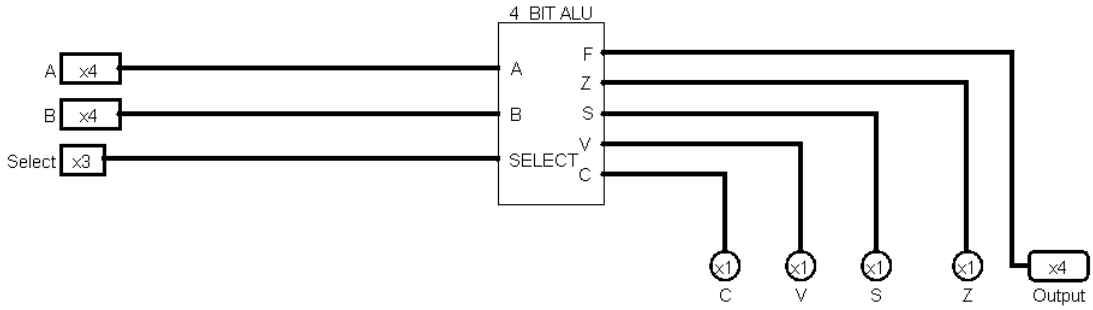

Figure 1: 4 bit ALU Block Diagram

5 Complete Circuit diagram

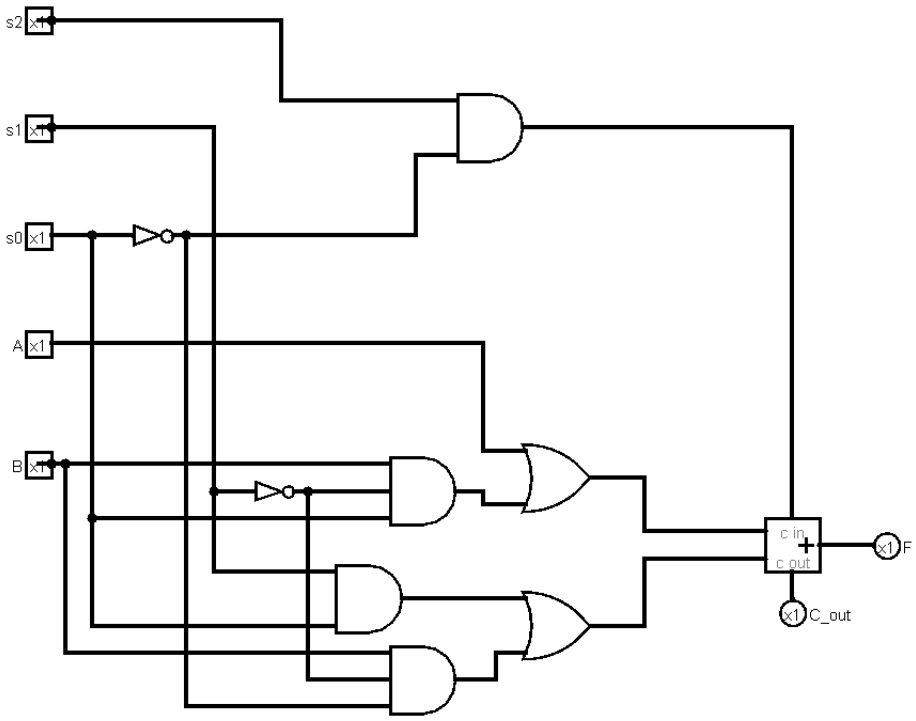

Figure 2: Circuit Diagram : 1 bit Combinational Circuit with Adder

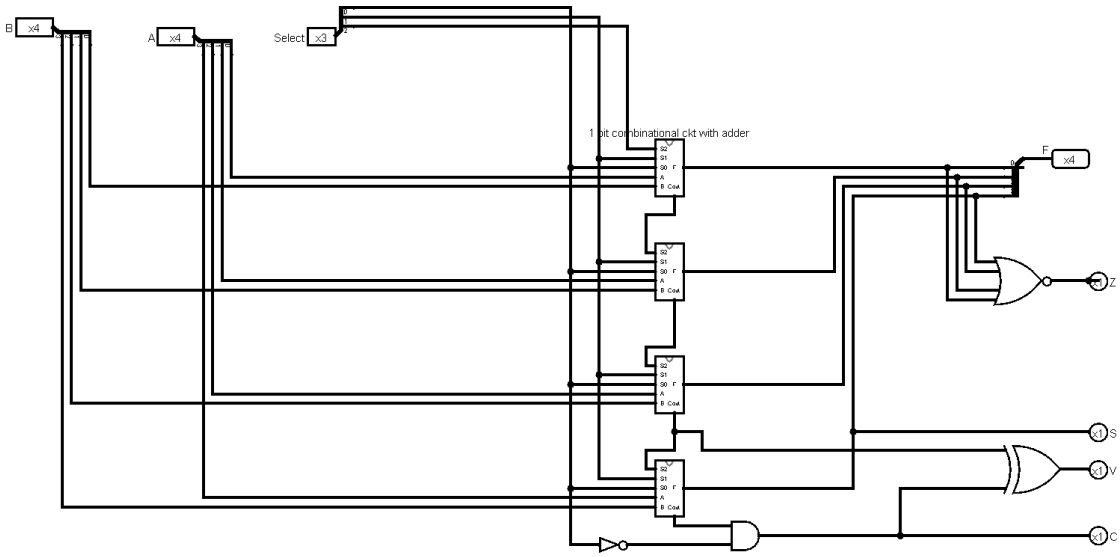

Figure 3: Circuit Diagram : 4 bit ALU

6 ICs used with count as a chart

7 Simulator

Logisim Version 2.7.1

8 Discussion

While implementing the circuit, we had to change our design several times. Some designs required a lot of ICs. To optimize number of ICs in our design, we had to discard those. Also, in some cases we reused some logic gate outputs to minimize the number of ICs used. Considering all these aspects, we finally implemented the most optimized design we could find.