ADC in ATMEGA32

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Relation with clock rate

1 ADC conversion takes 13 ADC cycle

Clock-rate ↓ Fast ↑ Accuracy ↓

The clock-rate is set using **prescaler**

Mechanism

- ADC Multiplexer Select (`ADMUX`) : MUX to select certain input ADC
- ADC Control and Status Register (`ADCSRA`) : to check if reading is converted to digital or not

Extra bits in MUX

- if first 2 bits are 0 , we can get exact input
- otherwise
  - we get difference of various combination of inputs

MUX4..0	Single Ended Input	Positive Differential Input	Negative Differential Input	Gain
00000	ADC0	N/A		
00001	ADC1			
00010	ADC2			
00011	ADC3			
00100	ADC4			
00101	ADC5			
00110	ADC6			
00111	ADC7			
01000	N/A	ADC0	ADC0	10x
01001		ADC1	ADC0	10x
01010		ADC0	ADC0	200x
01011		ADC1	ADC0	200x
01100		ADC2	ADC2	10x
01101		ADC3	ADC2	10x
01110		ADC2	ADC2	200x
01111		ADC3	ADC2	200x
10000		ADC0	ADC1	1x
10001		ADC1	ADC1	1x
10010		ADC2	ADC1	1x
10011		ADC3	ADC1	1x
10100		ADC4	ADC1	1x
10101		ADC5	ADC1	1x
10110		ADC6	ADC1	1x
10111		ADC7	ADC1	1x
11000		ADC0	ADC2	1x
11001		ADC1	ADC2	1x
11010		ADC2	ADC2	1x
11011		ADC3	ADC2	1x
11100		ADC4	ADC2	1x

- why do we need difference
  - when we need differnece
  - noise cancellation
    - one has void + noise , other has noise → so , we get only voice when we take difference of input
- internal noise

Why extra 5V in AVCC

can't drive multiple component with a single voltage source. we use diff. power source to diff. component.

Here, ATMEGA32 is designed in such a way to separate digital and analog part as much as possible. So we must give 5V in AVCC