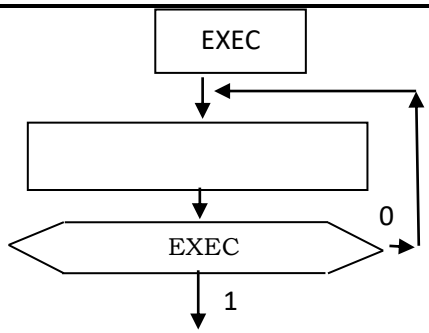
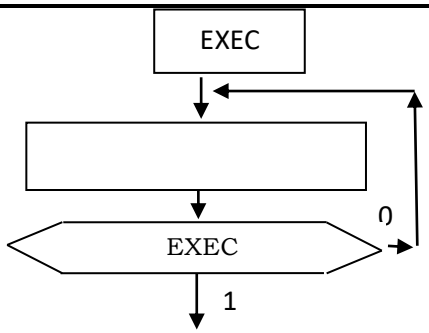
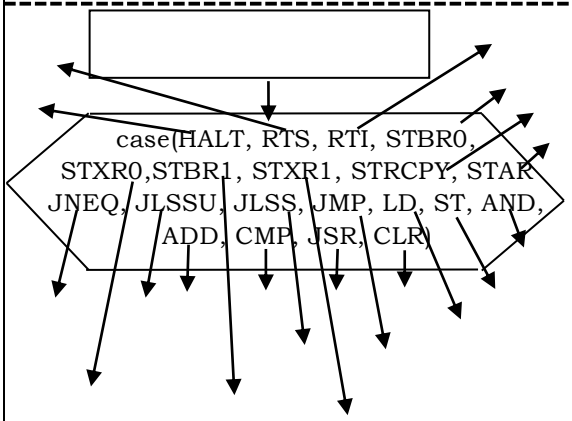
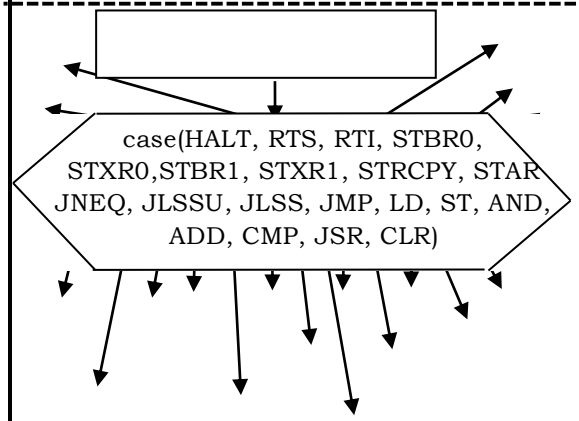
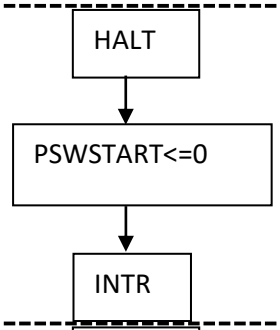
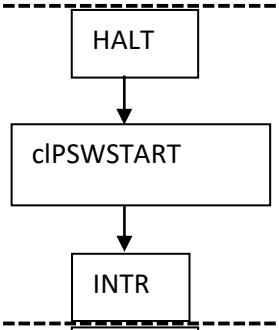
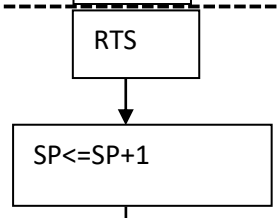
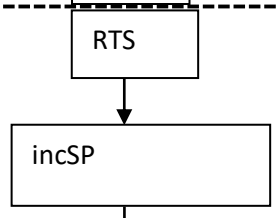
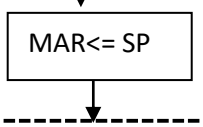
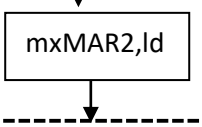
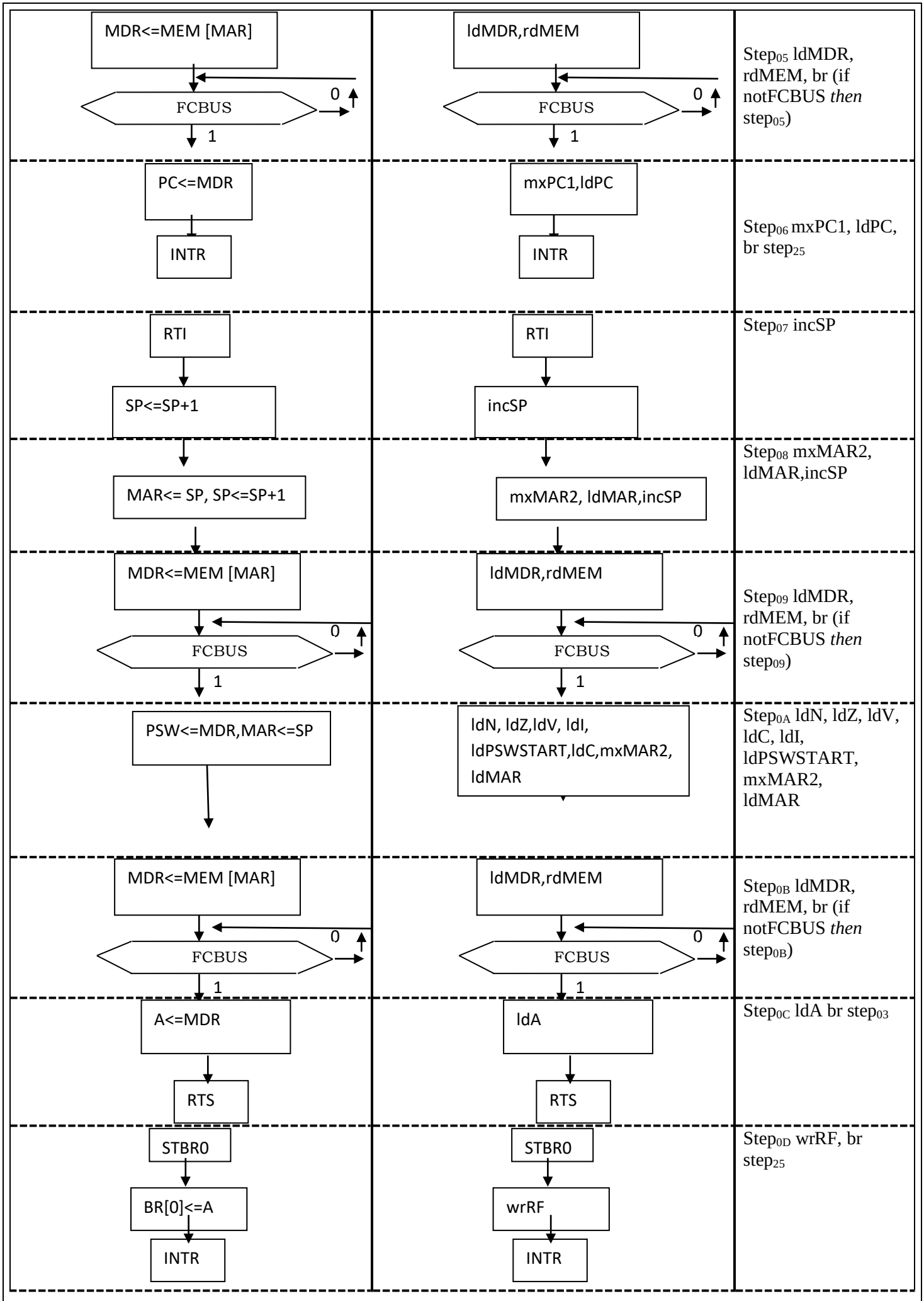
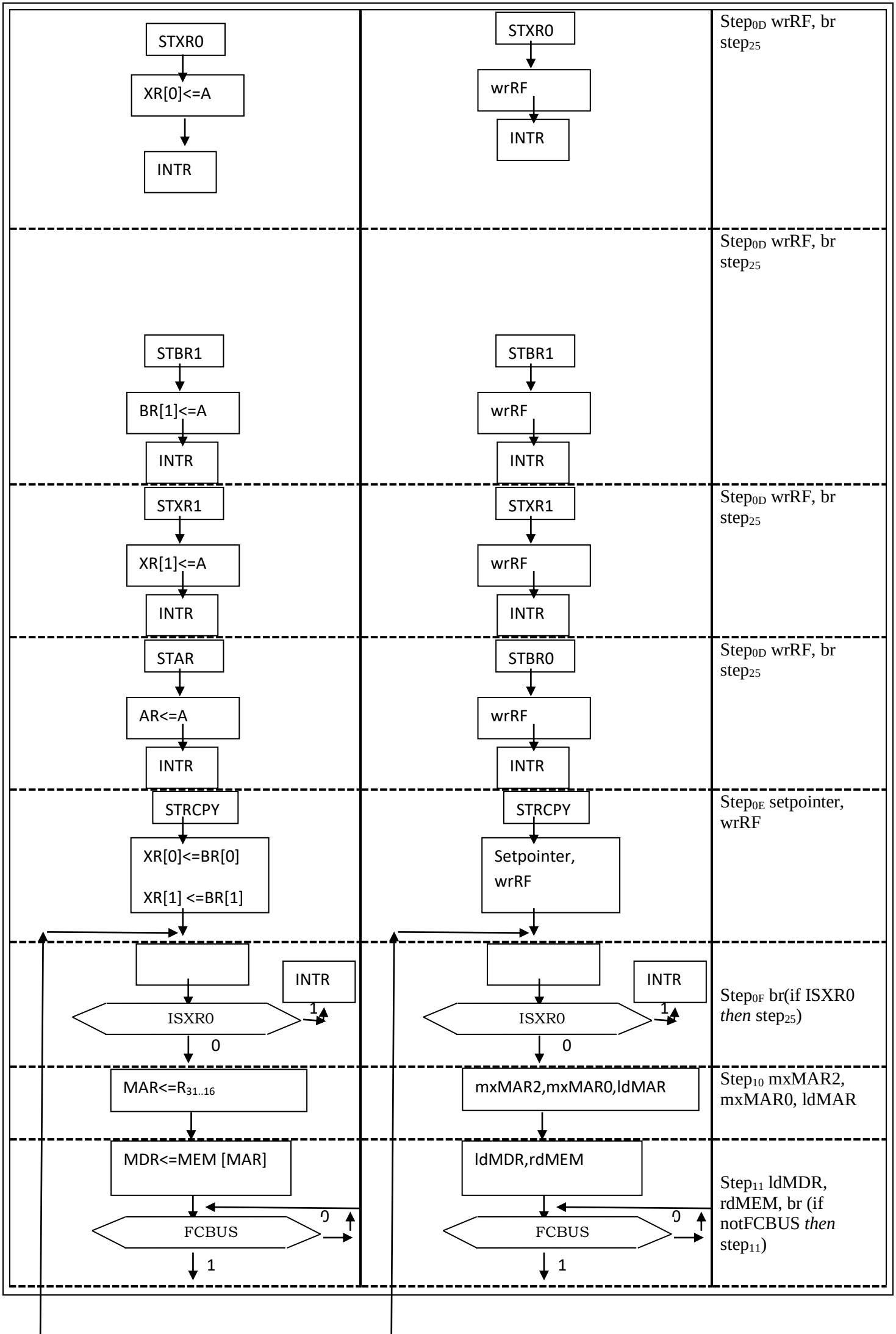
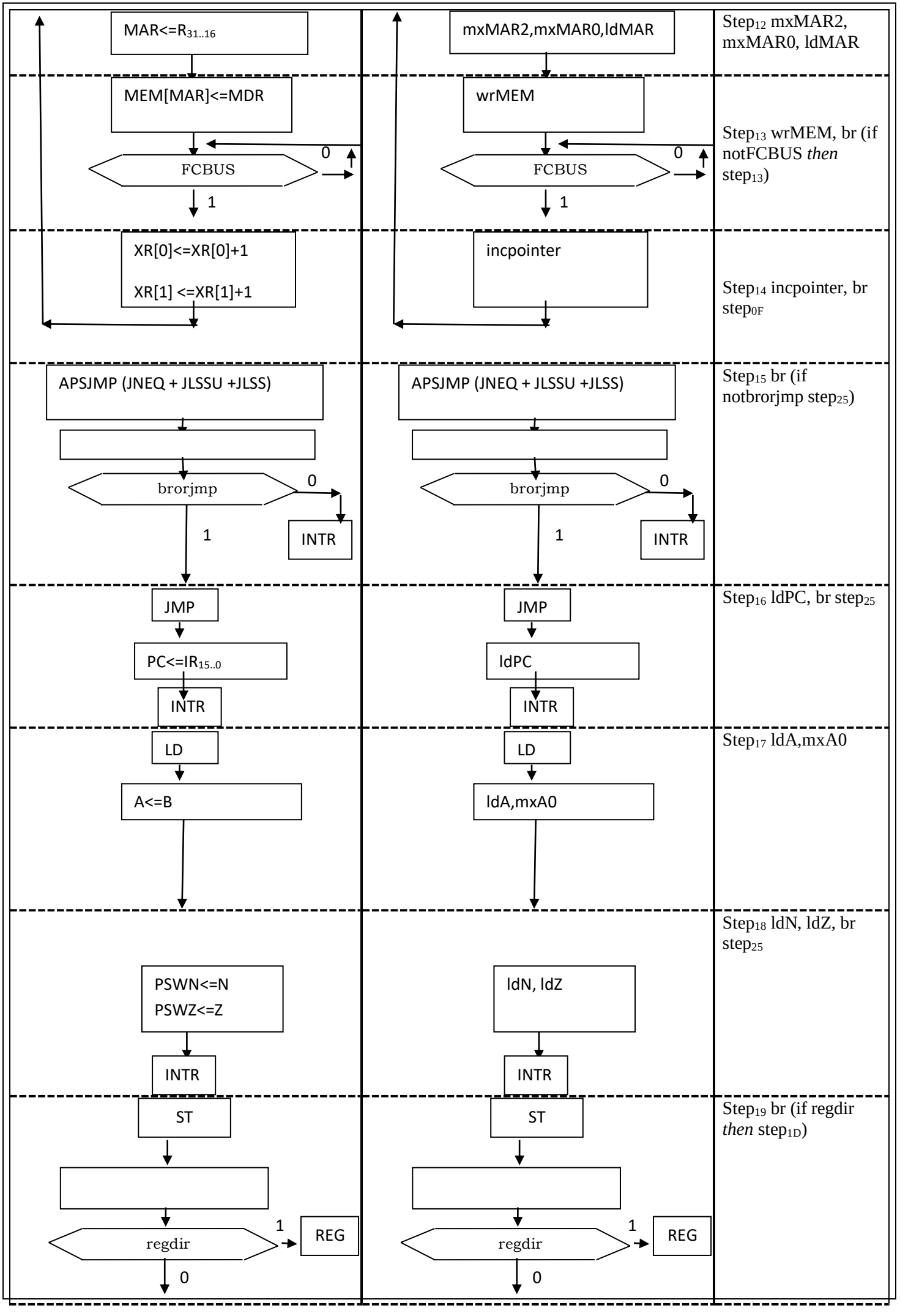
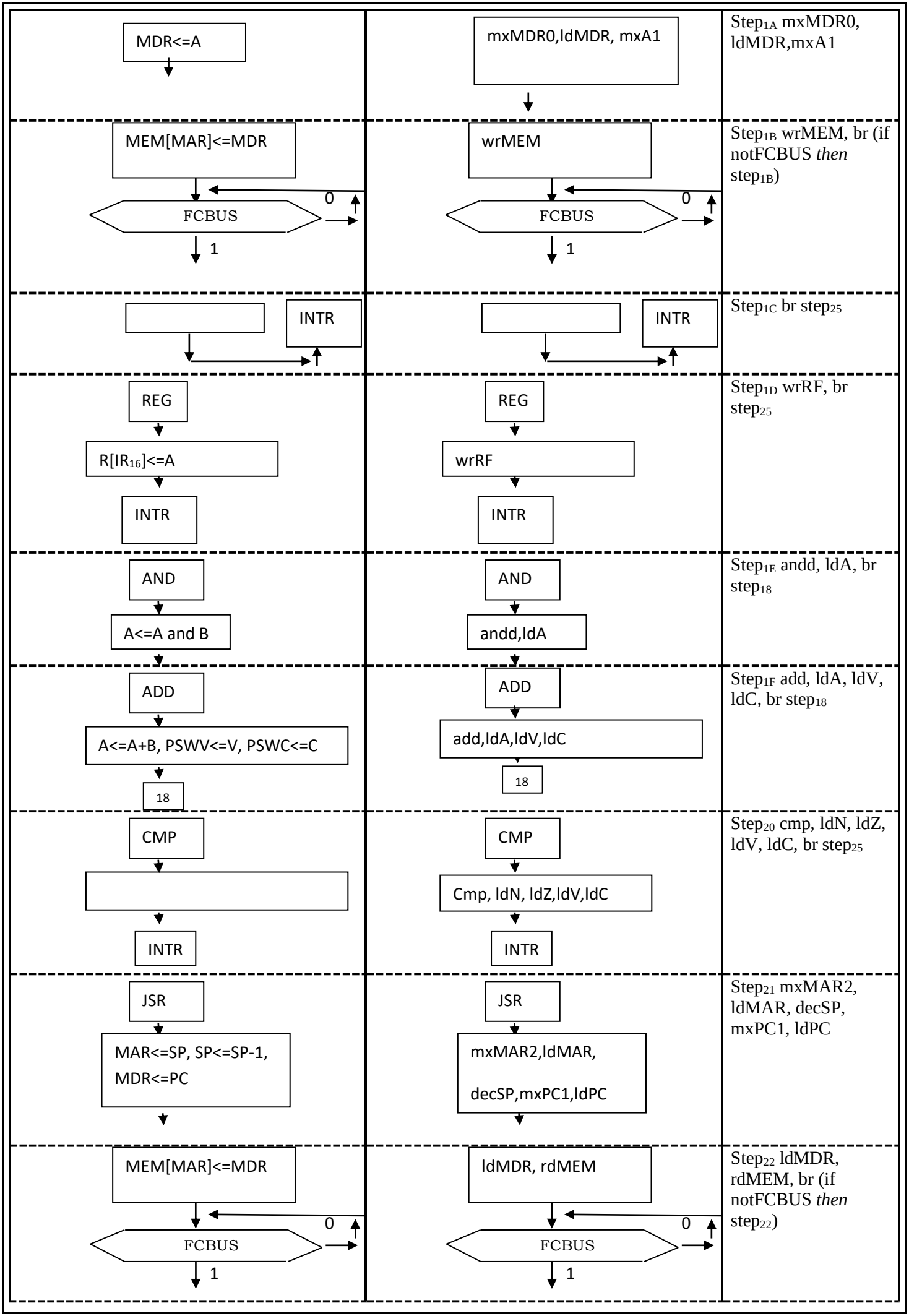
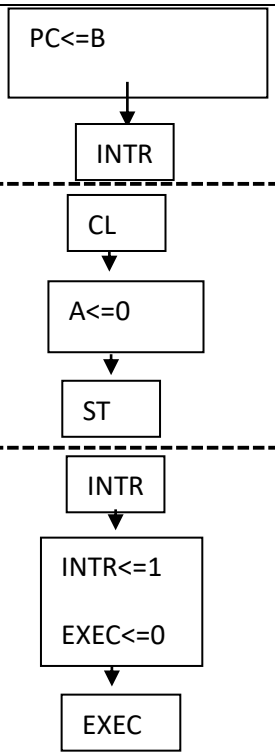
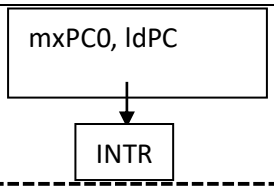
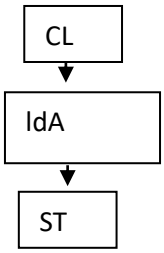
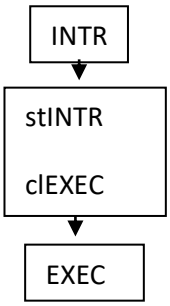
Microoperations flow diagram	Control signals flow diagram	Control signals sequence
		$Step_{00}$ br (if notEXEC *then* $step_{00}$)
		$Step_{01}$ br(case (HALT, RTS, RTI, STBR0, STXR0, STBR1, STXR1,STRCPY, STAR, JNEQ, JLSSU, JLSS, JMP, LD, ST, AND, ADD, CMP, JSR, CLR) *then* (HALT, $step_{02}$), (RTS, $step_{03}$), (RTI, $step_{07}$), (STBR0, $step_{0D}$), (STXR0, $step_{0D}$), (STBR1, $step_{0D}$), (STXR1, $step_{0D}$), (STRCPY, $step_{0E}$), (STAR, $step_{0D}$), (JNEQ, $step_{15}$), (JLSSU, $step_{15}$), (JLSS, $step_{15}$), (JMP, $step_{16}$), (LD, $step_{17}$), (ST, $step_{19}$), (AND, $step_{1E}$), (ADD, $step_{1F}$), (CMP, $step_{20}$), (JSR, $step_{21}$), (CLR, $step_{24}$))
		$Step_{02}$ clPSWSTART, br $step_{25}$
		$Step_{03}$ incSP
		$Step_{04}$ mxMAR2, ldMAR


MDR<=MEM [MAR]
FCBUS
0
1
ldMDR,rdMEM
FCBUS
0
1
Step05 ldMDR, rdMEM, br (if notFCBUS then step05)
PC<=MDR
INTR
mxPC1,ldPC
INTR
Step06 mxPC1, ldPC, br step25
RTI
SP<=SP+1
RTI
incSP
Step07 incSP
MAR<= SP, SP<=SP+1
mxMAR2, ldMAR,incSP
Step08 mxMAR2, ldMAR,incSP
MDR<=MEM [MAR]
FCBUS
0
1
ldMDR,rdMEM
FCBUS
0
1
Step09 ldMDR, rdMEM, br (if notFCBUS then step09)
PSW<=MDR,MAR<=SP
ldN, ldZ,ldV, ldI, ldPSWSTART,ldC,mxMAR2, ldMAR
Step0A ldN, ldZ, ldV, ldC, ldI, ldPSWSTART, mxMAR2, ldMAR
MDR<=MEM [MAR]
FCBUS
0
1
ldMDR,rdMEM
FCBUS
0
1
Step0B ldMDR, rdMEM, br (if notFCBUS then step0B)
A<=MDR
RTS
ldA
RTS
Step0C ldA br step03
STBR0
BR[0]<=A
INTR
STBR0
wrRF
INTR
Step0D wrRF, br step25


STXR0
XR[0]<=A
INTR
STXR0
wrRF
INTR
Step0D wrRF, br step25
STBR1
BR[1]<=A
INTR
STBR1
wrRF
INTR
STXR1
XR[1]<=A
INTR
STXR1
wrRF
INTR
STAR
AR<=A
INTR
STBR0
wrRF
INTR
STRCPY
XR[0]<=BR[0]
XR[1] <=BR[1]
STRCPY
Setpointer,
wrRF
Step0E setpointer, wrRF
INTR
ISXR0
1
0
INTR
ISXR0
1
0
Step0F br(if ISXR0 then step25)
MAR<=R31..16
mxMAR2,mxMAR0,ldMAR
Step10 mxMAR2, mxMAR0, ldMAR
MDR<=MEM [MAR]
ldMDR,rdMEM
FCBUS
0
1
FCBUS
0
1
Step11 ldMDR, rdMEM, br (if notFCBUS then step11)


MAR<=R31..16
mxMAR2,mxMAR0,ldMAR
Step12 mxMAR2, mxMAR0, ldMAR
MEM[MAR]<=MDR
wrMEM
FCBUS
0
1
Step13 wrMEM, br (if notFCBUS then step13)
XR[0]<=XR[0]+1
XR[1] <=XR[1]+1
incpointer
Step14 incpointer, br step0F
APSJMP (JNEQ + JLSSU +JLSS)
brorjmp
INTR
Step15 br (if notbrorjmp step25)
JMP
PC<=IR15..0
ldPC
Step16 ldPC, br step25
LD
A<=B
ldA,mxA0
Step17 ldA,mxA0
PSWN<=N
PSWZ<=Z
ldN, ldZ
Step18 ldN, ldZ, br step25
ST
regdir
REG
Step19 br (if regdir then step1D)


MDR<=A
mxMDR0,ldMDR, mxA1
Step1A mxMDR0, ldMDR,mxA1
MEM[MAR]<=MDR
wrMEM
0
FCBUS
1
Step1B wrMEM, br (if notFCBUS then step1B)
INTR
Step1C br step25
REG
R[IR16]<=A
wrRF
Step1D wrRF, br step25
AND
A<=A and B
andd,ldA
Step1E andd, ldA, br step18
ADD
A<=A+B, PSWV<=V, PSWC<=C
add,ldA,ldV,ldC
18
Step1F add, ldA, ldV, ldC, br step18
CMP
Cmp, ldN, ldZ,ldV,ldC
Step20 cmp, ldN, ldZ, ldV, ldC, br step25
JSR
MAR<=SP, SP<=SP-1, MDR<=PC
mxMAR2,ldMAR, decSP,mxPC1,ldPC
Step21 mxMAR2, ldMAR, decSP, mxPC1, ldPC
ldMDR, rdMEM
Step22 ldMDR, rdMEM, br (if notFCBUS then step22)

		$Step_{23}$ mxPC0, ldPC, br $step_{25}$
		$Step_{24}$ clA, br $step_{19}$
		$Step_{25}$ stINTR, clEXEC, br $step_{00}$