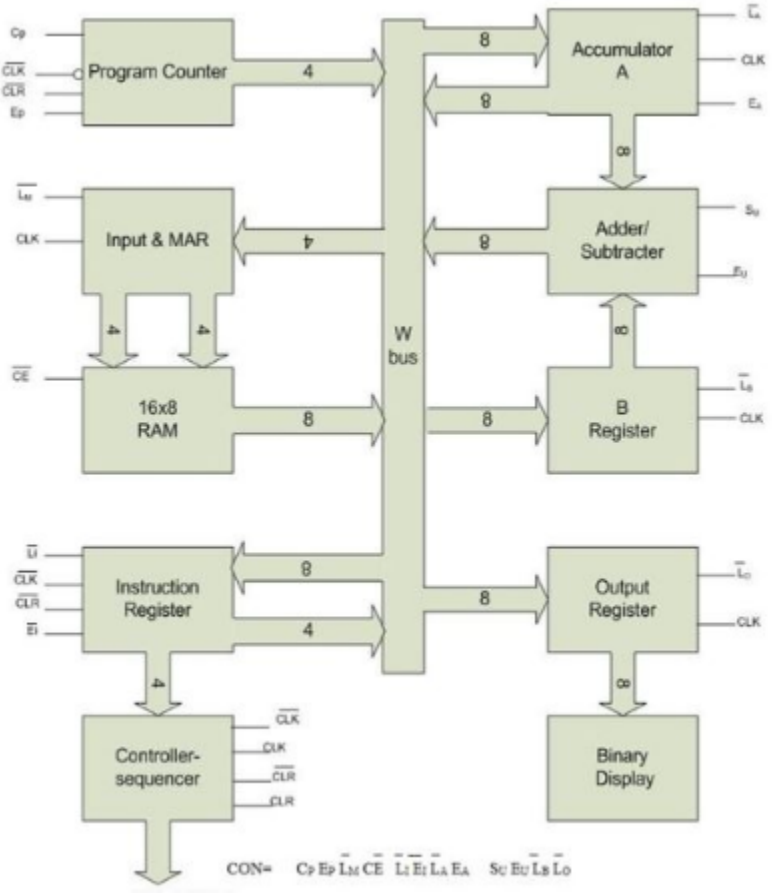
SAP-1 Architecture Assignment

SAP-1 Architecture

SAP is very basic model of microprocessor explained by Albert Paul Malvino. The SAP design contains the basic necessities for a functional Microprocessor. Its primary purpose is to develop a basic understanding of how a microprocessor works, interacts with memory and other parts of the system like input and output. The instruction set is very limited and is simple. SAP is specially designed for the academic purpose and nothing has to do with the commercial use.



SAP-1 use a single 8-bit bus for adder and data transfer and use 16-bytes memory(RAM). In SAP-1 program counter initializes from 00H(0d) to FFH(15d) during program execution.
An architecture is shown in figure. A bus-organized computer. All register outputs to the W bus are three states; this allows offerly transfer of data, all other register outputs are two states; these outputs continuously drive the boxed they are connected to.

Program Counter

SAP-1 count from 0000 to 1111 and it signals the memory address of next instruction to be fetched and executed.

SAP-1 Instruction Set

This means loading step-by-step instructions into the memory before the start of a computer run. Before you can program a computer, however, you must learn its instruction set, the basic operations it can perform. It is shown in following figure.

SAP-1 INSTRUCTION SET		
Mnemonics	**Operation**	**Description**
LDA	ACC ← RAM[MAR]	Load RAM data into accumulator
ADD	ACC ← ACC + B	Add RAM data to accumulator
SUB	ACC ← ACC – B	Subtract RAM data from accumulator
OUT	OUT ← ACC	Load accumulator data into output register
HLT	CLK ← 0	Stop processing

LDA

LDA stands for “Load Accumulator”. A complete LDA instruction includes the hexadecimal address of the data to be loaded.

ADD

Code Assembling in Memory

When the computer run begins , the pc sends address 0000 to the memory. The pc is then incremented to get 0001. After the first instruction is fetched and executed , the pc sends address 0001 to the memory and again the PC is incremented. After the second instruction is fetched and executed , the PC ends address 0010 to the memory. In this way the PC keeping track of the next instruction to be executed. SAP usese only 16 bytes of memory, it is because it uses four digit address and four digit address have sixteen combinations from 0000 to 1111.

Controller Sequencer

The 12 bits coming out of the Controller Sequencer from a word that control the rest of the computer. Before each operation a Clear (CLR) signal resets the computer. Before each operation a Clear(CLR) signal resets the computer.

The 12 wires carrying the control word are called the Control Bus. The control word has the format:

CON = Cp Ep Lm CE L1 E1 La Ea Su Eu Lb Lo

This word determine how the registers will react to the next positive clock(CLK) edge. For instance a high and a low means that the contents of Program Counter are latched into MAR on the next positive click edge. As another example , a low and a low mean that the addressed RAM word will be transferred to the accumulator on the next positive clock edge.