Electronic Devices and Circuits I [ELECENG 2EI4]
Project #2B

Instructor: Dr. Haddara

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As a future member of the engineering profession, the student is responsible for performing the required work in an honest manner, without plagiarism and cheating. Submitting this work with my name and student number is a statement and understanding that this work is my own and adheres to the Academic Integrity Policy of McMaster University and the Code of Conduct of the Professional Engineers of Ontario. Submitted by **[Zayeed Ghori, ghoriz1, 400398943]**

Properties of an Ideal Switch

1. There is no limit to the forward or reverse current when the switch is in the ON state.
2. No limit to the amount of voltage across the switch when in OFF state.
3. No voltage drop when in ON-state.
4. Infinite OFF-state resistance.
5. Infinitely fast switching times (instant ON to OFF or vice-versa).
6. Zero power is lost.
7. Zero inductance when ON.
8. Zero capacitance when ON.
9. Zero resistance when in ON.

Non-Idealities

Qualitative Non-Idealities

1. There is some power loss when the switch is ON. The voltage that goes in is not the exactly the same as the voltage out.
2. The switch takes time to turn on and off.

Quantitative Non-Idealities of a Real Switch

1. Limited current when ON (Max I = max power / R^2) and limited voltage drop (max voltage depends on gap between contacts and dielectric breakdown properties of insulator) when OFF.
2. Finite time to switch states (t > 0)
3. R > 0, V drop > 0.
4. Power losses = V drop * I

Test Plan

i. **Values that you will set for V control, V supply and and v1.**
Vcontrol = Pulse (5V to 0V) to determine if switch is closed when pulse is LOW and open when HIGH, V supply = 5V, V1 = 5V for both switches.

ii. **Values that you will measure.**
- **a.** Switch 1: V2, 5V when switch is closed and 0V when the switch is open.
- **b.** Switch 2: Va, Vb (Should be 5V when active and 0V when inactive).

iii. **Values, if any, that you will calculate based on the measurement.**
Vdrop, the voltage loss between V1 input and outputs (V2, Va and Vb) when ON, and then efficiency.
Leakage current when OFF.

Switch 1

i. **A circuit schematic of your design.**

Figure 1: Circuit Schematic of Design for Switch 1

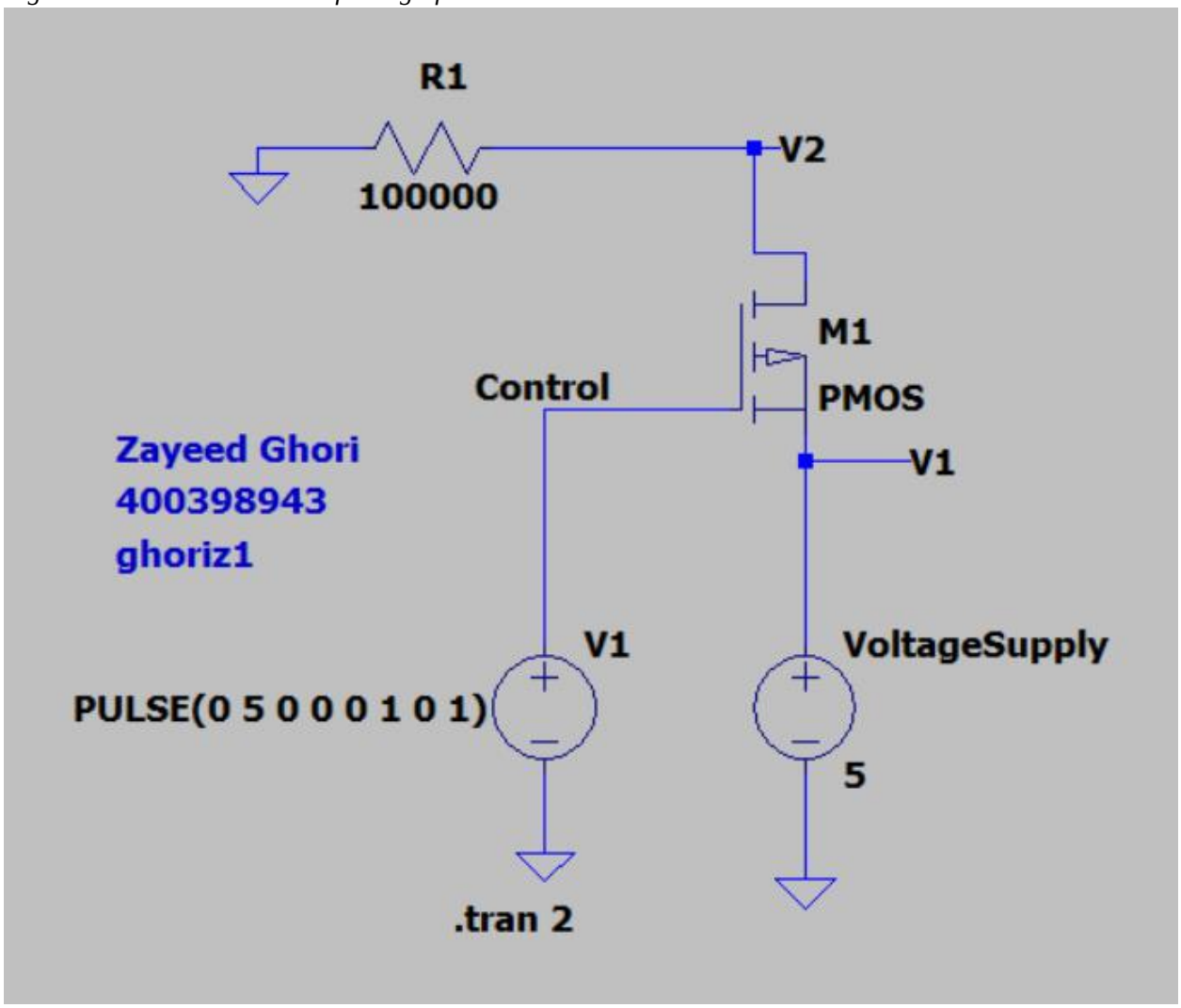


Figure 2: LTSpice Simulation of V1 and V2

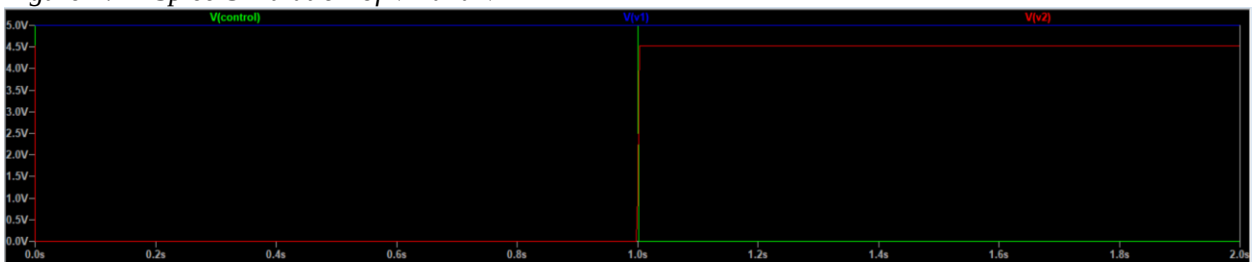
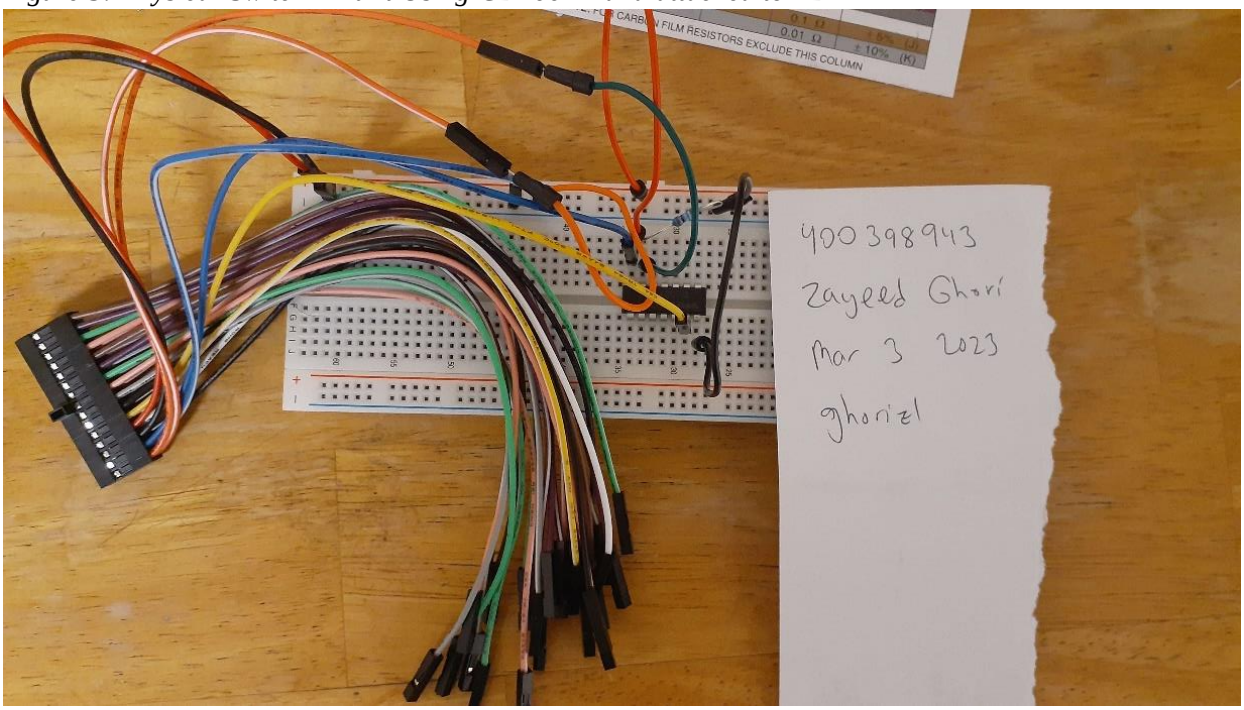


Figure 3: Physical Switch 1 Built Using CD4007B and attached to AD2



ii. Measurements performed according to the test plan.

Figure 4: AD2 Oscilloscope Switch 1 Measurement – V1 = Yellow, V2 = Blue

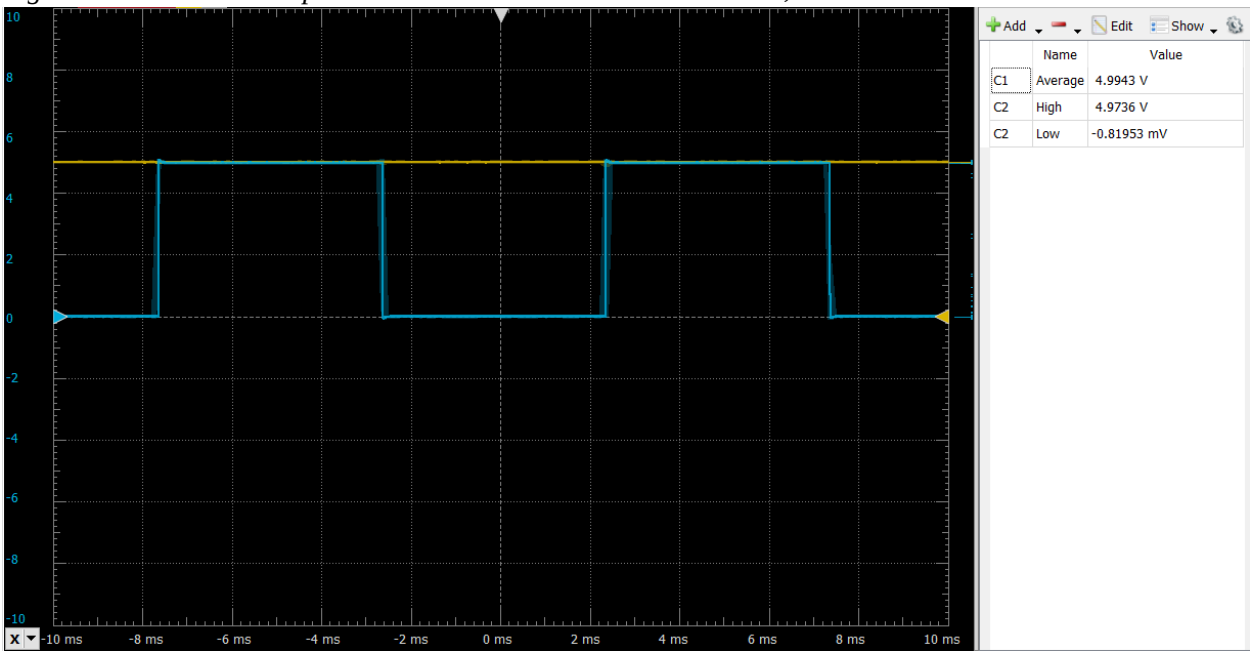
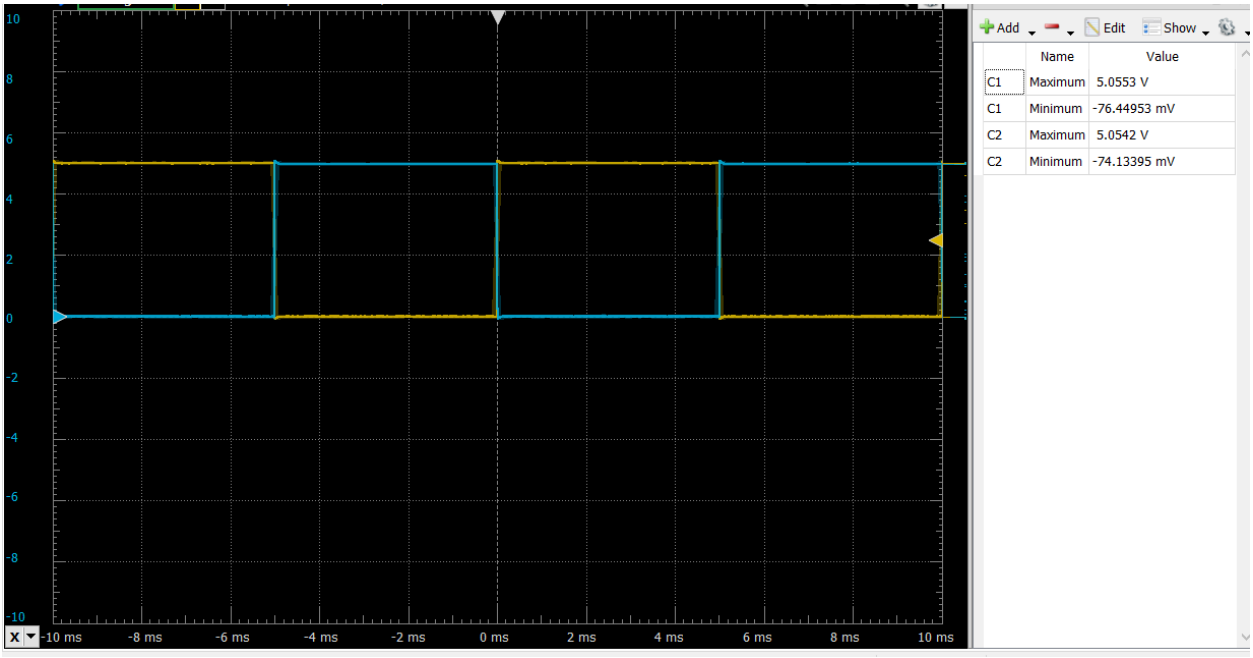


Figure 5: AD2 Oscilloscope Switch 1 Measurement – Vcontrol = Yellow, V2 = Blue



Measured Values:

- V2 is HIGH when Vcontrol is LOW.
- V2 when HIGH (avg) = 4.9736 V
- V2 when LOW (avg) = -0.81953 mV
- V1 (avg) = 4.9943 V

Calculated Values:

Vdrop = V1 – V2 = 4.9943 V – 4.9736 V = 0.0207 V

% eff ON = 100% - 0.0207 V / 4.9943 V = 99.6%

Leakage current when OFF = -0.081953 V / 100kOhms = -0.81953 uA

iii. Theoretical explanation for the results obtained and comparison of the quantitative results with theory.

When Vcontrol is HIGH (~5V), V2 is LOW (~0V) and when Vcontrol is LOW, V2 is HIGH, so the switch is closing and opening when it should be. When comparing V2 to the theoretical and simulation values, theoretically V2 should be 5V when HIGH and 0V when LOW, V2 in the simulation is just above 4.5V when HIGH and 0V when LOW, and V2 experimental results show that it is 4.9736V when HIGH and -0.082V when LOW.

By just observing the V2 HIGH value between each result, the experiment proved to be more closer to the theoretical value (5V) than the simulation, probably due to the overestimation of current flowing from the drain of the PMOS to ground through the resistor.

The V2 LOW value on the other hand was below 0V in the experiment, this could be due to error within the AD2 or interference.

The Voltage Loss (ie. Vdrop) across the switch was higher in the simulation (~0.5V) compared to the experiment (0.0207V). This would also be due to the overestimation of current flowing through the resistor when the switch is closed. Also in the experiment V1 was 4.9943V, slightly lower than 5V in the first place, so the difference was not as massive. This was also due to AD2 error, excess resistance within the circuit's wires, etc.

iv. Design tradeoffs. What tradeoffs did you make in your design for performance, complexity, and cost?

A PMOS transistor was chosen as the component for the switch to be based around, mainly due to the NMOS potentially requiring an additional resistor at the gate to ensure noise will not accidentally turn the MOSFET ON.

The 100k resistor was used due to that being the highest resistor with a number that was easy to work with in our 2EI4 kit. A higher resistor would have worked better in theory, to make sure as little current as possible was directed to ground when the switch was close, but the 100k resistor was high enough to achieve a good efficiency which being available and lowering the complexity.

Switch 2

i. A circuit schematic of your design.

Figure 6: Circuit Schematic of Design for Switch 2

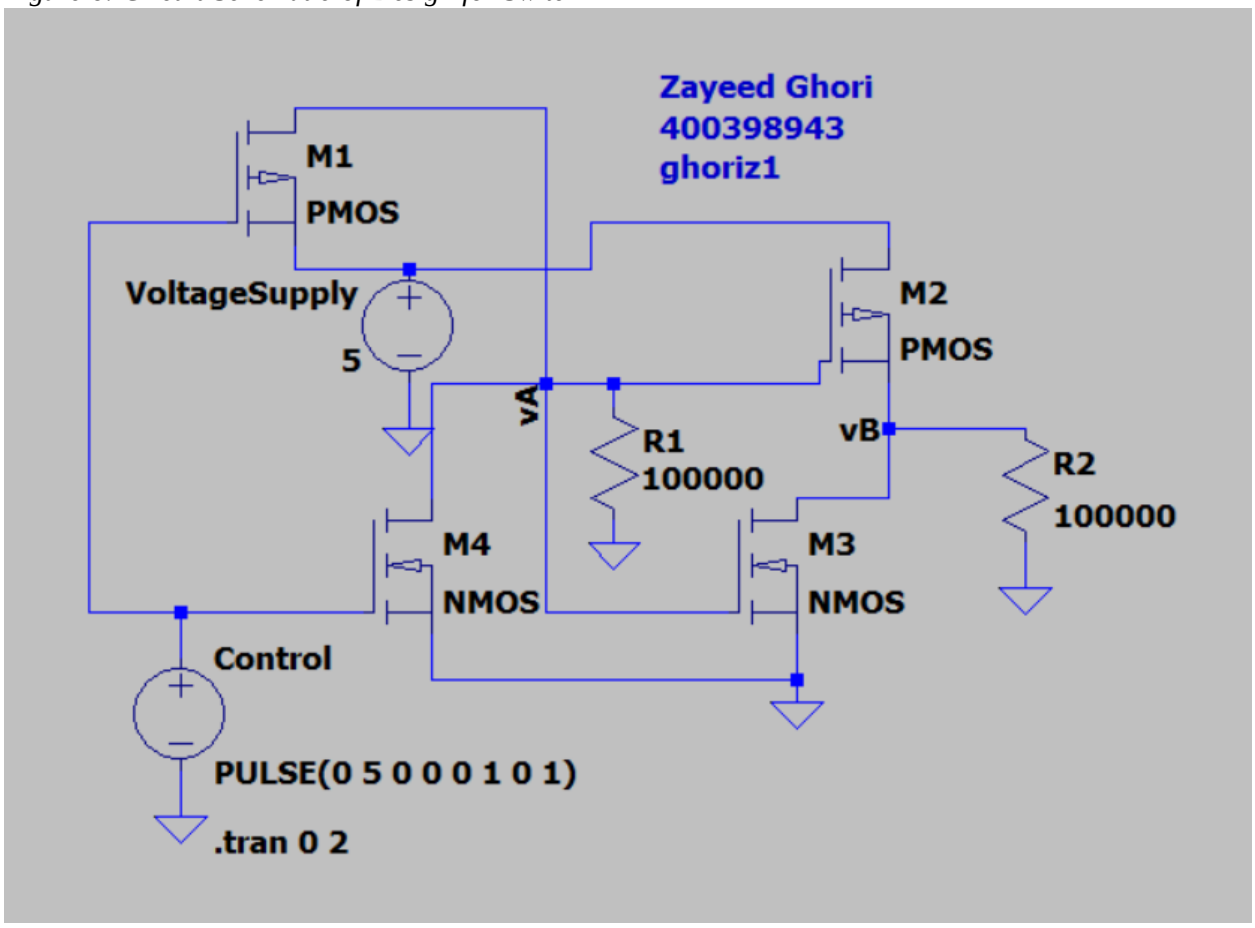


Figure 7: LTSpice Simulation of Vcontrol (Green), V1 (Turquiose), Vb (Red), Va (Blue)

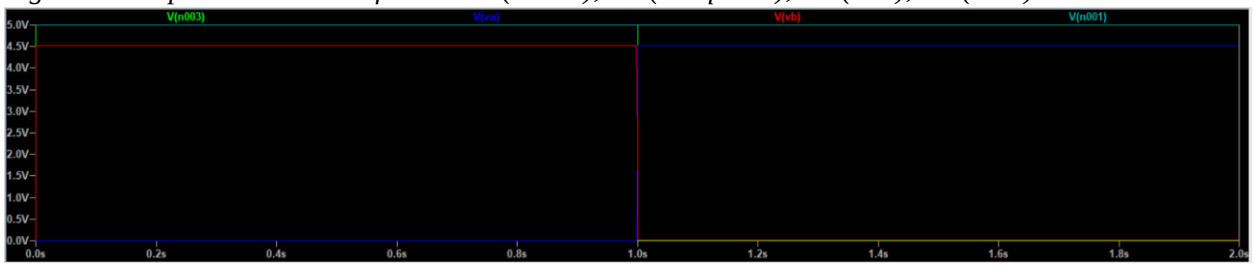
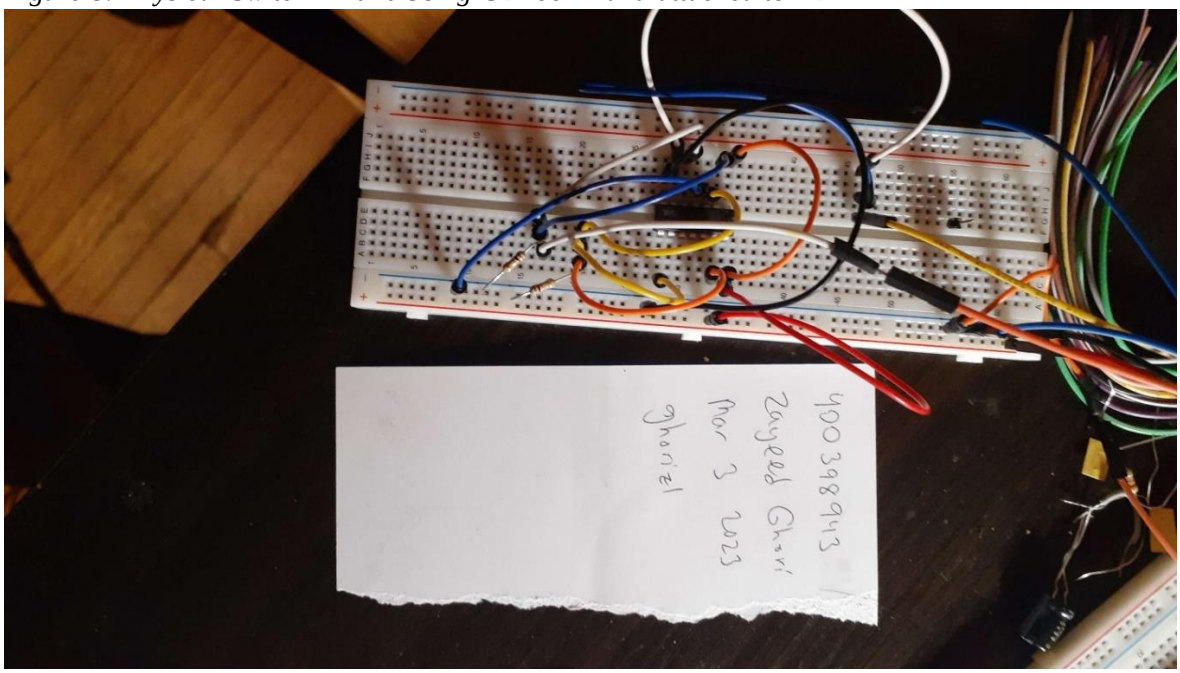


Figure 8: Physical Switch 2 Built Using CD4007B and attached to AD2



ii. Measurements performed according to the test plan.

Figure 9: AD2 Oscilloscope Switch 2 Measurement – Va = Blue, Vcontrol = Yellow

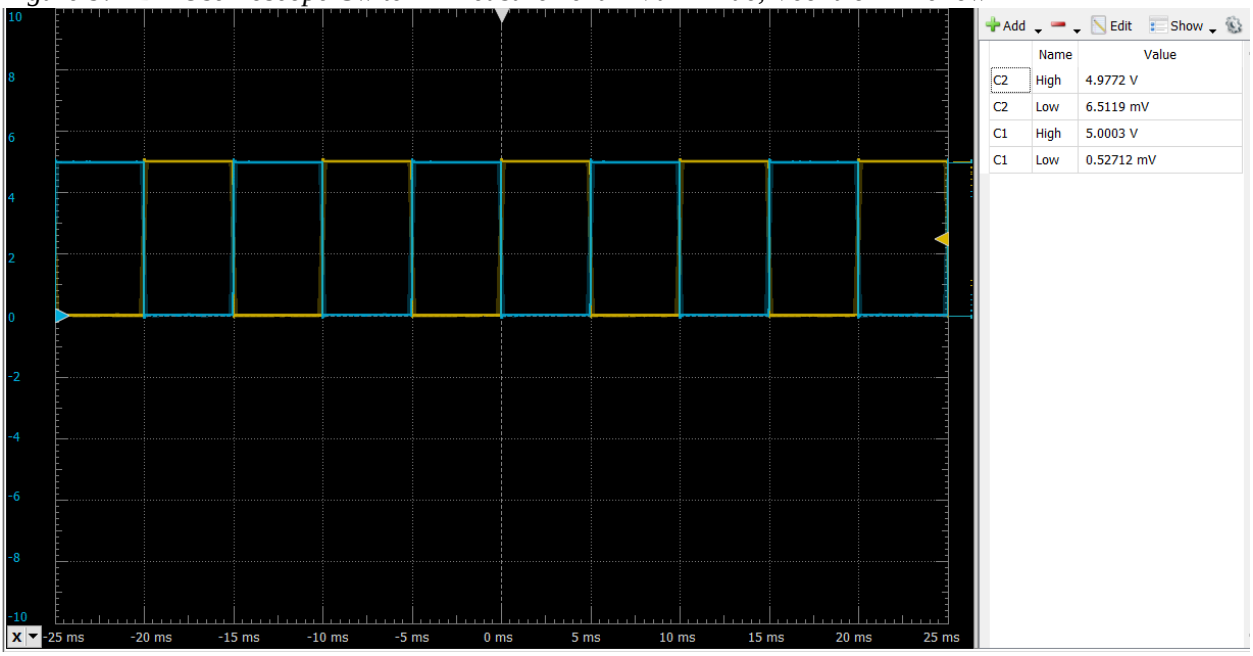


Figure 10: AD2 Oscilloscope Switch 2 Measurement – Vb = Blue, Vcontrol = Yellow

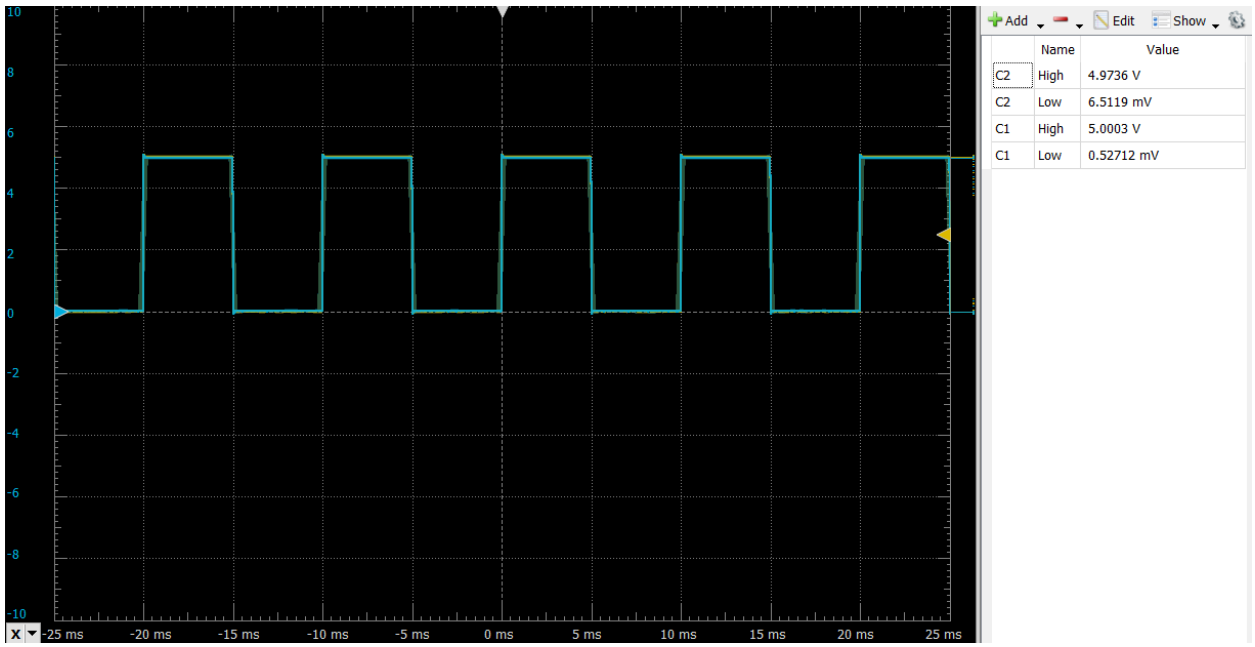


Figure 11: AD2 Oscilloscope Switch 2 Measurement – V1 = Yellow, Va = Blue

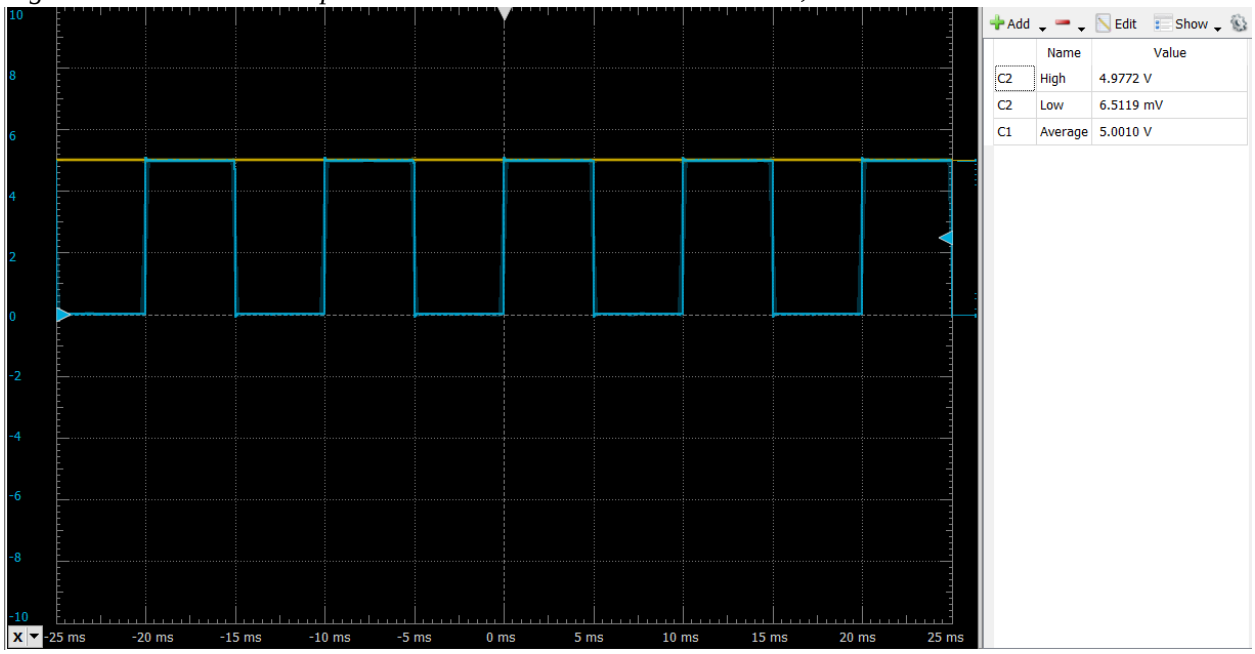
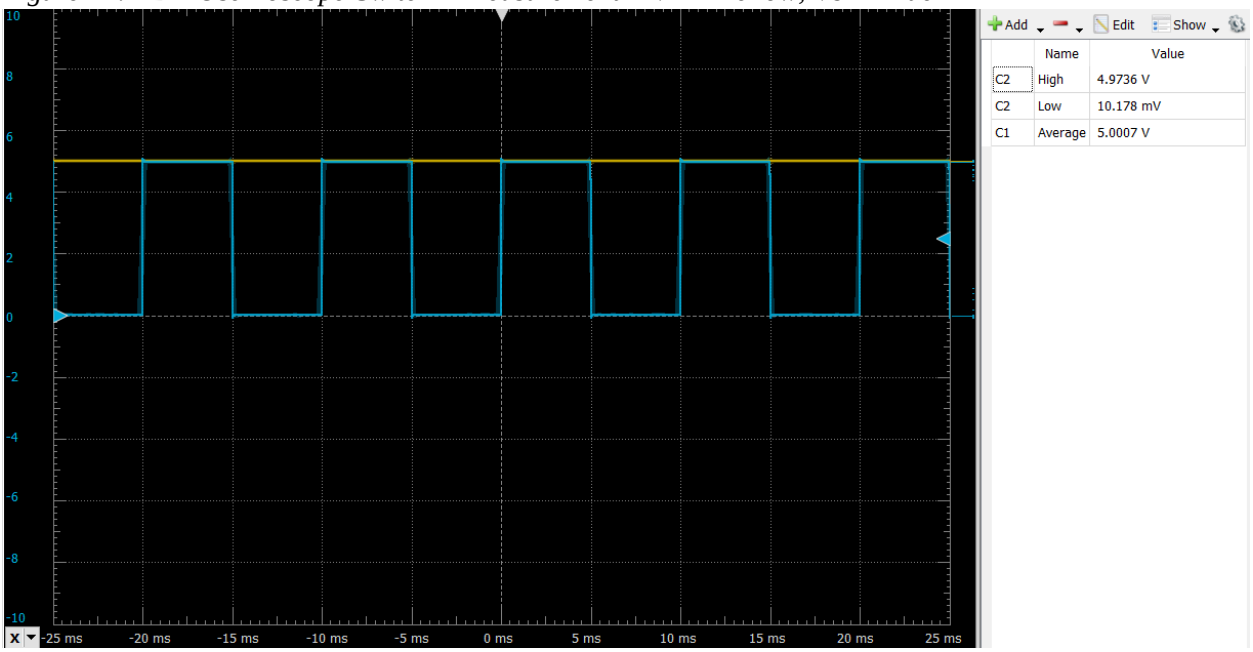


Figure 12: AD2 Oscilloscope Switch 1 Measurement – V1 = Yellow, Vb = Blue



Measured Values:

- Va is HIGH when Vcontrol is LOW
- Vb is HIGH when Vcontrol is HIGH
- Va when HIGH (avg) = 4.9772 V
- Va when LOW (avg) = 6.5119 mV
- Vb when HIGH (avg) = 4.9736 V
- Vb when LOW (avg) = 10.178 mV
- V1 (avg) = 5.001 V

Calculated Values:

- Values for Va
  - Vdrop = V1 – Va = 5.001 V – 4.9772 V = 0.0274 V
  - % eff ON = 100% - 0.0274 V / 5.001 V = 99.5%
  - Leakage current when OFF = 6.5119 mV / 100kOhms = 65.119 nA
- Values for Vb
  - Vdrop = V1 – Va = 5.001 V – 4.9736 V = 0.0238 V
  - % eff ON = 100% - 0.0238 V / 5.001 V = 99.5%
  - Leakage current when OFF = 6.5119 mV / 100kOhms = .10178 uA

iii. Theoretical explanation for the results obtained and comparison of the quantitative results with theory.

When Vcontrol is HIGH (~5V), Vb is HIGH (~5V) and when Vcontrol is LOW, Va is HIGH, so the switch is switching outputs when it should be. When comparing Va and Vb to the theoretical and simulation values; theoretically Va and Vb should be 5V when HIGH and 0V when LOW; Va and Vb in the simulation are just above 4.5V when HIGH and 0V when LOW; Va is 4.9772V when HIGH and 6.5119 mV when LOW, Vb is 4.9736 V when HIGH and 10.178 mV when LOW experimentally.

By just observing the Va and Vb's HIGH values between results, the experiment proved to be closer to the theoretical value (5V) than the simulation, probably due to the overestimation of current flowing from the drain of the PMOS to ground through the resistors.

The Va and Vb LOW value on the other hand was above 0V in the experiment, this could be due to current leaking through the resistors or error within the AD2, or interference.

The Voltage Loss (ie. Vdrop) across the switch was higher in the simulation (~0.5V) compared to the experiment (0.0274V and 0.0238 for Va and Vb respectively). This would also be due to the overestimation of current flowing through the resistor when the switch is closed.

iv. Design tradeoffs. What tradeoffs did you make in your design for performance, complexity, and cost?

Both PMOS and NMOS transistors were used to simplify the design and make sure that the switch would switch between two outputs. Although PMOS or NMOS MOSFETs could have been used exclusively, this would not allow the gates to be connected together to allow for a simpler design.

The 100k resistors were used due to that being the highest resistor with a number that was easy to work with in our 2EI4 kit. A higher resistor value would have worked better in theory, to make sure as little current as possible was directed to ground when the switch was close, but the 100k resistor was high enough to achieve a good efficiency which being available and lowering the complexity.