

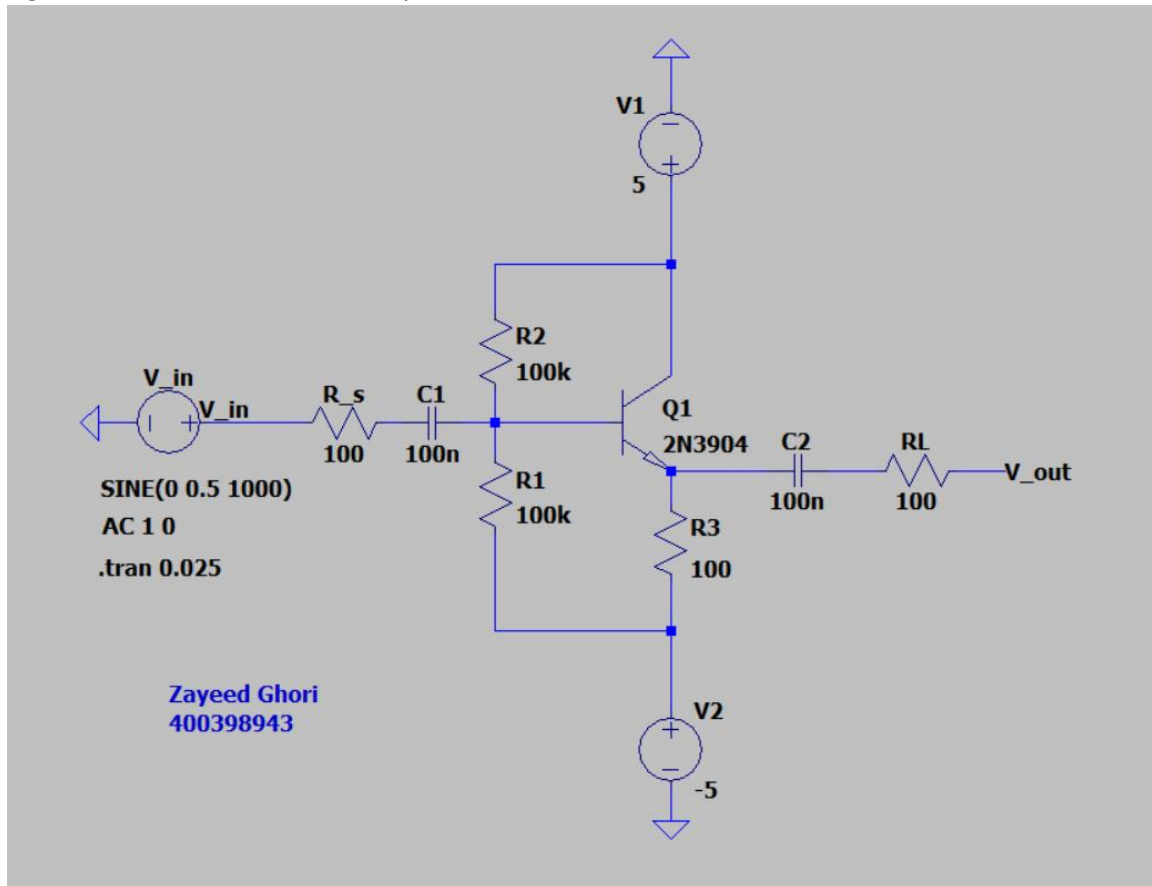
# Electronic Devices and Circuits I [ELECENG 2EI4] Project #3

Instructor: Dr. Haddara

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As a future member of the engineering profession, the student is responsible for performing the required work in an honest manner, without plagiarism and cheating. Submitting this work with my name and student number is a statement and understanding that this work is my own and adheres to the Academic Integrity Policy of McMaster University and the Code of Conduct of the Professional Engineers of Ontario. Submitted by **[Zayeed Ghori, ghoriz1, 400398943]**

2. Figure 1: Circuit Schematic on LTSpice

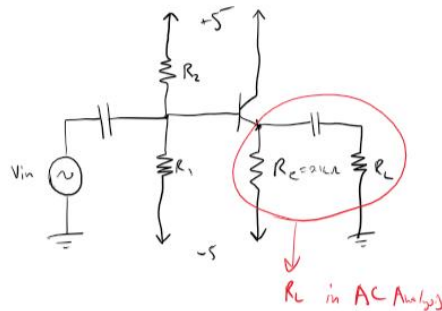


- An NPN BJT transistor was used due to its ability to route current from the base to the emitter. This can amplify low-level signals to higher amplitudes with less distortion. The need for a high gain means that a higher  $g_m$  value is needed, so a BJT is used.
- A Common Collector (CC) topology is used for this amplifier due to the low input and output impedance of this topology that can help minimize attenuation. For this project the input source impedance of the source is low, so a low impedance topology helps match that. This project also had a low required resistance (100 ohms), so a low output impedance can drive a higher load with lower attenuation.

c. Figure 1: Calculations

$$|V_{in}| = (0.2)(u)(1 + g_m R_L) \quad u = 5mV_{RST}$$

$$A \leq 0.9 \quad |V_{in}| = 0.5$$



BJT chosen: required  $g_m$  is high  
CC

$$|0.2 V_T (1 + g_m R_L)| \geq V_i$$

$$(0.2)(25 \times 10^{-3})(1 + g_m(100)) \geq 0.5$$

$$1 + g_m(100) \geq 100$$

$$100 g_m \geq 99$$

$$g_m \geq .995$$

$$g_m \geq 990ms$$

$$A_v \geq 0.9$$

$$\frac{g_m R_L}{1 + g_m R_L} \cdot \frac{R_{in}}{R_{in} + R_s} = A_v$$

$$\frac{(0.99)(100)}{1 + (0.99)(100)} \cdot \frac{R_{in}}{R_{in} + 100} \geq 0.9$$

$$\frac{0.9}{0.99} R_{in} + \frac{0.09}{0.99} \leq R_{in}$$

$$1k\Omega \leq R_{in}$$

$$\text{Choose } R_1 \& R_2 = 100k\Omega$$

$$R_{in}' = \frac{100k\Omega}{g_m} (1 + g_m R_L)$$

$$= \frac{100}{0.99} (1 + 0.99(100))$$

$$R_{in}' = 10.1k\Omega$$

$$R_{in} = R_1 \parallel R_2 \parallel R_{in}'$$

$$= 100k\Omega \parallel 100k\Omega \parallel 10.1k\Omega$$

$$R_{in} = 8402.66\Omega$$

$$R_{in} = 8.4k\Omega$$

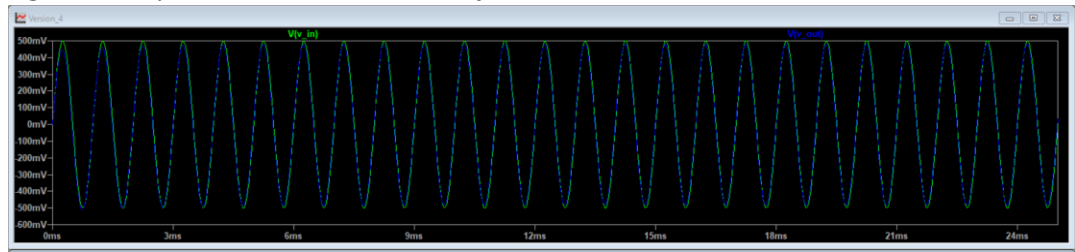
$$\therefore R_{in} > 1k\Omega$$

passive circuit

3.

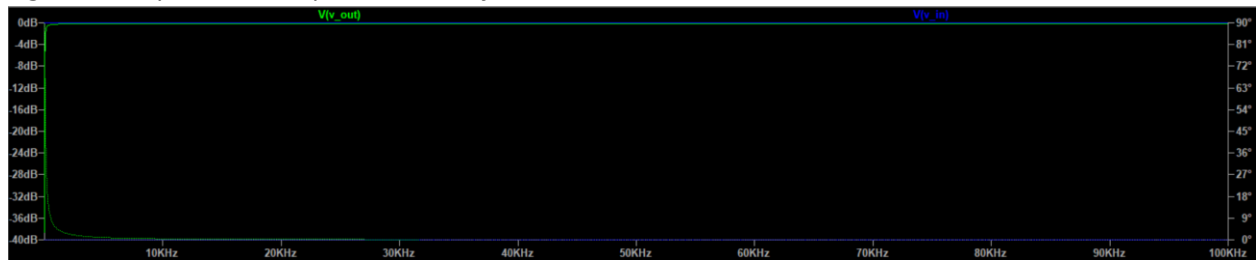
- a. The 2N3904 transistor provided in the 2EI4 component kit was conveniently modeled in LTSpice already and was simply taken and used for this design as shown in Figure 1. It was also the only NPN BJT available in the 2EI4 component kit.

- b. *Figure 2: LTSpice Transient Simulation of Vin vs. Vout*



Because the frequency of the output is 1kHz, a transient analysis went through 25 cycles the whole simulation taking 25ms.

*Figure 3: LTSpice AC Sweep Simulation of Vin vs. Vout*



The AC sweep ran 1000 samples from 1Hz to 100kHz in a linear sweep. The attenuation of Vout was

- c.  $A_v = V_{out} / V_{in} = (\text{Output peak amplitude}) / (\text{Input peak amplitude})$   
 $= (480 \text{ mV}) / (500 \text{ mV})$   
 $A_v = 0.960$

Since  $A_v > 0.9$ , it is a valid result.

- d. Another performance metric could be the input resistance:

$$R_{in} = (\text{Input Voltage}) / (\text{Input Current})$$

$$= (0.5 \text{ V}) / (26.11 \text{ uA}) = 19149 \text{ Ohms}$$

4. *Figure 4: Physical Circuit*

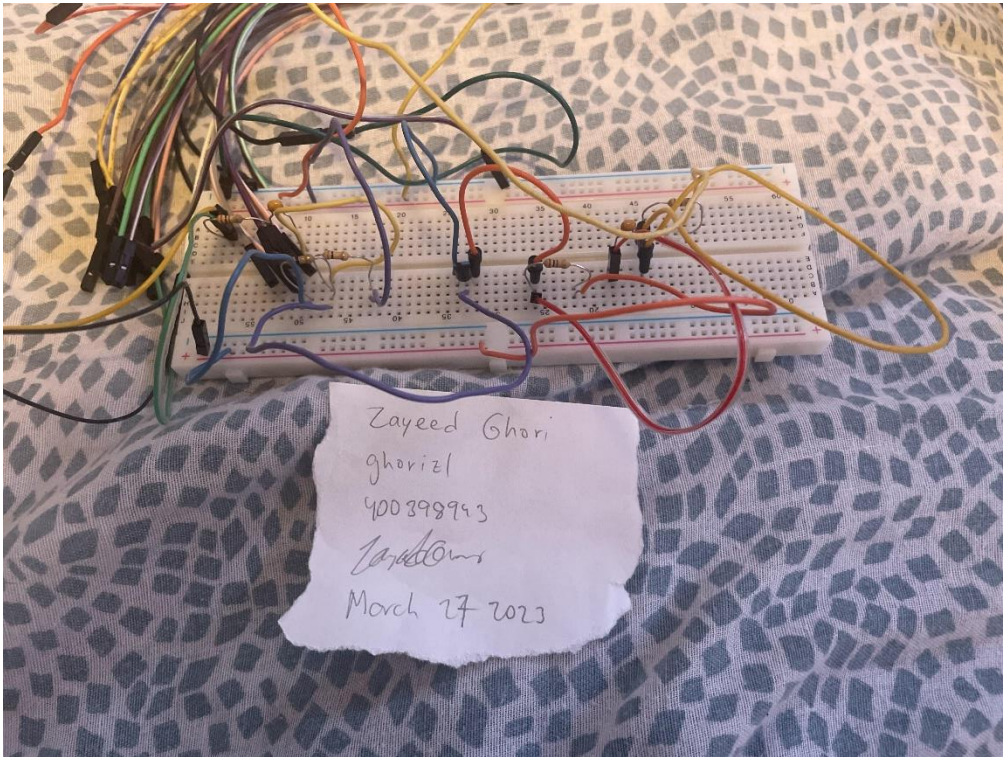
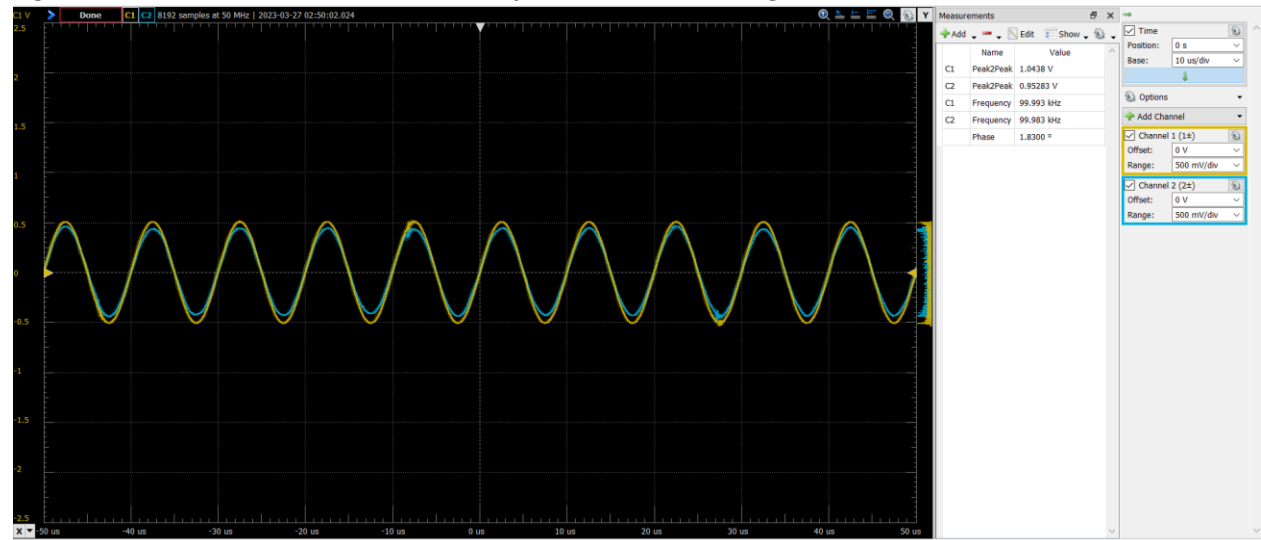


Figure 4 is the physical circuit, the top rail was +5V and the bottom was -5V from the AD2 V+ and V- respectively. The Voltage source is on the top left, from yellow W1 wire from the AD2 connecting to the 100 Ohm resistor which is then connected to a 100nF capacitor in series. The other end of the capacitor is connected to the middle node of two 100k resistors in series on the bottom half of the breadboard using a yellow wire. The left 100k resistor is connected to -5V and the right one is connected to +5V. The middle node is then connected to the base of the NPN BJT using the purple wire. The collector (on the left side) of the BJT is connected to +5V and the emitter (on the right side) is connected to another 100k and then to -5V using the orange wire. The emitter of the BJT is also connected using another orange wire to 100nF capacitor which a 100 Ohm resistor is in series with it to ground.

5.

a. *Figure 5: Vin (Yellow) vs. Vout (Blue) Waveforms Measured using AD2*



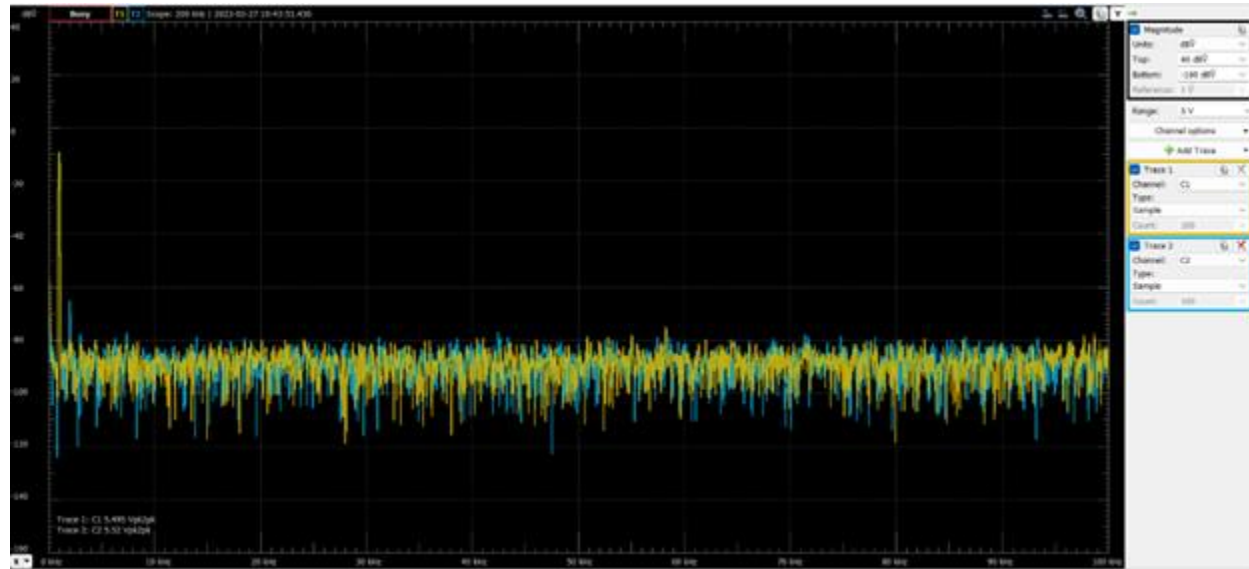
The physical circuit was measured using the oscilloscope channels using the AD2. The sine wave indicates that at different voltage levels, the gain is constant, pp voltages indicated the gain, the frequencies of both were the same meaning that there was no compression or stretch of the original waveform, and the ~1 deg phase difference shows that the delay was minimal.

b. The gain of the circuit is:

$$\begin{aligned}
 A_v &= V_{out} / V_{in} \\
 &= V_{outpp} / V_{inpp} \\
 &= (0.95283 \text{ V}) / (1.0438 \text{ V}) \\
 A_v &= 0.9129
 \end{aligned}$$

$A_v > 0.9$ , therefore the result is still valid. The simulated value shows a larger gain, but due to interference of the wires around my desk, the waveform did show to be a little unstable and the gain might not be as high as it should.

c. *Figure 6: Spectrum Analysis of Vin (Yellow) vs. Vout (Blue) from 0 to 100kHz*



The Vout seemed to stay very close to the Vin dB values throughout the test. This indicates that no new frequencies are being added with the amplifier design, demonstrating linearity in conjunction with Figure 5, showing that at different frequencies and voltages, the amplified waveform is very similar to the original in frequency and phase.