Elec Eng 2EI5
Design Project #4

Problem Statement
Design and build a MOSFET based XOR gate.

Report Requirements
This project does not have a simulation component. Submit a report according to the specifications below.

1. Cover page.
2. Page 1:
    a. (10 pts) Circuit schematic. This should be based on the design methodology studied in class for transistor level logic gates.
    b. (10 pts) Ideal sizing. Explain the ideal ratio between PMOS and NMOS sizes for the design.
    c. (10 pts) Explain whether you can implement the ideal sizing in your hardware design. If not, explain why not, and qualitatively explain the impact on circuit performance.
3. Page 2:
    a. (10 pts) Functional testing. Use the digital IO pins on the AD2 to demonstrate that the circuit implements the XOR function.
    b. (10 pts) Static level testing. Set one of the inputs to logic-1 (+5V). Set the 2nd input as a square wave between 0 and 5V. Measure the output on the oscilloscope. Determine V_H and V_L. Switch the two inputs and determine whether VH and VL change.
    c. (10 pts) Set one of the inputs to logic-1 (+5V). Set the 2nd input as a square wave with 2.5V offset. Gradually decrease the amplitude of this 2nd input until the logic function fails. Determine V_{IH} and V_{IL}.
4. Page 3:
    a. Timing. Set one of the inputs to logic-1 (+5V). Set the 2nd input as a square wave between 0 and 5V. Connect a 100 nF capacitor at the output to simulate a load (this is a very large load by VLSI standards but we will use it for illustration).
        i. (10 points) Determine the rise and fall times of the output waveform.
        ii. (20 points) Determine τ_{PLH}, τ_{PHL}, and τ_P.
5. Page 4: (BONUS) A design according to the methodology we study requires 12 transistors (all of the available MOSFETs on the two MC14007 chip that you have). There is an alternative design using pass transistors (similar to the transmission gates that you used in Project 2). You may obtain bonus marks on this project as follows:
    a. (10 points) Research and implement this alternative design. Provide the circuit schematic, build the circuit, and demonstrate functionality using the logic analyzer of the AD2.
    b. (10 points) Measure the voltage levels for this design and compare with the conventional design.

c. 10 points) Measure the timing performance of this design and compare with the conventional design.

In addition to the above, 10 points (non-bonus) will be assessed on presentation. This includes the layout of the report according to the above sections, quality of figures, neatness, and clarity of presentation in a professional style.