Electronic Devices and Circuits I [ELECENG 2EI4]
Project #4

Instructor: Dr. Haddara

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As a future member of the engineering profession, the student is responsible for performing the required work in an honest manner, without plagiarism and cheating. Submitting this work with my name and student number is a statement and understanding that this work is my own and adheres to the Academic Integrity Policy of McMaster University and the Code of Conduct of the Professional Engineers of Ontario. Submitted by **[Zayeed Ghori, ghoriz1, 400398943]**

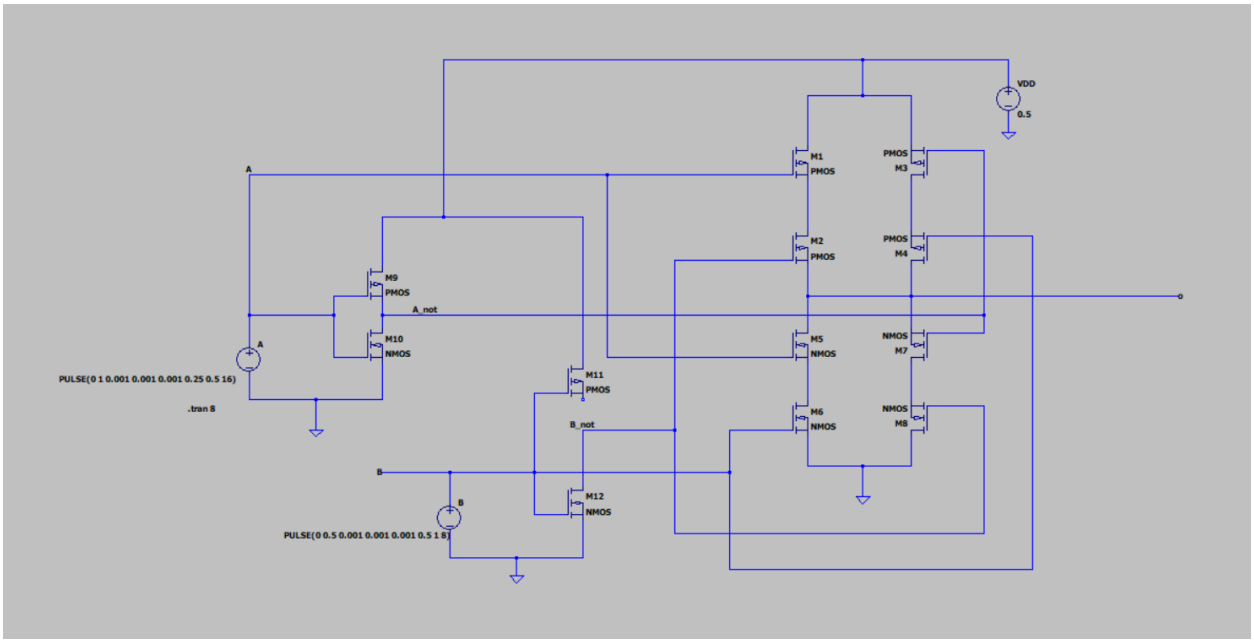

Figure 1: Circuit Schematic

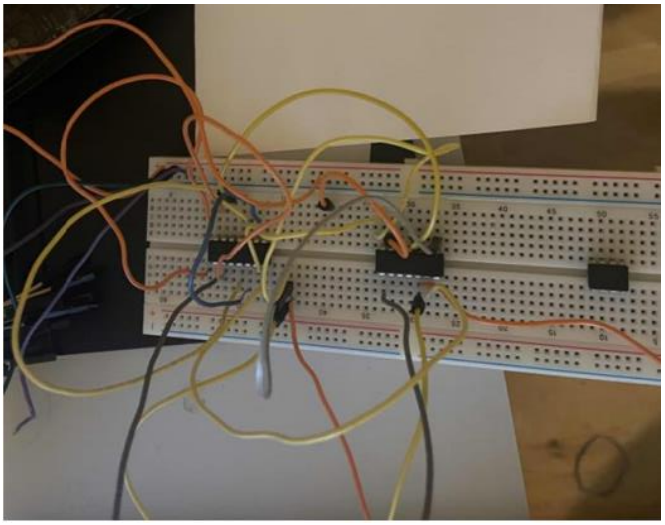

Figure 2: Physical Circuit

The ideal ratio for the PMOS and NMOS XOR circuit topology is 1:1 due to the resulting XOR equation:

Y = ((A'B') + (AB))

Since the equation requires an inverter for each input between A and B, MOSFETs would be required to invert the inputs. Because there are two inputs, a total of 2N and 2P MOSFETs would be needed to invert them. Otherwise, ANDing A' and B' and A and B can simply be performed by wiring the outputs of 2 N and 2P MOSs. To complete the OR functionality the 2 P and 2N MOSFETs were needed.

Also the number of PMOS's in the pull-up networks is the same as the number of NMOS's pull-down networks as shown the equation above, therefore the ideal ratio would be 1:1.

It is possible to achieve ideal sizing in hardware by utilizing the MC14007 chips, which have three MOSFETs of each type per piece. By using two MC14007 chips, it is feasible to create a 12 MOSFET circuit as designed. However, using multiple MOSFETs may result in poor output quality due to their high internal impedance, which can affect the output.

Functional Testing

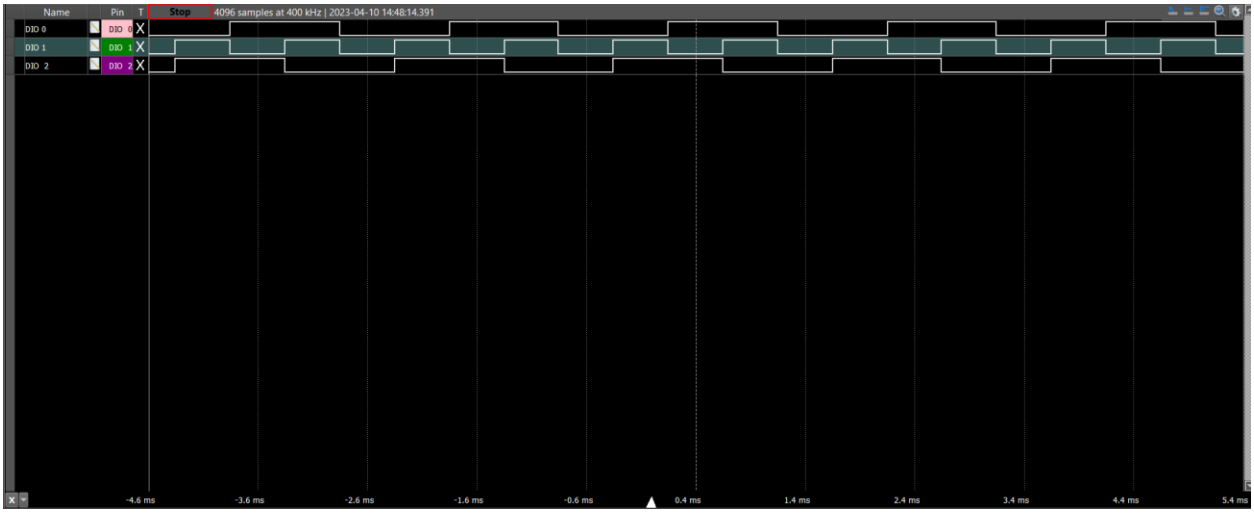

Figure 2: XOR Gate Inputs (from top to bottom) A and B and Output in AD2 Patterns Menu

The circuit demonstrates the functionality of an XOR gate, looking at the two inputs A and B (see Figure 1), the aligned output is HIGH when A or B is HIGH and LOW when A and B are HIGH or when A and B are LOW.

Static Testing

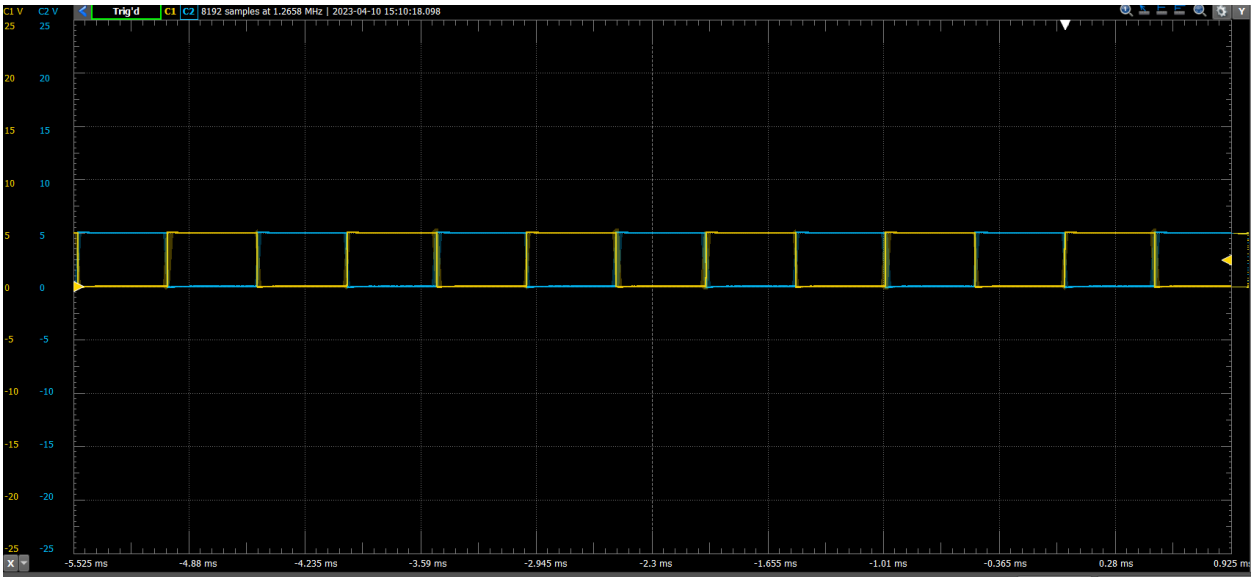

Figure 2: Static Testing on AD2 Oscilliscope, B input (Yellow) and Output (Blue)

Looking at the graph while A was HIGH and B was a 400kHz pulse, the output showed that Vh = ~5V and Vl = ~0V with very little deviation. This was the same when A was set to the pulse and B was set to HIGH.

Gradual Increase

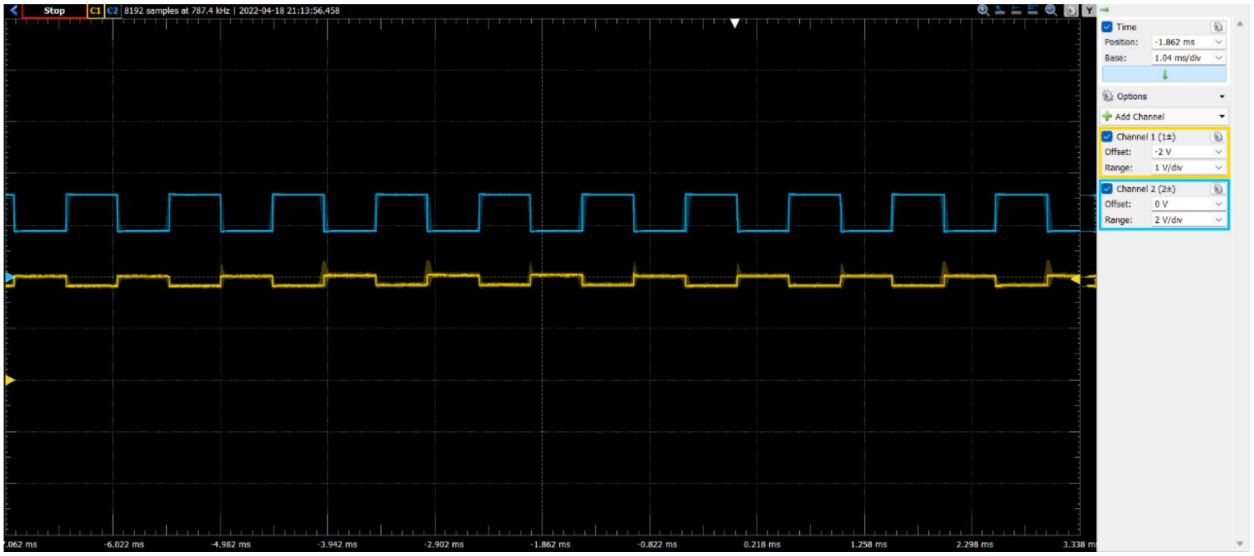

Figure 3: Static Testing with 2.5V offset to input A (blue) and Output (yellow)

For the output, VL is ~1.75V and VH is 2.01V.

Timing

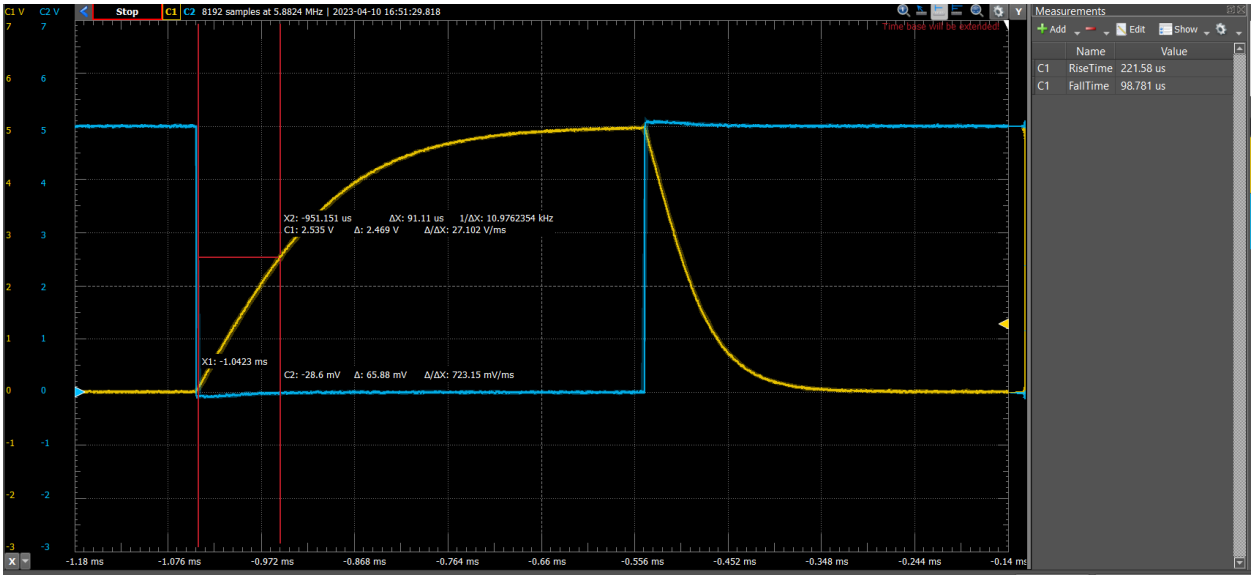

Figure 4: Graph of the Capacitor Rise time with TPLH

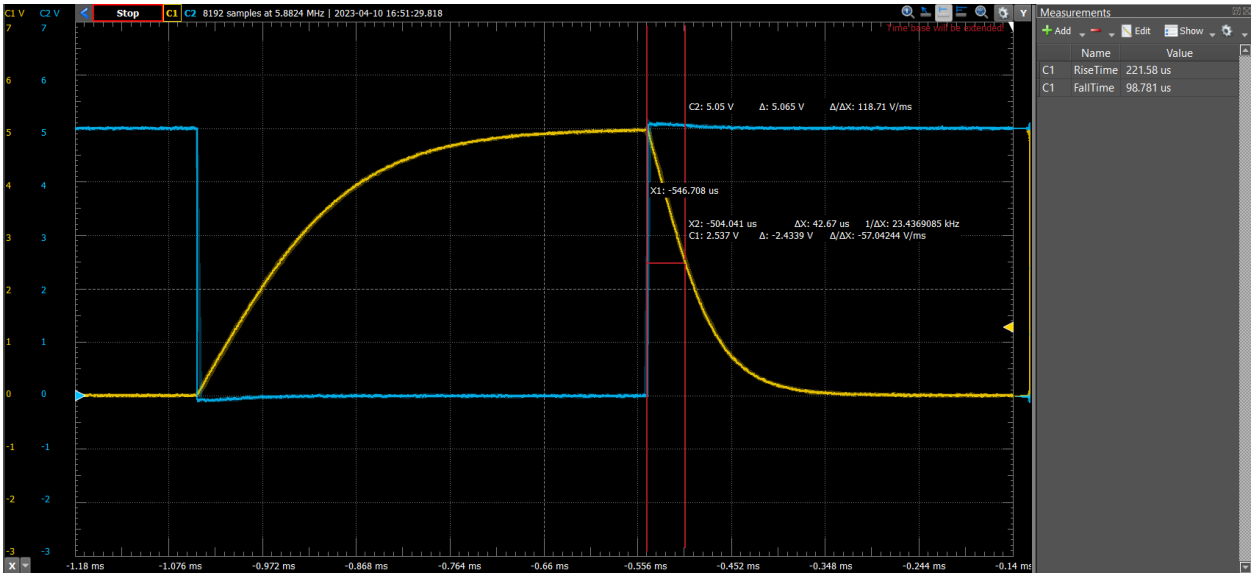

Figure 5: Graph of the Capacitor Rise time with TPHL

i. As shown in Figure 4 and 5, the rise time was 221.58us and the fall time 98.781us.

ii. From Figure 5 and 6 respectively:

TPLH = 91.11us
TPHL = 42.67us

TP = (91.11us + 42.67us) / 2 = 66.89 us