SDU	**Digital Design and Signal Processing - DDS Assignment #1**	IC	06.02.25

The purpose of this assignment is to:

- Create models of simple combinational circuits in the VHDL language. The circuits will be verified via simulation before and after implementation.
- Get some preliminary knowledge on using the Xilinx development tools

The assignment covers the use of the basic data types (std_logic and std_logic_vector), and different design principles (structural, behavioral), as well as the use of some VHDL operators and building testbenches for simulation.

All designs will be implemented in the Xilinx Vivado development tools with the Zedboard and ZYNQ System On chip (SOC)/FPGA as the target for implementation.

Question 1.1:
Write the VHDL code for an 8 bit adder. Use the std_logic_vector type for the 8 bit input and output signals and the std_logic type for the carry in and carry out signals.

- Document the functionality of the circuit by building a testbench and doing relevant simulations and show, that the implementation introduces delays in the circuit.

Question 1.2:
Write the VHDL code for a multiplexer with select inputs, four eight bit inputs and one eight bit output.

- Document the functionality of the circuit by building a testbench and doing relevant simulations before and after implementation, and show, that the implementation introduces delays in the circuit.

Question 1.3:
Design an 8 bit ALU with the inputs A, B and CarryIn and the outputs C and CarryOut. The ALU has the following functions: A + B, A and B, A or B, Invert A.

The ALU must consist of three building blocks, - one adder (from question 1.1.), one multiplexer (from question 1.2) and one logical block (the remaining).

- Create and test (and document) the remaining building block (logical block).
- Create a structural model of the total design including the three building blocks and the top-level input and output ports.
- Document the functionality of the circuit by building a testbench and doing relevant simulations before and after implementation.
- Document the number of used cells in the FPGA, and which component pins the layout has allocated.

Write a (short) document, describing the solutions, test benches, simulation results and what you have learned.