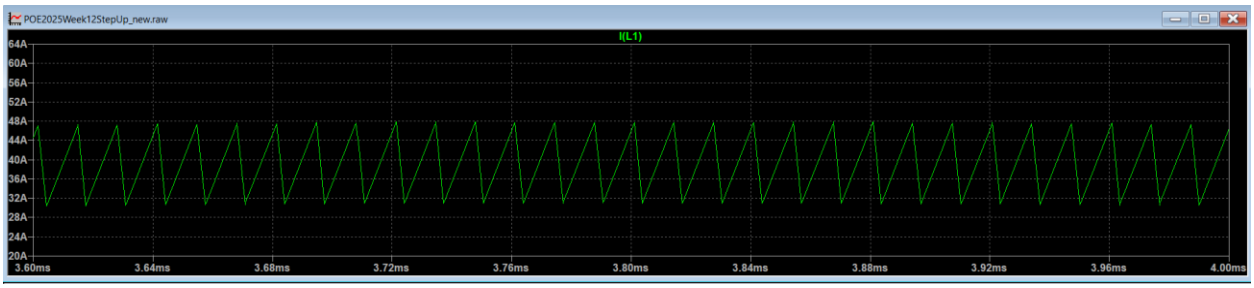
Zayin Conde
Power Electronics
Assignment 7
Step up converter
3/30/2025

POE2025 Week 12 Step Up Converter Hand in 7

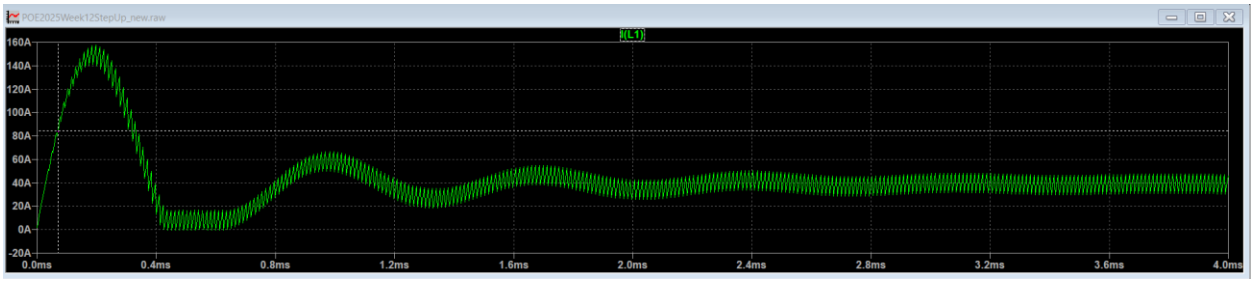
1. Simulate and document for the Step-up converter the current thru all the components at steady-state for duty-cycle D=50% by some screendumps – try to make the screen dumps line up in time if possible, so that you can follow what goes on in the circuit. Use the current probe.

NOTICE! – Simulations are done with 80% duty cycle. Scroll further down for 50% duty cycle!

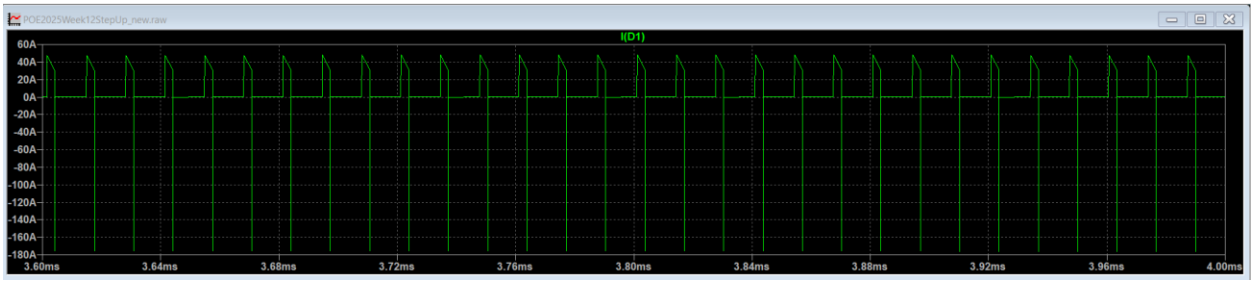
Inductor current oscillates from 30.5A to 47.5A



Note to self: In “steady state” the waveform still oscillates slightly. Roughly by 1A



Diode Current



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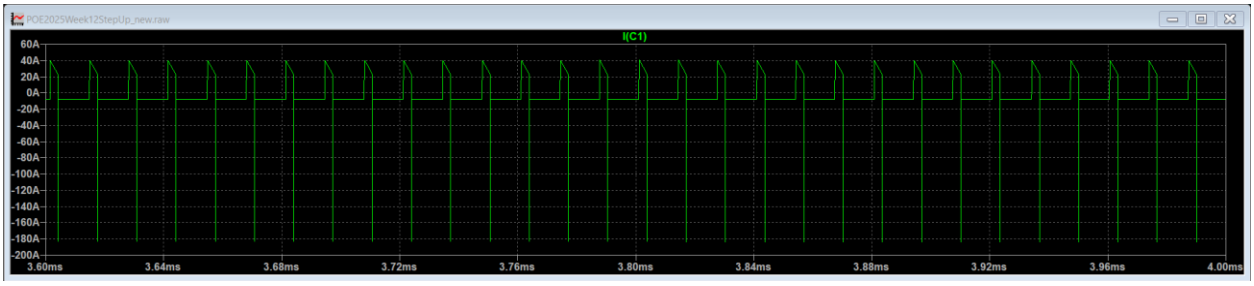
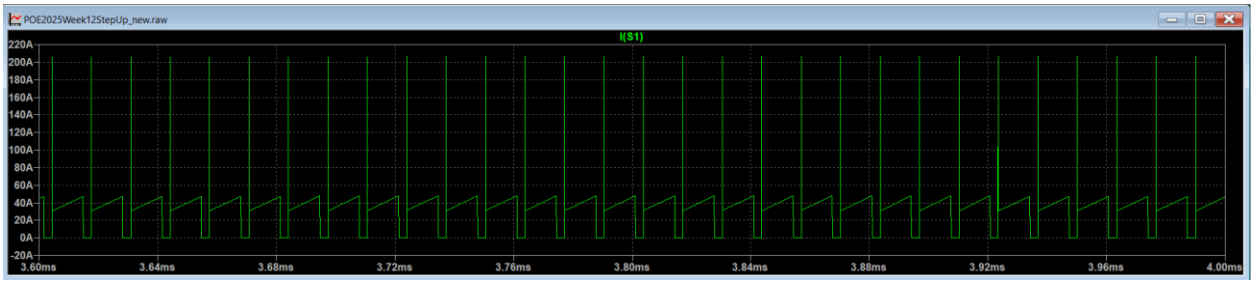
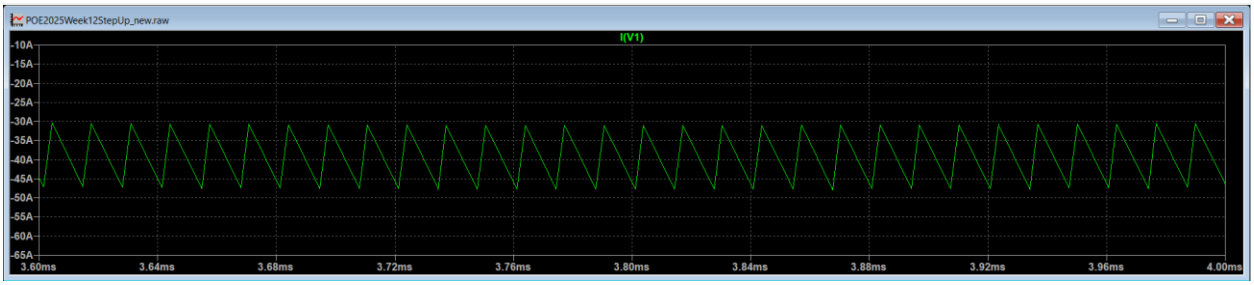
Capacitor Current



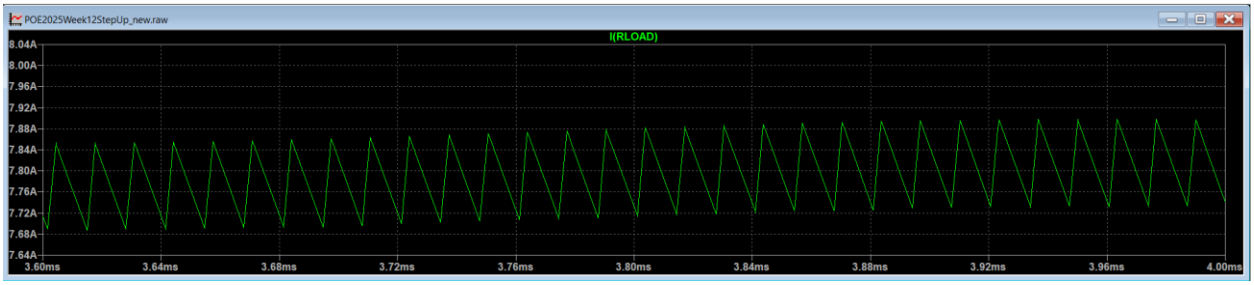
Switch current



V1 supply voltage Current



Load Resistor Current, entire waveform oscillates slightly even in steady state.



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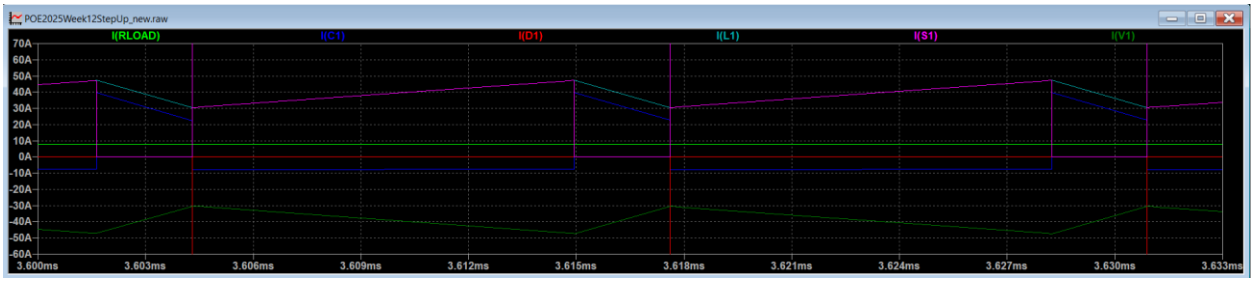
All currents together, difficult to ready.



NOTEICE - 50% Duty Cycle Simulations start here!

Just realized the previous simulation was at 80% duty cycle.

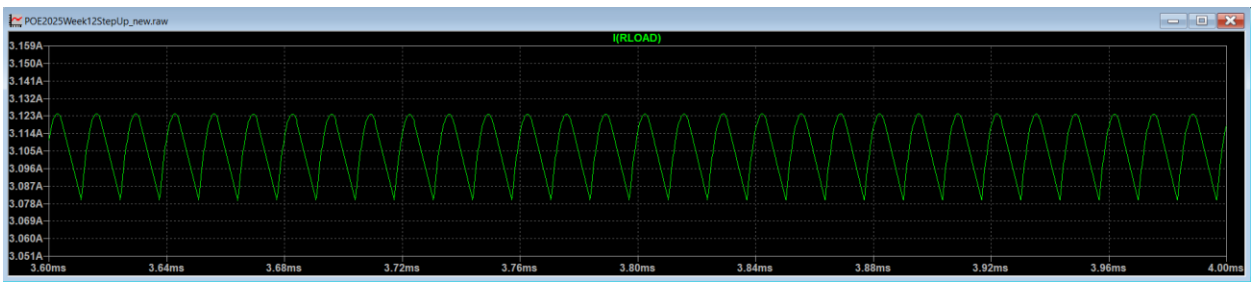
```
.param D = 0.80
.param T = 13.30u
```

```
.tran 0 4000u 0u 0.1u      PULSE(0 10 1n 1n 1n {D*T} {T} 1000)
.model INTER SW(Ron=0.1p Roff=1Meg Vt=5 Vh=0 Lser=0 Vser=0)
```

Change parameter D to 0.5 for 50% duty cycle. Then simulating again. ´

```
.param D=0.50
.param T = 13.30u
```

RLoad Current: Rload current waveform doesn't oscillate slightly like 80% duty cycle does



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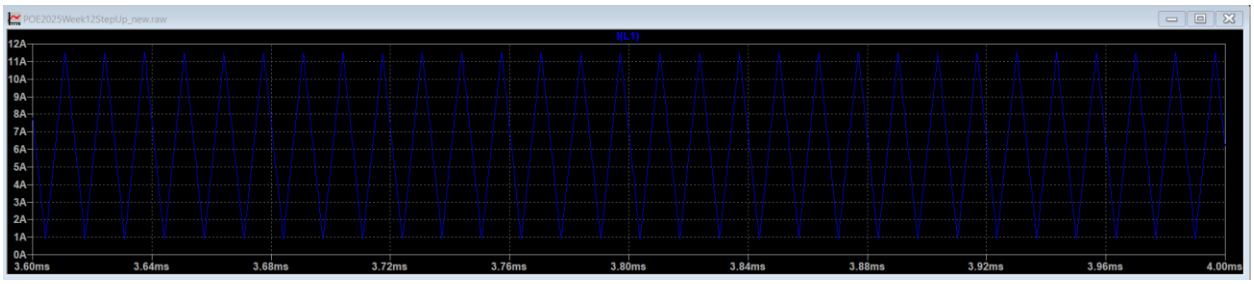
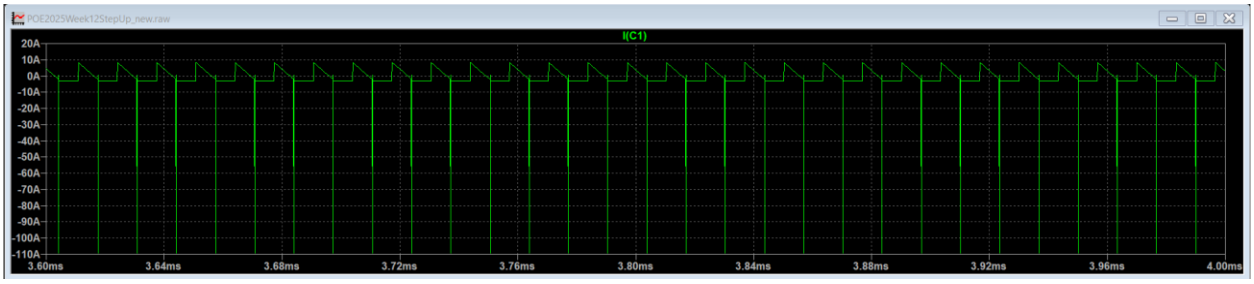
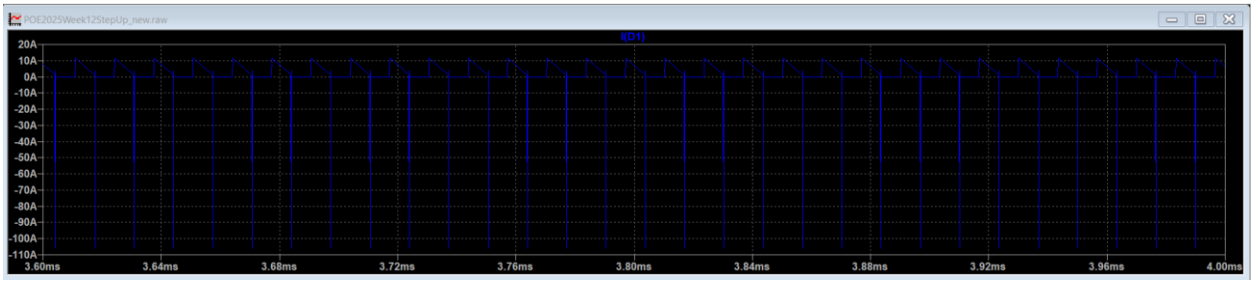
Inductor Current



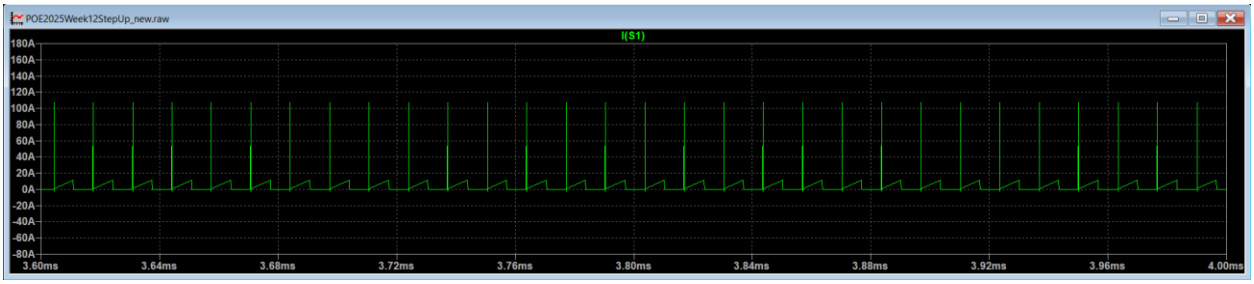
Capacitor current



Diode current



Switch current



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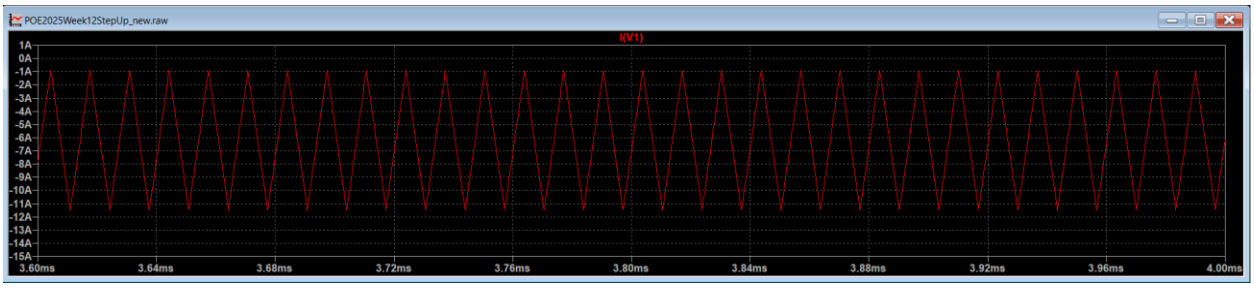
V1 supply voltage current



Frequency is 75%, period T is given as 13.3uS,

```
.param T = 13.30u
```

F=1/T,

1/0.1333=0.75, multiply 100% is 75%

2. Simulate and plot the output voltage as function of the duty-cycle D for RLOAD = 5Ω (see and fill table below, then plot the values of Vout(D) graph; You can use a tool like Excel or similar. Then compare it to the theoretical value and comment (use % deviation). The values must be STEADY STATE values.

Steady state evaluated between 3.6ms and 4ms

Dutycycle D	***Simulated Vout @ RLOAD = 0.5ohm***	***Calculated by theory Vout=Vin*(1/(1-D))***	***% Deviation***
0.1	8.519312514	8.888888889	4.157734221
0.2	9.610833729	10	3.891662709
0.3	11.03183552	11.42857143	3.471439216
0.4	12.9058348	13.33333333	3.206239003
0.5	15.5308819	16	2.931988151
0.6	19.47113783	20	2.644310871
0.7	26.02133666	26.66666667	2.419987538
0.8	38.97404747	40	2.564881332

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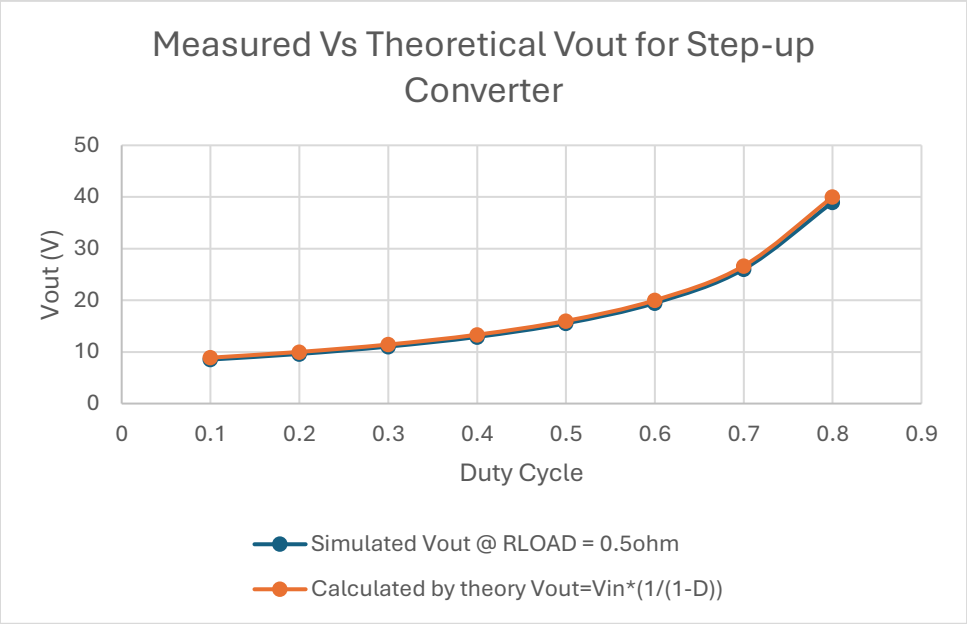

The graph shows and exponential increase in Vout as a function of increasing duty cycle.

The deviations are closer together in the step up converter compared to the step down converter.

Deviation decreases as duty cycle increases

Possibly reasons for deviations (in real world tests):

- Theoretical will not account for non-ideal components
- Losses in energy such as switching losses
- Parasitic effect

It seems that the LT-spice simulation is using ideal components, so I don't know why they vary from theoretical.
V2 voltage supply driving the switch does have some set delay on rise and fall times. Maybe these are the reasoning behind the deviations?
When duty cycle increases or decreases, the switching delay and possibly effect the output more or less significantly.

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5. Your small theory reflection about the Step-Up converter (a single A4 page of text/sketches that are your own words/drawings) – you can use the hints to explore the circuit. I'm not interested in copy-paste from the internet or books, but how you perceive/understand it.

Not finished