POE 2025 Week 10 IGBT vs. MOSFET Hand in 4

1. The Aim

Make knowledge about IGBT switching behavior more explicit.

This is done by evaluating simulations of IGBT in one of its typical applications where the focus is on some specific datasheet parameters that is important for the application.

The focus areas are:

1. The IGBT, Z1 in an inductive switch application with a freewheeling diode, D1. The inductor is simulated with a current source in the simulation setup. For the IGBT the ON and OFF switching is simulated with the focus on behavior of the Gate-Emitter voltage, VGE, Collector current, IC, and the Collector-Emitter voltage, UCE, over time.
   Below in figure 1, there is a test setup for the simulation in LT Spice. For comparison a MOSFET is in the same setup.
   The comparison focuses between the MOSFET vs IGBT: the Drain-Source voltage (MOSFET) versus the Collector-Emitter voltage (IGBT) and the turn-off time, where the IGBT will show a tailing-effect.

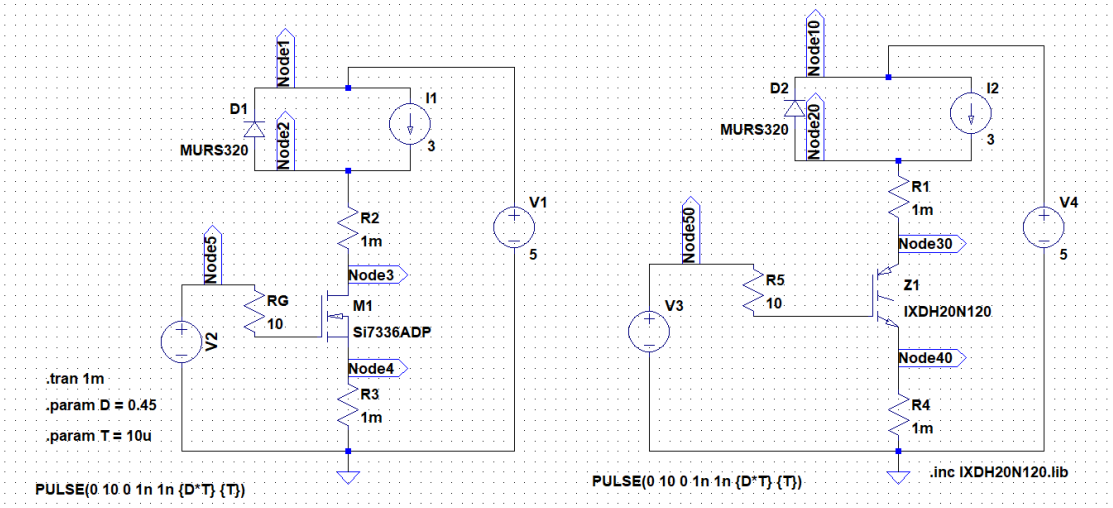

Figure 1. To the right side - the IGBT: The IGBT, Z1 and the Freewheeling diode, D2 in a classic switch setup. I2 models an Inductor. We can add a gate resistor RG of 1-10 Ohm, if the voltage on Node30 should oscillate. To the left side – the MOSFET in the same setup as the IGBT.

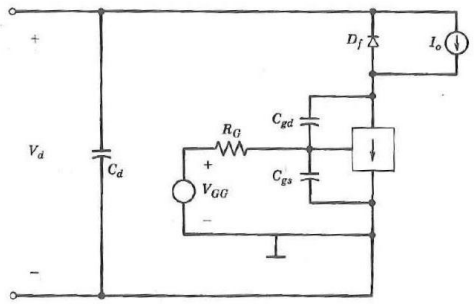

Figure 2: The IGBT model setup for the next three pictures are identical to the MOSFET. V2 from figure 1 is the VGG source. RG (Gate resistance – the purpose is to kill oscillations due to stray inductances interact with the gate capacitance in the IGBT – note that the IGBT model can have stray inductances build in, to model the wire bonding of the chip to the used housing). The circuit here is that of a step-down dc-dc converter. The equivalent circuit is valid for cutoff and active transient analysis.

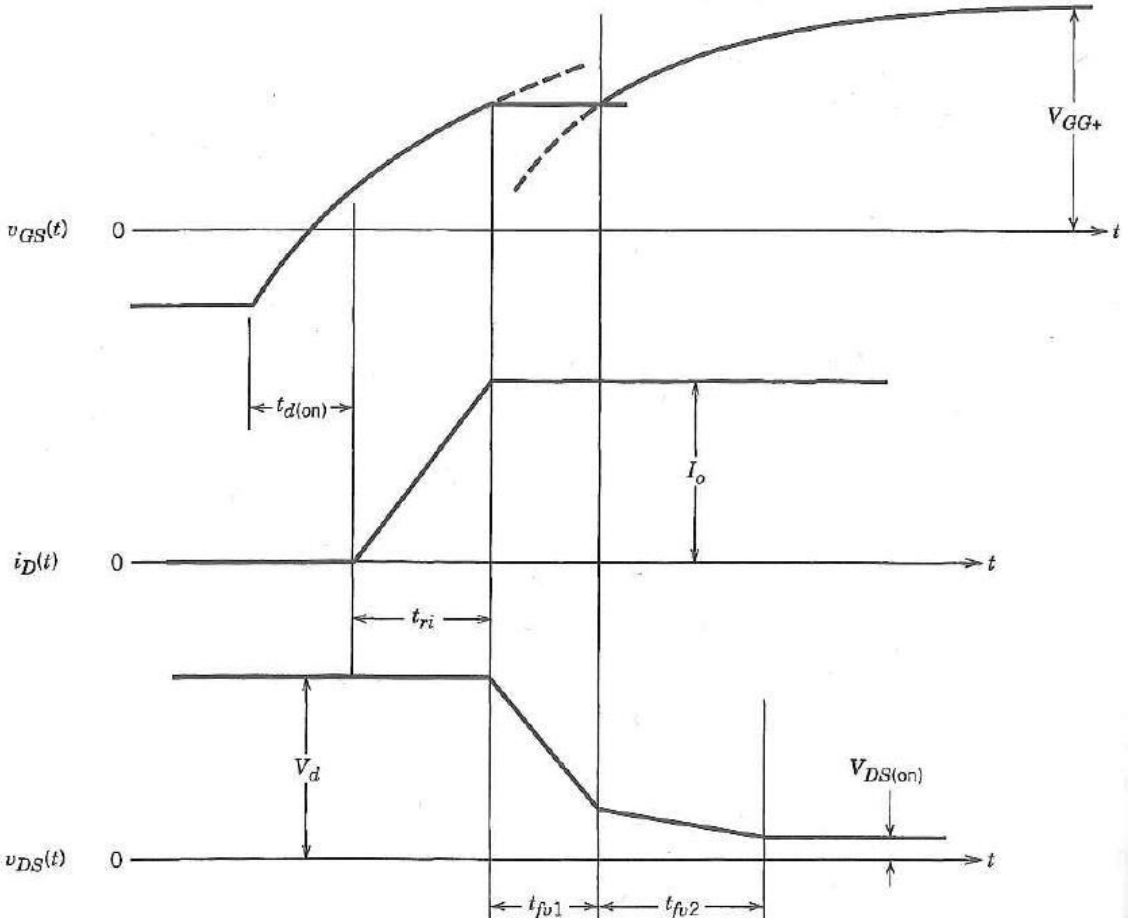

Figure 4: The IGBT Turn-**on** waveforms related to a switch setup for a DC-DC converter **with ideal Free-wheeling diode. Note: In the diverse power electronic literature some authors label the IGBT pins as for the MOSFET, and other label the pins as if the IGBT is made up of a MOSFET and BJT. In this picture VGS = VGE, ID = IC, and VDS = VCE.** Source: [1]

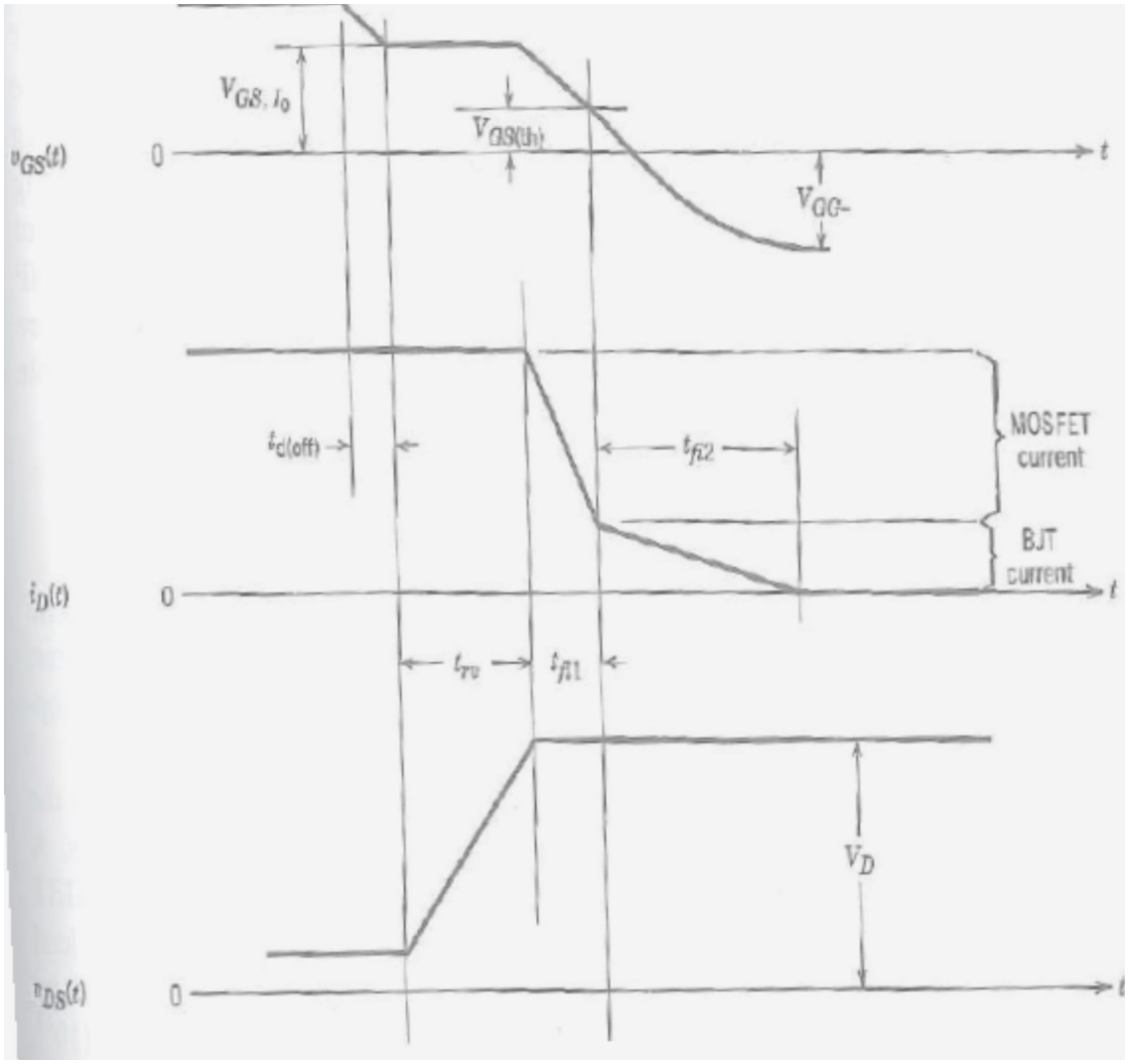

Figure 5: The IGBT **Turn-off** waveforms related to a switch setup for a DC-DC converter **with ideal Free-wheeling diode**. Source: [1]

Recommended approach:

1. Plan and describe your strategy to extract the needed data to the simulation setup from the datasheet and how to compare the simulation result with theory – figure 4-5, and other materials.
2. Describe your actual simulation setup and illustrated it with necessary screen dumps **(Use white background).**
3. The IGBT datasheet used as a reference is IXDH20N120 from IXYS /Littelfuse
4. The diode datasheet used as reference is MURS320 from Vishay.
5. Discuss the simulation result to the datasheets and the available literature.

6. **IGBT:** Simulate and compare your simulations to the Switching Characteristics in the datasheet for the IGBT. Focus on the Rise Time: tr (10%-90% of voltage span) and Fall Time: tf (90%-10% of voltage span) (VGE, VCE and IC). Please note the Datasheet measurement setup and how datasheet define the times. It is typical based on a standard test setup for IGBTs in the industry.
7. **Exploration:** Investigate what happens to the IGBT collector-emitter voltage, when the Freewheeling diode is replaced with a 1kOhm resistor or the diode is missing. Is the collector-emitter voltage in the simulation over the maximum allowable collector-emitter voltage given in the datasheet?

On Itslearning you can find:

LT SPICE file: IGBT_switch_w9_2024_littelfuse.asc AND
IGBT_switch_w9_2024_littelfuse_ideal_diode.asc

LT SPICE lib files: IXDH20N120.lib and IXDH20N120.OLB must be placed in the same folder as LT SPICE files

Reference for the pictures:

[1] **Power Electronics**. Converters, Applications and Design. Mohan, Underland and Robbins. 3rd Edition. ISBN: 0-471-22693-9

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LT Spice IGBT Model information from LTSpiceHelp:

Z. MESFET and IGBT Transistors

Symbol Names: MESFET, NIGBT, PIGBT

Syntax: Zxxx D G S model [area] [m=<value>] [off] [IC=<Vds, Vgs>] [temp=<value>]

A MESFET transistor requires a model card to specify its characteristics. The model card keywords NMF and PMF specify the polarity of the transistor. The MESFET model is derived from the GaAs FET model described in H. Statz et al., GaAs FET Device and Circuit Simulation in SPICE, IEEE Transactions on Electron Devices, V34, Number 2, February 1987 pp160-169.

Two ohmic resistances, Rd and Rs, are included. Charge storage is modeled by total gate charge as a function of gate-drain and gate-source voltages and is defined by the parameters Cgs, Cgd, and Pb.

Name	Description	Units	Default
Vto	Pinch-off voltage	V	-2.0
Beta	Transconductance parameter	A/V^2	1e-4
B	Doping tail extending parameter	1/V	0.3
Alpha	Saturation voltage parameter	1/V	2.0
Lambda	Channel-length modulation	1/V	0.0
Rd	Drain ohmic resistance	Ω	0.0
Rs	Source ohmic resistance	Ω	0.0
Cgs	Zero-bias G-S junction capacitance	F	0.0
Cgd	Zero-bias G-D junction capacitance	F	0.0
Pb	Gate junction potential	V	1.0
Kf	Flicker noise coefficient	-	0.0
Af	Flicker noise exponent	-	1.0
Fc	Forward-bias depletion coefficient	-	0.5
Is	Junction saturation current	A	1e-14

A device with a Z as prefix can also mean an IGBT transistor. Disambiguation between the MESFET and IGBT is via the model statement.

Syntax: Zxxx C G E MNAME [area] [m=<value>] [off] [temp=<value>]
.model MNAME NIGBT

The LTspice IGBT implementation is based on original work by Robert Ritchie of Linear Technology Corporation. It uses device equations out of a series of papers by Allen Hefner of NIST et al. with some exceptions, e.g., the LTspice implementation includes subthreshold conduction and stochastic noise mechanisms.

Name	Description	Units	Default
Agd	Gate-Drain overlap area	A/V^2	5e-6
area	Active area	m^2	1e-5
BVF	Avalanche uniformity factor	-	1.0
BVN	Avalanche multiplication exponent	-	4.0
Cgs	Gate-Source capacitance per unit area	F/cm^2	1.24e-8
Coxd	Gate-Drain oxide capacitance per unit area	F/cm^2	3.5e-8

Jsne	Emitter saturation current density	A/cm^2	6.5e-13
KF	Triode region factor	-	1.0
KP	MOSFET transconductance	A/V^2	0.38
MUN	Electron mobility	$cm^2/(V \cdot s)$	1500
MUP	Hole mobility	$cm^2/(V \cdot s)$	450
NB	Base doping	$1/cm^3$	2e14
Tau	Ambipolar recombination lifetime	sec	7.1e-6
Theta	Transverse field factor	1/V	0.02
Vt	Threshold voltage	V	4.7
Vtd	Gate-Drain overlap depletion threshold	V	1e-3
WB	Metallurgical base width	m	9e-5
subthres	Subthreshold current parameter	-	0.02
Kfn	Flicker noise coefficient	-	0.0
Afn	Flicker noise exponent	-	1.0
tnom	Parameter measurement temperature	°C	27