Zayin Conde
Power Electronics
Assignment 6
Step Down converter
3/29/2025

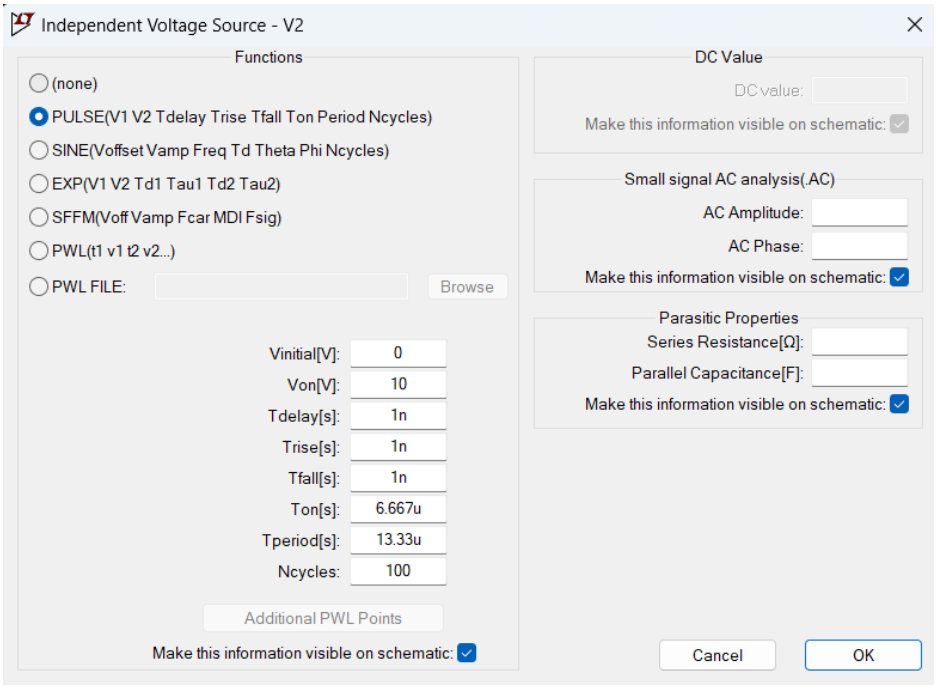
POE2025 Week 12 Step Down Converter Hand in 6

The tasks:

1. Simulate and document for the Step-Down converter the current thru all the components at steady-state for duty-cycle D=50% by some screendumps – try to make the screen dumps line up in time if possible, so that you can follow what goes on in the circuit. Let the background of the screendumps be white (is best to use in a presentation at the exam, due to the screen intensity).

Duty cycle- check V2 voltage, or calculate it from the pulse function Ton and Tperiod. For 50% then Ton should be Tperiod*0.5. Tperiod= 13.333

Duty cycle = (Ton/Tperiod)*100% => (6.667uS/13.333uS)*100% = 50%



Frequency => $f = \frac{1}{T}$, we know the period is 13.333uS

$$f = \frac{1}{0.01333333333} = 75\%$$

Frequency is indeed 75%

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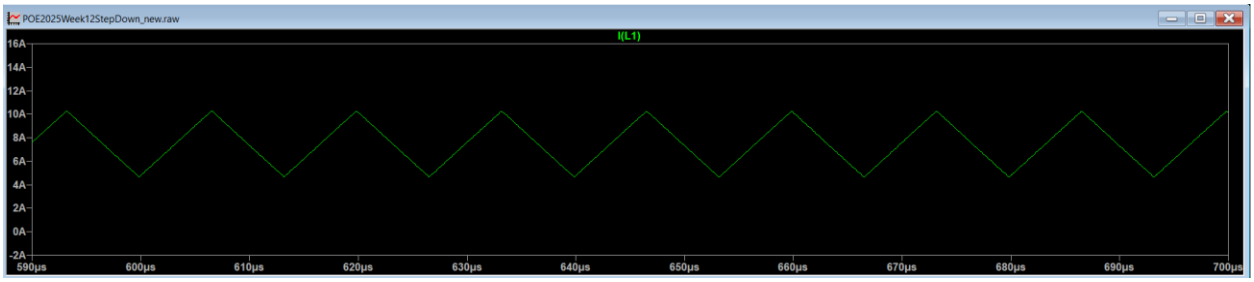
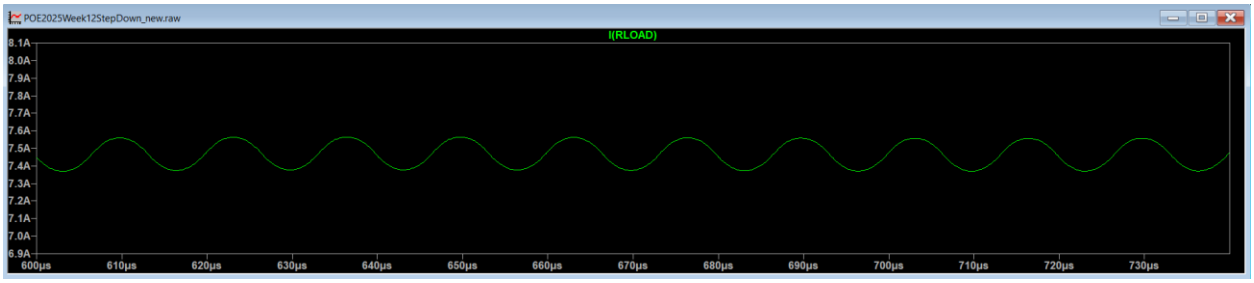
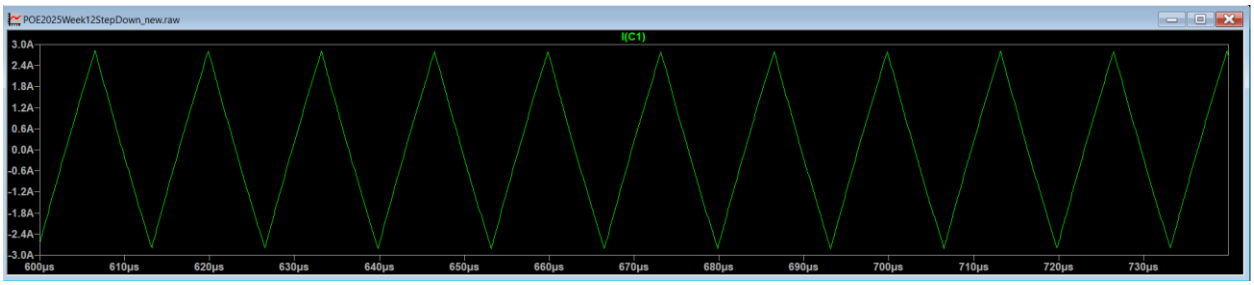
Inductor current oscillates from about 10A to 4.5A



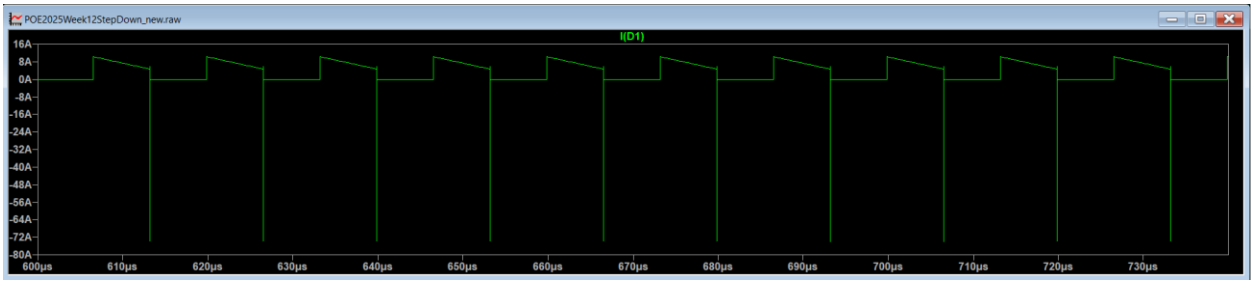
Load resistor current oscillates from about 7.3A to 7.5A



Capacitor current oscillates from -2.78A to 2.78A



Diode current rises to 10A then discharges.



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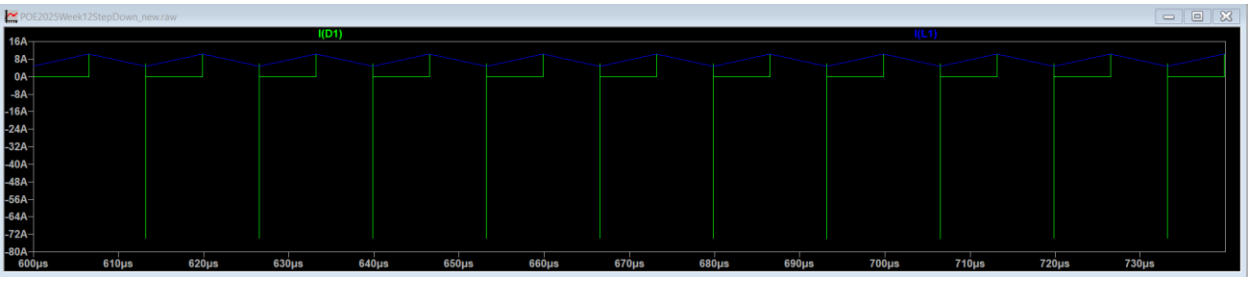
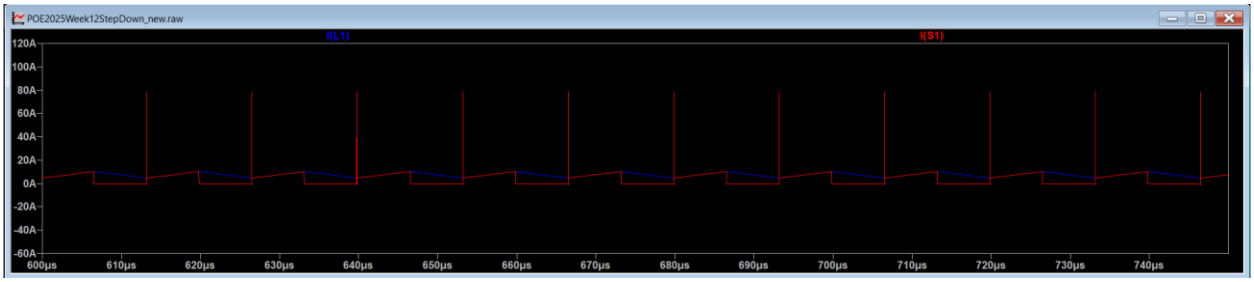
Inductor current discharges with diode current.



When switch is closed, inductor charges (current raises in inductor)



2. Simulate and plot the output voltage as function of the duty-cycle D for RLOAD = 0.5Ω (see and fill table below, then plot the values of Vout(D) as graph; You can use a tool like Excel or similar. Then compare to the theoretical value and comment (use % deviation). The values must be STEADY STATE values. See next page.

Dutycycle D	*Simulated Vout @ RLOAD = 0.5ohm*	*Calculated by theory Vout=Vin*D*	*% Deviation*
0.1	0.493672755	0.8	38.29090568
0.2	1.289909368	1.6	19.38066451
0.3	2.094343494	2.4	12.73568774
0.4	2.912690683	3.2	8.97841617
0.5	3.727465219	4	6.813369523
0.6	4.543869592	4.8	5.336050173
0.7	5.368290007	5.6	4.137678441
0.8	6.188683617	6.4	3.301818482

```
.MEAS TRAN AVG_VOUT AVG V(vout) FROM=600u TO=700u
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Calculated average Vout at SS (set to gather between 600u and 700u)

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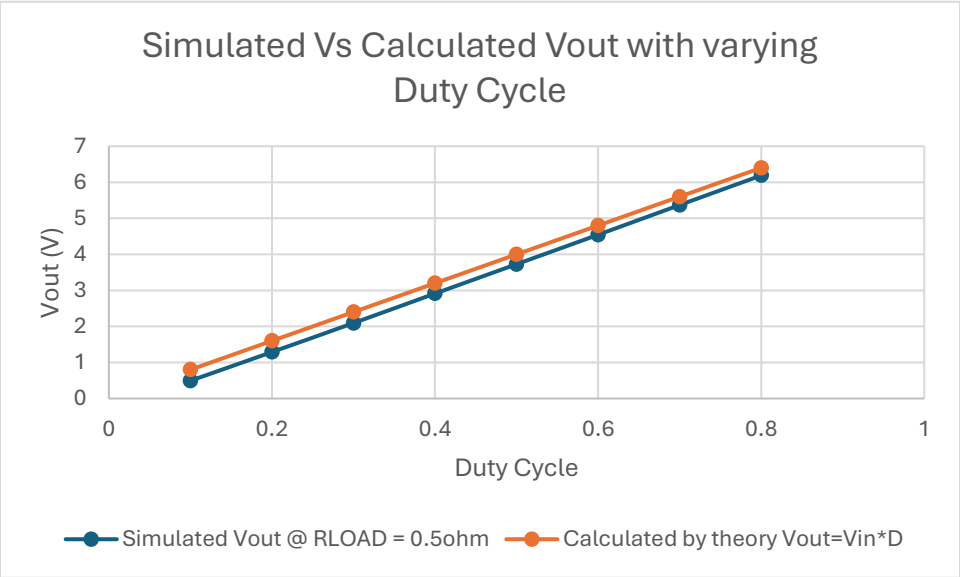

Notice higher deviations at lower duty cycle, as duty cycle increases the deviation decreases. Slope for both theoretical and measured are linear.

Possibly reasons for deviations (in real world tests):

- Theoretical will not account for non-ideal components
- Losses in energy such as switching losses
- Parasitic effect

It seems that the LT-spice simulation is using ideal components, so I don't know why they vary from theoretical.

V2 voltage supply driving the switch does have some set delay on rise and fall times. Maybe these are the reasoning behind the deviations?

When duty cycle increases or decreases, the switching delay and possibly effect the output more or less significantly.

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3. Harmonics in the output voltage of the Step-Down converter:
For the simulation please use the function FFT ***(Setup the Transient command to first log data when the converter is in <u>Steady state</u>, RUN, then R-click on Vout and Click VIEW-> FFT. Note: Please see Hand-In 1 for setting up for FTT appropriately)***, and simulate the amount of harmonic frequencies in Vout. Please note: Use the time for the FFT that clearly show that the Step-Down converter is operating in **steady state**.

```
.tran 0 1000u 600u 0.1u
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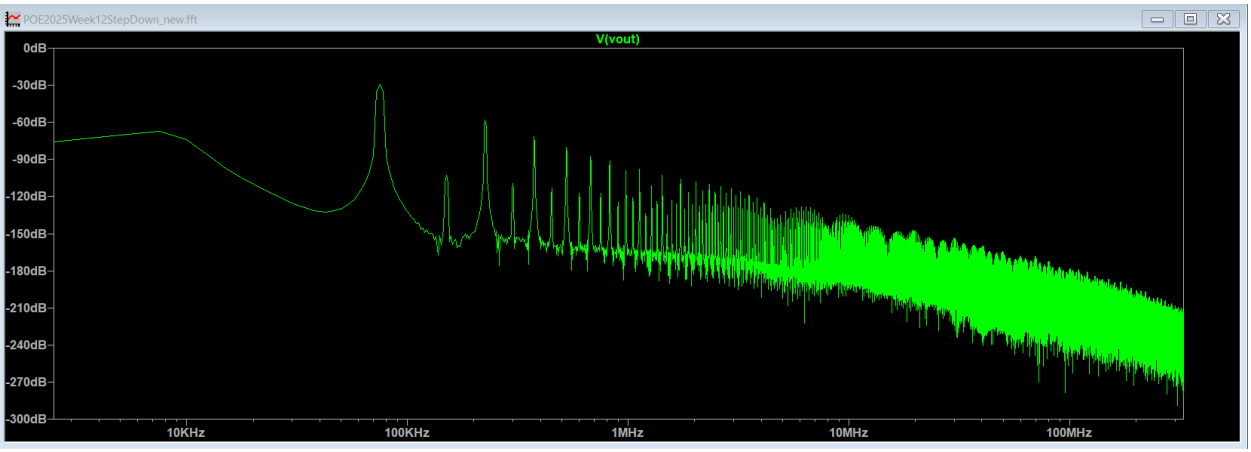
Changed .tran to start gathering data after 600uS cause that's what I did in the previous steps



5. Your small theory reflection about the Step Down converter (a single A4 page of text/sketches that are your own words/drawings) – you can use the hints to explore the circuit. I'm not interested in copy-paste from the internet or book, but how you perceive/understand it (a way to get help you to check your knowledge before the exam).

Step-down converter converts an higher input voltage to a lower output voltage, using step down converter can be more efficient then using a voltage divider n not finished