POE2025 Week 12 Step Down Converter Hand in 6

The Aim: We get to know the basic operation and signals in the Step-down converter based on a simulation.
The Theory: We can test the theory for the ideal vs the non-ideal for the Step-down converter.

Hint to look out for in the exercise:
Vout as function of the duty circle D,
Inductor (minimum and maximum currents and the inductor size),
Load resistor size (min, max),
and the filter capacitor size in relationship to the Vout ripple size (ΔVout/Vout) and switch frequency.

The Step-Down converter.

Download the Step-Down file (LT Spice) from Blackboard. POE2025Week12StepDown_new.asc

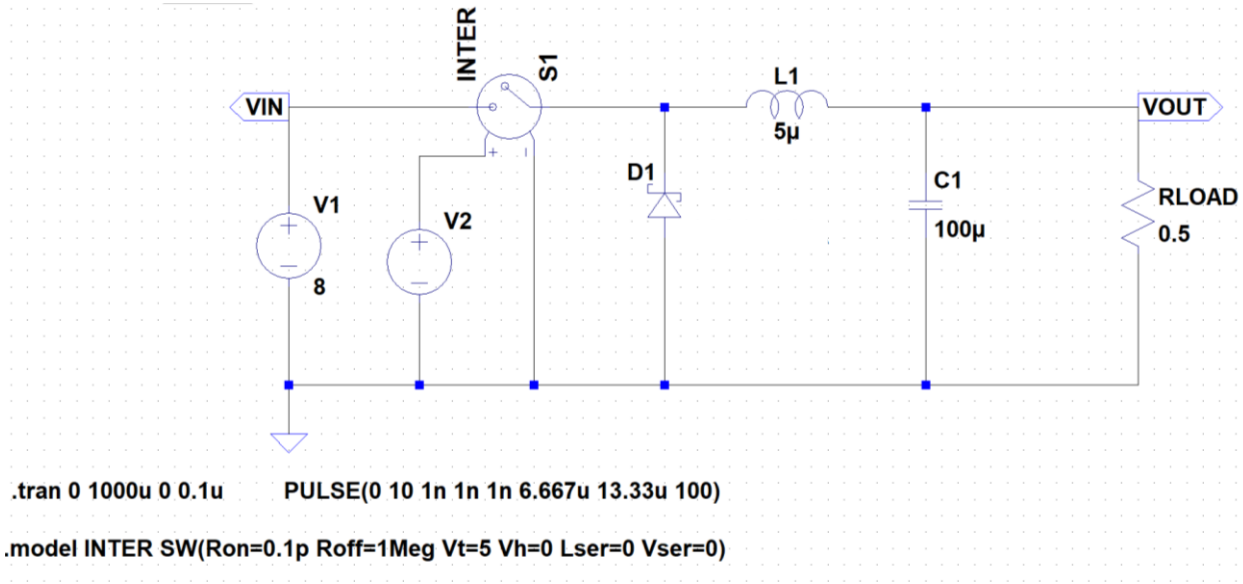


Figure 1. The Step-Down setup

The tasks:

1. Simulate and document for the Step-Down converter the current thru all the components at steady-state for duty-cycle D=50% by some screendumps – try to make the screen dumps line up in time if possible, so that you can follow what goes on in the circuit. Let the background of the screendumps be white (is best to use in a presentation at the exam, due to the screen intensity).

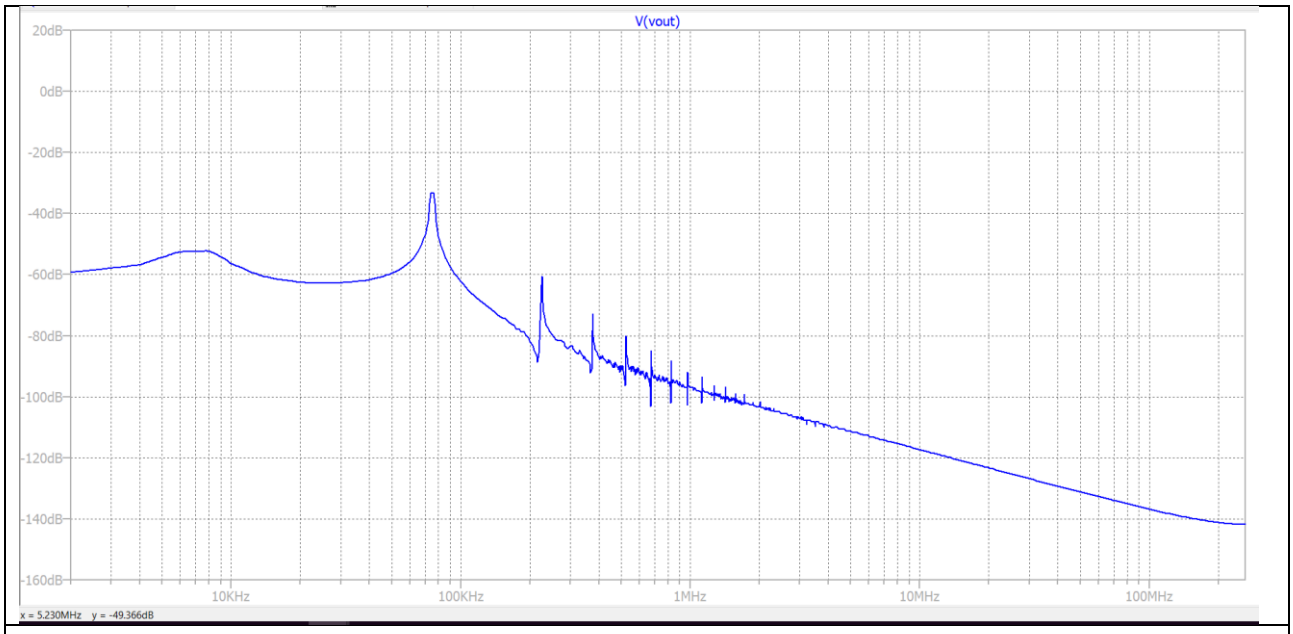
2. Simulate and plot the output voltage as function of the duty-cycle D for RLOAD = 0.5Ω (see and fill table below, then plot the values of Vout(D) as graph; You can use a tool like Excel or similar. Then compare to the theoretical value and comment (use % deviation). The values must be STEADY STATE values. See next page.

Dutycycle D	Simulated. Vout @RLOAD= 0.5Ω	Calculated by Theory Vout=Vin*D	Comparison & comments
0.1			
0.2			
0.3			
0.4			
0.5			
0.6			
0.7			
0.8			

Table 1: Values for the Step-Down converter.

3. Harmonics in the output voltage of the Step-Down converter:
For the simulation please use the function FFT ***(Setup the Transient command to first log data when the converter is in <u>Steady state</u>, RUN, then R-click on Vout and Click VIEW-> FFT. Note: Please see Hand-In 1 for setting up for FTT appropriately)***, and simulate the amount of harmonic frequencies in Vout. Please note: Use the time for the FFT that clearly show that the Step-Down converter is operating in **steady state**.

Practical: Take the screen shot of the Harmonics in Vout at D= 0.5 and RLOAD = 0.5Ohm. Investigate how the filter capacitor affects the harmonics, by increasing/decreasing the capacitor value with 100%.



For a FFT simulation we must set up the transient simulation to store data, when the signal is in its STEADY STATE. Otherwise we will get the startup transients to distort the picture of the STEADY STATE situation.

For the above sim the set up was: **.tran 0 1000u 500u 0.1u**

Figure 2: Example of a FFT simulation of harmonics in Vout in the steady state. The switch frequency of 75kHz can be seen in the output voltage, and the upstart transient can be seen from approx. 1 Hz to 10kHz.

Summary of recommended deliveries:

1. Screen dump of the current in the components measured by the current probe and visualized.
   Settings: D = 0.5, RLOAD = 0.5 Ohm, V2 frequency= 75 kHz.

2. A filled in Table 1, with your simulated and calculated values.

3. A graphical plot of your Table 1: Vout as a function of duty cycle D. The simulated and calculated values are drawn in the same graph, and the deviation is commented. You could use Excel to make the plot. Remember to name the axis. X-axis = Duty cycle, D and Y-axis = Vout. Add your comments to the simulated vs theory values – where do you think the deviations come from? (Hint: the components are not ideal)

4. Screen dump of the FFT, so that we can see the harmonics in Vout. The screen dump is made at D = 0.5 and RLOAD = 0.5 Ohm.

5. Your small theory reflection about the Step Down converter (a single A4 page of text/sketches that are your own words/drawings) – you can use the hints to explore the circuit. I'm not interested in copy-paste from the internet or book, but how you perceive/understand it (a way to get help you to check your knowledge before the exam).

If you have experimented with the component values effect on the output voltage ripple – which components affect the ripple the most?