POE2025 Week 8 Diode and MOSFET Hand in 2

1. The Aim

Make knowledge about power Diode and MOSFET switching behavior more explicit.

This is done by evaluating simulations of power MOSFET in one of its typical applications where the focus is on some specific datasheet parameters that is important for the application.

The focus areas are:

1. The MOSFET, M1 in an inductive switch application with a freewheeling diode, D1. The inductor is modeled as a constant current source in the simulation setup. For the MOSFET the ON and OFF switching is simulated with the focus on behavior of the Gate-Source voltage, VGS, Drain current, ID, and the Drain-Source voltage, UDS, over time. For the Diode, D1, the focus is the reverse recovery time trr, the maximum reverse current IRR, charge Qrr and an estimation of the Recovery Softness factor = snappiness factor. **Please see the note at the end of this document**.
   Below in figure 1, there is a test setup for the simulation in LT spice.

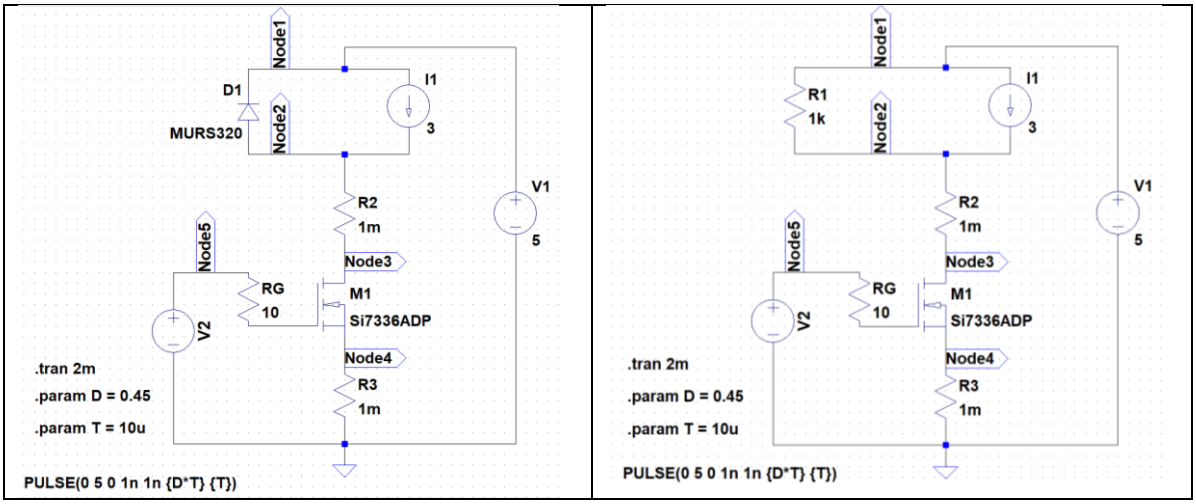


Figure 1. The MOSFET, M1 and the Freewheeling diode, D1 in a classic switch setup. I1 current source models an Inductor. R1 models the situation when there is no Freewheeling diode. (Note: an open circuit would make the SPICE mathcore calculate too long). In practice, we can add a gate resistor RG of 1-10 Ohm if the voltage on Node3 should oscillate. The oscillation can be caused by the inductor and the MOSFET's internal capacitances could act as a higher order system. The internal capacitor from the drain to the gate could feedback a signal from the drain to the gate – meaning we could have a system with poles close to the jω-axis, and therefore an underdamped system – typical with ringing when the input is a step transient.

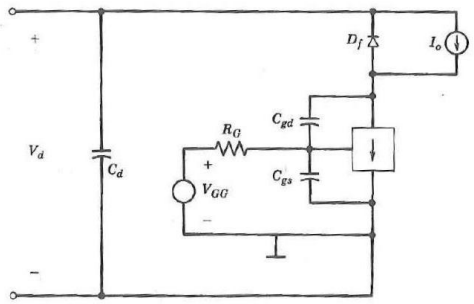


Figure 2: The Power MOSFET model setup for the next three pictures. V2 from figure 1 is the VGG source. RG (Gate resistance – the purpose is to kill oscillations due to stray inductances interact with the gate capacitance in the MOSFET – note that the Power MOSFET model can have stray inductances build in, to model the wire bonding of the chip to the used housing). The circuit here is that of a step-down dc-dc converter. The equivalent circuit is valid for cutoff and active transient analysis.

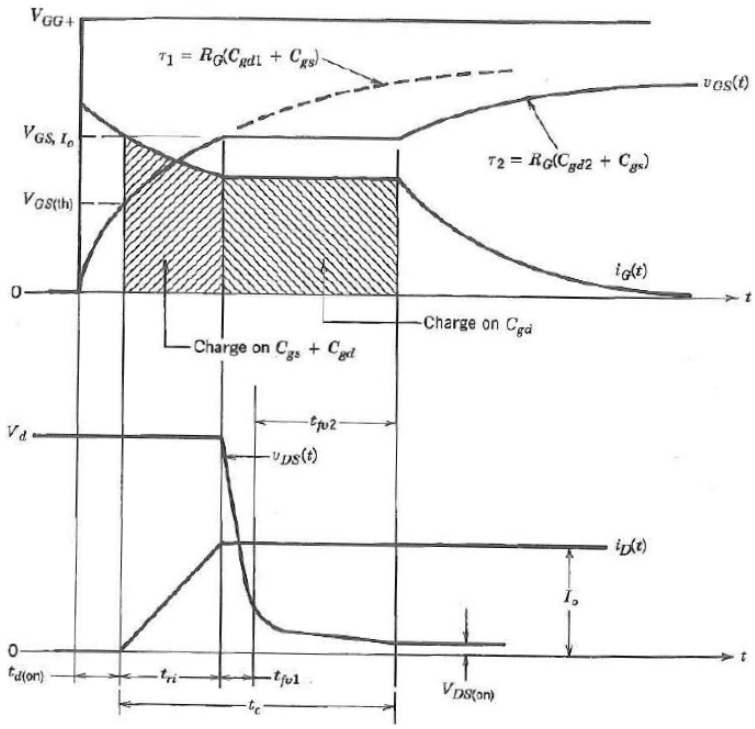
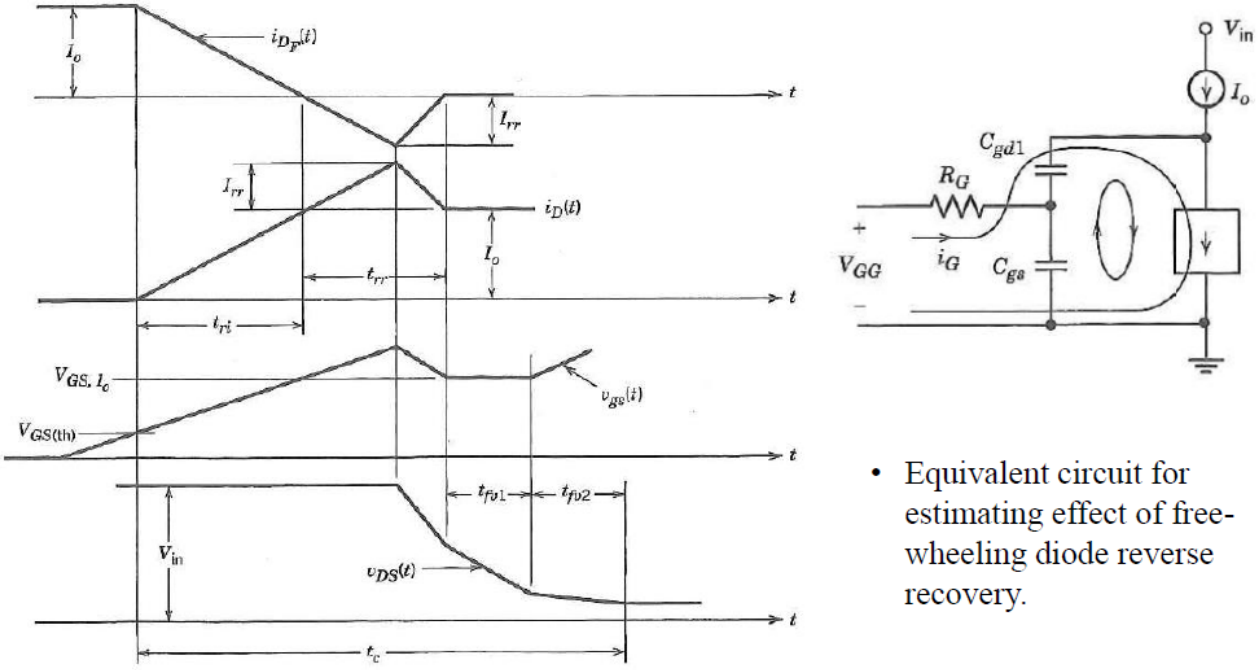


Figure 4: The Power MOSFET Turn-**on** waveforms related to a switch setup for a DC-DC converter **with ideal Free-wheeling diode.**



- Equivalent circuit for estimating effect of free-wheeling diode reverse recovery.

Figure 5: The Power MOSFET **Turn-on** waveforms related to a switch setup for a DC-DC converter **with none-ideal Free-wheeling diode (Reverse recovery is included in the used Diode model).**

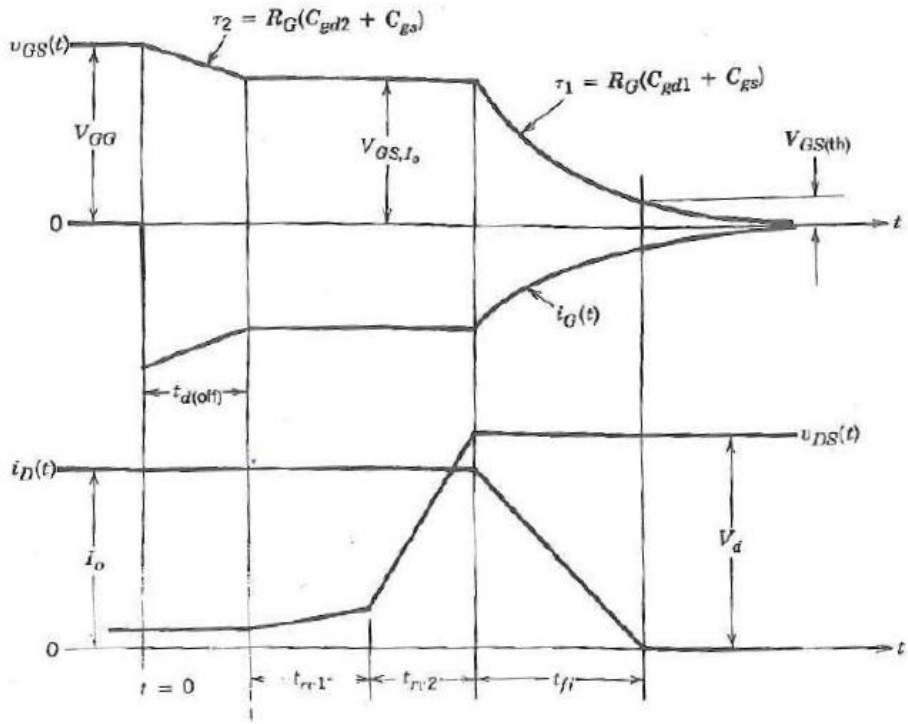


Figure 6: The Power MOSFET **Turn-off** waveforms related to a switch setup for a DC-DC converter **with ideal Free-wheeling diode**.

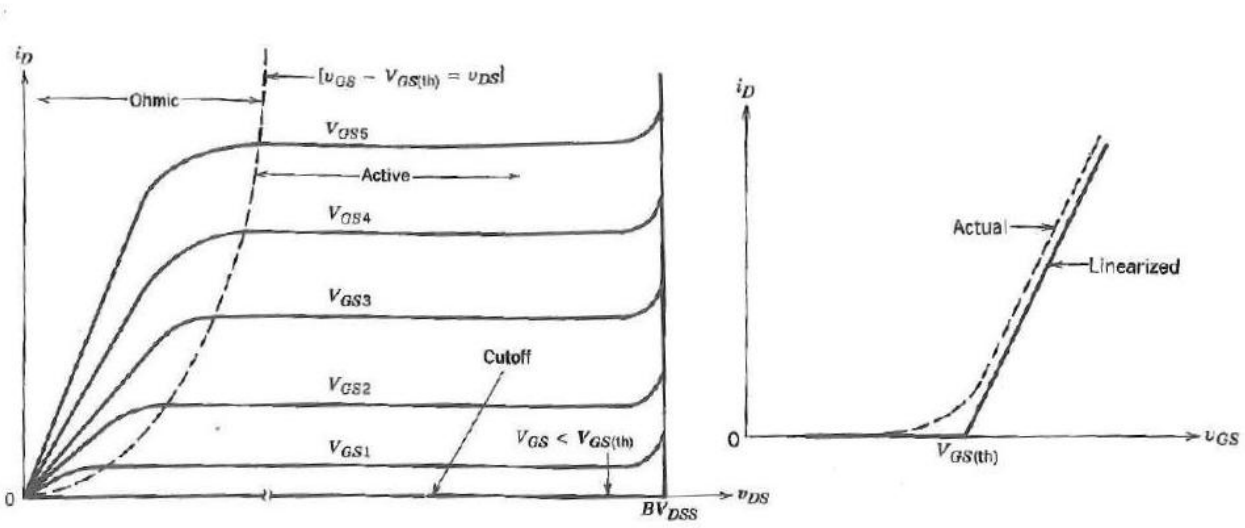


Figure 7: The Power MOSFET Characteristic.

Recommended delivery/approach:

1. Describe your actual simulation setup and illustrated it with necessary screen dumps with white backgrounds.
2. The Power MOSFET datasheet used as a reference is Si7336ADP from Vishay. (www.alldatasheet.com).
3. The diode datasheet used as reference is MURS320 from Vishay.
4. Discuss the simulation result to the datasheets and the available literature.
5. **MOSFET:** Simulate and compare your simulations to the Switching Characteristics in the datasheet for the MOSFET. Focus on the Rise Time: tr (10%-90% of voltage span) and Fall Time: tf (90%-10% of voltage span) (VGS, VDS and ID). Please note the Datasheet measurement setup and how datasheet define the times. It is typical based on a standard test setup for MOSFETs in the industry. **Your setup will most likely always be different to the datasheet because your design need will be different. How can we deal with this in a typical design situation?**
6. **DIODE:** For the Diode, D1, the focus is the simulation of the reverse recovery time trr, the maximum reverse current IRR, an estimation of the charge Qrr and an estimation of the snappiness factor (Please see definition in the note at the end of this document, together with the MicroNote 302). Note: the current directions.
7. **Exploration:** Investigate what happens to the MOSFET drain-source voltage, when the Freewheeling diode is replaced with a 1kOhm resistor, or the diode is missing. Is the drain-source voltage in the simulation over the maximum allowable drain-source voltage given in the datasheet?

Please have a “non-black” background color in the screen dump of simulations, because it is hard to read from a black background. Additionally, use the grid-option in the output window, to make the visual readings more easy.

Hand in is done in a “measurement-type” report in a Power Point Document and delivered as PDF-file.

Note on the Snappiness factor:

Soft Recovery and Snappiness factor

The old definition: Recovery Softness Factor = Snappiness factor, S = tb/ta. (MicroNote 302)

The new definition used by the industry:

JEDEC (Global standards for Microelectronics Industry) is now defining the snappiness factor based on diRR/dt: https://www.jedec.org/standards-documents/dictionary/terms/reverse-recovery-softness-factor-rrsf [Last accessed 10.02.2020]

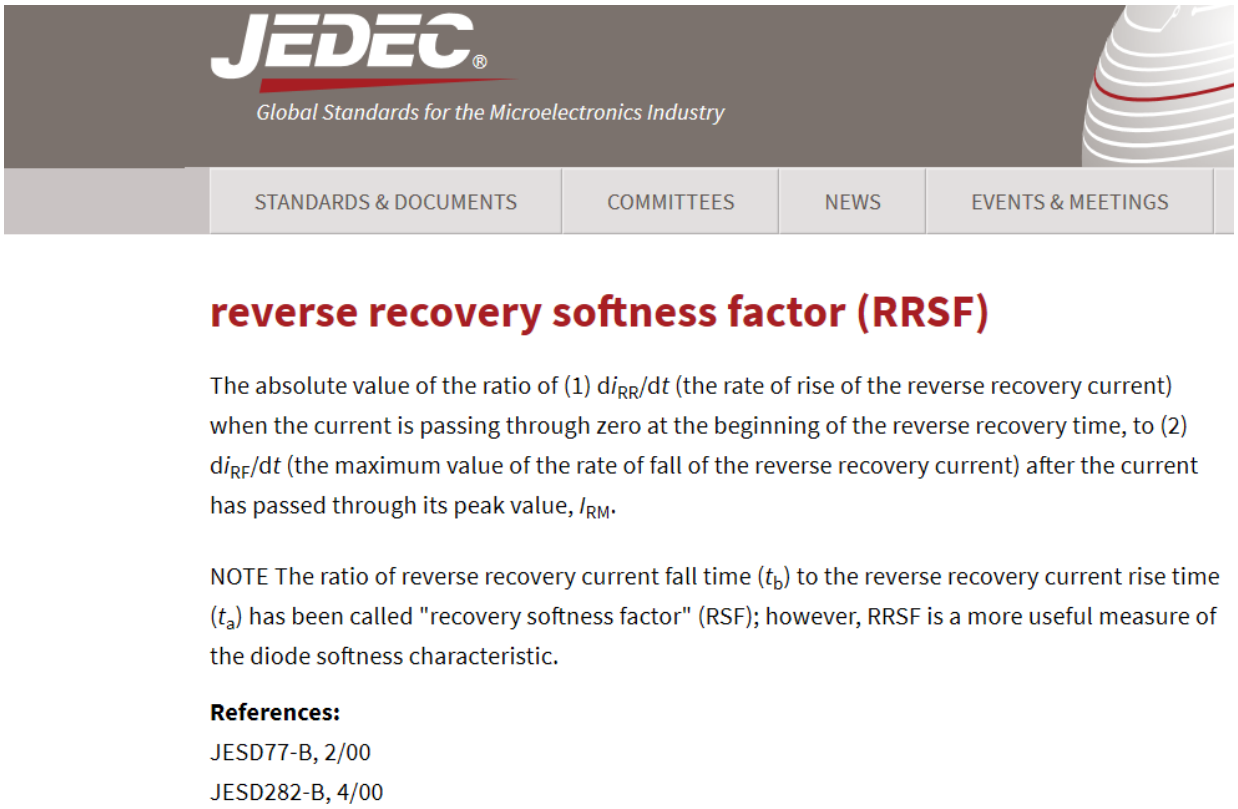


Figure 8: https://www.jedec.org/standards-documents/dictionary/terms/reverse-recovery-softness-factor-rrsf [Last accessed 07.02.2024]