2018《FPGA 应用实验》实验报告

实验编号：Lab01　　实验时间：2018.3.27

实验名称：利用 8 个发光二极管（LED）形成流水灯显示

班级：F1503006　学号：515030910141　姓名：翟拙存

1、实验平台

采用 Xilinx 公司的 FPGA 集成开发环境 Xilinx ISE Design Suite 10.1 sp3，实验开发板为 Xilinx Spartan-3E FPGA Starter Kit。

2、实验设计要求：

在 Spartan－3E FPGA Starter Kit Board 上有 8 个发光二极管（LED7 ～ LED0）。

使用开发板的全局时钟信号 CLK_50MHz，管脚为 P = C9。产生 1 Hz 的秒脉冲，每秒钟点亮一个 LED。

开始 8 个 LED 都为关闭状态（缺省值为：LEDOut = 8’b0000_0000）；即：

（0）LEDOut = 8’b0000_0000;

（1）LEDOut = 8’b0000_0001;

（2）LEDOut = 8’b0000_0011;

（3）LEDOut = 8’b0000_0111;

（4）LEDOut = 8’b0000_1111;

（5）LEDOut = 8’b0001_1111;

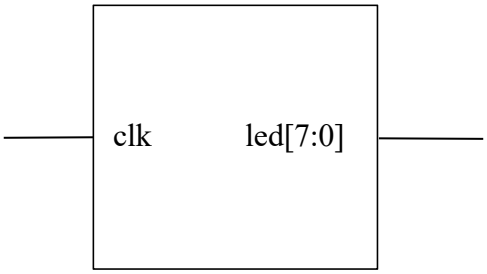
（6）LEDOut = 8’b0011_1111;

（7）LEDOut = 8’b0111_1111;

（8）LEDOut = 8’b1111_1111;

（9）不断重复（1）～（8）

3、模块设计框图



4、实验原理：

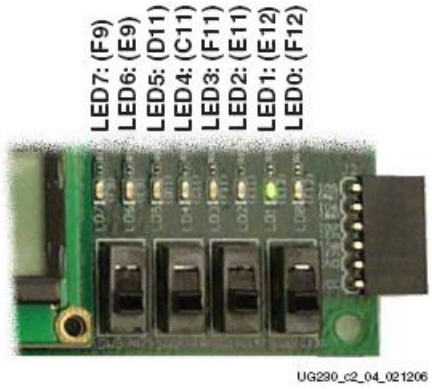
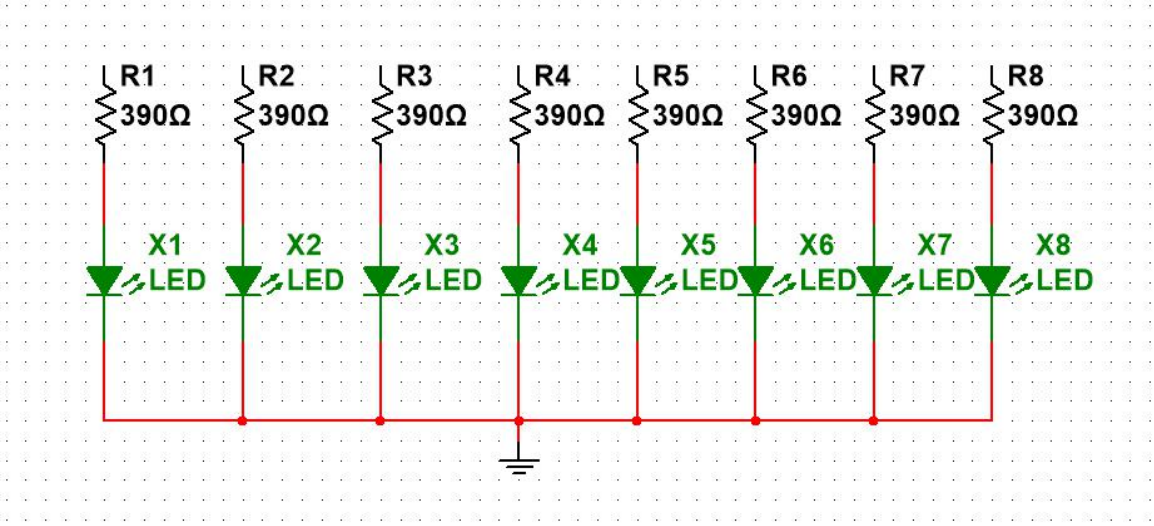


Figure 2-10: **Eight Discrete LEDs**



LED 一端接地，另一端通过 390 欧的限流电阻接到 Spartan-3E 上。要点亮一个 LED，向相应的控制位置高电平。

5、Verilog 模块设计

1. LED_Flowing.v:

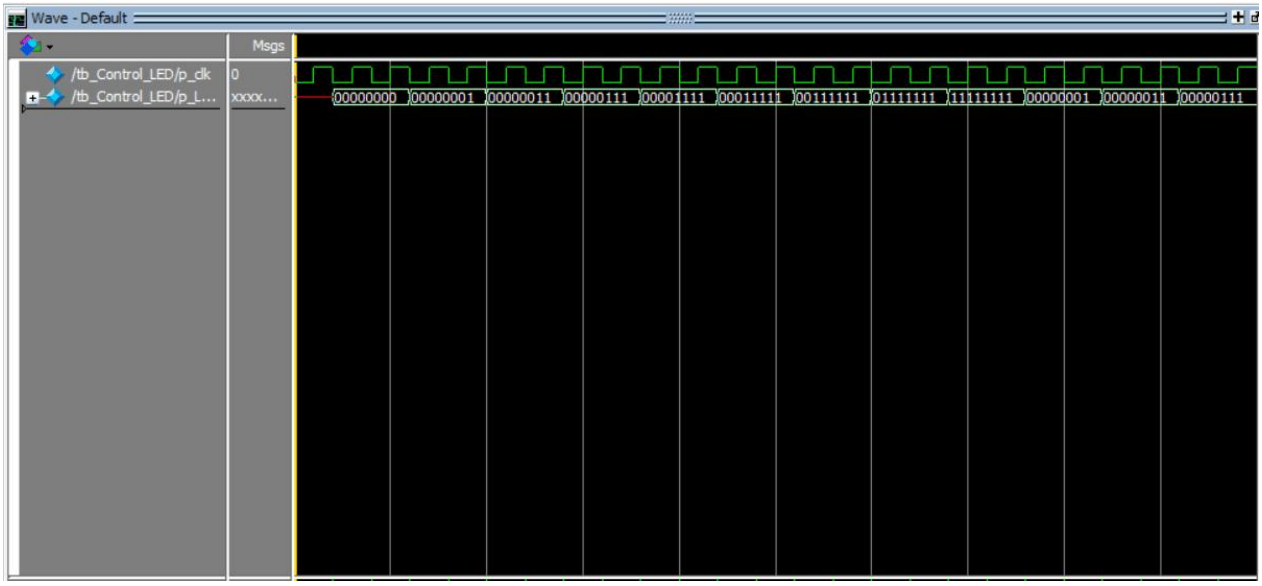
```
 module LEDflowing(
input clk,
output reg [7:0] led
);

 reg clk_1hz;
 reg [24:0] count;

 always @ (posedge clk)  // create a 1hz-clock from the provided 50mhz-clock
```

```
    begin
       if (count < 25'b1_0111_1101_0111_1000_0100_0000)
        // 25'b1_0111_1101_0111_1000_0100_0000 = 25000000
           count <= count+1;
       else
       begin
           count <= 0;
           clk_1hz <= ~clk_1hz;
       end
    end

    always @ (posedge clk_1hz)
    begin
       case(led)   // Finite State Machine
           8'b0000_0000: led<=8'b0000_0001;
           8'b0000_0001: led<=8'b0000_0011;
           8'b0000_0011: led<=8'b0000_0111;
           8'b0000_0111: led<=8'b0000_1111;
           8'b0000_1111: led<=8'b0001_1111;
           8'b0001_1111: led<=8'b0011_1111;
           8'b0011_1111: led<=8'b0111_1111;
           8'b0111_1111: led<=8'b1111_1111;
           8'b1111_1111: led<=8'b0000_0001;
           default: led <=8'b0000_0000;
       endcase
    end

Endmodule
```

2. LED_Flowing.ucf:

```
NET "clk" LOC = "C9" | IOSTANDARD = LVCMOS33 ;
NET "led[7]" LOC = "F9" | IOSTANDARD = LVTTL | SLEW = SLOW | DRIVE = 8 ;
NET "led<6>" LOC = "E9" | IOSTANDARD = LVTTL | SLEW = SLOW | DRIVE = 8 ;
NET "led<5>" LOC = "D11" | IOSTANDARD = LVTTL | SLEW = SLOW | DRIVE = 8 ;
NET "led<4>" LOC = "C11" | IOSTANDARD = LVTTL | SLEW = SLOW | DRIVE = 8 ;
NET "led<3>" LOC = "F11" | IOSTANDARD = LVTTL | SLEW = SLOW | DRIVE = 8 ;
NET "led<2>" LOC = "E11" | IOSTANDARD = LVTTL | SLEW = SLOW | DRIVE = 8 ;
NET "led<1>" LOC = "E12" | IOSTANDARD = LVTTL | SLEW = SLOW | DRIVE = 8 ;
NET "led<0>" LOC = "F12" | IOSTANDARD = LVTTL | SLEW = SLOW | DRIVE = 8 ;
```

6、试验仿真结果和分析



仿真结果显示，输出端形成以下循环：

（0）LEDOut = 8’b0000_0000;

（1）LEDOut = 8’b0000_0001;

（2）LEDOut = 8’b0000_0011;

（3）LEDOut = 8’b0000_0111;

（4）LEDOut = 8’b0000_1111;

（5）LEDOut = 8’b0001_1111;

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（7）LEDOut = 8’b0111_1111;

（8）LEDOut = 8’b1111_1111;

（9）不断重复（1）～（8）

满足实验要求。