Performance characterisation of 8-bit RISC and OISC architectures

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Introduction

This is a bunch of text for introductions that describes project, what it is about and that it compares RISC versus OISC architectures.

OISC

- Bunch of instructions
- Efficient instruction space
- Generally easy to use but damn to low number of registers.
- Needs optimisation.

OISC

OISC is fun. Some graphs here.

- Only one instruction
- Not so efficient instruction space
- Takes forever to write in assembly
- Takes no time to improve. It just asking for more data buses!