Pad Frame Information.

1 Introduction

IIT_Frame_PR.mag is a 40-pin pad frame with 38 bidirectional IO, one Vdd and one Gnd pads and a poly ring of dimensions 2900x2900 lambda sq. and 150 lambda wide.

The area of the entire frame is 5000x5000 lambda sq and 2994x2994 lambda sq is the available design area.

2 Connections to Pads

1. Input Pads: Connect OEN, DO to ground. DI and DIB follows Pad.
2. Output Pads: Connect OEN to VDD, DI to Ground. Pad follows DO.
3. Unused Pads: Connect OEN, DO and DI to ground.

DI and DO arc buffered I/O connections.

Use metal2 to connect pads to the design and metall to connect Vdd and Gnd to the design. Use metal2 on pads to attach labels to pads.

3 How to Simulate Your Design with Pad Frame?

To run Layout Verification by Simulation for the design inside a pad frame, do the following:

1. Copy all the pads and the pad frame to your directory. It is recommended that you create a separate directory for your final assembled layout. That is, keep the functionally-correct version of your project core in a separate directory and work on copy of it. Before sending designs for fabrication, you will have to simulate through the pads.
2. DO NOT alter the pads or the frame in any way (i.e. flip, rotate, etc.).
3. Insert your circuit using the :getcell command.
4. Connect the Gnd and Vdd rings and all the pads to your design.
5. Use metal2 over all the pads and label them accordingly.
6. Run :ext in Magic to create *Filename.ext* file.

7. Exit magic
8. Run ~/Scripts/iitcells_polyresfix *.ext on the extracted circuit.
9. Run ext2sim -TSCN3ME_SUBM.30 *Filename.ext*
11. Run ext2spice -TSCN3ME_SUBM.30 *Filename. ext*
12. Simulate and Verify.

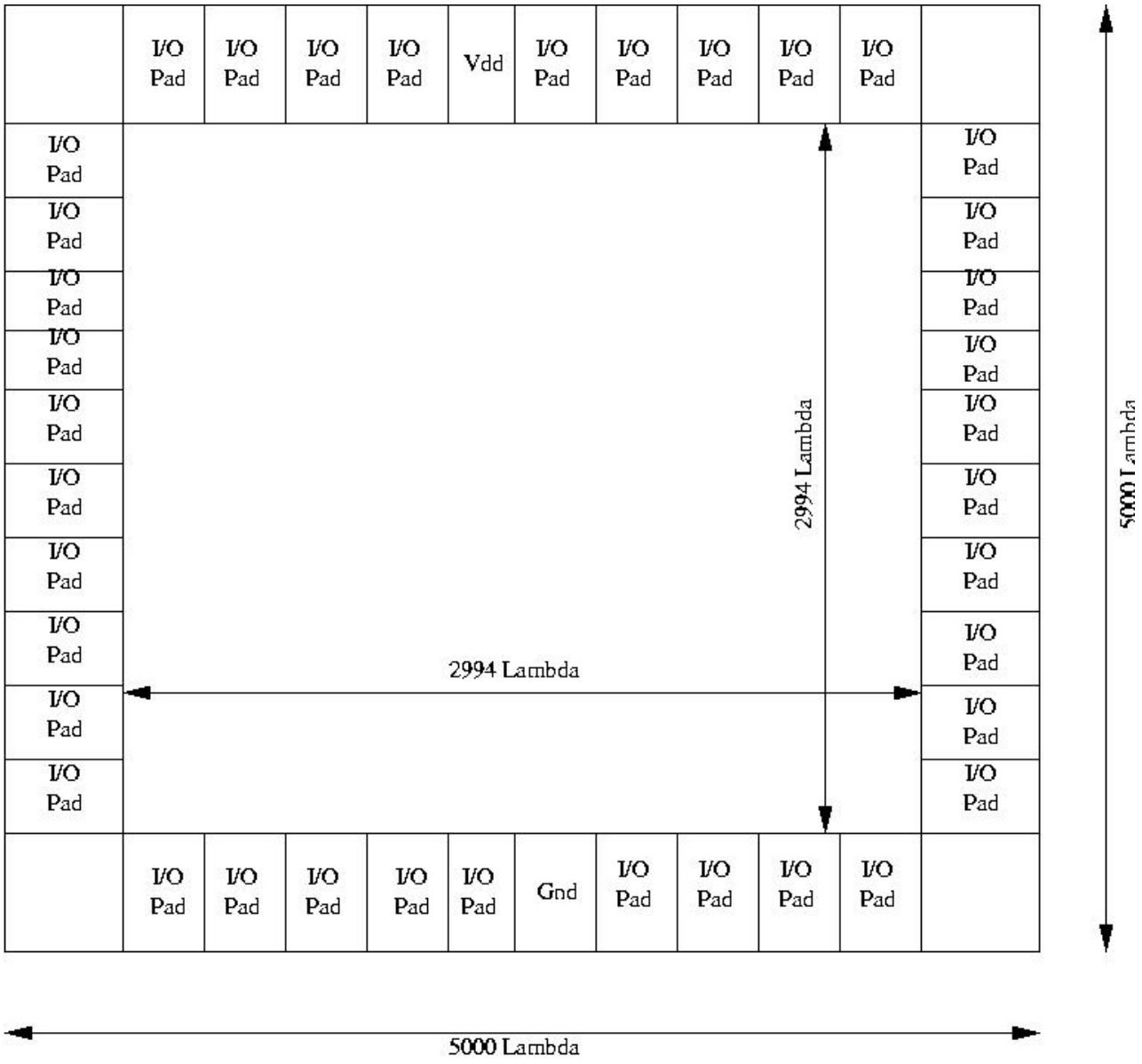
To obtain the final design for fab, proceed as follows:

1. Finish your design with the pad frame and flatten it using *:cif flat* command.
2. Reopen the design using Magic and use metal2 over pad rings and label them as you need.
3. Simulate and Verify as mentioned above.

4 Pad Diagram

The pad diagram for the supplied pad frame is as shown in the next page.

Tips: If any warning message occurs during extraction, flatten the design using *:cif flat* command and re-extract the design in Magic.


I/O Pad
Vdd
Gnd
2994 Lambda
2994 Lambda
5000 Lambda
5000 Lambda