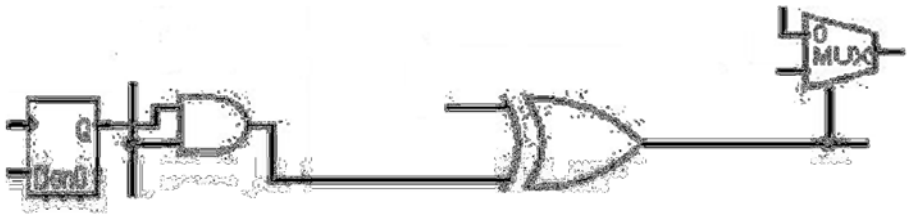
DELAY ESTIMATION USING THE DATASHEET

Given below is the sample delay calculation- the explanation is given below.

	AND			XOR-1			MUX-1			
	A	B	OUT	A	B	OUT	A	B	OUT-Pre	OUT1
Pin Cap(Rise)	0.0216	0.0214		0.0536	0.0536		0.032	0.032	0.036	-
Pin Cap(Fall)	0.0216	0.0215		0.0633	0.0637		0.032	0.032	0.036	-
Cout(Rise)			0.0536			0.0364				0.016
Cout(Fall)			0.0637			0.0364				0.016
Drv Strength(Rise)			1800			1600				1600
Drv Strength(Fall)			2210			1470				1470
T_r			0.0964			0.0582				0.026
T_f			0.1407			0.0535				0.024
Tp_{lh}		0.136		0.195	0.218		0.174	0.161	0.247	
Tp_{hl}		0.185		0.19	0.215		0.152	0.157	0.234	
Td(Avg)	0.151	0.1605		0.1925	0.2165	0.2165	0.163	0.159	0.2405	0.2405
$T_{d(Max)}$	0.167	0.185	0.185	0.195	0.218	0.218	0.174	0.161	0.247	0.247
			0.185			0.218				0.247

This is for a simple circuit where the AND gate output is connected to the input of an XOR gate, the output of the XOR gate is the select line of a mux. Note that we will be doing the estimate for the critical path.



Step 1: Fill in the pin cap for rise and fall in the table. This is given in the datasheet, which is the input capacitance.

Step 2: Check which input the output of the AND gate is driving. It is the input of XOR Gate, hence the out capacitance of the AND gate is the input capacitance of the XOR gate.

Step 3: Note down the drive strength of the gate under consideration. T_r and T_f filled in is equal to

(Drive Strength x Cout) / 1000

Step 4: Check the data sheet for finding Tp_{LH} and Tp_{HL}, AND gate will have four tables for determining this value. First check the table that shows the output switching from Low to High when the A input is changing,

(01A=>01Y) find the closest value to C_L= 0.0216 and Ts= 0.0964, the value you get is Tp_{LH}= 0.135, now check **(10A=>10Y),** C_L= 0.0216 and Ts= 0.1407, Tp_{HL} = 0.167

Step 5: Similarly fill in the value for B column also and take the maximum value of the delay into the column Tdmax

Step 6: after you add up the maximum delays of all the gates in the critical path, also add the setup time of the last flip flop and the Clock to Q delay of the first flipflop.