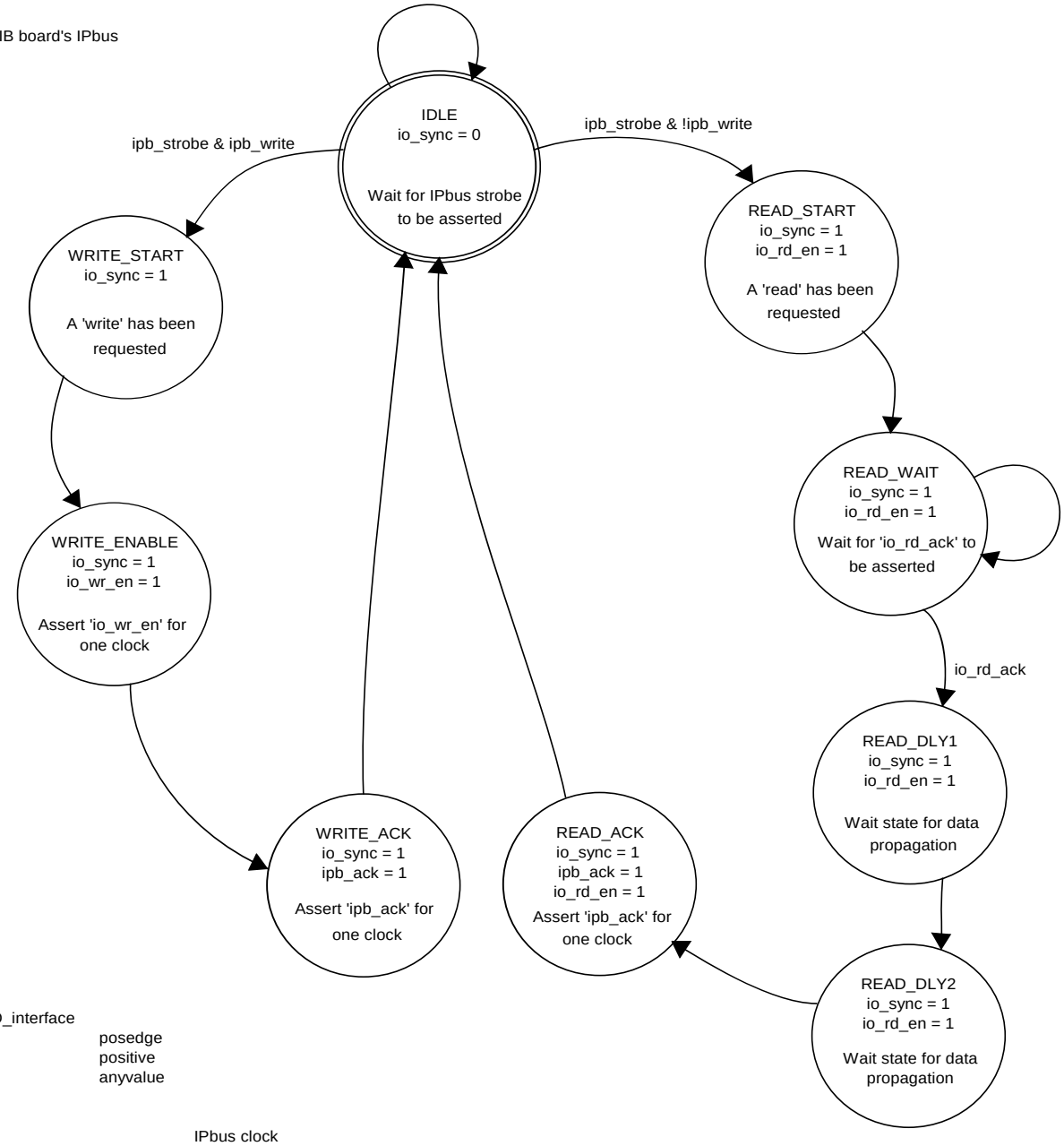
Interface between the GLIB board's IPbus
and the verilog 'io' bus



STATE MACHINE			
name	IPB_IO_interface		
clock	clk	posedge	
reset_signal	res	positive	
reset_state	IDLE	anyvalue	
implied_loopback	1		
INPUTS			
clk			IPbus clock
res			Global reset
ipb_strobe			IPbus strobe
ipb_write			IPbus write
io_rd_ack			verilog ack
OUTPUTS			
io_sync	1	comb	An operation is in progress
io_wr_en	0	comb	one cycle long write enable
ipb_ack	0	comb	one cycle long ack back to IPbus
io_rd_en	0	comb	full operation long read enable
STATES			
io_sync	1	output	An operation is in progress
io_wr_en	0	output	one cycle long write enable
ipb_ack	0	output	one cycle long ack back to IPbus
io_rd_en	0	output	full operation long read enable
TRANSITIONS			
equation	1	def_type	