Collaborate on the RISC-v platform standards

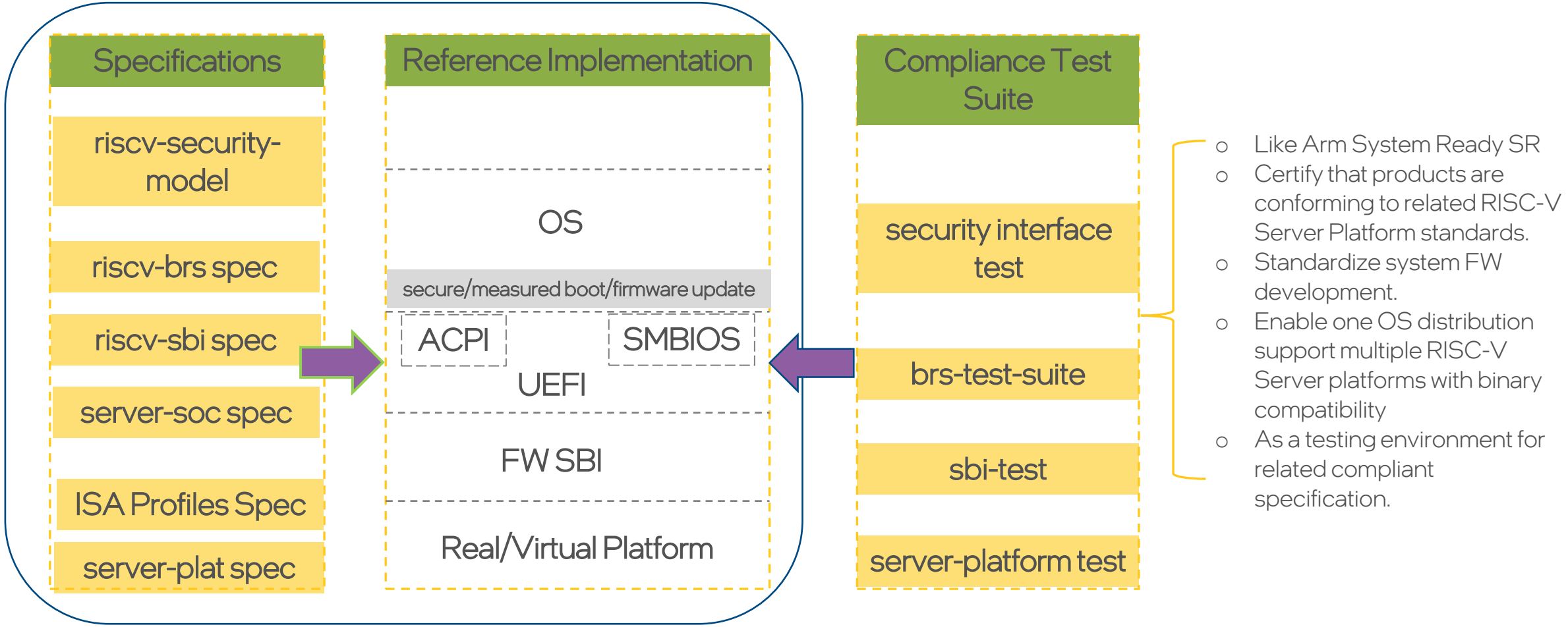
Agenda

- Problem Statement
- Standardize the Future RISC-V Server platform
- RISC-V Server Platform Spec
  - RISC-V ISA Profiles Spec
  - RISC-V BRS Spec
  - RISC-V SBI Spec
  - RISC-V Secure model spec
- Software Reference Implementation
- Compliance Test Suites
- Future Roadmap
- Call for action

Problem statement

- Diversity is a key feature for RISC-V, but server market has industry expectations that must be met:
  - Horizontally-integrated ecosystem (multiple Silicon players, OEMs/ODMs, integrators, OS vendors, VARs, etc), not vertical (one vendor does everything from nuts & bolts to sales & service).
  - Interoperability is a key requirement.
    - Just "another flavor" of server, like x86 and SystemReady SR (Arm). Cannot be too weird in terms of manufacture, deployment, support.
    - Must support single binary image OS distribution model (aka yesteryear's Debian ISO installs on next year's server).
    - Support for off-the-shelf hardware (e.g. PCIe), usual work flows (secure boot, network boot, management, monitoring, etc).
- Need well defined specifications for:
  - Interface between HW and FW
  - Interface between FW and OS
  - Security guarantees

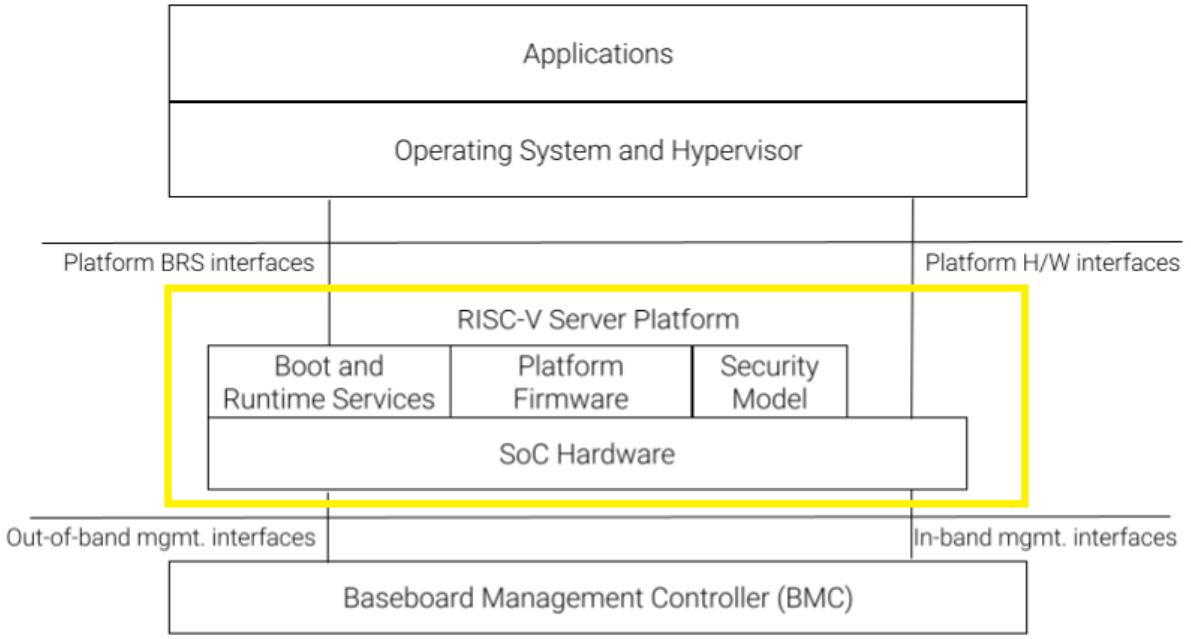
Standardize the future RISC-V Server platform



- Like Arm System Ready SR
- Certify that products are conforming to related RISC-V Server Platform standards.
- Standardize system FW development.
- Enable one OS distribution support multiple RISC-V Server platforms with binary compatibility
- As a testing environment for related compliant specification.

RISC-V Server Platform Spec

- Defined by the RISC-V Server Platform TG
- Specify a standardized set of hardware and software capabilities, that portable system software, such as operating systems and hypervisors, can rely on being present in a RISC-V server platform.
- https://github.com/riscv-non-isa/riscv-server-platform



Components of a RISC-V Server Platform

RISC-V Server Platform Spec

- Server Platform Hardware Requirements
  - RISC-V Harts must support RVA23 ISA Profiles Spec and extra extensions
    - Sv48/Sv48x4/Svadu/H/Sdtrig/Sdext/Sscofpmf/Zkr/Ssctr/Ssecorrupt/Ssccfg
  - RISC-V SoC must comply to the RISC-V Server SoC Spec
  - Peripherals
    - UART/USB/SATA/RTC Capabilities
- Server Platform Firmware Requirements
  - Comply to BRS-I recipe defined in RISC-V BRS Spec
- Server Platform Security Requirements
  - RoT/boot flow requirements will come from the RISC-V Platform Security Model Spec

RISC-V ISA Profiles Spec

- Defined by the RISC-V Profiles TG and specify small common set of ISA extensions that capture the most value for most users.
  - Enable the software community to focus resources on building a rich software ecosystem with application and operating system portability across different implementations
- Each profile is built on a standard base ISA plus a set of mandatory ISA extensions and provides a small set of optional ISA extensions to extend the mandatory components.
- RVA23 profile include RVA23U64 and RVA23S64
  - RV64I is the mandatory base ISA
  - MAFDC/Zicsr/Zicnt etc. are mandatory extensions
  - Zvkng/Zvksg/Zacas/Zvbc/Zfh/Zbc/Zvfh are optional extensions
- https://github.com/riscv/riscv-profiles

RISC-V Server SoC Spec

- Defined by the RISC-V Server SoC TG and specify a standardized set of hardware capabilities that portable system software such as operating systems and hypervisors can rely on being present in a RISC-V server SoC.
  - Clocks and Timers requirements
    - Constant Freq in a unit of 1 ns/CSR updated at least 100MHz
  - Interrupt Controllers requirements
    - AIA/MSI for external IRQ/S-mode and VS-mode interrupt file etc.
  - IOMMU requirements
    - Must support RISC-V IOMMU Spec
    - DMA capable peripherals/PCIe root port must be governed by an IOMMU
  - PCIe subsystem requirements
    - Root complex with RCEC/RCRB/RCiEP/Root Port etc.
- https://github.com/riscv-non-isa/server-soc

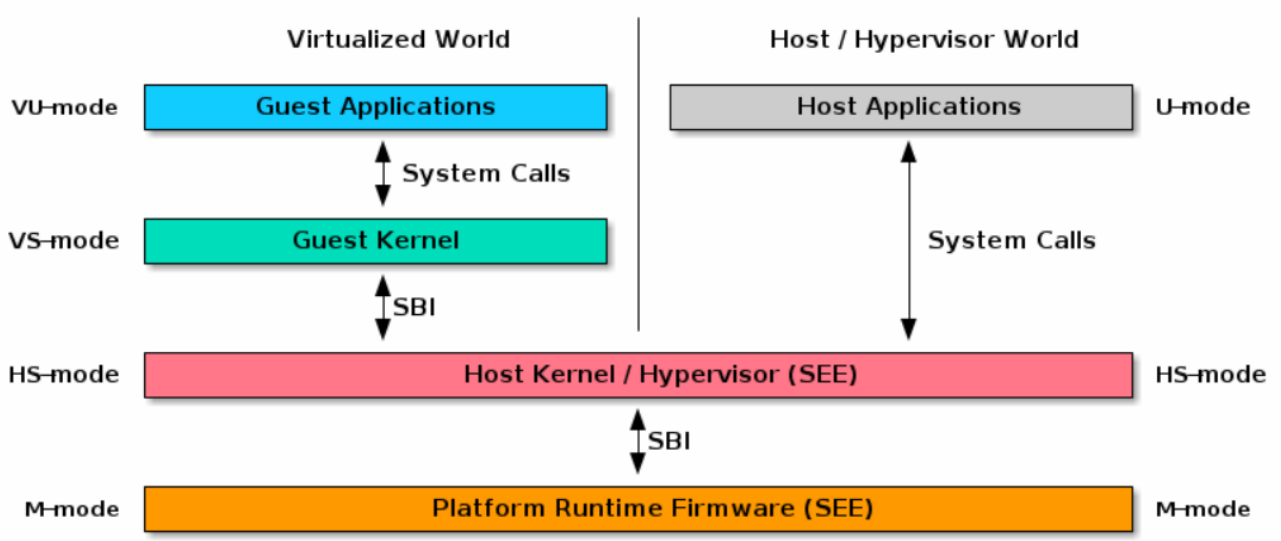
RISC-V BRS Spec

- Defined by the RISC-V BRS TG and specify the Boot and Runtime Services requirements for firmware on a RISC-V platform.
- Include two recipes: BRS-I(Interoperable) and BRS-B(Bespoke)
- BRS-I aims to ensure interoperability between different RISC-V platforms and OS/Hypervisor.
  - Hart requirements (>= RVA20S64)
  - SBI requirements (RISC-V Supervisor Binary Interface Spec v2.0 or later)
    - HSM is mandated, TIME/IPI/RFNC/PMU are conditionally required
  - UEFI requirements (>= UEFI 2.10/64 bits/Address Translation)
    - Security, I/O, Runtime Services, Firmware Update
  - ACPI requirements (>= ACPI 6.6/64 bits/hardware reduced mode)
    - ACPI Tables/Methods/Objects/IDs/DSD
  - SMBIOS requirements (>= SMBIOS 3.7.0, Structure Type 02/03 …)
- https://github.com/riscv-non-isa/riscv-brs

RISC-V SBI Spec (BRS dependency)

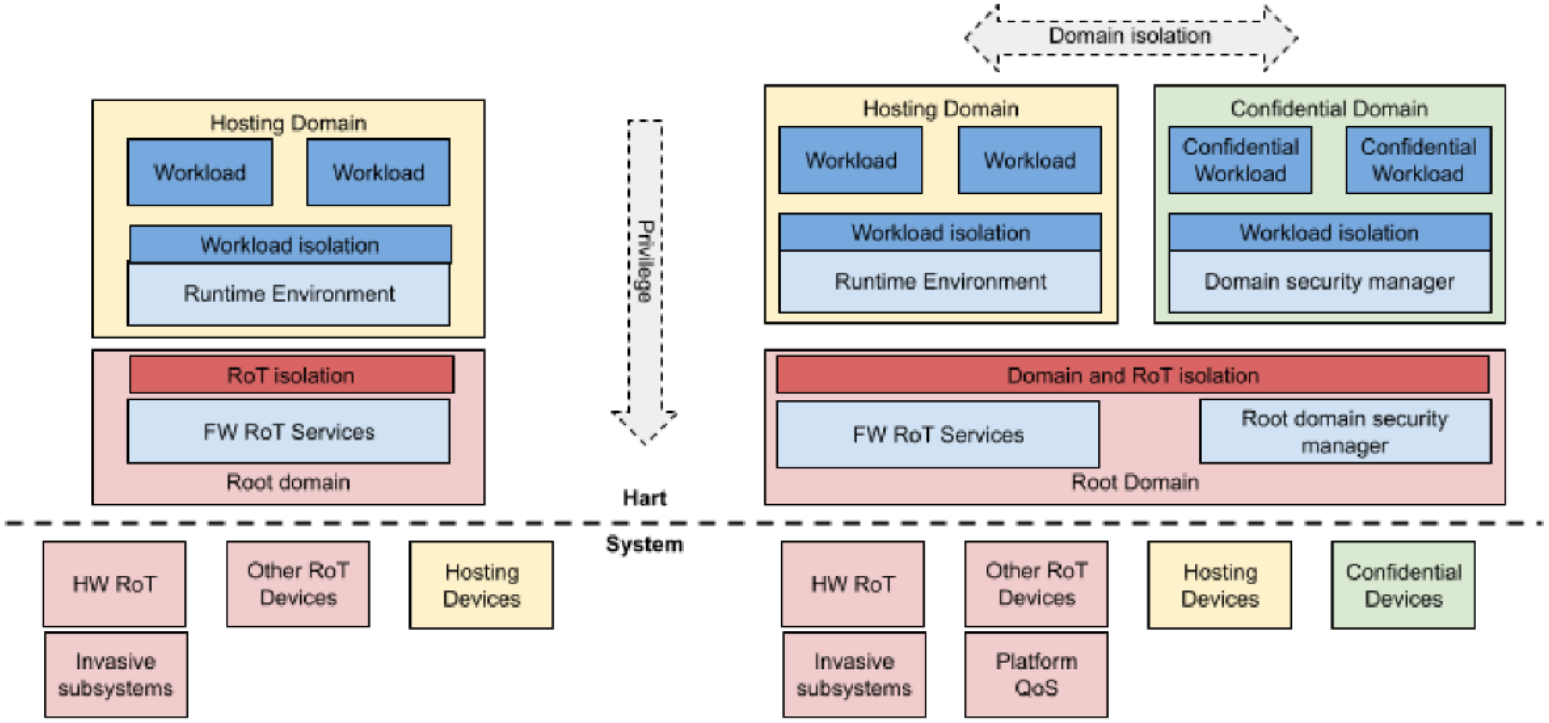
- Defined by the RISC-V PRS TG and specify Supervisor Binary Interface which allows supervisor-mode (S-mode or VS-mode) software to be portable across all RISC-V implementations by defining an abstraction for platform (or hypervisor) specific functionality.
- https://github.com/riscv-non-isa/riscv-sbi-doc

- An SBI extension defines a set of SBI functions which provides a particular functionality to supervisor-mode software.
  - HSM - Hart start/stop
  - SRST - System reset
  - ...



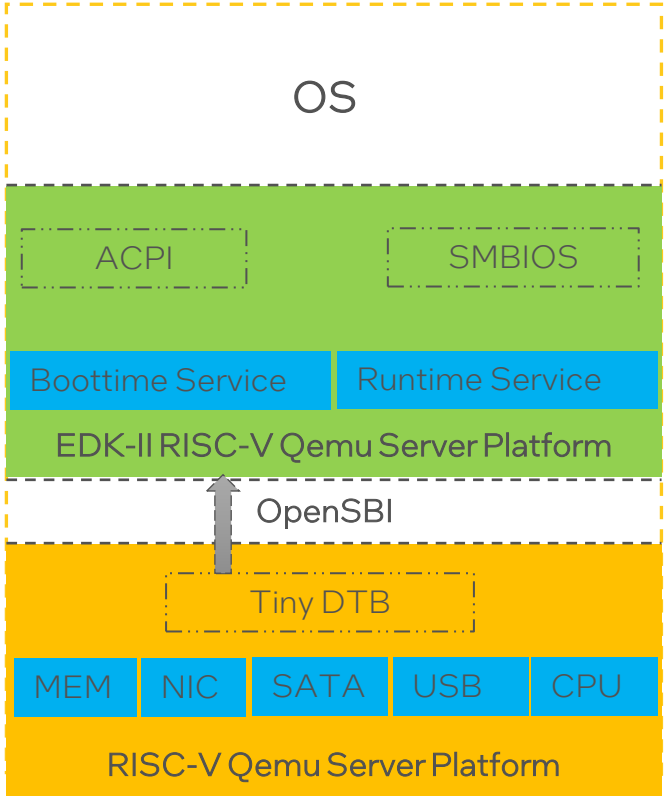
RISC-V Platform Security Model Spec

- Defined by the RISC-V Security Model TG and aims to provide guidelines for how RISC-V security building blocks can be used to build secure system.
- https://github.com/riscv-non-isa/riscv-security-model



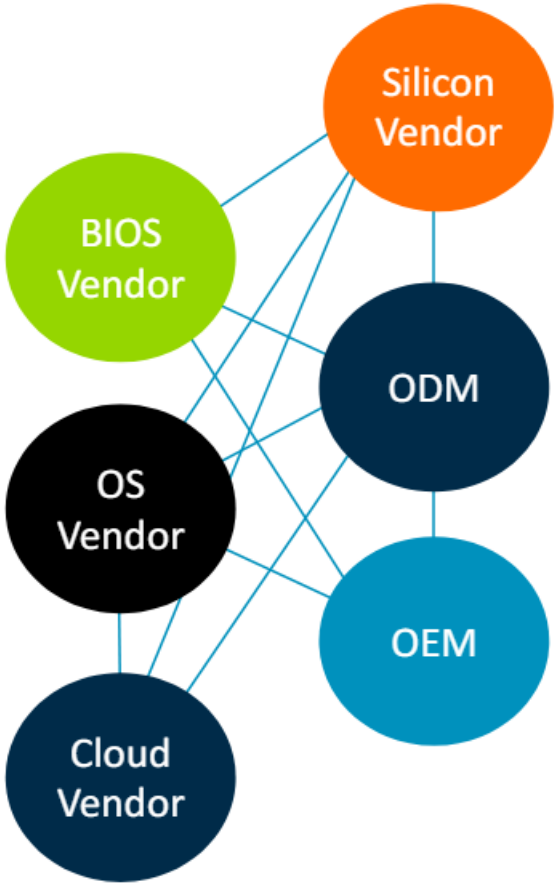
RISC-V Server Platform Reference Implementation

- Qemu RISC-V Server Platform Machine
  - Qemu virt machine based on RISC-V Server Platform Spec
  - Basic server platform devices(SATA/USB/NIC etc.)
  - No virtio/fw_cfg devices
  - No ACPI/SMBIOS tables generation
  - Serve as a test bed for CTS/FW development and test
- EDK-II RISC-V Qemu Server Platform
  - UEFI implementation for Qemu Server Platform Machine
  - Following RISC-V BRS-I Spec
  - Basic device drivers(SATA/USB/NIC etc.)
  - Provide ACPI/SMBIOS tables
  - A reference implementation for Server Platform FW

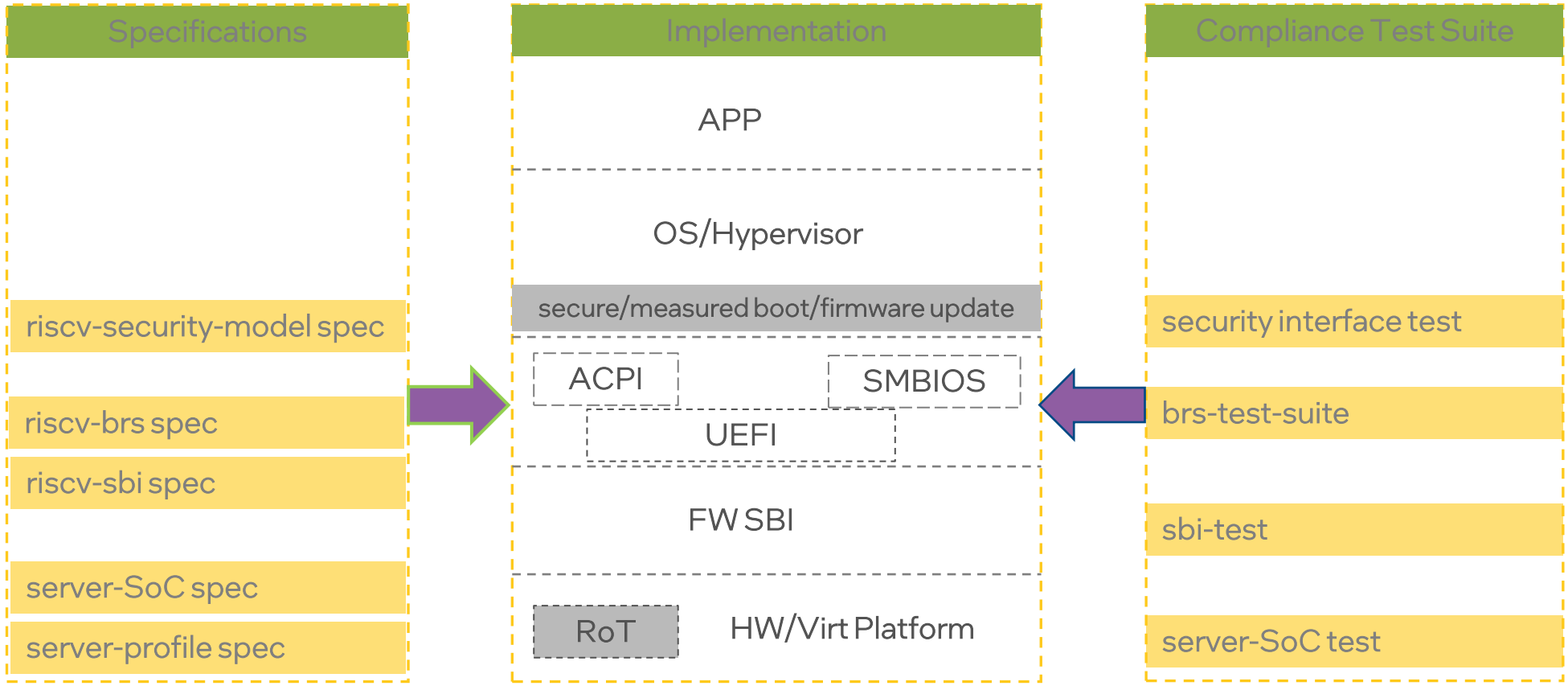


RISC-V Server Platform Compliance Test Suite

- Server segment is complex and has many players
- OSV can't verify their products on every system
- But a Test Suite can help one vendor verify the service provided by another
  - OEM can verify Silicon vendor HW was compliant with RISC-V Server SoC Spec
  - OSV can verify ODM was compliant with RISC-V Server SoC and BRS Spec
- No specification without verification
- The approach is through the compliance test by leveraging industry standards as well as RISC-V specifications

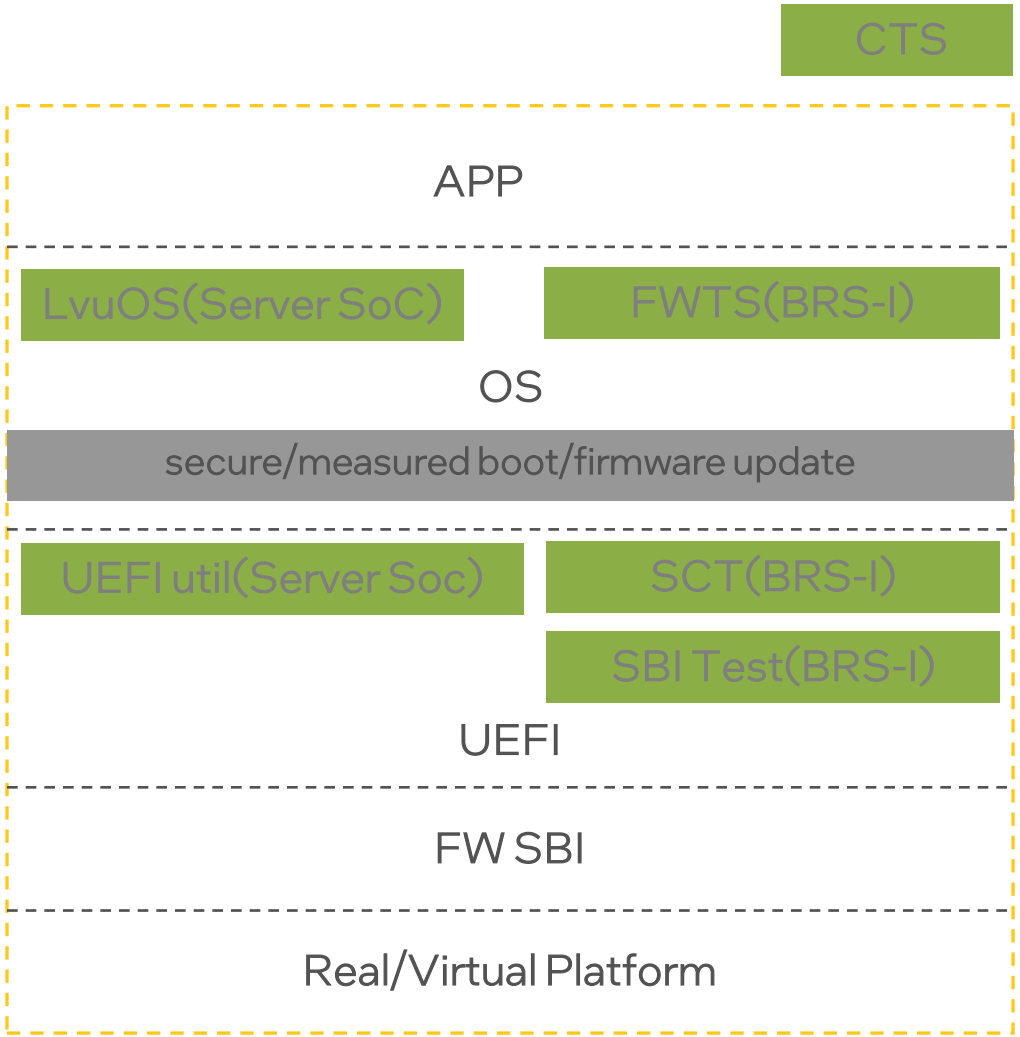


RISC-V Server Platform Compliance Test Suite

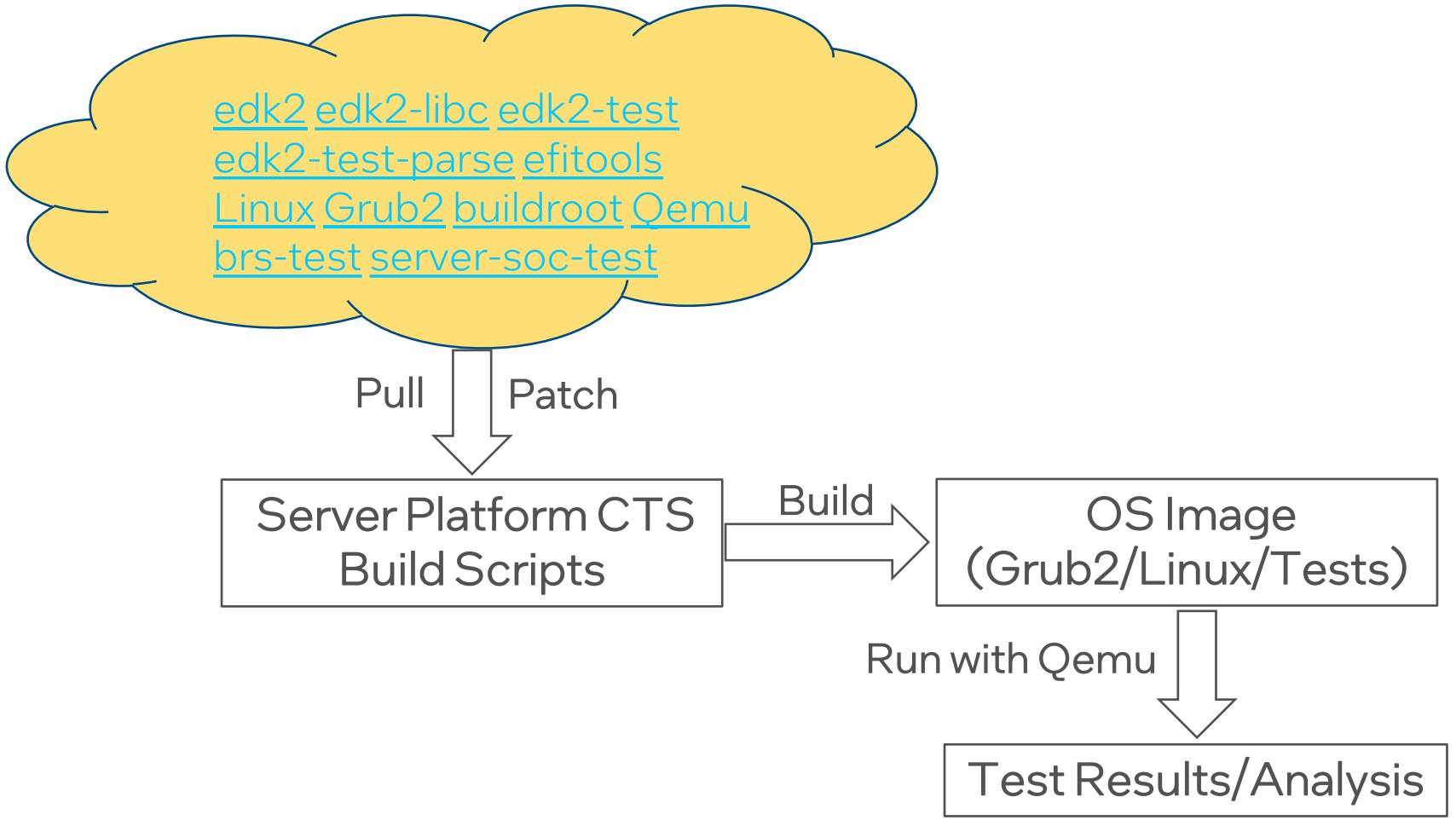


RISC-V Server Platform Compliance Test Suite

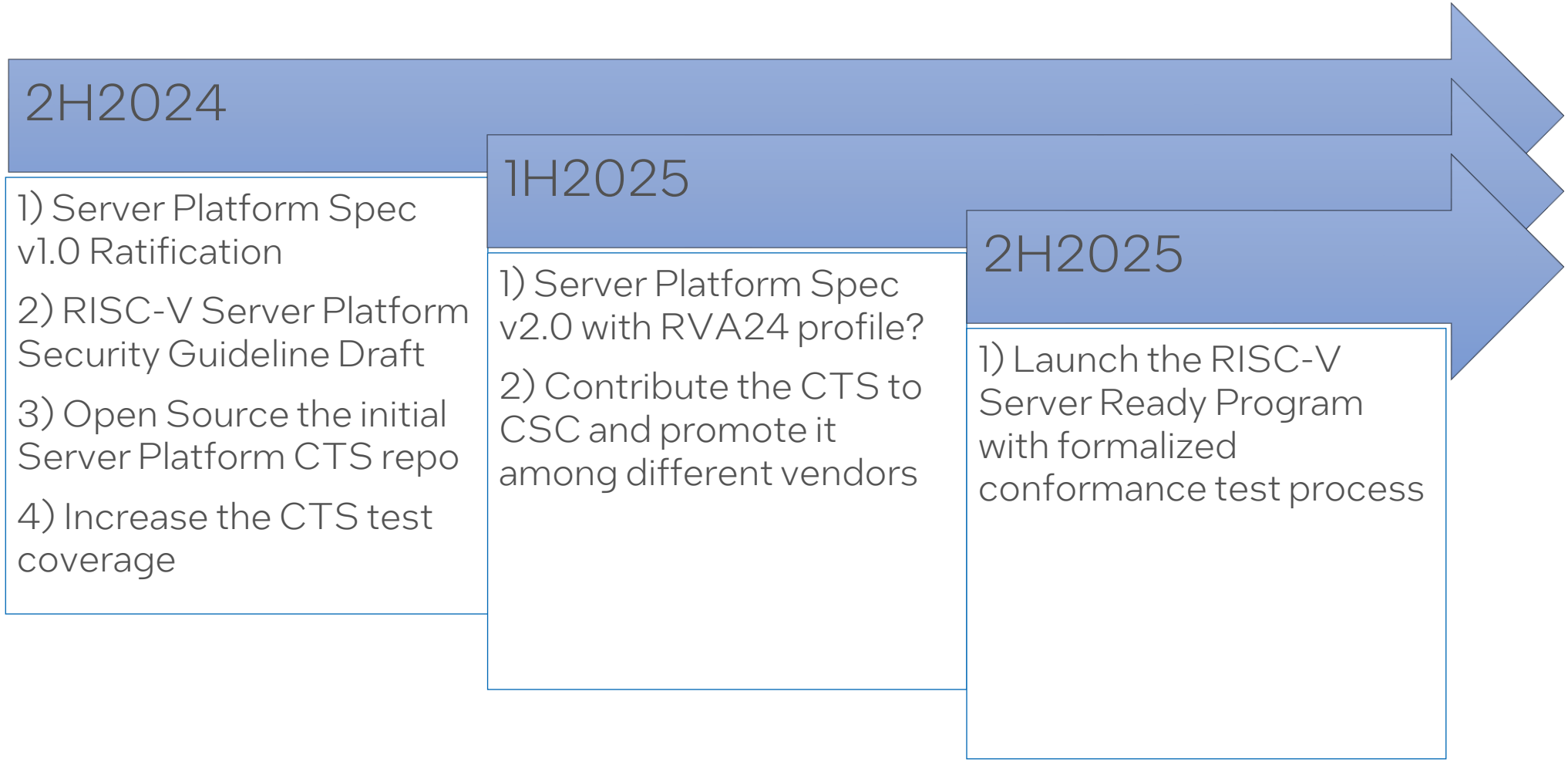
- Lvu and UEFI util verify hardware requirements of Server SoC Spec
  - Hart Profile
  - AIA/IOMMU
  - PCIe
- FWTS/SCT and SBI test verify FW requirements of BRS-I
  - SBI
  - UEFI
  - ACPI
  - SMBIOS
- Secure/measured boot and FW update was verified in FWTS



RISC-V Server Platform Compliance Test Suite



Future Roadmap



Call for action

- Review and provide feedbacks on RISC-V server-platform Spec
- Vendors'(SoC/OS/FW etc.) review and testing
- Work on Qemu machine for RISC-V Server Platform
- Contribute to increase CTS test coverage
  - BRS test suite
  - Server SoC test suite
  - Security Interface test suite (ref Arm BBSR test)
  - SBI APIs test suite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