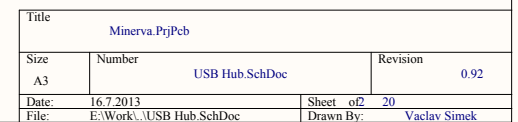
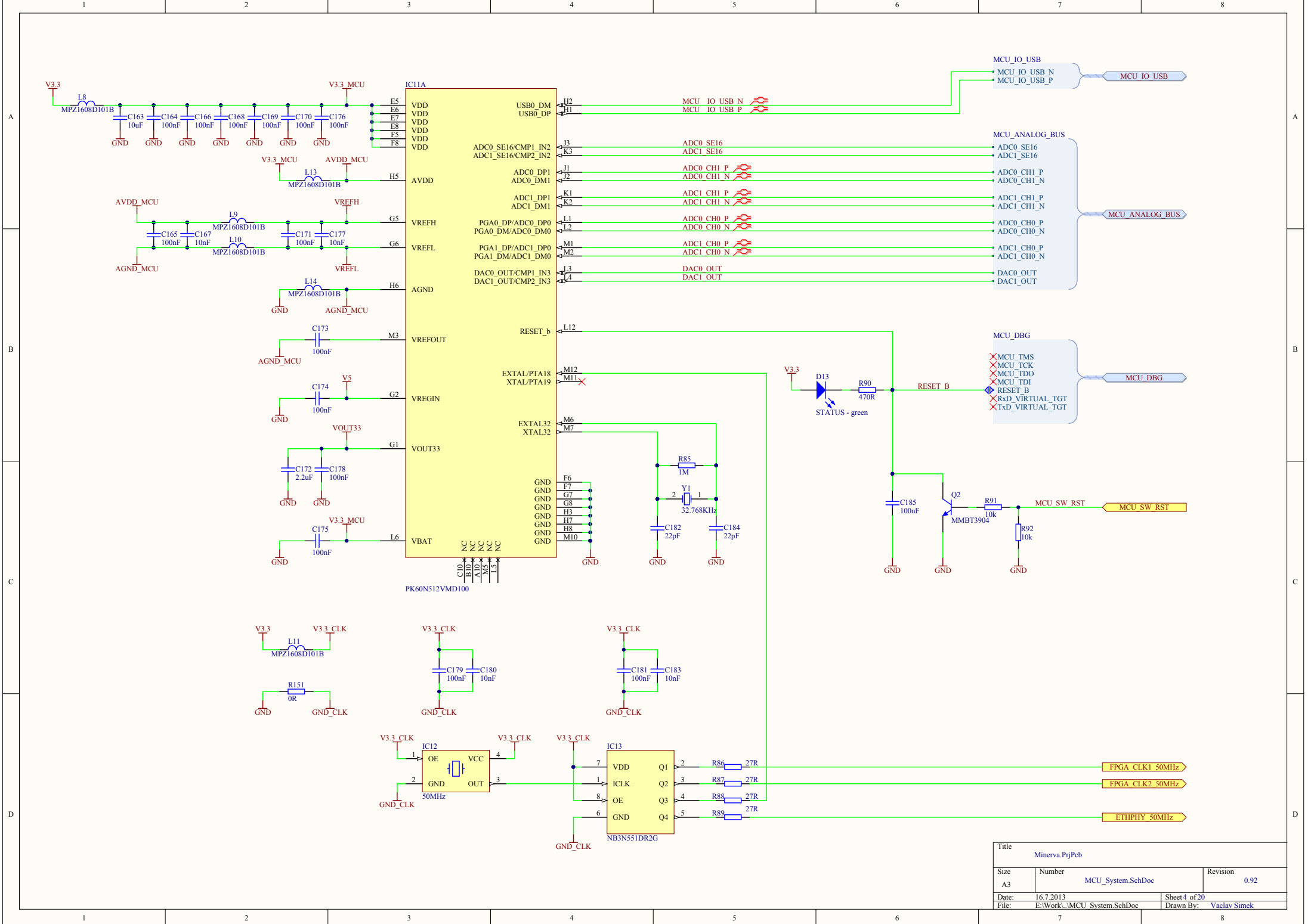
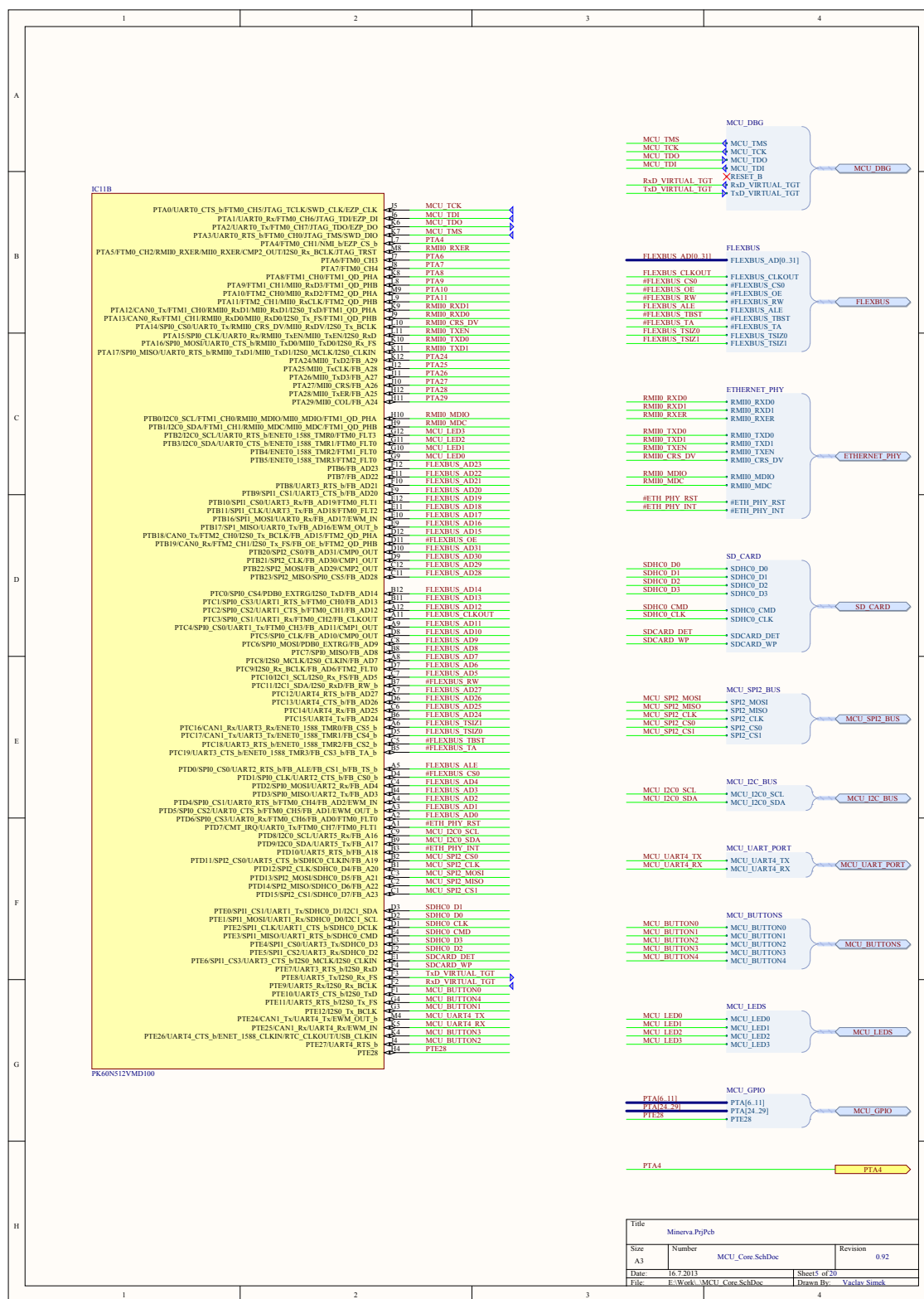
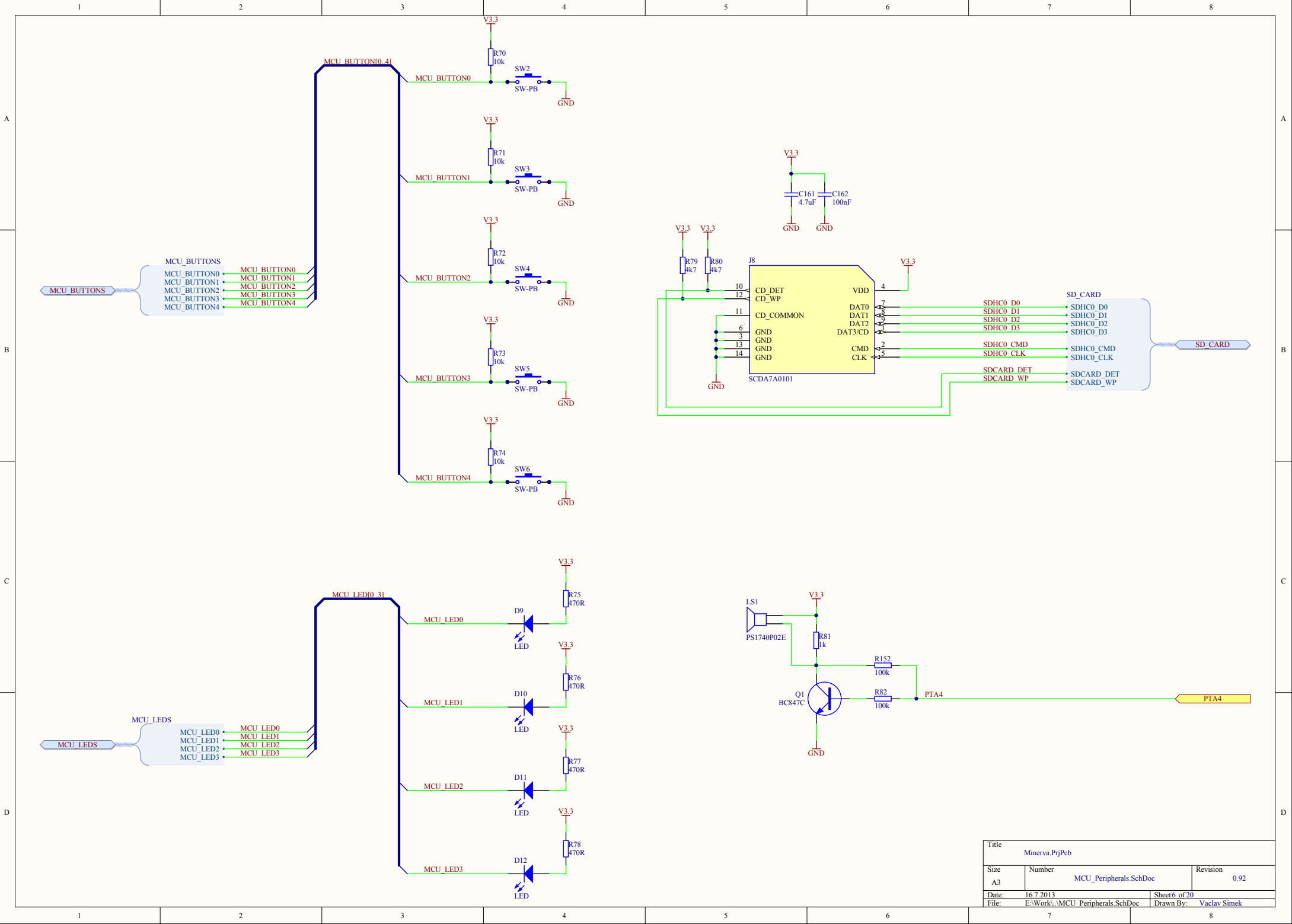


Title			Minerva.PtjPcb
Size	Number	Revision	
A3	Minerva.SchDoc	0.92	
Date:	16.7.2013	Sheet 1 of 20	
File:	E:\Work\Minerva.SchDoc	Drawn By: Vaclav Simek	









A

B

C

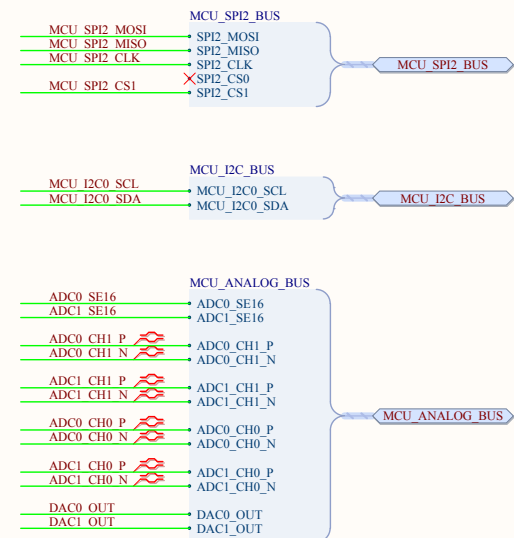
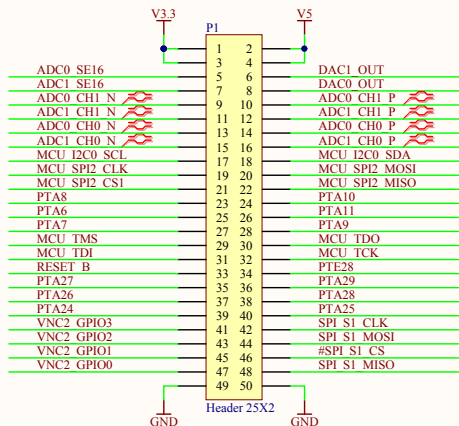
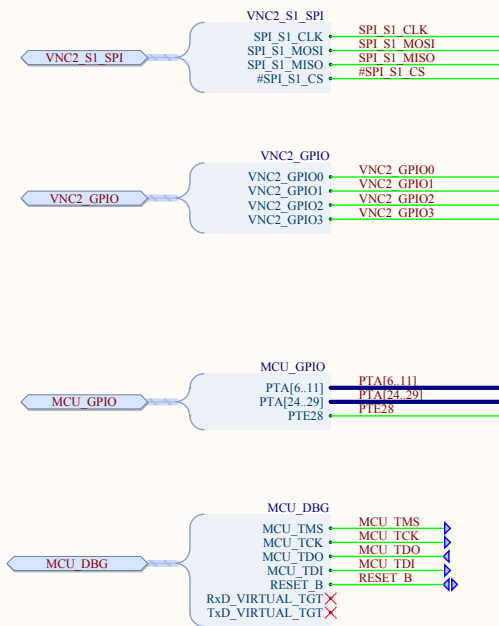
D

A

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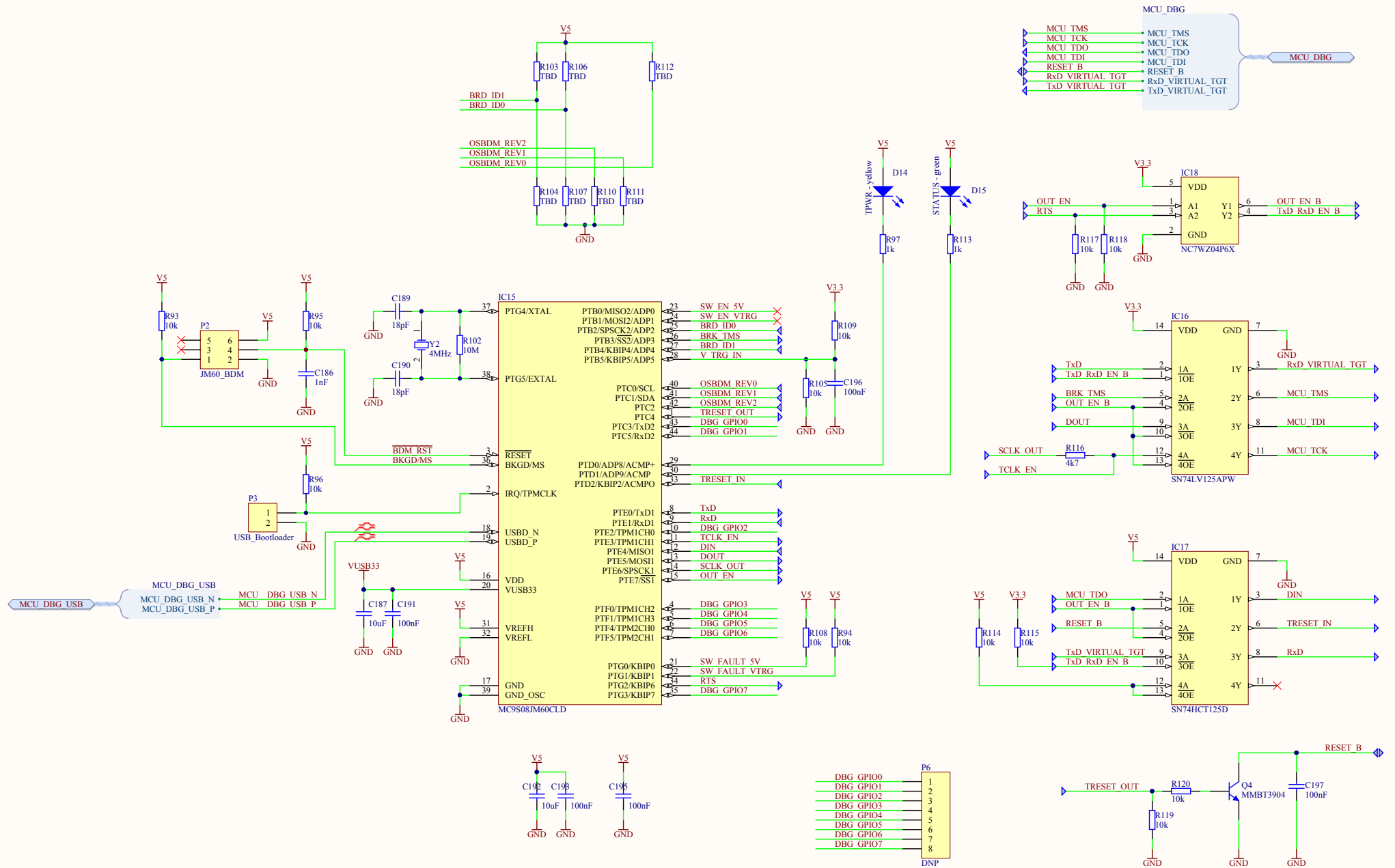
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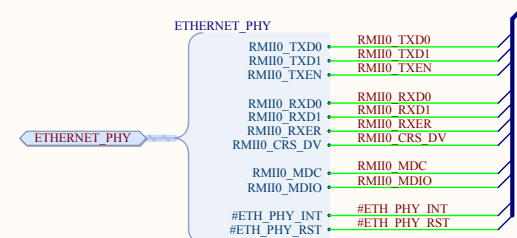
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Size	Number	Revision	0.92
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Date:	16.7.2013	Sheet 7 of 20	
File:	E:\Work\MCU_Expansion.SchDoc	Drawn By:	Vaclav Simek

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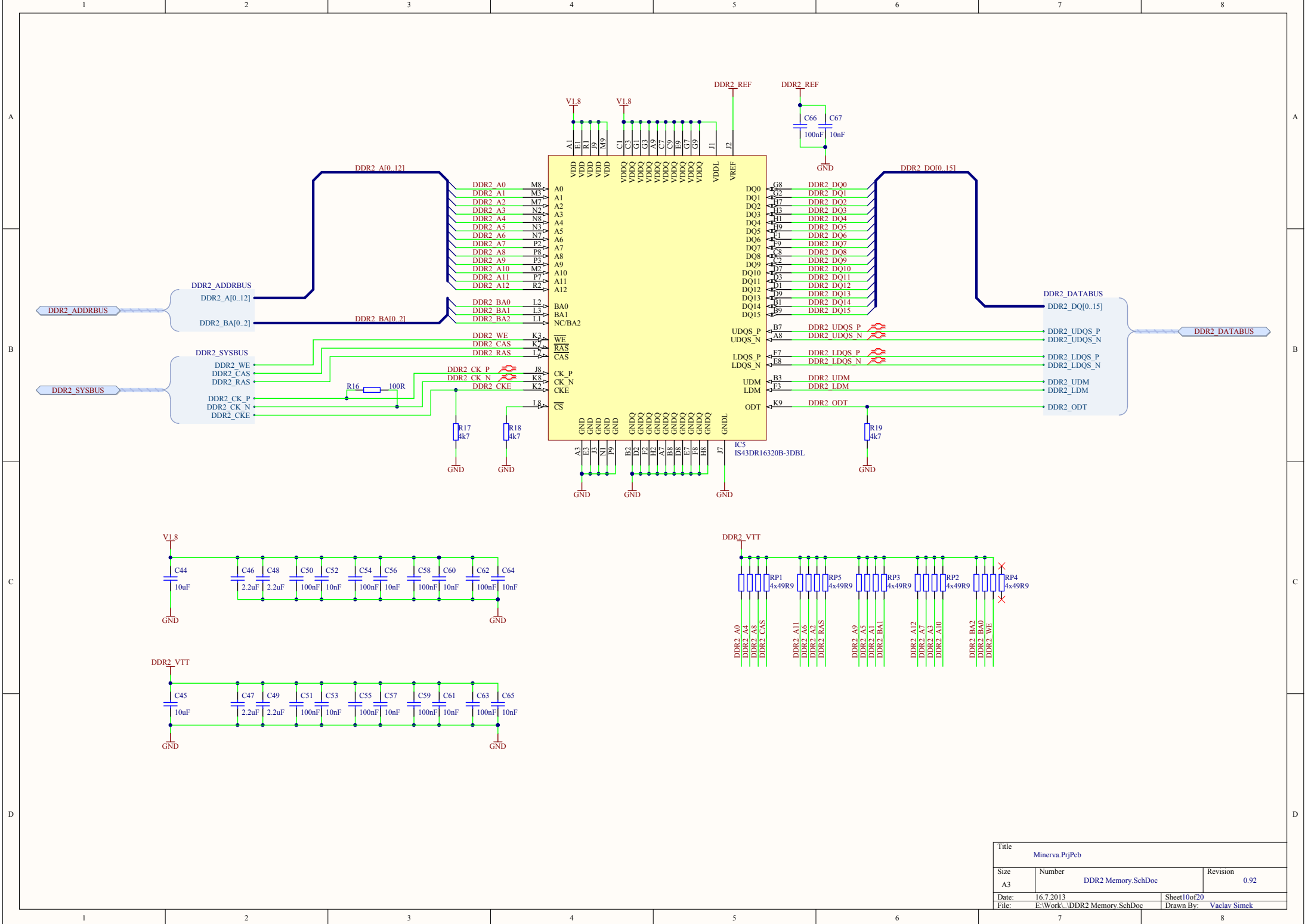
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Title Minerva.PrjPcb			
Size A3	Number MCU Debug.SchDoc	Revision 0.92	
Date: 16.7.2013	Sheet 8 of 20		
File: E:\Work\1.MCU Debug.SchDoc	Drawn By: Václav Simek		



Title Minerva.PrjPcb		
Size A3	Number Ethernet PHY_SchDoc	Revision 0.92
Date: 16.7.2013	Sheet9 of 20	
File: E:\Work\Ethernet PHY_SchDoc	Drawn By:	Vaclav Simek



1

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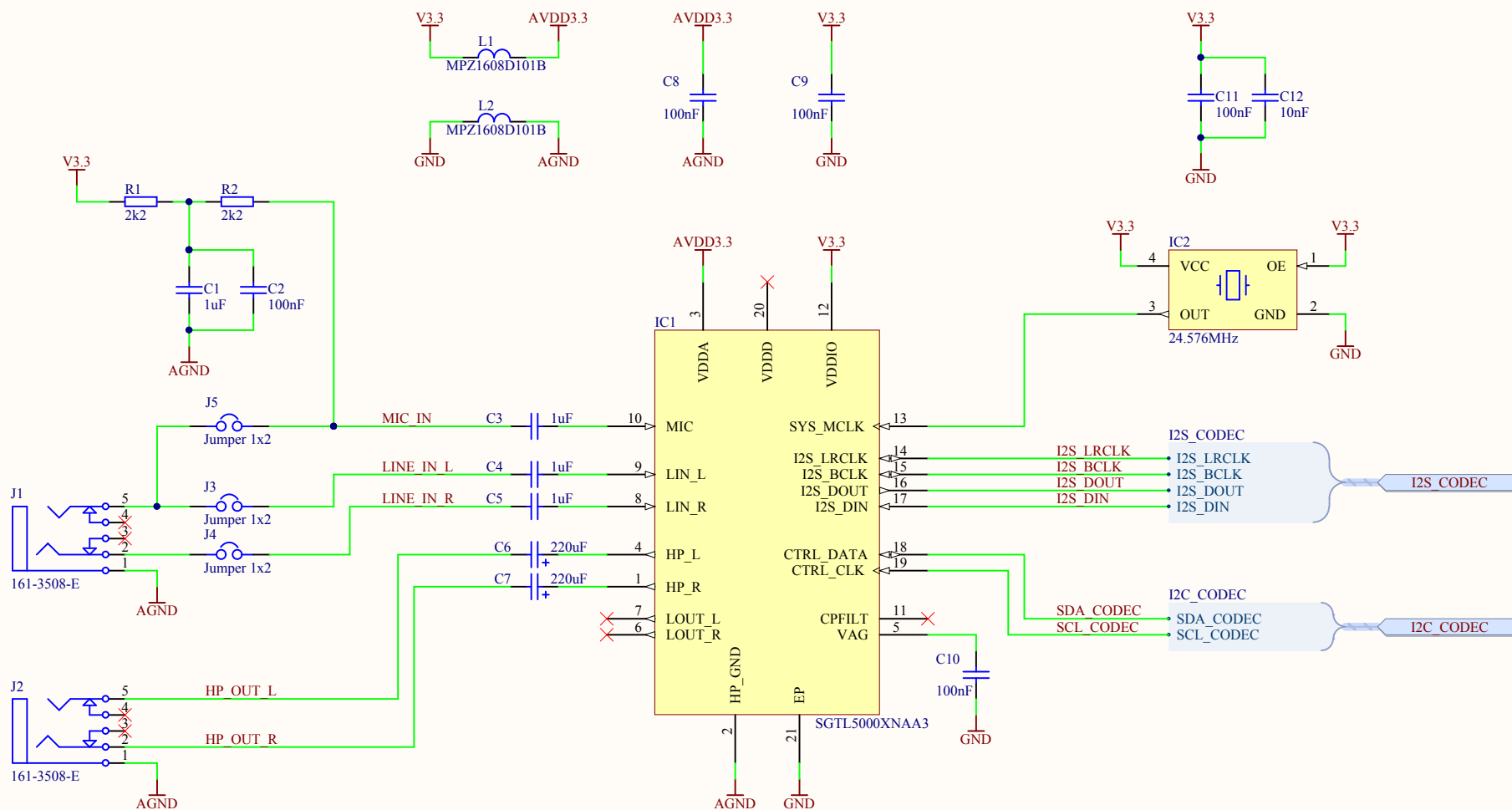
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D



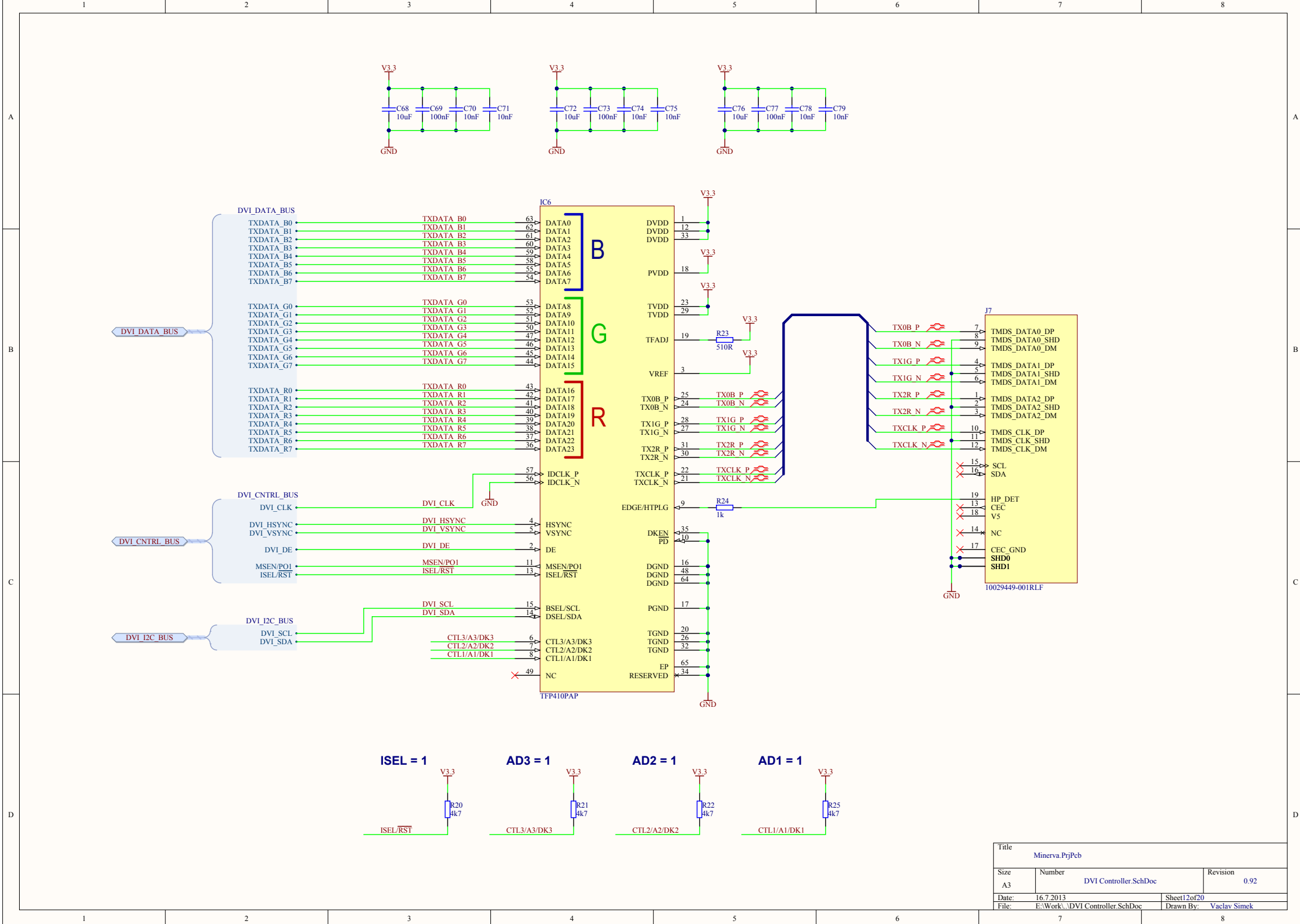
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Size	Number	Revision	
A4	Audio CODEC.SchDoc	0.92	
Date:	16.7.2013	Sheet 1 of 20	
File:	E:\Work\...\Audio CODEC.SchDoc	Drawn By: Vaclav Simek	

1

2

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4



IC9A

BANK 0

IO_L1P_HSWAPEN_0	D4	FLEXBUS AD17
IO_L1N_VREF_0	C4	FLEXBUS AD22
IO_L2P_0	A2	FLEXBUS AD23
IO_L2N_0	D6	FLEXBUS AD29
IO_L3P_0	C6	FLEXBUS AD30
IO_L3N_0	B3	FLEXBUS AD20
IO_L4P_0	A3	FLEXBUS AD21
IO_L4N_0	B4	FLEXBUS AD18
IO_L5P_0	A4	FLEXBUS AD19
IO_L5N_0	C5	FLEXBUS AD15
IO_L6P_0	A5	FLEXBUS AD16
IO_L6N_0	B6	FLEXBUS AD31
IO_L8P_0	A6	#FLEXBUS OE
IO_L8N_VREF_0	C7	FLEXBUS AD28
IO_L10P_0	A7	FLEXBUS AD14
IO_L10N_0	D8	MCU I2C0 SDA
IO_L11P_0	C8	FLEXBUS AD13
IO_L11N_0	B8	FLEXBUS AD12
IO_L33P_0	A8	FLEXBUS AD10
IO_L33N_0	D9	FLEXBUS CLKOUT
IO_L34P_GCLK19_0	C9	MCU I2C0_SCL
IO_L34N_GCLK18_0	B9	FLEXBUS AD9
IO_L35P_GCLK17_0	A9	FLEXBUS AD6
IO_L35N_GCLK16_0	D11	FLEXBUS AD27
IO_L36P_GCLK15_0	C11	FLEXBUS AD24
IO_L36N_GCLK14_0	C10	FLEXBUS AD26
IO_L37P_GCLK13_0	A10	FLEXBUS AD5
IO_L37N_GCLK12_0	G9	FLEXBUS AD11
IO_L38P_0	F9	FLEXBUS AD8
IO_L38N_VREF_0	B11	FLEXBUS AD25
IO_L39P_0	A11	FLEXBUS TSIZ0
IO_L39N_0	B12	FLEXBUS AD7
IO_L41P_0	A12	#FLEXBUS RW
IO_L41N_0	B14	#FLEXBUS CS0
IO_L62P_0	A14	#FLEXBUS TBST
IO_L62N_VREF_0	F13	FLEXBUS ALE
IO_L63P_SCP7_0	E13	FLEXBUS TSIZ1
IO_L63N_SCP6_0	C15	FLEXBUS AD1
IO_L64P_SCP5_0	A15	FLEXBUS AD4
IO_L64N_SCP4_0	D14	FLEXBUS AD3
IO_L65P_SCP3_0	C14	#FLEXBUS TA
IO_L65N_SCP2_0	B16	FLEXBUS AD0
IO_L66P_SCP1_0	A16	FLEXBUS AD2
IO_L66N_SCP0_0		

XC6SLX9-2CSG324C

V3.3

R46

DNP

R47

4k7

GND

FLEXBUS

FLEXBUS_AD[0..31]

FLEXBUS_AD[0..31]

FLEXBUS_CLKOUT

FLEXBUS_CLKOUT

#FLEXBUS_CS0

#FLEXBUS_CS0

#FLEXBUS_OE

#FLEXBUS_OE

#FLEXBUS_RW

#FLEXBUS_RW

FLEXBUS_ALE

FLEXBUS_ALE

#FLEXBUS_TBST

#FLEXBUS_TBST

#FLEXBUS_TA

#FLEXBUS_TA

FLEXBUS_TSIZ0

FLEXBUS_TSIZ0

FLEXBUS_TSIZ1

FLEXBUS_TSIZ1

FLEXBUS

MCU_I2C_BUS

MCU_I2C0_SCL

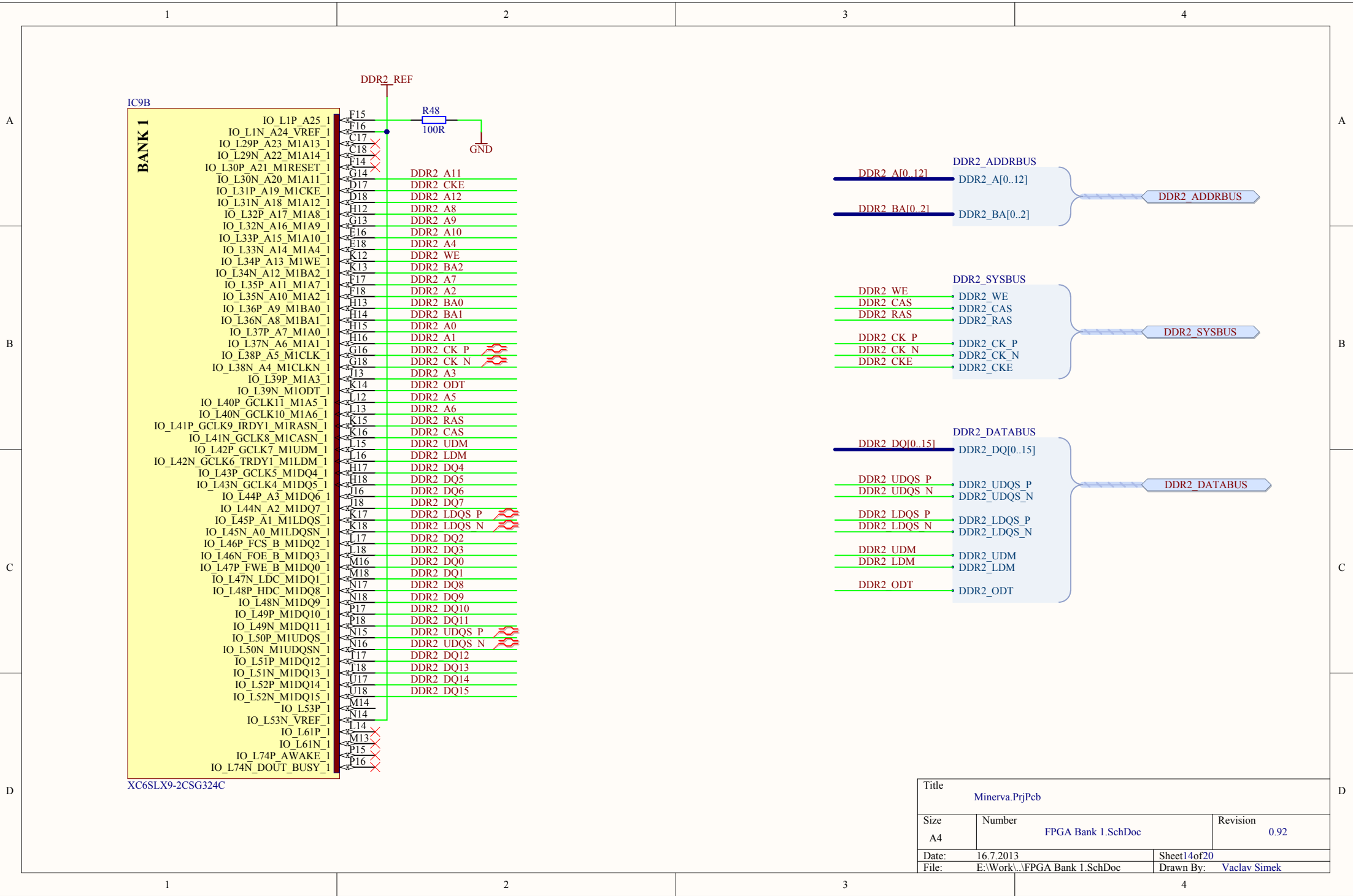
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MCU_I2C0_SDA

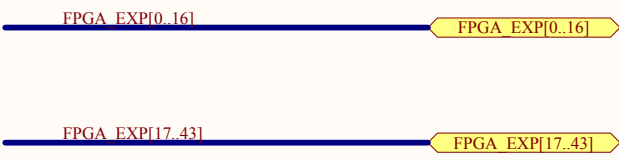
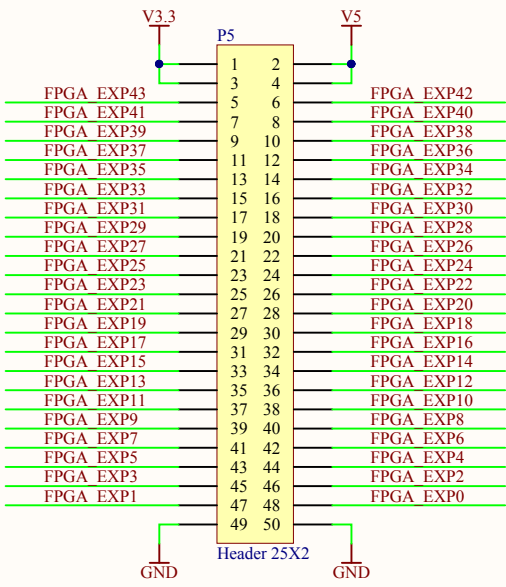
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MCU_I2C_BUS

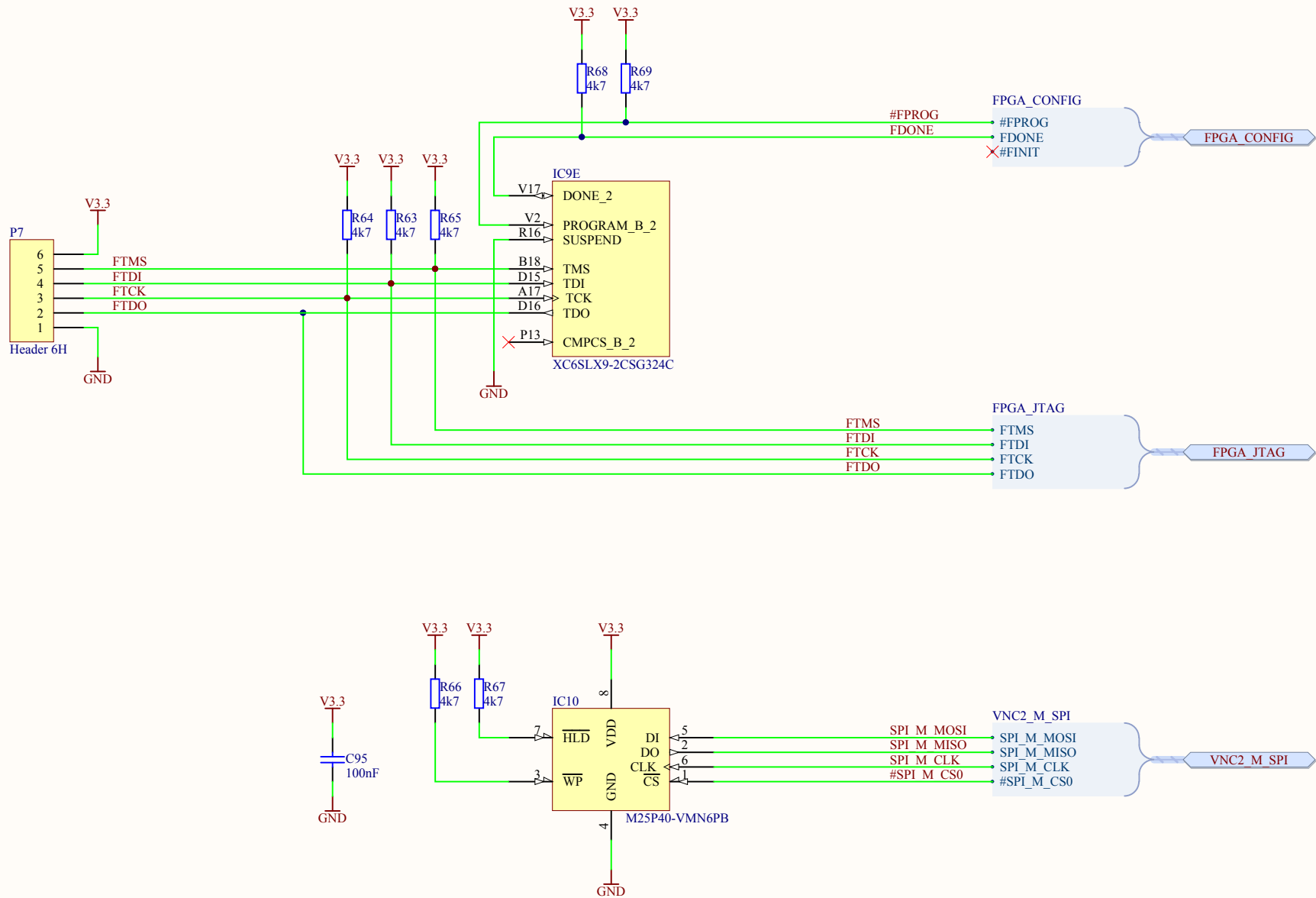
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Size	Number	Revision	
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Date:	16.7.2013	Sheet13of20	
File:	E:\Work\...\FPGA Bank 0.SchDoc	Drawn By: Vaclav Simek	



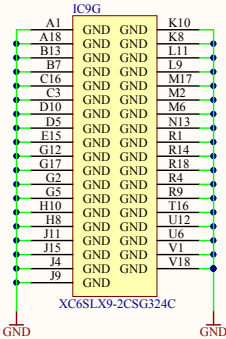
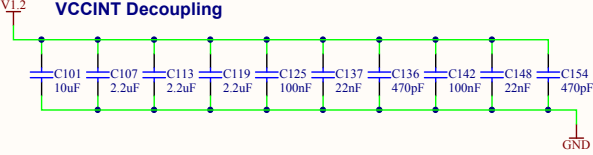
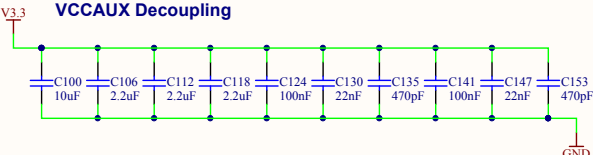
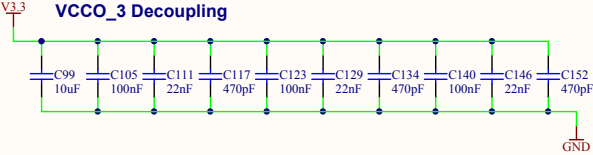
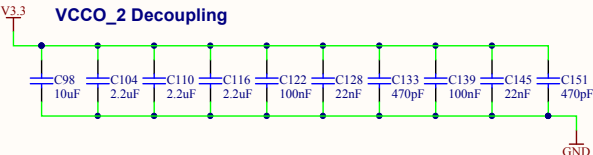
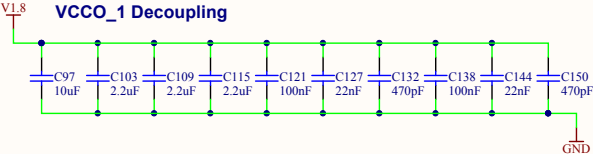
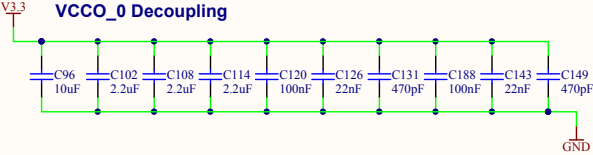
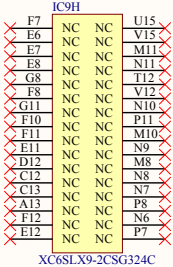
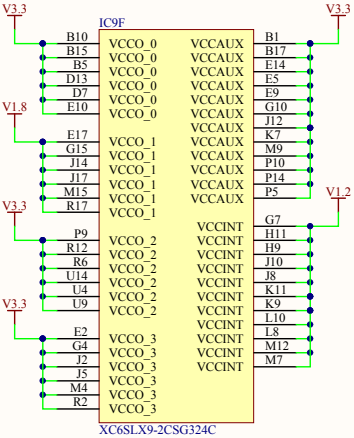
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Size	Number	Revision	
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Date:	16.7.2013	Sheet14of20	
File:	E:\Work\...\FPGA Bank 1.SchDoc	Drawn By:	Vaclav Simek



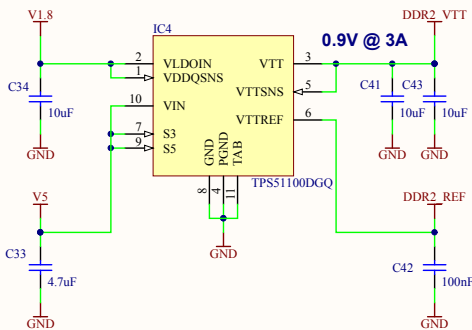
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Size	Number		Revision
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Date:	16.7.2013		Sheet17of20
File:	E:\Work\...\FPGA_Expansion.SchDoc		Drawn By: Vaclav Simek



Title			
Minerva.PrjPcb			
Size	Number	Revision	
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Date:	16.7.2013	Sheet18of20	
File:	E:\Work\...\FPGA Config.SchDoc	Drawn By: Vaclav Simek	



Title			Minerva.PrjPcb
Size	Number	Revision	
A3	FPGA Power.SchDoc	0.92	
Date:	16.7.2013	Sheet19of20	
File:	E:\Work\...FPGA Power.SchDoc	Drawn By: Vaclav Simek	



Size A3	Number Board Power.SchDoc	Revision 0.92
Date:	16.7.2013	Sheet20of20
File:	E:\Work\Board Power.SchDoc	Drawn By: Vaclav Simek