Marvell® ARMADA 16x Applications Processor Family

Hardware Manual

Doc. No. MV-S301545-00, Rel. -

November 2010 PUBLIC RELEASE

Document Conventions

	**Note:** Provides related information or information of special importance.
	**Caution:** Indicates potential damage to hardware or software, or loss of data.
	**Warning:** Indicates a risk of personal injury.

Document Status

Draft	For internal use. This document has not passed a complete technical review cycle and ECN signoff process.
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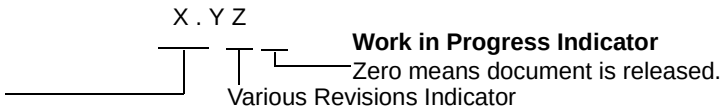

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Revision History

Public Release, Release - / (November 2010)

- Initial Release

1 Introduction

Note

Here's how to correlate the various Public Release versions of Marvell® ARMADA 16x Applications Processor Family documentation:

Rev. - : signifies initial version of any release.

Rev. A: first revision of any release.

Rev. B: second revision of any release.

Rev. B1: first minor revision of Rev. B, usually to correct documentation errors not attributed to engineering changes.

This chapter describes:

The Marvell® ARMADA 16x Applications Processor Family (also referred to as the ARMADA 16x Applications Processor Family) is a high-performance and highly integrated family of devices optimized for digital picture frames, personal media players, and other personal consumer devices. Featuring an advanced 1 GHz processor ARM v5TE-compatible core with an integrated 2-D graphics engine, the ARMADA 16x Applications Processor Family offers performance headroom and flexibility for today and future applications. The common software base provides a scalable platform to cover a breadth of product offerings.

Multiple complete turn-key hardware/software reference designs are available for digital picture frame, personal navigation, and portable media applications for rapid development and quick time to market. The digital picture frame platform is based on the optimized chipset of the ARMADA 16x Applications Processor Family, Marvell Power Management IC, and Marvell Wi-Fi component. Ideal for digital picture frame applications, the ARMADA 16x Applications Processor Family-based platform delivers fast response time for sophisticated user interfaces, image processing, and multimedia applications. Software supports multiple A/V standards and photo-editing capabilities for pan, zoom, and media effects. The ARMADA 16x Applications Processor Family is designed for high performance and low power, delivering extended battery life for personal consumer devices.

1.1 Product Summary

The ARMADA 16x Applications Processor Family comprises several products. These products support a variety of options for packaging, speed, on-chip cache and peripheral support. Table 1 shows a breakdown of the ARMADA 16x Applications Processor Family and the options available.

Refer to Table 2 for the basic features of the ARMADA 16x Applications Processor Family.

Table 1: ARMADA 16x Applications Processor Family Feature Breakdown

	ARMADA 162	ARMADA 166	ARMADA 166E	ARMADA 168
Package	BGA-320	BGA-320	BGA-320	BGA-320
Max CPU Speed	400 MHz	800 MHz	800 MHz	1.066 GHz
WMMX2	Yes	Yes	Yes	Yes
Memory (x16 DRAM)	LP-DDR1-200 DDR2-400 DDR3-400	LP-DDR1-200 DDR2-800 DDR3-800	LP-DDR1-200 DDR2-800 DDR3-800	LP-DDR1-200 DDR2-1066 DDR3-1066
L1, L2 Caches	32/32/64 KB	32/32/128 KB	32/32/128 KB	32/32/128 KB
LCD Max Res, Color	XGA 24bpp	WUXGA 24bpp	WUXGA 24bpp	WUXGA 24bpp
2D and Qdeo™ ICR	Yes	Yes	Yes	Yes
USB2.0 HS + PHY*	1 OTG, 1 host	1 OTG, 1 host	1 OTG, 1 host	1 OTG, 1 host
xD Picture Card	Yes	Yes	Yes	Yes
CompactFlash+	Yes	Yes	Yes	Yes
FE MAC	-	Yes	Yes	Yes
PCIe2.0 x1 Lane	-	-	-	Yes
ElectroPhoretic Display (EPD)	-	-	Yes	-

Table 2: ARMADA 16x Applications Processor Family Hardware Features[2]

Feature Group	Feature	Description
Marvell® Sheeva™ Core and Internal Memory	Marvell® Sheeva™ Embedded CPU Technology	ARM* v5TE instruction set compliant
	L1 Instruction and Data Cache	32 KB I$ + 32 KB D$
	L2 Cache	128 KB
	Internal Boot ROM	Support boot from 8-bit NAND, 16-bit NAND, MMC, SD, OneNAND, SLC, MLC NAND, SSP SPI, and XIP
MULTIMEDIA	Multimedia acceleration with WMMX Hardware 2D graphics	• Decode H.264 up to WVGA and MPEG-4 up to 720p • Scaling • Color Space Conversion • Overlaying • Rotation

Table 2: ARMADA 16x Applications Processor Family Hardware Features[2]

Feature Group	Feature	Description
	2D Graphics	Bit blt
	Qdeo™ Intelligent Color Remapping	• Qdeo™ ICR enhances color to make vivid images without hue shifts or clipping • Part of the award-winning Qdeo suite of video processing
	CCIR-656 Camera Interface	
	LCD Controller	• Up to WUXGA (1920x1200) • 16-, 18- or 24[1]-bpp color depth
DMA	DMA Controller Interface	
EXTERNAL MEMORY	DDR Memory Controller	• 2 Chip Selects • 16-bit DDR2/DDR3 at up to 533 MHz • LP-DDR1
	Static Memory Controller	• 2 Chip Selects • AA/D and A/D Muxed Mode support • Support for VLIO or Companion Chips
	NAND Memory Controller	• 2 Chip Selects • SLC and MLC NAND • x8 and x16[1] small block and large block
	Compact Flash Controller	• 2 Chip Selects • Compliant with CompactFlash (CF+) Spec 4.1
	xD Card Controller	• 1 Chip Select • Compliant with xD-Picture Card Specification Version 1.20
	MultiMediaCard/SD/SDIO Card and MS/MSPRO Controller	• Up to 4 MMC/SD/SDIO Controllers • 1 Memory Stick Pro Controller w/ support for 1 Card and support serial interface and 4-bit parallel interface

Table 2: ARMADA 16x Applications Processor Family Hardware Features[2]

Feature Group	Feature	Description
PERIPHERALS	USB 2.0 Host Controller	1 High-Speed USB2.0 Host with integrated transceiver
	USB 2.0 OTG Controller	1 High-Speed USB2.0 OTG with integrated transceiver and boot support
	Fast Ethernet Interface	• MII interface support 10/100 Ethernet Operation • MDC/MDIO interface for external PHY control
	Synchronous Serial Port Controller	• Up to 52 MHz with Master and Slave modes for frame sync and bit clock • I^2S support • Up to 5 general purpose SSPs
	Universal Asynchronous Serial Port Controller	• 3 UART Controllers • Up to 3.6 Mbps data rate
	Two Wire Serial Bus Interface (TWSI)[1]	• Interfaces to TWSI* peripherals • Up to 3.4 Mbps with 7-bit addressing
	Power Two Wire Serial Bus Interface (PWR_TWSI)[1]	• Interfaces to TWSI* peripherals • Up to 400 kbps with 7-bit addressing
	JTAG Controller	JTAG support for debugging and testing Program Flash
	Pulse Width Modulator (PWM) Controller	4 PWM Controllers
	HW Timers	• Provides three 32-bit General Purpose Timers • Provides one 16-bit Watchdog timer
	AC '97 Interface	Supports the Audio *CODEC'97 Component Specification*, Revision 2.3
	One-Wire Interface	Serial bus operation to receive/transmit 1-Wire bus data
	Keypad Controller	• Support for up to 8x8 Matrix Keys • Support for up to 8 Direct Keys
	General Purpose Input/Output (GPIO) Controller	Up to 123 Multi-Function Pins with alternate GPIO functionality

1. Two-Wire Serial Interface (formerly referred to as I^2C)
2. Not all features may be present in all SKUs - contact your Marvell sales rep.

1.2 Document Purpose

This document constitutes the hardware specifications for the ARMADA 16x Applications Processor Family, including electrical, mechanical, and thermal information, functional overview, mechanical data, package signal locations, targeted electrical specifications, functional bus waveforms, and board design considerations. For software specifications including register programming information, refer to the *Marvell® ARMADA 16x Application Processor Family Software Manual (MV-S301544-00).*

SPECIAL NOTE: Not all of the devices listed in this hardware manual have external hardware connections. Refer to the software manual (MV-S301544-00) for more information.

1.3 Number Representation

All numbers in this document are decimal (base 10) unless designated otherwise. Hexadecimal numbers have a prefix of 0x, and binary numbers have a prefix of 0b. For example, 107 is represented as 0x6B in hexadecimal and 0b110_1011 in binary.

1.4 Naming Conventions

All signal and register-bit names appear in uppercase. Active low items are prefixed with a lowercase “n”.

Pins within a signal name are enclosed in **angle brackets**:

```
EXTERNAL_ADDRESS<31:0>
nCS<1>
```

Bits within a register bit field are enclosed in **square brackets**:

```
REGISTER_BITFIELD[3:0]
REGISTER_BIT[0]
```

Single-bit items have either of two states:

- **Clear** — the item contains the value 0b0
- **Set** — the item contains the value 0b1

1.5 Applicable Documents

Table 3 lists supplemental information sources for the ARMADA 16x Applications Processor Family. Contact a Marvell representative for the latest document revisions and ordering instructions.

Table 3: Supplemental ARMADA 16x Applications Processor Family Documentation, Releases, and Availability

Document Title	Available
ARMADA 16x Applications Processor Family Hardware Manual (MV-S301545-00) Public Release Available	**Now**
ARMADA 16x Applications Processor Family Software Manual (MV-S301544-00) Public Release Available	**Now**
ARMADA16x Applications Processor Family Alternate Function Spreadsheet	**Now**
ARMADA 16x Applications Processor Family Boot ROM Reference Manual Public Release Available	**Now**
ARMADA 16x Applications Processor Family PMIC Application Note	**Now**
USB 2.0 PHY Calibration/ Compliance Guidelines for ARMADA 16x Applications Processor Family (*MV-S301722-00)*	**Now**
ARMADA 16x Applications Processor Family JTAG Application Note (MV-S301720-00)	**Now**
ARMADA 16x Applications Processor Family Board Design and Layout Guidelines *(MV-S301721-00)*	**Now**
ARMADA 16x Applications Processor Family Temperature Sensor App Note (MV-S301707-00)	**Now**

Table 3: Supplemental ARMADA 16x Applications Processor Family Documentation, Releases, and Availability (Continued)

Document Title	Available
ARMADA16x Applications Processor Family Spec Update(s)	Spec Updates are released periodically
Check the Marvell website for the latest versions of available documents	

Note

Refer to the *Marvell*® ARMADA 16x Applications Processor Family *Specification Update* (MV-S501140-00) for corrections and updates to content *between* documentation releases. The specification update is revised on a periodic basis.

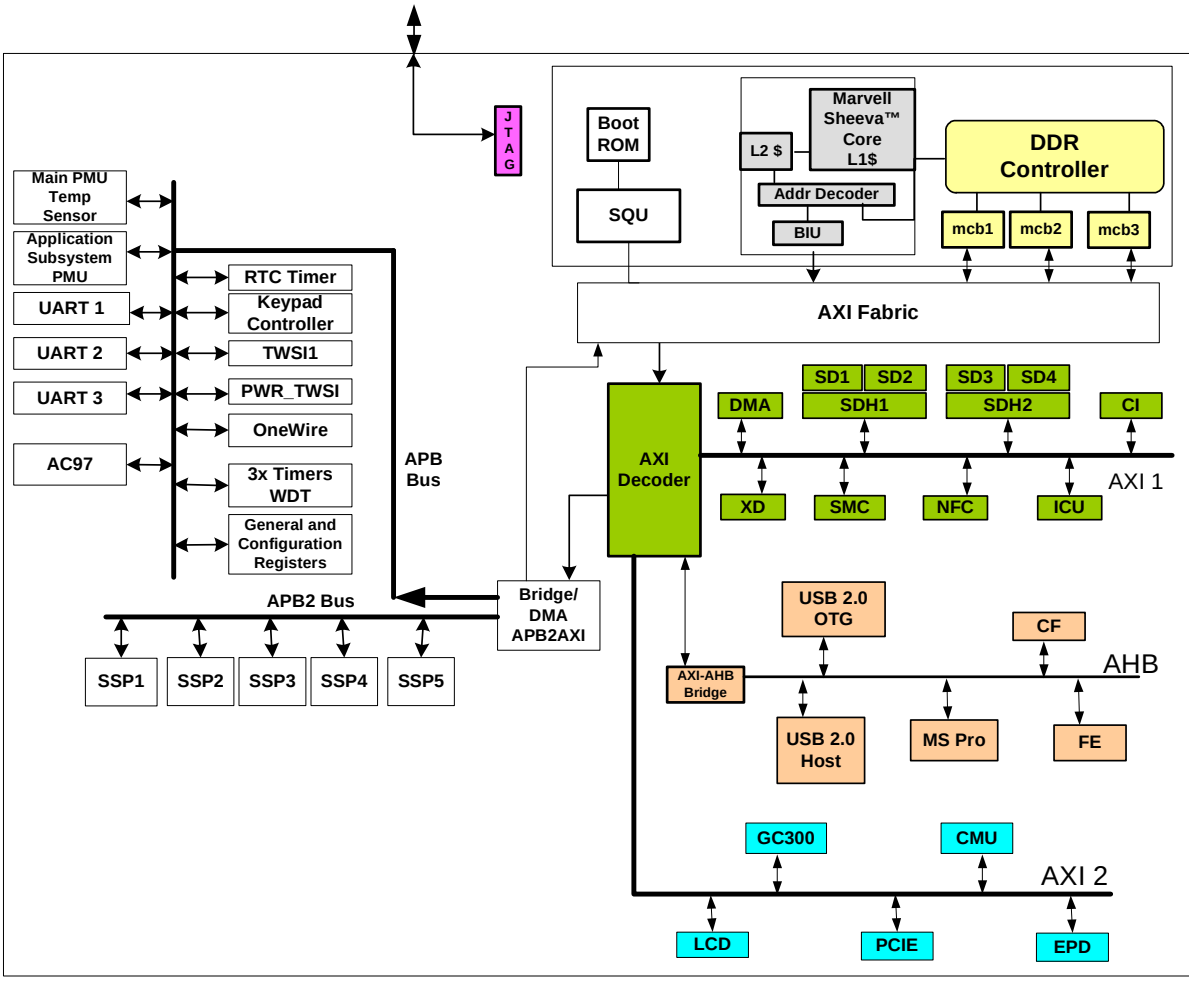
2 Product Overview

The ARMADA 16x Applications Processor Family application is an integrated system-on-a-chip microprocessor targets mid- to high-end picture frame, personal navigation devices, and smart-monitor applications, among others. It incorporates the Marvell® Sheeva™ Embedded CPU Technology microarchitecture with sophisticated power management to provide optimum MIPS/mW performance across its wide range of operating frequencies. The ARMADA 16x Applications Processor Family complies with the ARM* Architecture V5TE instruction set (excluding floating point instructions) and follows the ARM* programmers model. The ARMADA 16x Applications Processor Family multimedia coprocessor provides enhanced Intel® WMMX 2 instructions to accelerate audio and video processing. The ARMADA 16x Applications Processor Family is available in a discrete package configuration.

The ARMADA 16x Applications Processor Family memory architecture provides greater flexibility and higher performance than that of previous products. The ARMADA 16x Applications Processor Family provides the configuration support for two dedicated memory interfaces to support high-speed DDR SDRAM, VLIO devices, and NAND Flash devices. This flexibility enables high performance “store and download” as well as “execute-in-place” system architectures. The ARMADA 16x Applications Processor Family memory architecture features a memory switch that allows multiple simultaneous memory transactions between different sources and targets. For example, the ARMADA 16x Applications Processor Family architecture allows memory traffic between the core and DDR SDRAM to move in parallel with DMA-generated traffic between the camera interface and the LCD Controller.

Figure 1 illustrates the ARMADA 16x Applications Processor Family. The diagram shows a multi-port memory switch and system bus architecture with the core attached, along with an LCD Controller and hardware accelerators for graphics and color remapping. The key features of all of the sub-blocks are described in this section, with more detail provided in the respective chapters.

Figure 1: ARMADA 16x Applications Processor Family Block Diagram



3 Pin and Ball Map Views

In the following pin and ball map figures, the lowercase letter “n”, which normally indicates negation, appears as uppercase “N”. “RFU” means “Reserved For Future Use”. NC means “No Connect”. Do not connect these pins.

3.1 ARMADA 168 (88AP168) Applications Processor 15mm x 15mm TFBGA Ball Map

Figure 2 shows the ball map for the 320-ball 15mm x 15mm TFBGA ARMADA 168 (88AP168) Applications Processor package.

Figure 2: ARMADA 168 (88AP168) Applications Processor 15mm x 15mmTF-BGA Ball Map - Top View

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	
A	MFP_92	MFP_88	MFP_86	MFP_84	MFP_80	MFP_76	MFP_72	MFP_68	MFP_64	MFP_63	MFP_59	MFP_35	MFP_31	MFP_29	MFP_22	MFP_19	MFP_17	MFP_16	A
B	MFP_93	MFP_90	MFP_87	MFP_85	MFP_81	MFP_77	MFP_73	MFP_69	MFP_65	MFP_62	MFP_58	MFP_33	MFP_30	MFP_28	MFP_21	MFP_18	MFP_15	MFP_14	B
C	MFP_97	MFP_95	MFP_91	VDD_IO2	MFP_82	VSS	VDD_IO2	MFP_70	VDD_IO2	VSS	MFP_57	MFP_34	MFP_27	MFP_24	MFP_20	VSS	MFP_13	MFP_12	C
D	MFP_101	MFP_98	MFP_94	MFP_89	MFP_83	MFP_78	MFP_74	MFP_71	MFP_66	MFP_61	MFP_56	MFP_32	MFP_25	MFP_23	MFP_11	MFP_10	MFP_9	MFP_8	D
E	MFP_104	MFP_102	MFP_99	MFP_96	VDD_IO4	MFP_79	MFP_75	VDD_CORE	MFP_67	MFP_60	VDD_CORE	MFP_36	MFP_26	VDD_IO0	MFP_7	MFP_6	MFP_5	MFP_4	E
F	MFP_106	MFP_105	MFP_103	MFP_100	VDD_IO4		VSS	VSS	VSS	VSS	VSS	VSS		VDD_IO0	MFP_3	MFP_2	MFP_1	MFP_0	F
G	MFP_110	MFP_109	MFP_108	MFP_107	VDD_CORE	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD_CORE	MFP_55	MFP_54	MFP_53	MFP_52	G
H	MFP_114	MFP_113	MFP_112	MFP_111	VDD_CORE	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD_CORE	MFP_51	MFP_50	MFP_49	MFP_48	H
J	MFP_118	MFP_117	MFP_116	MFP_115	VDD_IO3	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD_IO1	MFP_44	MFP_45	MFP_46	MFP_47	J
K	MFP_119	MFP_120	MFP_121	MFP_122	VDD_IO3	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD_IO1	MFP_40	MFP_41	MFP_42	MFP_43	K
L	RESET_IN_N	PWR_SCL	PWR_SDA	PRI_TDI	VDD_CORE	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD_CORE	MFP_37	MFP_38	USBID	VSS	L
M	PRI_TMS	PRI_TCK	PRI_TDO	PRI_TRST_N	VDD_CORE	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD_CORE	MFP_39	AVDD_UHC	USBH_P	USBH_N	M
N	VREF	JTAG_SEL	EXT_WAKEUP	CALPAD	SEC_CS_EN		VSS	VSS	SDCKE1	nSDCS1	VSS	VSS		VSS	AVDD_OTG	VSS	USBOTG_P	USBOTG_N	N
P	DQM0	MDQ0	MDQ1	MDQ2	VSS	MDQ12	VSS	VDD_CORE	VDD_M	SDBA2	VDD_CORE	VSS	MA13	VSS	VSS	AVDD_OSC	USBVBUS	AVDD5_USB	P
R	DQS0_N	VDD_M	MDQ3	VDD_M	MDQ10	MDQ13	SDCKE0	nSDCS0	SDBA1	MA0	MA3	MA9	MA12	MA14	RFU_R15	RT_SEN	A_ISET	PXTAL_IN	R
T	DQS0	VSS	MDQ4	VSS	MDQ11	MDQ14	VDD_M	VSS	SDBA0	VDD_M	VSS	MA8	VDD_M	VSS	AVDDT_PCIE	VSS	VDD_CORE	PXTAL_OUT	T
U	MDQ5	MDQ6	VDD_M	MDQ9	VDD_M	VSS	MDQ15	ODT	nSDWE	MA1	MA4	MA7	MA11	ODT1	PCIETXP	AVDD_PCIE	PCIERXP	PCIECLKKP	U
V	MDQ7	MDM1	MDQ8	DQS1_N	DQS1	SDCLK0	SDCLK0_N	nSDRAS	nSDCAS	MA2	MA5	MA6	MA10	nDDR_RESET	PCIETXN	VSS	PCIERXN	PCIECLKKN	V
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	

3.2 ARMADA 166 (88AP166) Applications Processor 15mm x 15mm TFBGA Ball Map

Figure 3 shows the ball map for the 320-ball 15mm x 15mm TFBGA ARMADA 166 (88AP166) Applications Processor package.

Figure 3: ARMADA 166 (88AP166) Applications Processor 15mm x 15mmTF-BGA Ball Map - Top View

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	
A	MFP_92	MFP_88	MFP_86	MFP_84	MFP_80	MFP_76	MFP_72	MFP_68	MFP_64	MFP_63	MFP_59	MFP_35	MFP_31	MFP_29	MFP_22	MFP_19	MFP_17	MFP_16	A
B	MFP_93	MFP_90	MFP_87	MFP_85	MFP_81	MFP_77	MFP_73	MFP_69	MFP_65	MFP_62	MFP_58	MFP_33	MFP_30	MFP_28	MFP_21	MFP_18	MFP_15	MFP_14	B
C	MFP_97	MFP_95	MFP_91	VDD_IO2	MFP_82	VSS	VDD_IO2	MFP_70	VDD_IO2	VSS	MFP_57	MFP_34	MFP_27	MFP_24	MFP_20	VSS	MFP_13	MFP_12	C
D	MFP_101	MFP_98	MFP_94	MFP_89	MFP_83	MFP_78	MFP_74	MFP_71	MFP_66	MFP_61	MFP_56	MFP_32	MFP_25	MFP_23	MFP_11	MFP_10	MFP_9	MFP_8	D
E	MFP_104	MFP_102	MFP_99	MFP_96	VDD_IO4	MFP_79	MFP_75	VDD_CORE	MFP_67	MFP_60	VDD_CORE	MFP_36	MFP_26	VDD_IO0	MFP_7	MFP_6	MFP_5	MFP_4	E
F	MFP_106	MFP_105	MFP_103	MFP_100	VDD_IO4		VSS	VSS	VSS	VSS	VSS	VSS		VDD_IO0	MFP_3	MFP_2	MFP_1	MFP_0	F
G	MFP_110	MFP_109	MFP_108	MFP_107	VDD_CORE	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD_CORE	MFP_55	MFP_54	MFP_53	MFP_52	G
H	MFP_114	MFP_113	MFP_112	MFP_111	VDD_CORE	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD_CORE	MFP_51	MFP_50	MFP_49	MFP_48	H
J	MFP_118	MFP_117	MFP_116	MFP_115	VDD_IO3	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD_IO1	MFP_44	MFP_45	MFP_46	MFP_47	J
K	MFP_119	MFP_120	MFP_121	MFP_122	VDD_IO3	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD_IO1	MFP_40	MFP_41	MFP_42	MFP_43	K
L	RESET_IN_N	PWR_SCL	PWR_SDA	PRI_TDI	VDD_CORE	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD_CORE	MFP_37	MFP_38	USBID	VSS	L
M	PRI_TMS	PRI_TCK	PRI_TDO	PRI_TRST_N	VDD_CORE	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD_CORE	MFP_39	AVDD_UHC	USBH_P	USBH_N	M
N	VREF	JTAG_SEL	EXT_WAKEUP	CALPAD	SEC_CS_EN		VSS	VSS	SDCKE1	nSDCS1	VSS	VSS		VSS	AVDD_OTG	VSS	USBOTG_P	USBOTG_N	N
P	DQM0	MDQ0	MDQ1	MDQ2	VSS	MDQ12	VSS	VDD_CORE	VDD_M	SDBA2	VDD_CORE	VSS	MA13	VSS	VSS	AVDD_OSC	USBVBUS	AVDD5_USB	P
R	DQS0_N	VDD_M	MDQ3	VDD_M	MDQ10	MDQ13	SDCKE0	nSDCS0	SDBA1	MA0	MA3	MA9	MA12	MA14	VSS	RT_SEN	A_ISET	PXTAL_IN	R
T	DQS0	VSS	MDQ4	VSS	MDQ11	MDQ14	VDD_M	VSS	SDBA0	VDD_M	VSS	MA8	VDD_M	VSS	VSS	VSS	VDD_CORE	PXTAL_OUT	T
U	MDQ5	MDQ6	VDD_M	MDQ9	VDD_M	VSS	MDQ15	ODT	nSDWE	MA1	MA4	MA7	MA11	ODT1	VSS	VSS	VSS	VSS	U
V	MDQ7	MDM1	MDQ8	DQS1_N	DQS1	SDCLK0	SDCLK0_N	nSDRAS	nSDCAS	MA2	MA5	MA6	MA10	nDDR_RESET	VSS	VSS	VSS	VSS	V

3.3 ARMADA 162 (88AP162) Applications Processor 15mm x 15mm TFBGA Ball Map

Figure 4 shows the ball map for the 320-ball 15mm x 15mm TFBGA ARMADA 162 (88AP162) Applications Processor package.

Figure 4: ARMADA 162 (88AP162) Applications Processor 15mm x 15mmTF-BGA Ball Map - Top View

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	
A	MFP_92	MFP_88	MFP_86	MFP_84	MFP_80	MFP_76	MFP_72	MFP_68	MFP_64	MFP_63	MFP_59	MFP_35	MFP_31	MFP_29	MFP_22	MFP_19	MFP_17	MFP_16	A
B	MFP_93	MFP_90	MFP_87	MFP_85	MFP_81	MFP_77	MFP_73	MFP_69	MFP_65	MFP_62	MFP_58	MFP_33	MFP_30	MFP_28	MFP_21	MFP_18	MFP_15	MFP_14	B
C	MFP_97	MFP_95	MFP_91	VDD_IO2	MFP_82	VSS	VDD_IO2	MFP_70	VDD_IO2	VSS	MFP_57	MFP_34	MFP_27	MFP_24	MFP_20	VSS	MFP_13	MFP_12	C
D	MFP_101	MFP_98	MFP_94	MFP_89	MFP_83	MFP_78	MFP_74	MFP_71	MFP_66	MFP_61	MFP_56	MFP_32	MFP_25	MFP_23	MFP_11	MFP_10	MFP_9	MFP_8	D
E	MFP_104	MFP_102	MFP_99	MFP_96	VDD_IO4	MFP_79	MFP_75	VDD_CORE	MFP_67	MFP_60	VDD_CORE	MFP_36	MFP_26	VDD_IO0	MFP_7	MFP_6	MFP_5	MFP_4	E
F	MFP_106	MFP_105	MFP_103	MFP_100	VDD_IO4		VSS	VSS	VSS	VSS	VSS	VSS		VDD_IO0	MFP_3	MFP_2	MFP_1	MFP_0	F
G	MFP_110	MFP_109	MFP_108	MFP_107	VDD_CORE	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD_CORE	MFP_55	MFP_54	MFP_53	MFP_52	G
H	MFP_114	MFP_113	MFP_112	MFP_111	VDD_CORE	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD_CORE	MFP_51	MFP_50	MFP_49	MFP_48	H
J	MFP_118	MFP_117	MFP_116	MFP_115	VDD_IO3	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD_IO1	MFP_44	MFP_45	MFP_46	MFP_47	J
K	MFP_119	MFP_120	MFP_121	MFP_122	VDD_IO3	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD_IO1	MFP_40	MFP_41	MFP_42	MFP_43	K
L	RESET_IN_N	PWR_SCL	PWR_SDA	PRI_TDI	VDD_CORE	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD_CORE	MFP_37	MFP_38	USBID	VSS	L
M	PRI_TMS	PRI_TCK	PRI_TDO	PRI_TRST_N	VDD_CORE	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD_CORE	MFP_39	AVDD_UHC	USBH_P	USBH_N	M
N	VREF	JTAG_SEL	EXT_WAKEUP	CALPAD	SEC_CS_EN		VSS	VSS	SDCKE1	nSDCS1	VSS	VSS		VSS	AVDD_OTG	VSS	USBOTG_P	USBOTG_N	N
P	DQM0	MDQ0	MDQ1	MDQ2	VSS	MDQ12	VSS	VDD_CORE	VDD_M	SDBA2	VDD_CORE	VSS	MA13	VSS	VSS	AVDD_OSC	USBVBUS	AVDD5_USB	P
R	DQS0_N	VDD_M	MDQ3	VDD_M	MDQ10	MDQ13	SDCKE0	nSDCS0	SDBA1	MA0	MA3	MA9	MA12	MA14	VSS	RT_SEN	A_ISET	PXTAL_IN	R
T	DQS0	VSS	MDQ4	VSS	MDQ11	MDQ14	VDD_M	VSS	SDBA0	VDD_M	VSS	MA8	VDD_M	VSS	VSS	VSS	VDD_CORE	PXTAL_OUT	T
U	MDQ5	MDQ6	VDD_M	MDQ9	VDD_M	VSS	MDQ15	ODT	nSDWE	MA1	MA4	MA7	MA11	ODT1	VSS	VSS	VSS	VSS	U
V	MDQ7	MDM1	MDQ8	DQS1_N	DQS1	SDCLK0	SDCLK0_N	nSDRAS	nSDCAS	MA2	MA5	MA6	MA10	nDDR_RESET	VSS	VSS	VSS	VSS	V
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	

4 Package Information

This chapter describes the following:

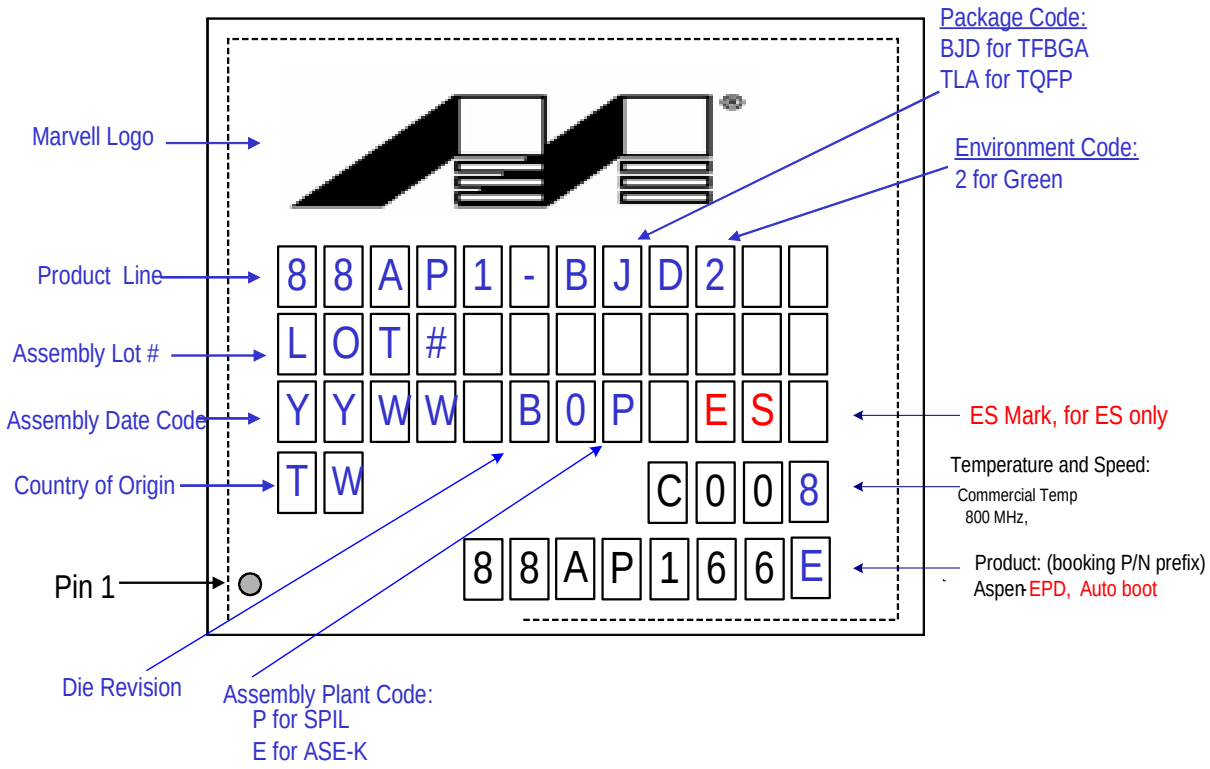
4.1 Introduction

This chapter provides the package marking and mechanical specifications for the ARMADA 16x Applications Processor Family.

4.2 Package Marking

Figure 5 shows an example of the package marking for the ARMADA 16x Applications Processor Family. The Booking Part Number for this specific example is 88AP166EB0-BJD2C008

Figure 5: Sample Package Marking



NOTE: The individual text boxes illustrated above are only used to demonstrate the relative location for the marking.

4.3 Packaging Materials

Table 4 shows the solder ball material list.

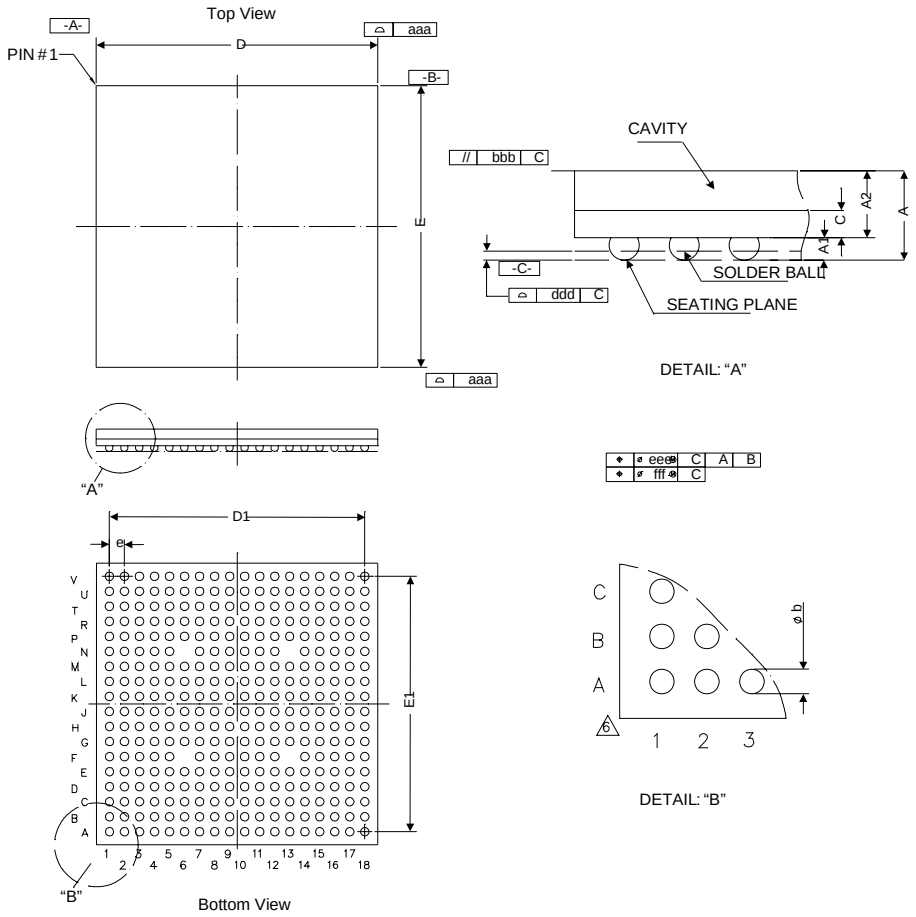
Table 4: Package Materials

Solder Balls (SAC305)
Solder balls: 96.5 Sn/3.0 Ag/0.5 Cu
NOTE: Pb-free parts, lead has not been added intentionally, but lead may persist as an impurity below 1000 ppm

4.4 ARMADA 16x Applications Processor Family 15mm x 15mm TFBGA Packaging

Figure 6 shows the 320-ball TFBGA packaging for the ARMADA 16x Applications Processor Family. Table 5 provides TFBGA package dimensions.

Figure 6: ARMADA 16x Applications Processor Family 15mm x 15mm TFBGA Package Information



1. Solder Ball size: 0.45mm
2. BGA solder ball pad: 0.4mm SMD

Table 5: TFBGA Package Dimensions

Symbol	Dimensions in mm			Dimensions in inch (see Note)		
	Min	Nom	Max	Min	Nom	Max
A	---	---	1.40	---	---	0.055
A1	0.30	0.35	0.40	0.012	0.014	0.016
A2	0.84	0.89	0.94	0.033	0.035	0.037
c	0.32	0.36	0.40	0.013	0.014	0.016
D	14.90	15.00	15.10	0.587	0.591	0.594
E	14.90	15.00	15.10	0.587	0.591	0.594
D1	---	13.60	---	---	0.535	---
E1	---	13.60	---	---	0.535	---
e	---	0.80	---	---	0.031	---
b	0.40	0.45	0.50	0.016	0.018	0.020
aaa		0.15			0.006	
bbb		0.10			0.004	
ddd		0.12			0.005	
eee		0.15			0.006	
fff		0.08			0.003	
MD/WE		18/18			18/18	

NOTE: If the PCB is designed with English units on outer rows, solder balls may not align with PCB pads due to rounding error from converting from mm to inches. Once solder ball and PCB pad positional tolerances are factored, there is a risk of SMT failure due to outer balls not aligning with PCB pads.

5 Maximum Ratings and Operation Conditions

This chapter discusses:

- Section 5.1, Absolute Maximum Ratings
- Section 5.2, Operating Conditions

5.1 Absolute Maximum Ratings

The absolute maximum ratings (shown in Table 6) define limitations for electrical and thermal stresses. These limits prevent permanent damage to the ARMADA 16x Applications Processor Family.

Note Absolute maximum ratings are *not* operating ranges. Operation at absolute maximum ratings is *not* guaranteed.

Table 6: Absolute Maximum Ratings

Symbol	Description		Min	Max	Units
T_S	Storage temperature		–40	125	°C
V_{CC_HV}	Voltage applied to IO peripherals VDD_IO0, VDD_IO1, VDD_IO2, VDD_IO3, VDD_IO4		VSS–0.3	VSS+4.0	V
	AVDD_UHC (AVDD_USB03P3) and AVDD_OTG (AVDD_USB13P3)		VSS–0.3	VSS+3.6	V
V_{CC_MV}	Voltage applied to DDR supply pins (VDD_M)		VSS–0.5	VSS+2.3	V
V_{CC_LV}	Voltage applied to V_{DD_Core} supply pins		VSS-0.3	VSS+1.155	V
V_{IP_X}	Voltage applied to analog blocks (XTAL_IN, XTAL_OUT, AVDD_OSC)		VSS–0.3	VSS+1.9	V
V_{ESD}	Maximum ESD stress voltage, three stresses maximum: • Any pin to any supply pin, either polarity, or • Any pin to all non-supply pins together, either polarity	HBM[1]	—	2000	V
		CDM[2]	—	500	V
I_{EOS}	Maximum DC input current (electrical overstress) for any non-supply pin		—	5	mA

Table 6: Absolute Maximum Ratings (Continued)

Symbol	Description	Min	Max	Units
NOTE: 1. HBM = human body model 2. CDM = charge device model				

5.2 Operating Conditions

This section discusses operating voltage, frequency, and temperature specifications for the ARMADA 16x Applications Processor Family.

Refer to the “Clocks Controller and Power Management Unit” chapter of the *Marvell®ARMADA 16x Applications Processor Family Software Manual* for supported frequencies and clock-register settings as listed in Table 7.

Table 7: Voltage, Temperature, and Frequency Electrical Specifications

Symbol	Description	Min	Typical	Max	Units	Notes
Operating Temperature						
Tj	Junction Temperature	-25	—	+85	°C	1
Tj	Junction Temperature	-40	—	+105	°C	1
Tcase	Case Temperature	—	—	See Notes 2 and 3	°C	4, 5, 6, 8
Ψ_{jt}	Thermal parameter characterization junction to top center of package	0.2	—	7.20	°C / watt	—
AVDD_OSC Voltage						
Vccosc_1	Voltage applied on VDD_OSC	1.70	1.80	1.90	V	—
Tsysramp	Ramp Rate	—	—	25.00	mV/µs	—
AVDD CORE Voltage at Frequency Ranges (A0 Stepping)				**Max[10]**		
Vcccore_1	Voltage applied for modes 0 and 1	0.9	1.00	1.155	V	12, 13, 20
Vcccore_2	Voltage applied for modes 2, 2.3, 3 and 3.1	1.05	1.10	1.155	V	14, 15, 16, 17, 20, 21
Tpwrramp	Ramp Rate	1.0	—	25.00	mV/µs	
AVDD CORE Voltage at Frequency Ranges (B0 Stepping)				**Max[11]**	**Max[10]**		
Vcccore_1	Voltage applied for modes 0 and 1	0.90	0.945	1.000	1.155	V	12, 13, 22
Vcccore_2	Voltage applied for modes 2, 2.3, 3 and 3.1	0.97	1.000	1.030	1.155	V	14, 15, 16, 17, 22

Table 7: Voltage, Temperature, and Frequency Electrical Specifications (Continued)

Symbol	Description	Min	Typical	Max		Units	Notes
Vcccore_3	Voltage applied for modes 4 and 4.1	1.086	1.120	1.155	1.155	V	18, 19, 21
Tpwrramp	Ramp Rate	1.0	—	25.00	25.00	mV/µs	
VDD_M Voltage							
Vcc_m_1	Voltage applied on VDD_M	1.425	1.5	1.575		V	—
Tsysramp	Ramp Rate	—	—	25.00		mV/µs	—
VDD_IO{0,1,2,3,4} Voltage							
Vcciox_1	Voltage applied when using 1.8v devices	1.70	1.80	1.98		V	—
Vcciox_3	Voltage applied when using 3.3v devices	2.97	3.30	3.63		V	—
Tsysramp	Ramp Rate	—	—	25.00		mV/µs	—
VDD_USB Voltage							
Vccusb_0	Voltage applied on AVDD_OTG	3.00	3.30	3.6		V	—
Vccusb_1	Voltage applied on AVDD_UHC	3.00	3.30	3.6		V	—
Tsysramp	Ramp Rate	—	—	25.00		mV/µs	—
AVDD5_USB (USB OTG 5V supply)							
vccusb_0	Voltage applied on AVDD5_USB	4.5	5.0	5.5		V	—
Tsysramp	Ramp Rate	—	—	25.00		mV/µs	—

Table 7: Voltage, Temperature, and Frequency Electrical Specifications (Continued)

Symbol	Description	Min	Typical	Max	Units	Notes

NOTE:

1. Minimum/maximum junction temperature depends on SKU
2. The case temperature spec for Marvell® ARMADA 16x Applications Processor Family is a function of the Ψjt value that varies pending OEM system configuration. Ψjt value should be modeled and/or tested for each system configuration.
3. Allowable case temperature should be calculated using following formula. Maximum Ψjt can be used for maximum allowable case temperature calculation where testing or modeling resources are nor available or system can absorb the extra guard band introduced using max Ψjt values
4. $Tcase_{(max)} = Tj_{(max)} - \Psi jt * P_{(max)}$
5. $Tcase_{(max)}$ = Maximum allowable case temperature (°C).
6. $Tj_{(max)}$ = Maximum allowable junction temperature (°C)
7. $P_{(max)}$ = Maximum Sustainable ARMADA Power (W)
8. System design must ensure that the device case temperature is maintained within the specified limits. In some system applications it may be necessary to use external thermal management (for example, a package-mounted heat spreader) or configure the device to limit power consumption and maintain acceptable case temperatures.
9. The voltage ranges specified for VDD_CORE are the targeted voltage ranges for the product. These ranges may extend or narrow depending on actual product performance and product SKUs. Marvell recommends that extended voltage and current capabilities be designed into the power management IC to accommodate future changes to this specification without requiring changes to the power management IC.
10. Maximum allowable operating voltage on VDD_CORE.
11. Maximum allowable voltage on VDD_CORE to meet maximum 1.4 W Pmax
12. Mode 0 is PCLK = 156 MHz and DCLK = 156 MHz
13. Mode 1 is PCLK = 400 MHz and DCLK = 200 MHz
14. Mode 2 is PCLK = 624 MHz and DCLK = 312 MHz
15. Mode 2.3 is PCLK = 624 MHz and DCLK = 156 MHz
16. Mode 3 is PCLK = 800 MHz and DCLK = 400 MHz
17. Mode 3.1 is PCLK = 800 MHz and DCLK = 200 MHz
18. Mode 4 is PCLK = 1.066 GHz and DCLK = 533 MHz
19. Mode 4.1 is PCLK = 1.066 GHz and DCLK = 355 MHz
20. Maximum VDD_CORE power (Pmax) is 1.5W
21. Maximum full chip power (Pmax_fullchip) is 2.0W
22. Maximum full chip power (Pmax_fullchip) is 1.9W.

6 Electrical Specifications

This chapter includes DC voltage and current characteristics as well as crystal and oscillator specifications for the ARMADA 16x Applications Processor Family.

6.1 DC Voltage and Current Characteristics

The DC characteristics for each pin include input-sense levels, output-drive levels, current and pullup/down resistive values. These parameters can be used to determine maximum DC loading and to determine maximum transition times for a given load.

Table 8 shows the DC operating conditions for the input, output, and I/O pins used by the Dynamic Memory Controller. Table 9 shows operating conditions for DDR3.

Table 8: LPDDR1/LPDDR2 Input, Output and I/O pins AC/DC Operating Conditions

Symbols	Description	Min	Typical	Max	Unit	Notes
$Vih_{(dc)}$	Input high voltage	VREF + 0.125	—	VDD_M	V	—
$V_{il(dc)}$	Input low voltage	VSS	—	VREF - 0.125	V	—
$Vih_{(ac)}$	Input high voltage	VREF + 0.200	—	6	V	—
$V_{il(ac)}$	Input low voltage	6	—	VREF - 0.200	V	—
V_{OH}	High-level output voltage Absolute Load Current achieving Voh	1.4	—		V	1, 2
V_{OL}	Low-level output voltage Absolute Load Current achieving Vol	—	—	0.4	V	1, 2
RTT	Rtt Effective impedance value	120	150	180	Ω	3, 4, 5
		60	75	90	Ω	3, 4, 5
Cpin	Pin Capacitance	4	4.5	5	pF	

Table 8: LPDDR1/LPDDR2 Input, Output and I/O pins AC/DC Operating Conditions (Continued)

Symbols	Description	Min	Typical	Max	Unit	Notes

NOTE:
1. $IOH_{(min)}$ = 13.4 mA
2. Measurement conditions VDDIO=1.8V, ZPDRV=ZNDRV=0xF, ZPR=ZNR=0xF, ZD=1
3. Refer to the Functional Description section in the DDR Memory Controller chapter in the *Marvell® ARMADA 16x Applications Processor Family Software Manual* for ODT configuration.
4. Measurement definition for RTT:
   Apply VREF +/- 0.25 to input pin separately, then measure current I(VREF + 0.25) and I(VREF - 0.25) respectively.
   Current does not include the current flowing through the pullup/pulldown resistor.
5. $RTT = 0.5 / (I_{(VREF + 0.25)} - I_{(VREF - 0.25)})$
6. Input DC Operating Conditions (SSTL receiver)
   V_{IH} overshoot: V_{IH} (max) = VDD_M + 0.7V for a pulse width less than or equal to 3ns and the pulse width can not be greater than 1/3 the cycle rate.
   V_{IL} undershoot: V_{IL} (min) = -1.0V for a pulse width less than or equal to 3ns and the pulse width can not be greater than 1/3 the cycle rate
   Where VDD_M <=1.8V

Table 9: DDR3 Input, Output, and I/O Pins AC/DC Operating Conditions

Symbols	Description/Test Condition	Min	Typical	Max	Unit	Notes
VIL (AC)	Input low level AC	Note 7	--	VREF - 0.175	V	--
VIH (AC)	Input high level AC	VREF + 0.175	--	Note 7	V	--
VIL (DC)	Input low level DC	VSS	--	VREF - 0.100	V	--
VIH (DC)	Input high level DC	VREF + 1.00	--	VDDIO	V	--
VDIL	Differential input low level	Note 6	--	-0.2	V	6
VDIH	Differential input high level	0.2	--	Note 6	V	6
VOL	Output low level/ See Note 6	--	--	0.2*VDDIO	V	7
VOH	Ouput high level/ See Note 6	0.8*VDDIO	--	--	V	7
RTT	Rtt effective impedance value/See Note 2	48	60	72	0hm	1, 2
Cpin	Pin capacitance	--	4	4.5	pF	--

Table 9: DDR3 Input, Output, and I/O Pins AC/DC Operating Conditions

Notes:
1. See SDRAM functional description section for ODT configuration
2. Measurement defintion for RTT: Apply VREF +/-0.25 to input pin separately. Then measure current I(VREF + 0.25) and I(VREF - 0.25), respectively. **RTT = 0.35/$I_{(VREF +0.175)}$ - $I_{(VREF - 0.175)}$**
3. Includes pad + pkg cap
4. This current does not include the current flowin g through the pullup/pulldown resistor.
5. Limitations are same as for single-ended signals.
6. Defined when driver impedance is calibrated to 21 ohm.
See JEDEC Overshoot and Undershoot Spec.

Table 10 applies to all signals powered by VCC_high. VCC_high is the term used to refer to the collective groups of high voltage supplies which consist of VDD_IO0, VDD_IO1, VDD_IO2, VDD_IO3, VDD_IO4, VDD_M, VDD_OTG, VDD_PLL and VDD_UHC.

Table 10: MFP Input, Output, and I/O Pins DC Operating Conditions

Symbols	Description	Min	Typical	Max	Unit	Notes
Input DC Operating Conditions (vcc = 1.8 V Typical)						
Vih	Input high voltage	VCC_high * 0.8	—	VCC_high + 0.3	V	3
V_{il}	Input low voltage	-0.3	—	VCC_high * 0.2	V	3
V_{hys}	Hysteresis (V_{IT+} - V_{IT-})	0.4	—	VCC_high * 0.5	V	3
R_{PULLUP}	Pullup Resistance	40[1]	110	200[2]	KΩ	4
$R_{PULLDOWN}$	Pulldown Resistance	40[1]	110	200[2]	KΩ	5
Input DC Operating Conditions (3.3 V Typical)						
Vih	Input high voltage	0.8 * VCC_high	—	VCC_high + 0.3	V	3
V_{il}	Input low voltage	-0.3	—	VCC_high * 0.2	V	3
V_{hys}	Hysteresis (V_{IT+} - V_{IT-})	0.4	—	VCC_high * 0.5	V	3
R_{PULLUP}	Pullup Resistance	20[1]	45	100[2]	KΩ	4
$R_{PULLDOWN}$	Pulldown Resistance	20[1]	45	100[2]	KΩ	5

Table 10: MFP Input, Output, and I/O Pins DC Operating Conditions (Continued)

Symbols	Description	Min	Typical	Max	Unit	Notes
Output DC Operating Conditions (VCC = 1.8 V Typical) (Normal IO Pins)						
V_{OH}[6] 1X 2X 3X	High-level output voltage Absolute Load Current achieving Voh	0.9 * VCC_high	—	VCC_high	V	I_{OH} = (mA min) -3 -6 -9
V_{OL}[6] 1X 2X 3X	Low-level output voltage Absolute Load Current achieving Vol	VSS	—	0.1 * VCC_high	V	I_{OL} = (mA min) 3 6 9
Output DC Operating Conditions (VCC = 1.8 V Typical) (Fast IO Pins (MFP_<56:85>))						
V_{OH}[6] 1X 2X 3X 4X	High-level output voltage Absolute Load Current achieving Voh	0.9 * VCC_high	—	VCC_high	V	I_{OH} = (mA min) -3 -6 -8 -10
V_{OL}[6] 1X 2X 3X 4X	Low-level output voltage Absolute Load Current achieving Vol	VSS	—	0.1 * VCC_high	V	I_{OL} = (mA min) 3 6 8 10
Output DC Operating Conditions (vccp = 3.3 V Typical) (Normal IO Pins)						
V_{OH}[6] 1X 2X 3X	High-level output voltage Absolute Load Current achieving Voh	VCC_high * 0.9	—	VCC_high	V	I_{OH} = (mA min) -3 -9 -11
V_{OL}[6] 1X 2X 3X	Low-level output voltage Absolute Load Current achieving Vol	VSS	—	0.1 * VCC_high	V	I_{OL} = (mA min) 3 6 11
Output DC Operating Conditions (vccp = 3.3 V Typical) (Fast IO Pins (MFP_<56:85>))						

Table 10: MFP Input, Output, and I/O Pins DC Operating Conditions (Continued)

Symbols	Description	Min	Typical	Max	Unit	Notes
V_{OH}[6] 1X 2X 3X 4X	High-level output voltage Absolute Load Current achieving Voh	VCC_high * 0.9	—	VCC_high	V	I_{OH} = (mA min) -5.0 -8.0 -10.0 -12.0
V_{OL}[6] 1X 2X 3X 4X	Low-level output voltage Absolute Load Current achieving Vol	VSS	—	0.1 * VCC_high	V	I_{OL} = (mA min) 5.0 8.0 10.0 12.0
Output DC Operating Conditions (VCC = 1.8 and 3.3 V Typical)						
I_{OZ}	Three-state output leakage current	—	—	40	nA	—
I_{DDQ}	Quiescent supply current	—	—	1	nA	—

NOTE:
1. Max voltage, Minimum temperature
2. Min voltage, Maximum temperature
3. VCC_high references to VDD_IO0, VDD_IO1, VDD_IO2, VDD_IO3, VDD_IO4, VDD_M, VDD_OTG, VDD_PLL and VDD_UHC supplies.
4. Use MFPRxx[pull_sel] and MFPRxx[pullup_en] bits to enable or disable pullups.
5. Use MFPRxx[pull_sel] and MFPRxx[pulldown_en] bits to enable or disable pulldowns.
6. Multi-Function Pin (MFP) drive strength is programmable using MFPRxx[drive] bitfield. MFPR register definitions are found in the *Marvell® ARMADA 16x Applications Processor Family Software Manual.*

6.2 Oscillator Electrical Specifications

6.2.1 26.000 MHz Oscillator Specifications

The 26.000 MHz crystal is connected between the PXTAL_IN (amplifier input) and PXTAL_OUT (amplified output). Table 11 lists the 26.000 MHz crystal specifications.

To drive the 26.000 MHz crystal pins from an external source:

1. Drive the PXTAL_IN pin with a digital signal with low and high levels as listed in Table 12.
2. Float the PXTAL_OUT pin

Table 12 lists the 26.000 MHz oscillator specifications. Figure 7 shows recommended GND shielding to xtal_in and xtal_out.

Figure 7: Recommended GND Shielding to xtal_in and xtal_out

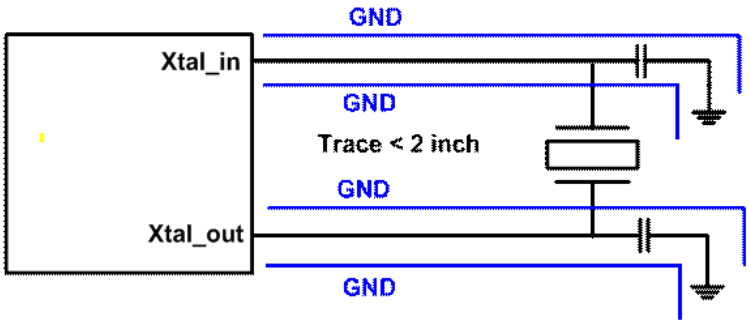


Table 11: Typical 26.000 MHz Crystal Requirements

Parameter	Minimum	Typical	Maximum	Units
Frequency range	25.997	26.000	26.002	MHz
Frequency tolerance at 25°C	–50	—	+50	ppm
Oscillation mode	Fundamental Parallel Resonant			—
Maximum change over temperature range	–50	—	+50	ppm
Drive level	—	10	100	uW
Load capacitance (C_L)	—	10	—	pf
Series resistance (R_S)	—	50	—	Ω
NOTE:				

Table 12: Typical External 26.000 MHz Oscillator Requirements

Symbol	Description	Min	Typical	Max	Units
Amplifier Specifications					
VIH_X	Input high voltage, PXTAL_IN	1.7	1.8	1.9	V
VIL_X	Input low voltage, PXTAL_IN	–0.10	0.00	0.10	V
IIN_XP	Input leakage, PXTAL_IN	—	—	10	µA
CIN_XP	Input capacitance, PXTAL_IN/PXTAL_OUT	—	20	25	pf
tS_XP	Stabilization time	—	—	7	ms
SR_XP	Slew Rate	1	—	—	V/ns

Table 12: Typical External 26.000 MHz Oscillator Requirements (Continued)

Symbol	Description	Min	Typical	Max	Units
Board Specifications					
RP_XP	Parasitic resistance, PXTAL_IN/PXTAL_OUT to any node	20	—	—	MΩ
CP_XP	Parasitic capacitance, PXTAL_IN/PXTAL_OUT, total	—	—	5	pf
COP_XP	Parasitic shunt capacitance, PXTAL_IN to PXTAL_OUT	—	—	0.4	pf

7 AC Electrical Characteristics

This chapter includes alternating-current (AC) characteristics, timing diagrams and timing parameters for the ARMADA 16x Applications Processor Family controllers/interfaces listed below.

7.1 DDR SDRAM Timing Diagrams and Specifications

This section describes the timing diagrams and timing parameters for the DDR Controller.

The following diagrams are included in this section:

- Figure 8, Differential Clock
- Figure 9, LPDDR1 SDRAM Timing Diagrams 1
- Figure 10, LPDDR1 SDRAM Timing Diagrams 2
- Figure 11, LPDDR1 SDRAM Timing Diagrams 3
- Figure 12, LPDDR1 SDRAM Timing Diagrams 4
- Figure 13, Basic Write Timing Parameters
- Figure 14, DQ to DQS Write Skew
- Figure 15, CLK to Address/Command Write Skew
- Figure 16, DQS to CLK Write Skew
- Figure 17, DQ to DQS Read Skew

Refer to Table 15 through Table 18 for the DDR specifications. Refer to the *JEDEC Spec* for complete timing diagrams and specifications.

7.1.1 Measurement Conditions

The diagrams in the section use the following conventions:

Table 13: Standard Input, Output, and I/O-Pin AC Operating Conditions

Symbol	Description	Min	Typical	Max	Units
C_{IO}	IO capacitance, all standard I/O pins	—	—	5	pf

Figure 8: Differential Clock

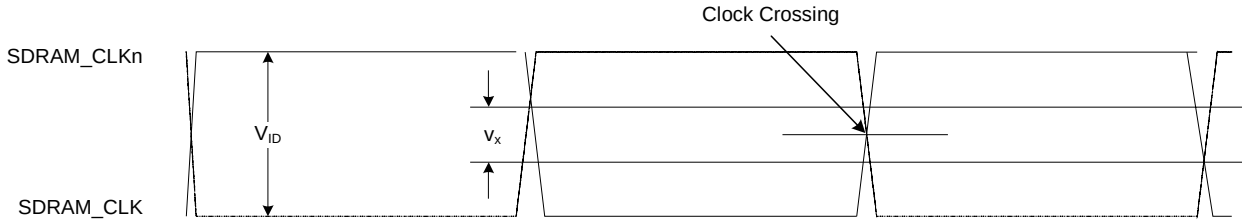


Table 14: Clock Parameters

Symbol	Description	Min	Typical	Max	Units
Vx	Differential Clock Cross over point relative to gnd	0.45*VDDQ	—	0.55*VDDQ	V
VID	DC Differential Output Voltage	1.36	1.44	1.52	V

7.1.2 DDR SDRAM Timing Diagrams and Specifications

Figure 9 through Figure 12 shows the typical LPDDR1 SDRAM timings. Figure 15 shows the skew timings. Refer to Table 15 for the DDR specifications. Refer to the *JEDEC Spec* for complete timing diagrams and specifications.

Figure 9: LPDDR1 SDRAM Timing Diagrams 1

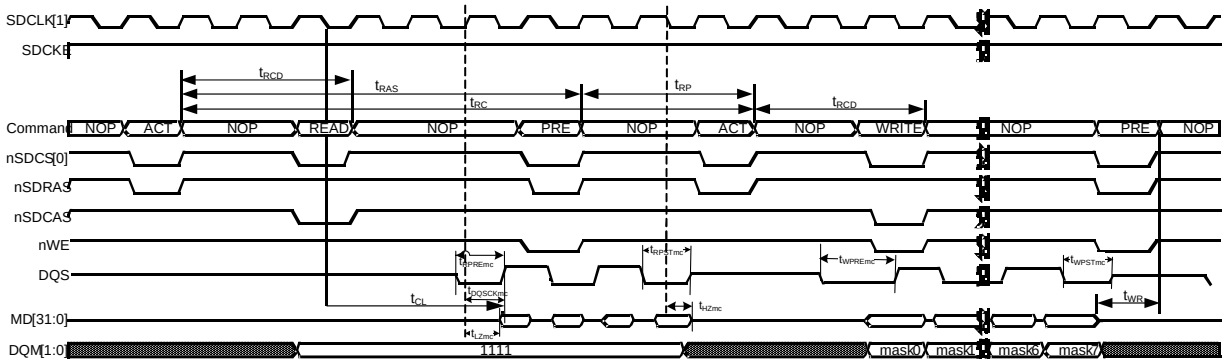


Figure 10: LPDDR1 SDRAM Timing Diagrams 2

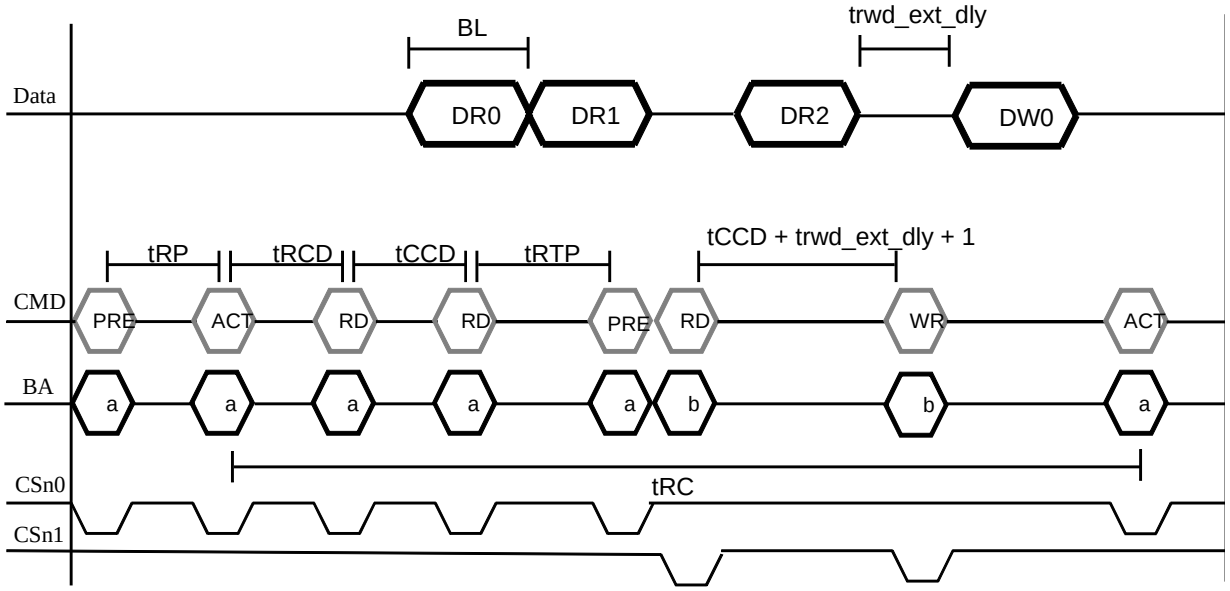


Figure 11: LPDDR1 SDRAM Timing Diagrams 3

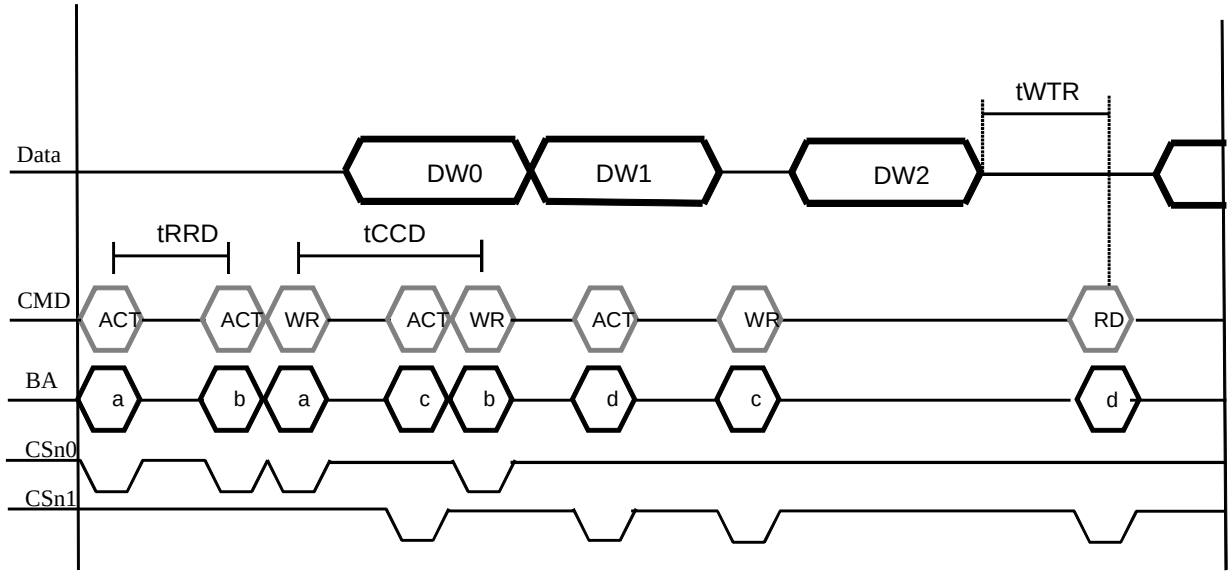


Figure 12: LPDDR1 SDRAM Timing Diagrams 4

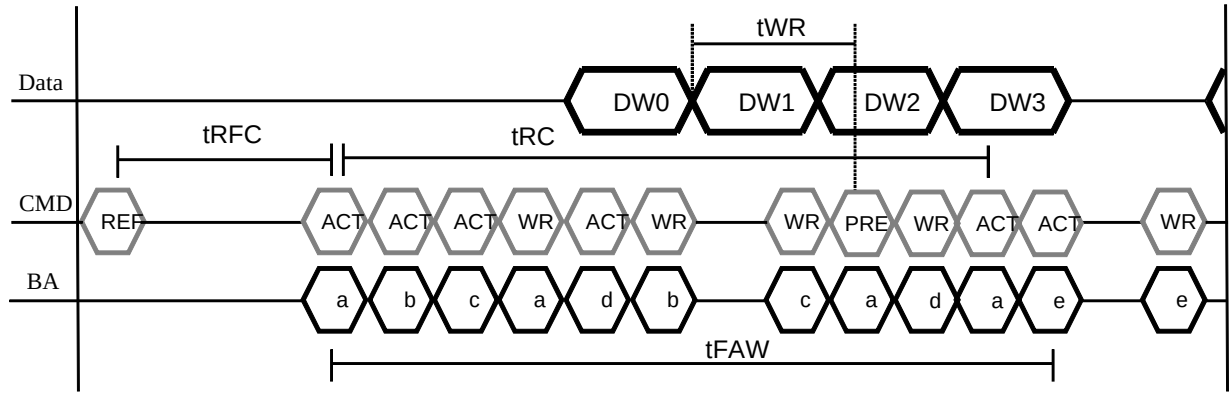
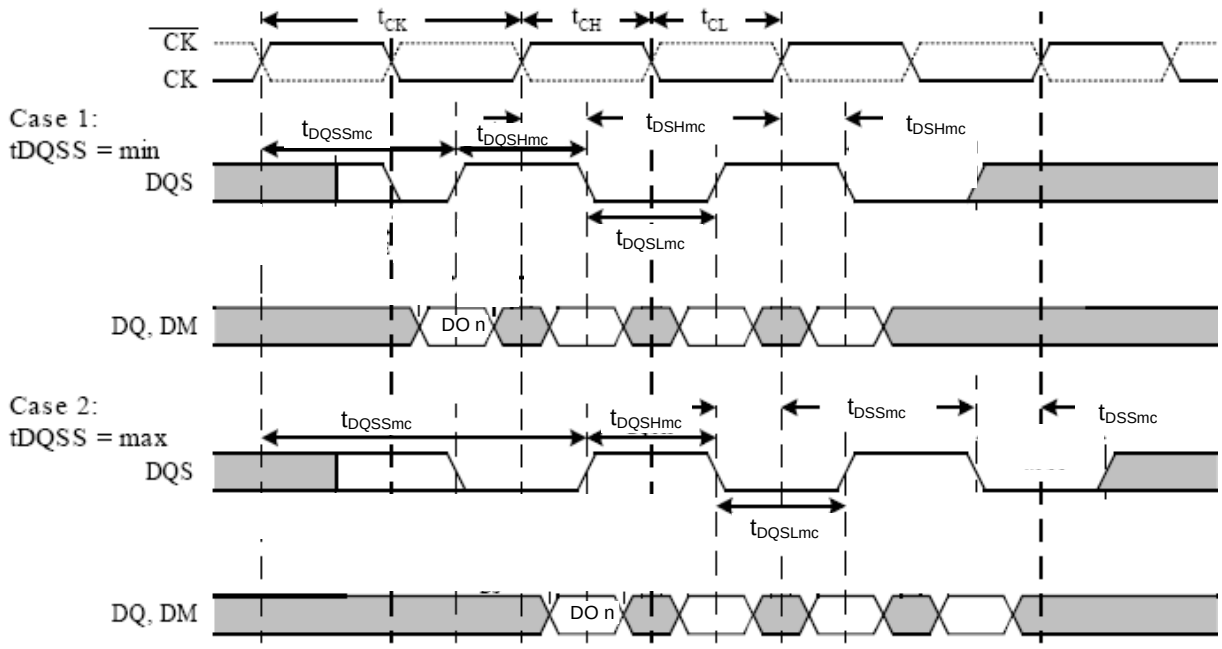


Figure 13 Basic Write Timing Parameters.

Figure 13: Basic Write Timing Parameters



1) DO n = Data Out for column n
2) 3 subsequent elements of Data Out are applied in the programmed order following DO n = Don't Care
3) tDQSS: each rising edge of DQS must fall within the +/-25 % window of the corresponding positive clock edge

7.1.3 DDR SDRAM Skew Timings

Figure 15 shows the Data, Command and Address skew parameters for read and write accesses. Refer to Table 15 for timing specifications for these parameters.

Figure 14 Shows the DQ to DQS skew during Write cycles.

Figure 14: DQ to DQS Write Skew

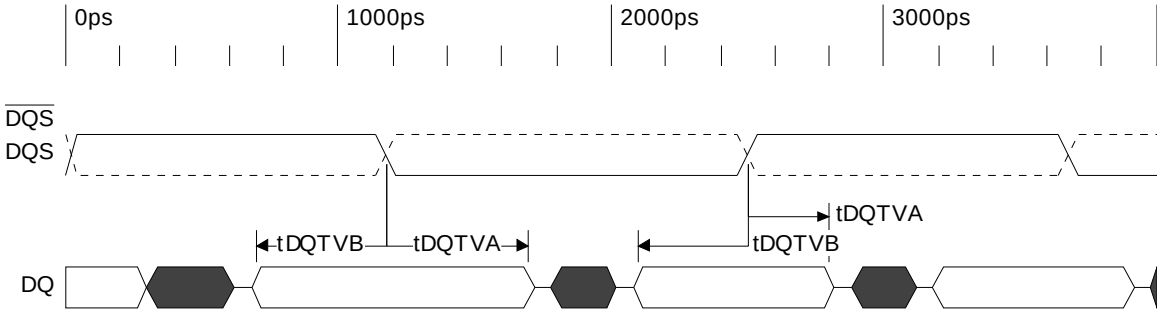


Figure 15 Shows the CLK to Address/Command skew during Write cycles.

Figure 15: CLK to Address/Command Write Skew

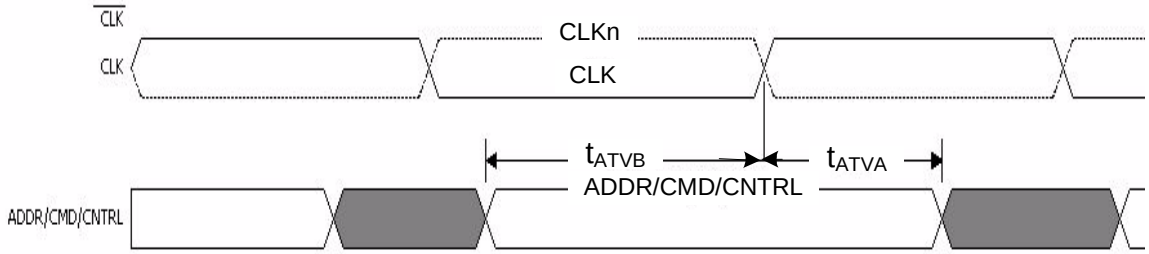


Figure 16 shows the DQS-to-CLK skew during Write cycles.

Figure 16: DQS to CLK Write Skew

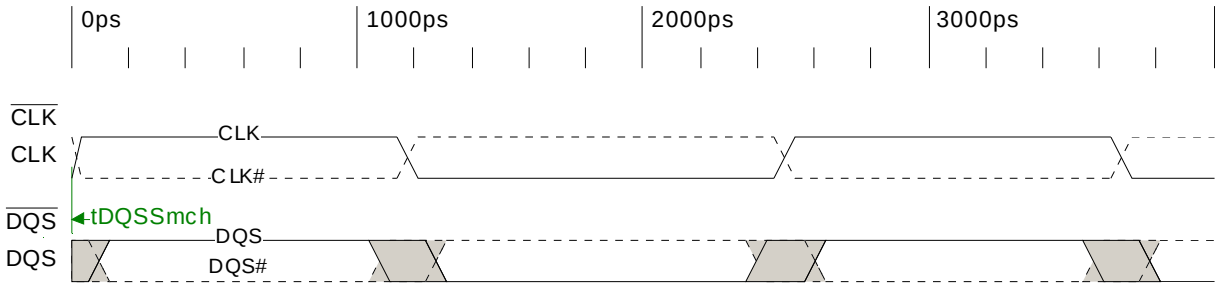


Figure 17 Shows the DQ to DQS allowable skew during read cycles.

Figure 17: DQ to DQS Read Skew

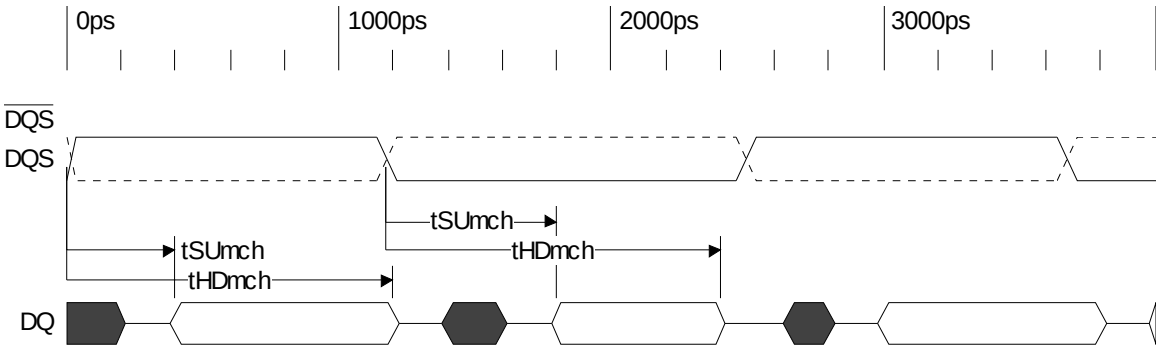


Table 15: DDR Timing Specifications

Symbol	Description	Min	Typical	Max	Units
t_{RCD}	ACTIVE to internal read or write delay time	1	SDRAM_TIMING_2[tRCD]	15	DCLK
t_{RAS}	Active to Precharge command period	1	SDRAM_TIMING_5[tRAS]	63	DCLK
t_{RC}	ACTIVE-to-ACTIVE or REFRESH (same bank) command delay	1	SDRAM_TIMING_1[tRC]	63	DCLK
t_{RP}	Pre-charge command period	1	SDRAM_TIMING_2[tRP]	15	DCLK
t_{CCD}	CAS# to CAS# command delay	1	SDRAM_TIMING_1[tCCD]	7	DCLK
t_{XP}	Exit power down to next valid command delay	1	SDRAM_TIMING_3[tXP] SDRAM_TIMING_3[tXARDS]	7	DCLK
t_{CL}	CAS Latency	1	SDRAM_CTRL4[CAS_LATENCY]	7	DCLK
$t_{CCD\_CCS\_EXT\_DLY}$	CAS# to CAS# read command delay (System level requirement)	1	SDRAM_TIMING_5[tCCD_CCS_EXT_DLY]	7	DCLK
$t_{RWD\_EXT\_DLY}$	READ to WRITE command delay (System level requirement)	1	SDRAM_TIMING_4[tRWD_EXT_DLY]	7	DCLK
$t_{CCD\_CCS\_WR\_EXT\_DLY}$	CAS# to CAS# write command delay		SDRAM[TIMING_5[tCCD_CCS_WR_EXT_DLY]		DCLK
t_{WTR}	Internal write to read delay	1	SDRAM_TIMING_1[tWTR]	15	DCLK
t_{RRD}	ACTIVE bank A to ACTIVE bank B command period	1	SDRAM_TIMING_2[tRRD]	15	DCLK
t_{WR}	Write recovery	1	SDRAM_TIMING_2[tWR]	15	DCLK

Table 15: DDR Timing Specifications (Continued)

Symbol	Description	Min	Typical	Max	Units
t_{FAW}	Maximum number of ACTIVE or per-bank refreshes within this period.	2	SDRAM_TIMING_5[tFAW]	2	DCLK
t_{XSR}	Self refresh exit to next valid command delay	1	SDRAM_TIMING_3[tXSNR] SDRAM_TIMING_3[tXSRD]	511	DCLK
t_{CKE}	CKE minimum pulse width (High and low pulse width)	1	SDRAM_TIMING_4[tCKE]	7	DCLK
t_{MRD}	Mode Register Set command cycle time	1	SDRAM_TIMING_2[tMRD]	7	DCLK
t_{REFI}	Auto-Refresh Interval Counter	1	SDRAM_TIMING_1[tREFI]	65535	FCLK
t_{RFC}	Refresh to Active or Refresh to Refresh internal	1	SDRAM_TIMING_2[tRFC]	511	DCLK
t_{CCD}	CAS# to CAS# command delay	1	SDRAM_TIMING_1[tCCD]	7	DCLK
t_{RTP}	Internal Read to Precharge command delay	1	SDRAM_TIMING_1[tRTP]	7	DCLK
t_{INIT_COUNT}	Power up delay after stable power and clocks	1	SDRAM_TIMING_4[INIT_COUNT]	255	DCLK
$t_{INIT\_COUNT\_NOP}$	Power up delay after stable power and clocks	1	SDRAM_TIMING_4[INIT_COUNT_NOP]	255	DCLK

NOTE:
1. Timing Specified to Reference Load (50 Ohms T line connected to 20pF)
2. The setup and hold timing is for reference slew rate of 1V/ns for DQ and 1V/ns for DQS. For slower slew rates, apply 100ps extra derating for setup/hold.
3. Drive Strength reference setting for timing ZPR=ZNR=0111

Table 16: DDR Timing Specifications for 533 MHz (VDD_M = 1.8V)

Symbol	Description	Min	Typical	Max	Units	Notes
$t_{CK(Jitter)}$	CLK Jitter at output pin (c-c)	-100	—	100	ps	
t_{CL}	Clock low level width	0.47	—	0.53	t_{CK}	
t_{CH}	Clock high level width	0.47	—	0.53	t_{CK}	
t_{CK_DC}	Duty Cycle at output pin	0.42	—	0.53	t_{CK}	
t_{DQTVB}	DQ Valid time before DQS	0.27	—	—	ns	1
t_{DQTVA}	DQ Valid time after DQS	0.3	—	—	ns	1
t_{ATVB}	ADDR/CMD/CNTRL (RAS, CS, CAS, WE, CKE, ADDR) Valid time before CK	0.6	—	—	ns	1

Table 16: DDR Timing Specifications for 533 MHz (VDD_M = 1.8V) (Continued)

Symbol	Description	Min	Typical	Max	Units	Notes
t_{ATVA}	ADDR/CMD/CNTRL (RAS, CS, CAS, WE, CKE, ADDR) Valid time after CK	0.64	—	—	ns	1
t_{DQSSmc}	DQS Output access time from CLK pos edge	—	—	0.08	ns	1
t_{SUmc}	Max Setup skew allowed between DQ and DQS during READ from DQS transition	—	—	0.29	ns	2
t_{HDmc}	Hold factor for valid DQ w.r.t DQS rising/falling edge during READ	0.65	—	—	ns	2
t_{DIPWmc}	DQ and DM output pulse width	0.45	—	—	t_{CK}	
t_{DQSHmc}	DQS output high pulse width	0.45	—	—	t_{CK}	
t_{DQSLmc}	DQS output low pulse width	0.45	—	—	t_{CK}	
t_{DSSmc}	DQS falling edge to CLK-CLKn rising edge	0.4	—	—	t_{CK}	
t_{DSHmc}	DQS falling edge from CLK-CLKn rising edge	0.4	—	—	t_{CK}	
t_{DQSSmc}	Write command to first DQS latching transition	-0.1	—	0.1	t_{CK}	
t_{WPREmc}	DQS write preamble	0.4	—	—	t_{CK}	
t_{WPSTmc}	DQS write postamble	0.45	—	0.55	t_{CK}	
t_{IPWmc}	Address and Control output pulse width	0.9	—	—	t_{CK}	
t_{RPREmc}	DQS read preamble	0.9	—	1.1	t_{CK}	
t_{RPSTmc}	DQS read postamble	0.4	—	0.6	t_{CK}	
$t_{DQSCKmc}$	DQS input access time from CLK/CLKn	2.0	—	7.0	ns	
t_{LZmc}	DQ and DQS low-impedance time from CLK/CLKn	1	—	—	ns	
t_{HZmc}	DQ and DQS high-impedance time from CLK/CLKn	—	—	7	ns	

NOTE:
1. Timing Specified to Reference Load (50 Ohms T line connected to 20pF)
2. The setup & hold timing is for reference slew rate of 1V/ns for DQ and 1V/ns for DQS. For slower slew rates, apply 100ps extra derating for setup/hold.
3. Drive Strength reference setting for timing ZPR=ZNR=0111

Table 17: DDR Timing Specifications for 400 MHz (VDD_M = 1.8V)

Symbol	Description	Min	Typical	Max	Units	Notes
$t_{CK(Jitter)}$	CLK Jitter at output pin (c-c)	-100	—	100	ps	

Table 17: DDR Timing Specifications for 400 MHz (VDD_M = 1.8V) (Continued)

Symbol	Description	Min	Typical	Max	Units	Notes
t_{CL}	Clock low level width	0.47	—	0.53	t_{CK}	
t_{CH}	Clock high level width	0.47	—	0.53	t_{CK}	
t_{CK_DC}	Duty Cycle at output pin	0.42	—	0.53	t_{CK}	
t_{DQTVB}	DQ Valid time before DQS	0.42	—	—	ns	1
t_{DQTVA}	DQ Valid time after DQS	0.42	—	—	ns	1
t_{ATVB}	ADDR/CMD/CNTRL (RAS, CS, CAS, WE, CKE, ADDR) Valid time before CK	0.9	—	—	ns	1
t_{ATVA}	ADDR/CMD/CNTRL (RAS, CS, CAS, WE, CKE, ADDR) Valid time after CK	0.94	—	—	ns	1
t_{DQSSmc}	DQS Output access time from CLK pos edge	—	—	0.06	ns	1
t_{SUmc}	Max Setup skew allowed between DQ and DQS during READ from DQS transition	—	—	0.41	ns	2
t_{HDmc}	Hold factor for valid DQ w.r.t DQS rising/falling edge during READ	0.84	—	—	ns	2
t_{DIPWmc}	DQ and DM output pulse width	0.45	—	—	t_{CK}	
t_{DQSHmc}	DQS output high pulse width	0.45	—	—	t_{CK}	
t_{DQSLmc}	DQS output low pulse width	0.45	—	—	t_{CK}	
t_{DSSmc}	DQS falling edge to CLK-CLKn rising edge	0.4	—	—	t_{CK}	
t_{DSHmc}	DQS falling edge from CLK-CLKn rising edge	0.4	—	—	t_{CK}	
t_{DQSSmc}	Write command to first DQS latching transition	-0.1	—	0.1	t_{CK}	
t_{WPREmc}	DQS write preamble	0.4	—	—	t_{CK}	
t_{WPSTmc}	DQS write postamble	0.45	—	0.55	t_{CK}	
t_{IPWmc}	Address and Control output pulse width	0.9	—	—	t_{CK}	
t_{RPREmc}	DQS read preamble	0.9	—	1.1	t_{CK}	
t_{RPSTmc}	DQS read postamble	0.4	—	0.6	t_{CK}	
$t_{DQSCKmc}$	DQS input access time from CLK/CLKn	2.0	—	7.0	ns	
t_{LZmc}	DQ and DQS low-impedance time from CLK/CLKn	1	—	—	ns	
t_{HZmc}	DQ and DQS high-impedance time from CLK/CLKn	—	—	7	ns	

Table 17: DDR Timing Specifications for 400 MHz (VDD_M = 1.8V) (Continued)

Symbol	Description	Min	Typical	Max	Units	Notes
NOTE: 1. Timing Specified to Reference Load (50 Ohms T line connected to 20pF) 2. The setup & hold timing is for reference slew rate of 1V/ns for DQ and 1V/ns for DQS. For slower slew rates, apply 100ps extra derating for setup/hold. 3. Drive Strength reference setting for timing ZPR=ZNR=0111						

Table 18: DDR Timing Specifications for 200 MHz (VDD_M = 1.8V)

Symbol	Description	Min	Typical	Max	Units	Notes
$t_{CK(Jitter)}$	CLK Jitter at output pin (c-c)	-100	—	100	ps	
t_{CL}	Clock low level width	0.47	—	0.53	t_{CK}	
t_{CH}	Clock high level width	0.47	—	0.53	t_{CK}	
t_{CK_DC}	Duty Cycle at output pin	0.42	—	0.53	t_{CK}	
t_{DQTVB}	DQ Valid time before DQS	1.02	—	—	ns	1
t_{DQTVA}	DQ Valid time after DQS	1.05	—	—	ns	1
t_{ATVB}	ADDR/CMD/CNTRL (RAS, CS, CAS, WE, CKE, ADDR) Valid time before CK	2.1	—	—	ns	1
t_{ATVA}	ADDR/CMD/CNTRL (RAS, CS, CAS, WE, CKE, ADDR) Valid time after CK	2.14	—	—	ns	1
t_{DQSSmc}	DQS Output access time from CLK pos edge	—	—	0.05	ns	1
t_{SUmc}	Max Setup skew allowed between DQ and DQS during READ from DQS transition	—	—	1.04	ns	2
t_{HDmc}	Hold factor for valid DQ w.r.t DQS rising/falling edge during READ	1.46	—	—	ns	2
t_{DIPWmc}	DQ and DM output pulse width	0.45	—	—	t_{CK}	
t_{DQSHmc}	DQS output high pulse width	0.45	—	—	t_{CK}	
t_{DQSLmc}	DQS output low pulse width	0.45	—	—	t_{CK}	
t_{DSSmc}	DQS falling edge to CLK-CLKn rising edge	0.4	—	—	t_{CK}	
t_{DSHmc}	DQS falling edge from CLK-CLKn rising edge	0.4	—	—	t_{CK}	
t_{DQSSmc}	Write command to first DQS latching transition	-0.1	—	0.1	t_{CK}	
t_{WPREmc}	DQS write preamble	0.4	—	—	t_{CK}	
t_{WPSTmc}	DQS write postamble	0.45	—	0.55	t_{CK}	
t_{IPWmc}	Address and Control output pulse width	0.9	—	—	t_{CK}	

Table 18: DDR Timing Specifications for 200 MHz (VDD_M = 1.8V) (Continued)

Symbol	Description	Min	Typical	Max	Units	Notes
t_{RPREmc}	DQS read preamble	0.9	—	1.1	t_{CK}	
t_{RPSTmc}	DQS read postamble	0.4	—	0.6	t_{CK}	
$t_{DQSCKmc}$	DQS input access time from CLK/CLKn	2.0	—	7.0	ns	
t_{LZmc}	DQ and DQS low-impedance time from CLK/CLKn	1	—	—	ns	
t_{HZmc}	DQ and DQS high-impedance time from CLK/CLKn	—	—	7	ns	

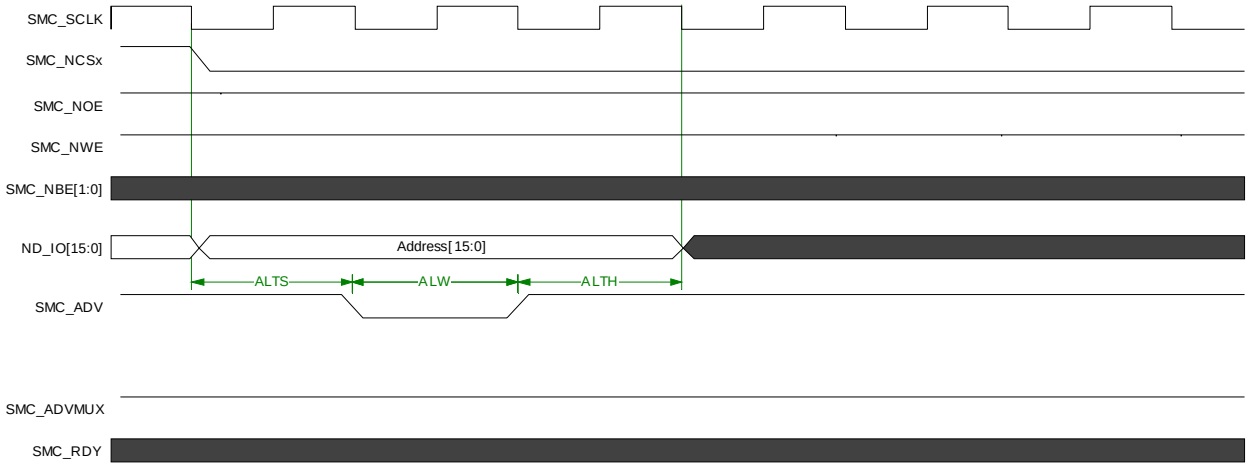
NOTE:
1. Timing Specified to Reference Load (50 Ohms T line connected to 20pF)
2. The setup & hold timing is for reference slew rate of 1V/ns for DQ and 1V/ns for DQS. For slower slew rates, apply 100ps extra derating for setup/hold.
3. Drive Strength reference setting for timing ZPR=ZNR=0111

7.2 Static Memory Controller Timing Diagrams and Specifications

7.2.1 Address Cycle

Figure 18 shows the timing for the address cycles during an A/D Operating mode access. Figure 19 shows the timing for the address cycles during an AA/D Operating mode access.The DFI Configuration Control Register for Chip Selects (SMC_CSDFICFGx) determines each timing parameter using the SMC_SCLK clock frequency. Refer to Table 19 for a list of registers used to program the address phase timing parameters.

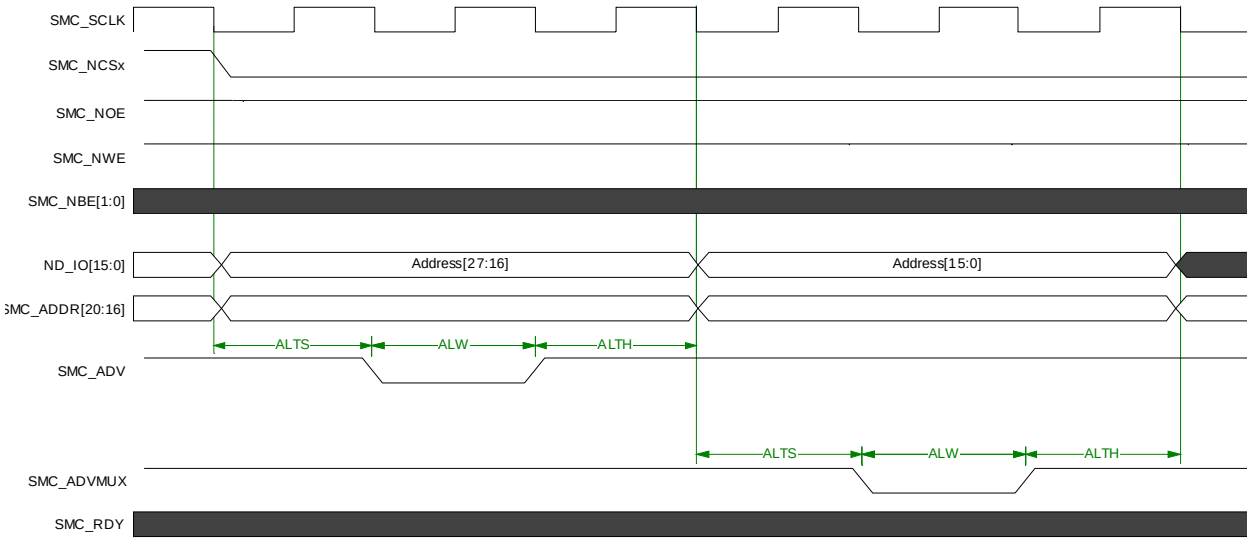
Figure 18: A/D Address Phase



Notes:

1. SMC_CSDFICFGx[ALTS] = 0x1
1. SMC_CSDFICFGx[ALTH] = 0x1
2. SMC_CSDFICFGx[ALW] = 0x1
3. SMC_CSDFICFGx[ADDMODE] = 0x0
4. SMC_WE_APx[WE_AP_VAL] = 0xFFF
5. SMC_OE_APx[OE_AP_VAL] = 0xFFF

Figure 19: AA/D Address Phase



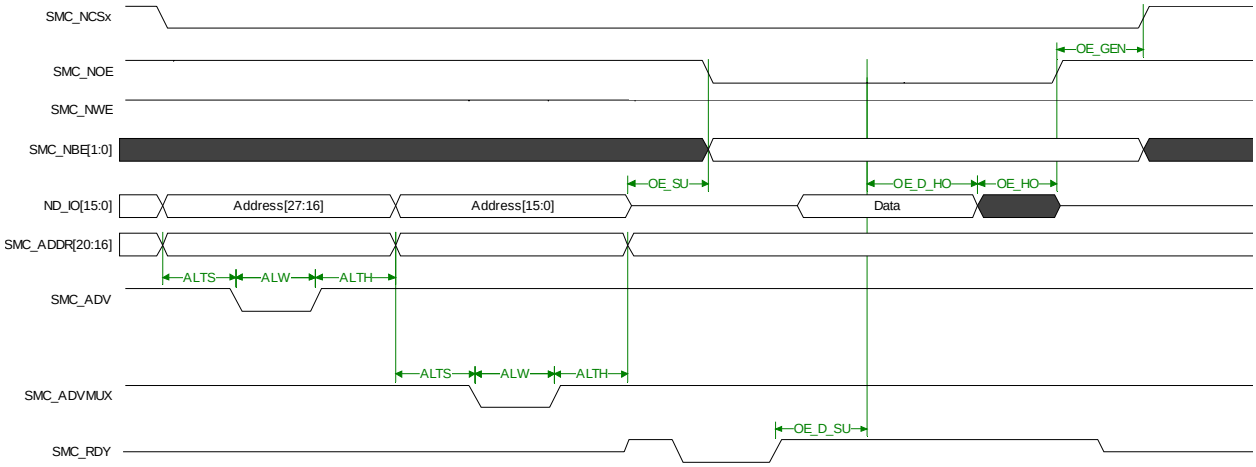
Notes:

1. SMC_CSDFICFGx[ALTS] = 0x1
1. SMC_CSDFICFGx[ALTH] = 0x1
2. SMC_CSDFICFGx[ALW] = 0x1
3. SMC_CSDFICFGx[ADDMODE] = 0x1
4. SMC_WE_APx[WE_AP_VAL] = 0xFFF
5. SMC_OE_APx[OE_AP_VAL] = 0xFFF

7.2.2 Read Access Data Phases

Figure 20 - Figure 23 show timing diagrams of the data phase during Read accesses. The Static Memory Control Register (SMC_MCSx) and Synchronous Static Memory Controller Register (SMC_SXCNFGx) determines each timing parameter using the SMC_SCLK clock frequency. Refer to Table 19 for a list of registers used to program the read data timing parameters.

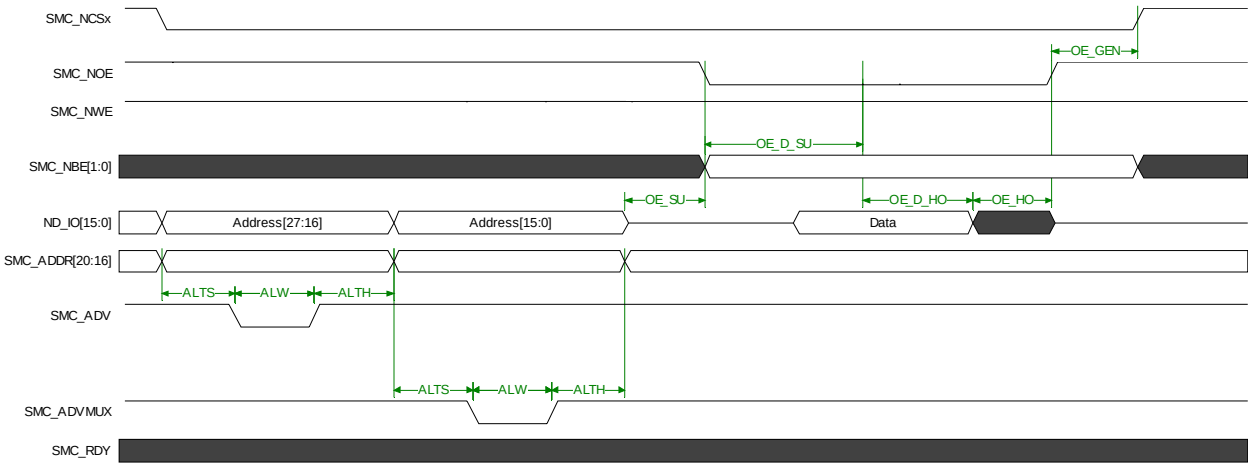
Figure 20: Asynchronous Read With RDY Signal



Notes:

1. SMC_CSDFICFGx[ALTS] = 0x1
1. SMC_CSDFICFGx[ALTH] = 0x1
2. SMC_CSDFICFGx[ALW] = 0x1
3. SMC_WE_APx[WE_AP_VAL] = 0xFFF
4. SMC_OE_APx[OE_AP_VAL] = 0xFFF
5. SMC_MCSx[OE_SU] = 0x1
6. SMC_MCSx[OE_GEN] = 0x1
7. SMC_CSDFICFGx[RDY_SPEC4] = 0x1
8. SMC_CSDFICFGx[RDY_SPEC3] = 0x0
9. SMC_CSDFICFGx[RDY_SPEC2_1] = 0x1 or 0x3
10. SMC_CSDFICFGx[RDY_SPEC0] = 0x1
11. SMC_CSDFICFGx[RDSYNC] = 0x2

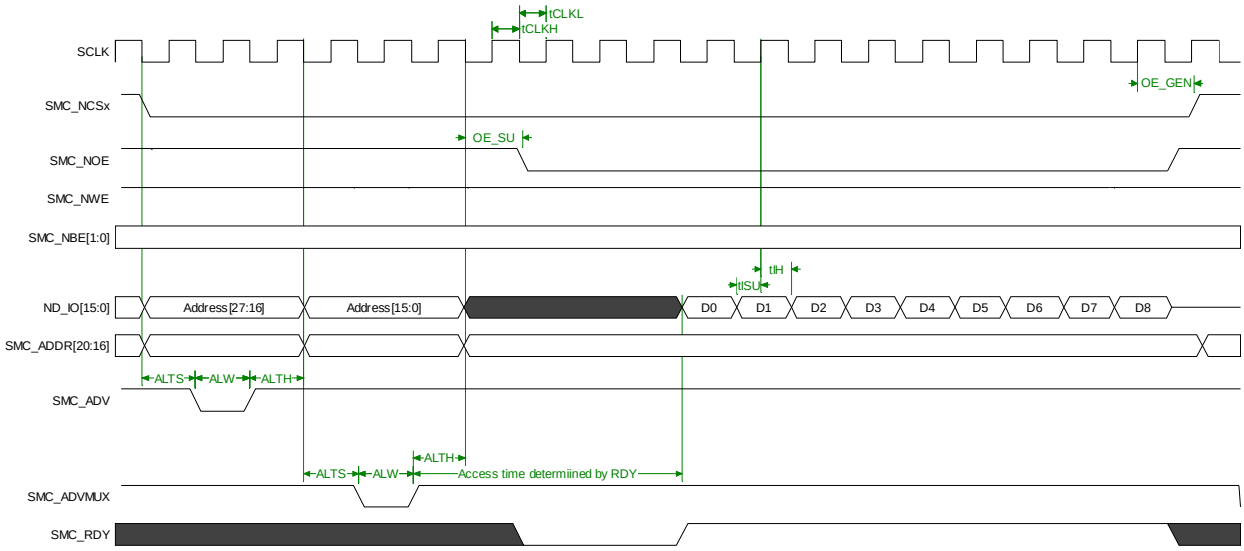
Figure 21: Asynchronous Read Without RDY Signal



Notes:

1. SMC_CSDFICFGx[ALTS] = 0x1
1. SMC_CSDFICFGx[ALTH] = 0x1
2. SMC_CSDFICFGx[ALW] = 0x1
3. SMC_WE_APx[WE_AP_VAL] = 0xFFF
4. SMC_OE_APx[OE_AP_VAL] = 0xFFF
5. SMC_MCSx[OE_SU] = 0x1
6. SMC_MCSx[OE_D_SU] = 0x3
7. SMC_MCSx[OE_D_HO] = 0x3
8. SMC_MCSx[OE_HO] = 0x1
9. SMC_MCSx[OE_GEN] = 0x1
10. SMC_CSDFICFGx[RDY_SPEC2_1] = 0x0 or 0x2
11. SMC_CSDFICFGx[RDSYNC] = 0x0

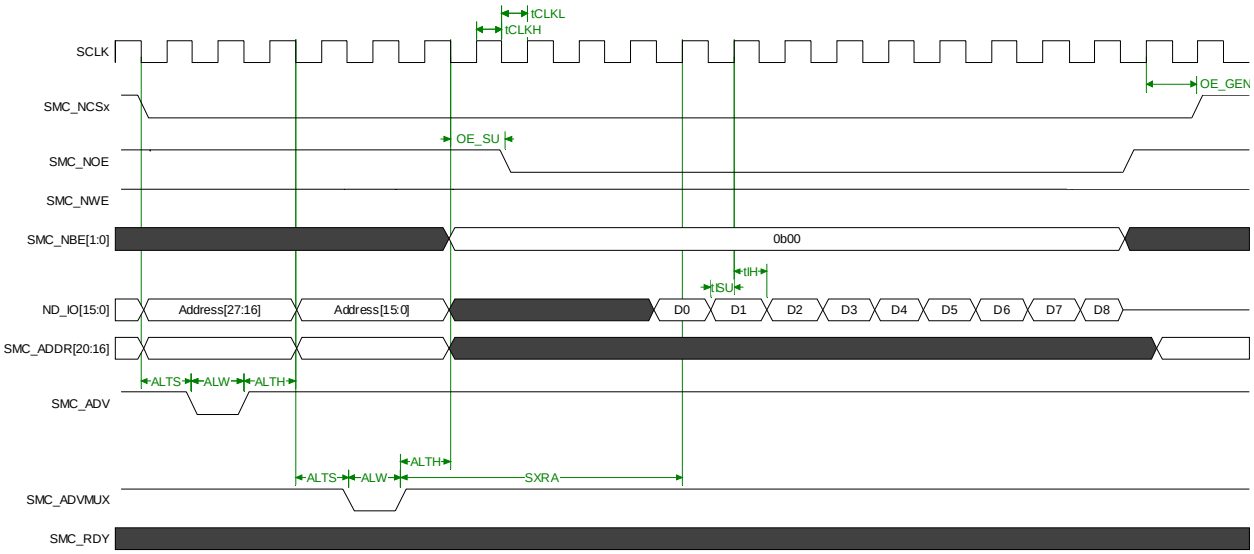
Figure 22: Synchronous Read With RDY Signal



NOTE:

1. SMC_CSDFICFGx[ALTS] = 0x1
1. SMC_CSDFICFGx[ALTH] = 0x1
2. SMC_CSDFICFGx[ALW] = 0x1
3. SMC_WE_APx[WE_AP_VAL] = 0xFFF
4. SMC_OE_APx[OE_AP_VAL] = 0xFFF
5. SMC_SXCNFGx[SXRA] = 0x5
6. SMC_MCSx[OE_SU] = 0x1
7. SMC_MCSx[OE_GEN] = 0x1
8. SMC_CSDFICFGx[RDY_SPEC4] = 0x1
9. SMC_CSDFICFGx[RDY_SPEC3] = 0x0
10. SMC_CSDFICFGx[RDY_SPEC2_1] = 0x1 or 0x3
11. SMC_CSDFICFGx[RDY_SPEC0] = 0x1
12. SMC_CSDFICFGx[RDSYNC] = 0x1

Figure 23: Synchronous Read Without RDY Signal



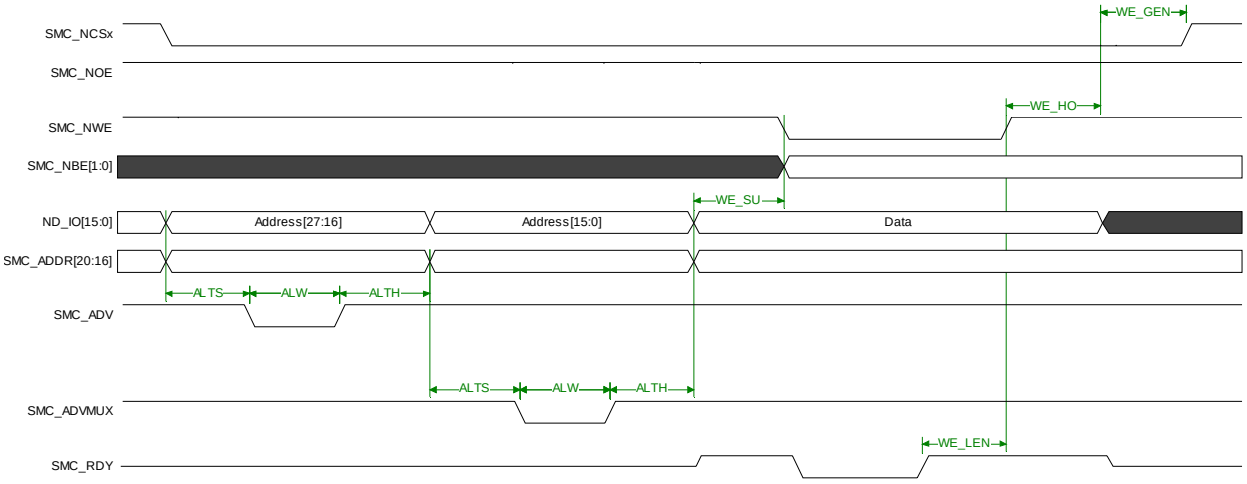
Notes:

1. SMC_CSDFICFGx[ALTS] = 0x1
1. SMC_CSDFICFGx[ALTH] = 0x1
2. SMC_CSDFICFGx[ALW] = 0x1
3. SMC_WE_APx[WE_AP_VAL] = 0xFFF
4. SMC_OE_APx[OE_AP_VAL] = 0xFFF
5. SMC_SXCNFGx[SXRA] = 0x6
6. SMC_MCSx[OE_SU] = 0x1
7. SMC_MCSx[OE_GEN] = 0x1
8. SMC_CSDFICFGx[RDY_SPEC2_1] = 0x0 or 0x2
9. SMC_CSDFICFGx[RDSYNC] = 0x1

7.2.3 Write Access Data Phases

Figure 24 - Figure 27 show timing diagrams of the data phase during Write accesses.The Static Memory Control Register (SMC_MCSx) and Synchronous Static Memory Controller Register (SMC_SXCNFGx) determines each timing parameter using the SMC_SCLK clock frequency. Refer to Table 19 for a list of registers used to program the write data timing paramaters.

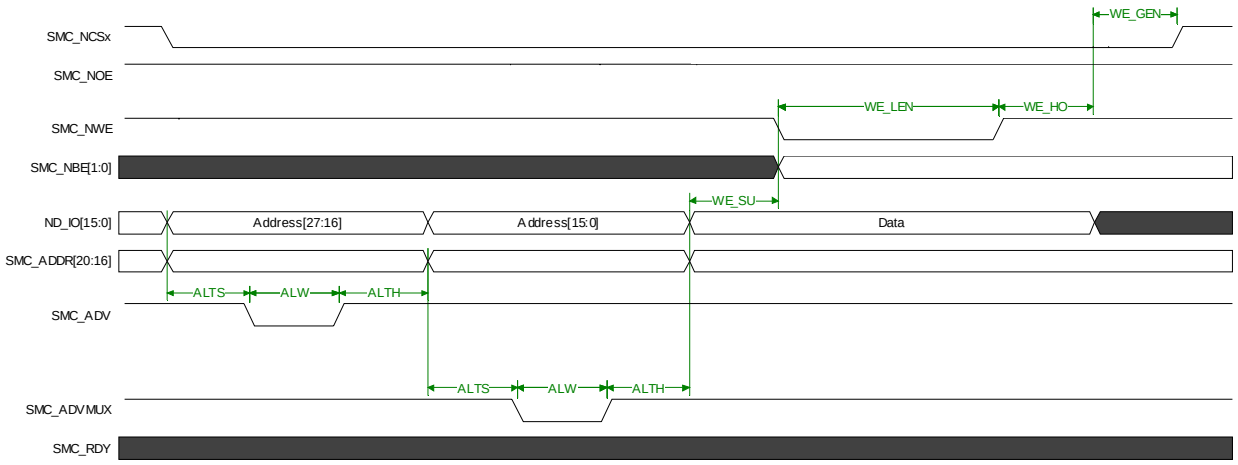
Figure 24: Asynchronous Write With RDY Signal



Notes:

1. SMC_CSDFICFGx[ALTS] = 0x1
2. SMC_CSDFICFGx[ALTH] = 0x1
3. SMC_CSDFICFGx[ALW] = 0x1
4. SMC_WE_APx[WE_AP_VAL] = 0xFFF
5. SMC_OE_APx[OE_AP_VAL] = 0xFFF
6. SMC_MCSx[WE_SU] = 0x1
7. SMC_MCSx[WE_LEN] = 0x1
8. SMC_MCSx[WE_D_HO] = 0x1
9. SMC_CSDFICFGx[RDY_SPEC4] = 0x1
10. SMC_CSDFICFGx[RDY_SPEC3] = 0x0
11. SMC_CSDFICFGx[RDY_SPEC2_1] = 0x2 or 0x3
12. SMC_CSDFICFGx[RDY_SPEC0] = 0x1
13. SMC_CSDFICFGx[WRSYNC] = 0x0

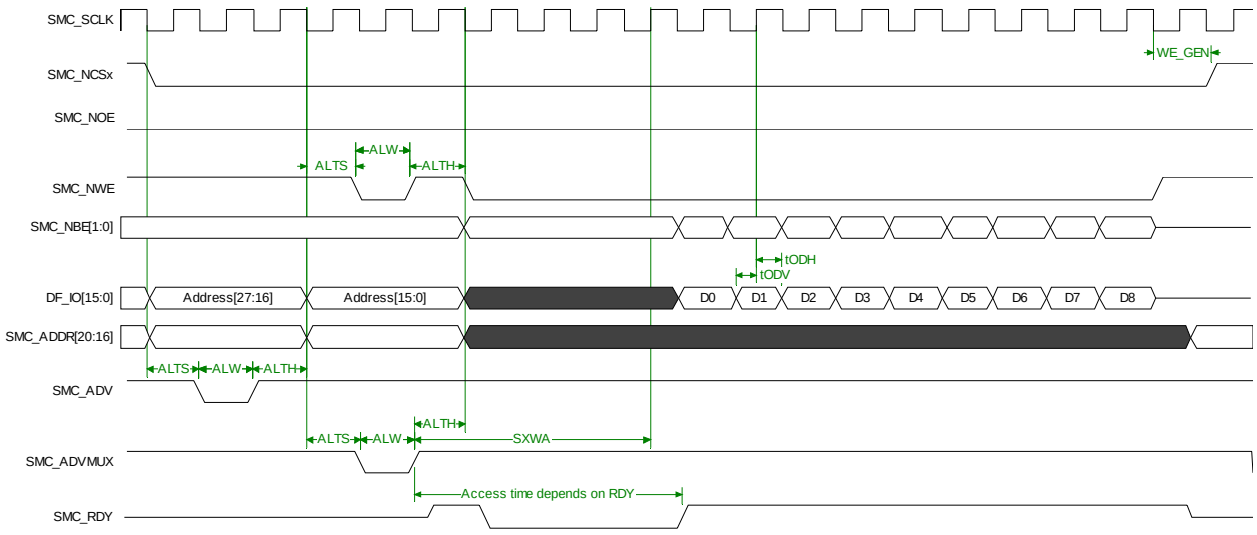
Figure 25: Asynchronous Write Data Phase Without RDY Signal



Notes:

1. SMC_CSDFICFGx[ALTS] = 0x1
2. SMC_CSDFICFGx[ALTH] = 0x1
3. SMC_CSDFICFGx[ALW] = 0x1
4. SMC_WE_APx[WE_AP_VAL] = 0xFFF
5. SMC_OE_APx[OE_AP_VAL] = 0xFFF
6. SMC_MCSx[WE_SU] = 0x1
7. SMC_MCSx[WE_LEN] = 0x1
8. SMC_MCSx[WE_D_HO] = 0x1
9. SMC_CSDFICFGx[RDY_SPEC2_1] = 0x0 or 0x1
10. SMC_CSDFICFGx[WRSYNC] = 0x2

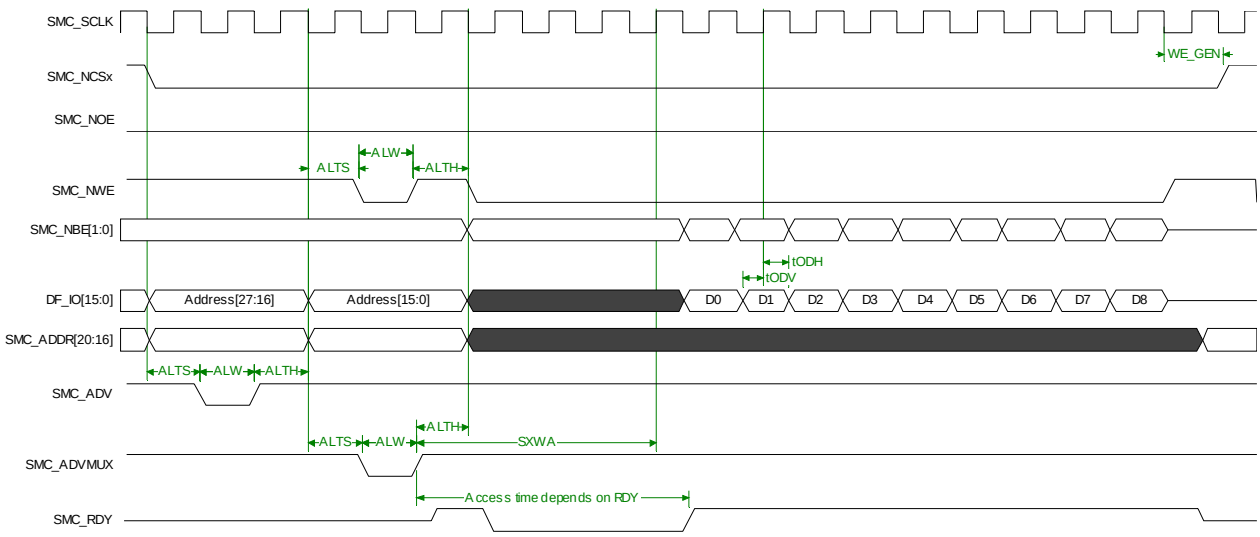
Figure 26: Synchronous Write With RDY Signal



Notes:

1. SMC_CSDFICFGx[ALTS] = 0x1
1. SMC_CSDFICFGx[ALTH] = 0x1
2. SMC_CSDFICFGx[ALW] = 0x1
3. SMC_WE_APx[WE_AP_VAL] = 0xFF7
4. SMC_OE_APx[OE_AP_VAL] = 0xFFF
5. SMC_CSDFICFGx[RDY_SPEC4] = 0x1
6. SMC_CSDFICFGx[RDY_SPEC3] = 0x0
7. SMC_CSDFICFGx[RDY_SPEC2_1] = 0x2 or 0x3
8. SMC_CSDFICFGx[RDY_SPEC0] = 0x1
9. SMC_CSDFICFGx[WRSYNC] = 0x1
10. SMC_SXCNFGx[SXWA] = 0x5

Figure 27: Synchronous Write Data Phase Without RDY Signal



Notes:

1. SMC_CSDFICFGx[ALTS] = 0x1
1. SMC_CSDFICFGx[ALTH] = 0x1
2. SMC_CSDFICFGx[ALW] = 0x1
3. SMC_WE_APx[WE_AP_VAL] = 0xFF7
4. SMC_OE_APx[OE_AP_VAL] = 0xFFF
5. SMC_SXCNFGx[SXWA] = 0x5
6. SMC_CSDFICFGx[RDY_SPEC2_1] = 0x0 or 0x1
7. SMC_CSDFICFGx[WRSYNC] = 0x1

Table 19: Static Memory Controller Interface Timing Specifications

Symbol	Description	Min[2]	Min[3]	Typical	Max	Units
t_{CK}	SMC_SCLK frequency	31.2	62.4	PMUA_SMC_CLK_RES_CTRL[SMC_CLK_SEL]	62.4	MHz
WE_GEN	Delay after the last data is latched until the chip select is de-asserted.	1	1	SMC_MCSx[WE_GEN]	3	SMC_SCLK
WE_D_HO	Data hold cycles after SMC_nWE latches the data	1	1	SMC_MCSx[WE_D_HO]	7	SMC_SCLK
WE_D_SU	Data setup time prior to SMC_nWE assertion	1	1	SMC_MCSx[WE_D_SU]	7	SMC_SCLK

Table 19: Static Memory Controller Interface Timing Specifications (Continued)

Symbol	Description	Min[2]	Min[3]	Typical	Max	Units
WE_LEN	Length of the SMC_nWE latch	1	1	SMC_MCSx[WE_LEN]	63	SMC_SCLK
OE_GEN	Delay after the last data is latched until the chip select is de-asserted.	1	1	SMC_MCSx[OE_GEN]	7	SMC_SCLK
OE_HO	Data hold cycles after SMC_nOE latches data	1	1	SMC_MCSx[OE_HO]	3	SMC_SCLK
OE_SU	Setup time prior to SMC_nOE assertion	1	1	SMC_MCSx[OE_SU]	7	SMC_SCLK
OE_D_HO	Hold prior to SMC_NOE de-assertion	1	1	SMC_MCSx[OE_D_HO]	7	SMC_SCLK
OE_D_SU	Read data setup prior to SMC_nOE latching the data.	1	1	SMC_MCSx[OE_D_SU]	63	SMC_SCLK
ALTS	Address Latch setup time	0	0	SMC_CSDIFCFGx[ALTS]	2	SMC_SCLK
ALTH	Address Latch hold time	0	0	SMC_CSDIFCFGx[ALTH]	2	SMC_SCLK
ALW	Address latch width	1	1	SMC_CSDIFCFGx[ALTW]	7	SMC_SCLK
SXWA	Access time for synchronous writes	3	3	SMC_SXCNFGx[SXWA]	10	SMC_SCLK
SXRA	Access time for synchronous reads	3	3	SMC_SXCNFGx[SXRA]	10	SMC_SCLK
t_{ISU}	Synchronous Read data setup time	4.04	4.04	—	—	ns
t_{IH}	Synchronous Read data hold time	2.0	2.0	—	—	ns
t_{ODV}	Synchronous Write data valid before SMC_SCLK	14.7	6.7	—	—	ns
t_{ODH}	Synchronous Write data hold time	17.3	9.3	—	—	ns

1. SMC_SCLK frequency depends on the APMU_SMC_CLK_RES_CTRL[SMC_CLK_SEL] programmed value
2. SMC_SCLK = 31.2 MHz (APMU_SMC_CLK_RES_CTRL[SMC_CLK_SEL = 0x1])
3. SMC_SCLK = 62.4 MHz (APMU_SMC_CLK_RES_CTRL[SMC_CLK_SEL = 0x0])

7.3 NAND Timing Diagrams and Specifications

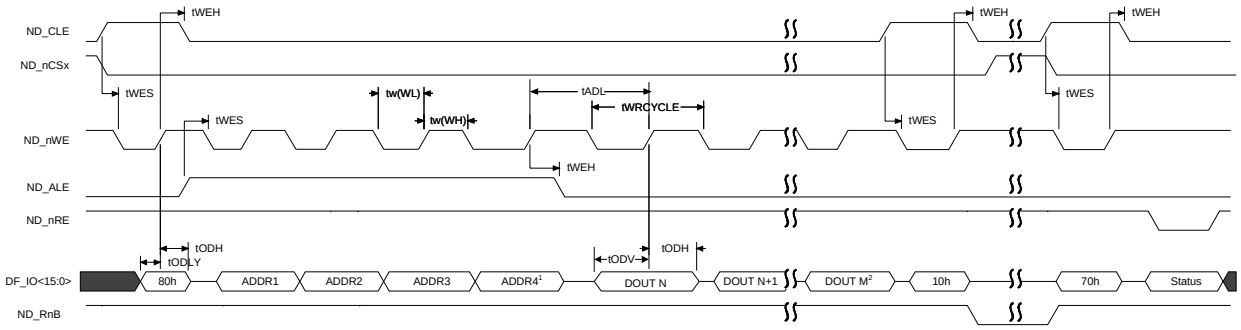
This section describes the timing diagrams for NAND flash programming, Erase, Read, Status Read, and ID Read with timing parameters.

7.3.1 NAND Flash Program Timing

Figure 28 illustrates the programming sequence for a Flash device. The Flash device is addressed with up to seven cycles depending on the value of Number of Address Cycles field (ADDR_CYC) in the NAND Controller Command Buffer 0 (NDCB0) register and the external NAND device requirements. Refer to Table 20 for the detailed descriptions of the timing parameters.

If the Auto-read Status bit (AUTO_RS) is set in the command, the NAND Flash Controller performs a status check (Command 0x70) to determine whether the program operation was successful.

Figure 28: NAND Flash Program Timing Diagram



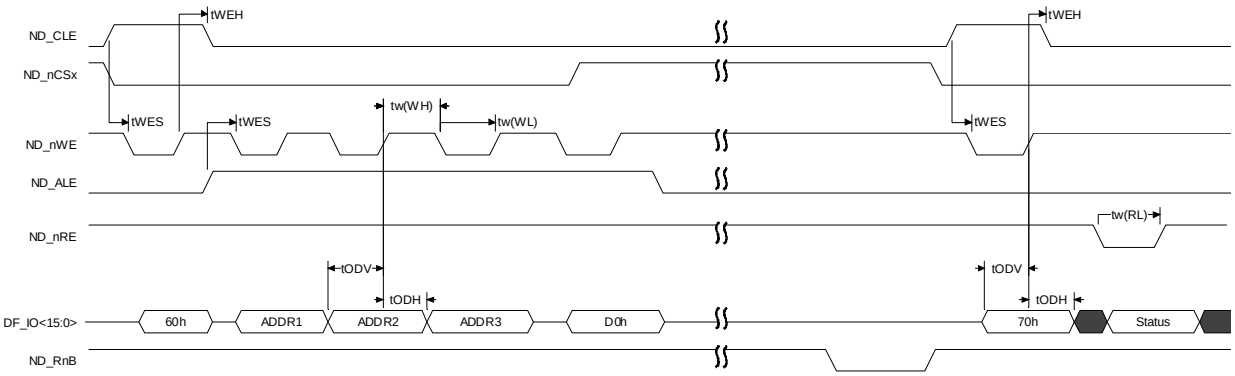
1. The number of address cycles depends on the NAND device being accessed and NDCB0[ADDR_CYC].
2. M is defined by the NDCR[PAGE_SZ], NDCR[SPARE_EN] and NDCR[ECC_EN] values.

7.3.2 NAND Flash Erase Timing

Figure 29 illustrates the erase sequence for a Flash device. The block to be erased in the Flash device is addressed in up to seven cycles depending on the value of Number of Address Cycles field (ADDR_CYC) in the NAND Controller Command Buffer 0 (NDCB0) register and the external NAND device requirements. Refer to Table 20 for the detailed descriptions of the timing parameters.

If the Auto-read Status bit (AUTO_RS) is set in the command, the NAND Flash Controller performs a status check (Command 0x70) to determine whether the Erase operation was successful.

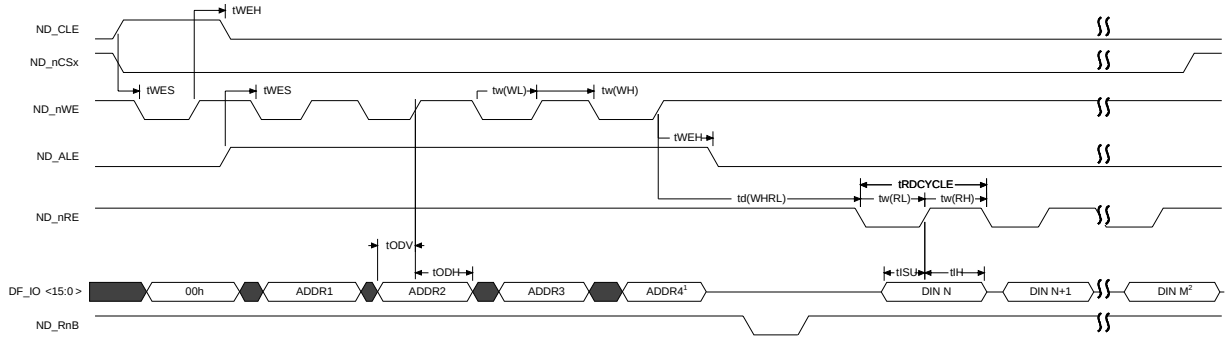
Figure 29: NAND Flash Erase Timing Diagram



7.3.3 Small Block NAND Flash Read Timing

Figure 30 illustrates the Read sequence for a Small-block Flash device. The Flash device is addressed in four cycles. Refer to Table 20 for detailed descriptions of the timing parameters.

Figure 30: NAND Flash Small Block Read Timing Diagram

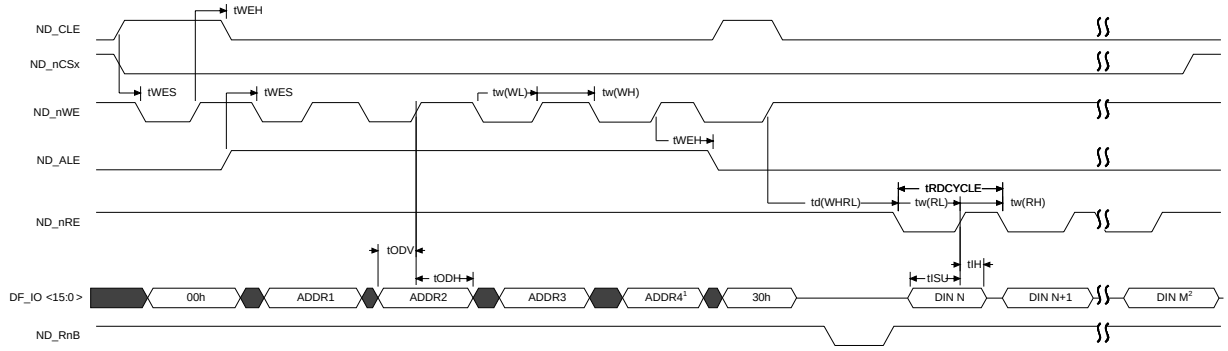


1. The number of address cycles depends on the NAND device being accessed and NDCB0[ADDR_CYC].
2. M is defined by the NDCR[PAGE_SZ], NDCR[SPARE_EN] and NDCR[ECC_EN] values.

7.3.4 Large Block NAND Flash Read Timing

Figure 31 illustrates the Read sequence for a Large-block Flash device. The Flash device is addressed in up to seven cycles depending on the value of Number of Address Cycles field (ADDR_CYC) in the NAND Controller Command Buffer 0 (NDCB0) register and the external NAND device requirements. Refer to Table 20 for detailed descriptions of the timing parameters.

Figure 31: NAND Flash Large Block Read Timing Diagram

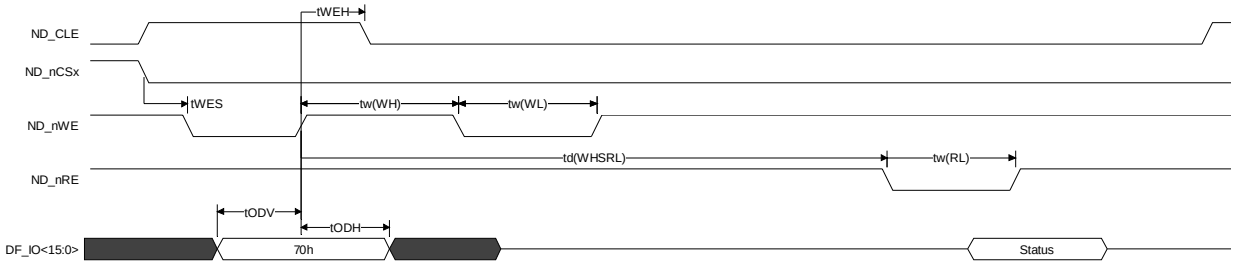


1. The number of address cycles depends on the NAND device being accessed and NDCB0[ADDR_CYC].
2. M is defined by the NDCR[PAGE_SZ], NDCR[SPARE_EN] and NDCR[ECC_EN] values.

7.3.5 NAND Flash Status Read Timing

Figure 32 illustrates the Status-Read sequence for a Flash device. Refer to Table 20 for detailed descriptions of the timing parameters.

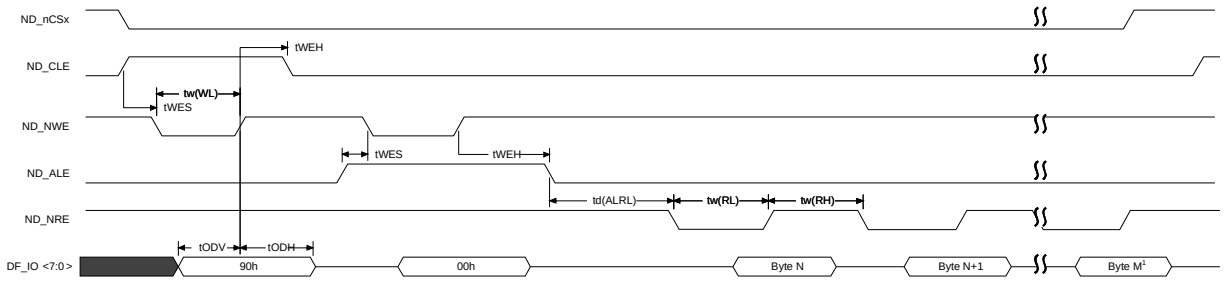
Figure 32: NAND Flash Status Read Timing Diagram



7.3.6 NAND Flash ID Read Timing

Figure 33 illustrates the ID Read sequence for a Flash device. Refer to Table 20 for detailed descriptions of the timing parameters.

Figure 33: NAND Flash ID Read Timing Diagram

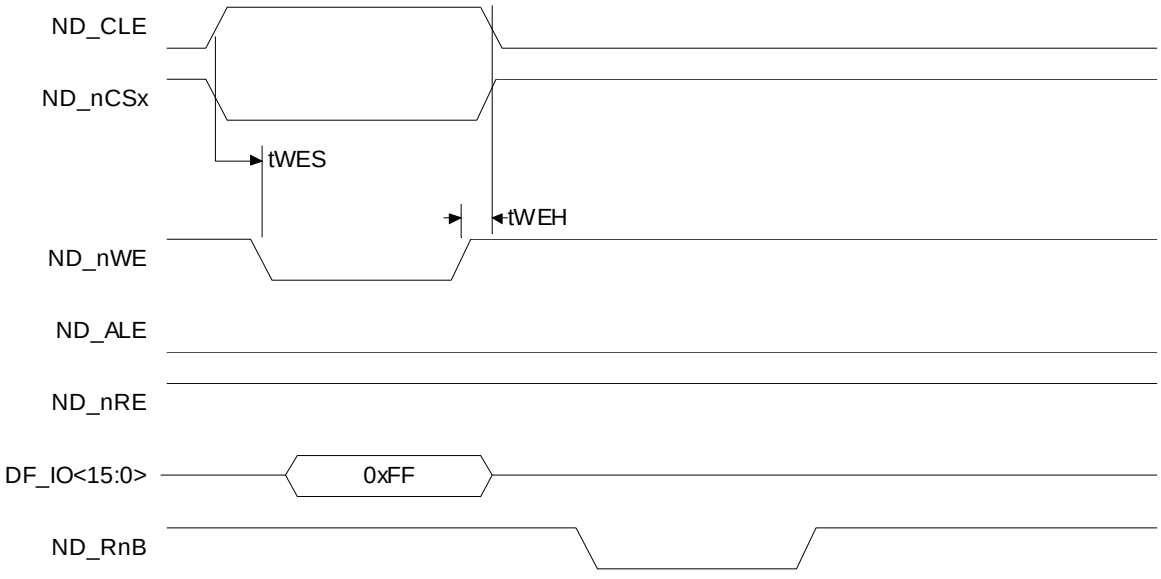


1. The total number of bytes is determined by the NDCR[RD_ID_CNT] value

7.3.7 NAND Flash Reset Timing

Figure 34 illustrates the reset sequence for a Flash device. Refer to Table 20 for detailed descriptions of the timing parameters.

Figure 34: NAND Flash Reset Timing Diagram



7.3.7.1 NAND Flash Timing Parameters

Table 20 provides the values for the timing parameters seen in Figure 28, Figure 29, Figure 30, Figure 31, Figure 31, Figure 32, Figure 33 and Figure 34.

Table 20: NAND Flash Interface Program Timing Specifications

Symbol	Description	Min[1]	Min[2]	Typical	Max	Units
t_{WES}	Setup time of ND_CLE, ND_ALE, ND_nCS to ND_nWE falling	1	1	NDTR0CS0[tCS] + 1	8	NCLK
t_{WEH}	Hold time from ND_nWE rising to ND_CLE and ND_ALE falling	2	2	Max (NDTR0CS0(tCH), NDTR0CS0(tWH)) + 1	8	NCLK
$t_{w(WL)}$	ND_nWE low pulse width	2	2	NDTR0CS0[tWP] + 1	8	NCLK
$t_{w(WH)}$	ND_nWE high pulse width	2	2	Max (TR0CS0(tCH), TR0CS0(tWH)) + 1	8	NCLK
$t_{w(RL)}$	ND_nRE low pulse width	2	2	NDTR0CS0[etRP, tRP] + 1	16	NCLK
$t_{w(RH)}$	ND_nRE high pulse width	2	2	NDTR0CS0[tRH] + 1	8	NCLK
$t_{d(WHRL)}$	ND_nWE rising to ND_nRE falling delay for Read	3900	3900	(NDTR1CS0[tR] + 2) + (NDTR0CS0[tCH] + 1)	65536[4] 1048576[5]	NCLK
$t_{d(WHRL)}$	ND_nWE rising to ND_nRE falling delay for Status Read/ Read ID	8	8	max(tWH,tCH) + max(tAR, max(0, tWHR-max(tWH,tCH))) + 3	15	NCLK
$t_{d(ALRL)}$	ND_ALE falling to ND_nRE falling delay for ID read	8	8	Max(NDTR1CS0(tAR),max(0,NDTR1CS0(tWHR) - max(NDTR0CS0(tWH, tCH))) + 2	15	NCLK
t_{ADL}	Final ND_nWE rising edge during the Address cycle to first ND_nWE rising edge during the Data cycle	1	1	max(tWH,tCH) + max(0, tADL-tWP-3) + tWP + 8	28	NCLK
t_{RHW}	Last ND_nRE rising edge to the first falling edge of ND_nWE when read command is immediately followed by another command.	1	1	NDTR1CS0[tRHW]	3	NCLK
t_{ODH}	DF_IO<15:0> output data hold time after ND_nWE rising	12.8	25.6	—	—	ns
t_{ODV}	DF_IO<15:0> data valid time before ND_nWE rising	19.2	38.5	—	—	ns
t_{Isu}	DF_IO<15:0> setup time requirement to nRE rising	3.7	3.7	—	—	ns
t_{IH}	DF_IO<15:0> hold time requirement to nRE rising	3.2	3.2	—	—	ns
$t_{RDCYCLE}$	Read cycle times	32	64	—	—	ns
$t_{WRCYCLE}$	Write cycle times	32	64	—	—	ns

Table 20: NAND Flash Interface Program Timing Specifications (Continued)

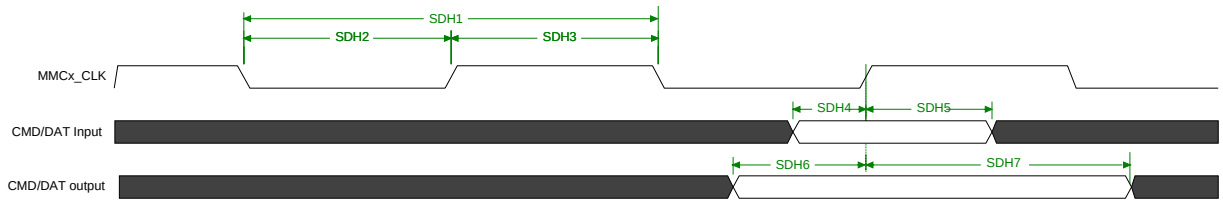
Symbol	Description	Min[1]	Min[2]	Typical	Max	Units

NOTE:
1. NCLK represents the clock period using a 156 MHz clock (APMU_NFC_CLK_RES_CTRL[NF_CLK_SEL] = 0)
2. NCLK represents the clock period using a 78 MHz clock (APMU_NFC_CLK_RES_CTRL[NF_CLK_SEL] = 1)
3. Refer to the *Aspen (88AP168) Processor Software Specifications Manual* for more information on the NDTR0CS0 and NDTR0CS1 registers.
4. NDTR1CS0[Prescale] = 0
5. NDTR1CS0[Prescale] = 1

7.4 SD Host Controller (SDH) Timing Diagrams and Specifications

Figure 35 and Table 21 define the MultiMedia Card Controller (MMC) AC timing specifications. Figure 35 and Table 22 define the Secure Digital (SD), and Secure Digital I/O (SDIO) AC timing specifications.

Figure 35: MultiMedia Card Timing Diagrams



Notes:
1. CMD/DAT input are inputs to the SD Host Controller and outputs from the card
2. CMD/DAT output are outputs from the SD Host Controller and inputs to the card

Table 21: MultiMedia Card Timing Specifications

Symbol	Parameter	Min	Max	Unit	Notes
SDH1	MMCx_CLK Frequency in Full Speed MMC Data Transfer Mode	0	26	MHz	1
SDH1	MMCx_CLK Frequency in High Speed MMC Data Transfer Mode	0	52	MHz	1
SDH1	MMCx_CLK Frequency Identification Mode	0	400	kHz	1
SDH2	Clock low time	9.6	—	ns	
SDH3	Clock high time	9.6	—	ns	
SDH4	Data input setup time	3.3	—	ns	
SDH5	Data input hold time	3	—	ns	

Table 21: MultiMedia Card Timing Specifications (Continued)

Symbol	Parameter	Min	Max	Unit	Notes
SDH6	Output data setup time	6.6	—	ns	
SDH7	Output data hold time	10.8	—	ns	

NOTE:
1. MMCx_CLK clock frequency is determined by the APMU_SDHx_CLK_RES_CTRL[SDH1_CLK_SEL] and SD_CLOCK_CTRL[SD_FREQ_SEL] register fields.

Table 22: SD/SDIO Timing Specifications

Symbol	Parameter	Min	Max	Unit	Notes
SDH1	MMCx_CLK Frequency in Full Speed SD/SDIO Data Transfer Mode	0	24	MHz	1
SDH1	MMCx_CLK Frequency in High Speed SD/SDIO Data Transfer Mode	0	48	MHz	1
SDH1	MMCx_CLK Frequency Identification Mode	0	400	kHz	1
SDH2	Clock low time	10.4	—	ns	
SDH3	Clock high time	10.4	—	ns	
SDH4	Data input setup time	3.3	—	ns	
SDH5	Data input hold time	3	—	ns	
SDH6	Output data setup time	7.4	—	ns	
SDH7	Output data hold time	11.6	—	ns	

NOTE:
1. MMCx_CLK clock frequency is determined by the APMU_SDHx_CLK_RES_CTRL[SDH1_CLK_SEL] and SD_CLOCK_CTRL[SD_FREQ_SEL] register fields.

7.5 LCD Controller Timing Diagrams and Specifications

Refer to the pins chapter in the *Marvell® Armada 16x Applications Processor Family Software Manual* for descriptions of the signals shown in Figure 36 through Figure 39 and in Table 24.

7.5.1 LCD Smart Panel Timing and Specifications

This section details the LCD Smart Panel timing requirements. Additional registers as shown in Table 24 are used to configure the LCD controller for smart panel operation.

Figure 36: Smart Panel Interface 8-bit 8080-Series Parallel Mode Read Interface Protocol

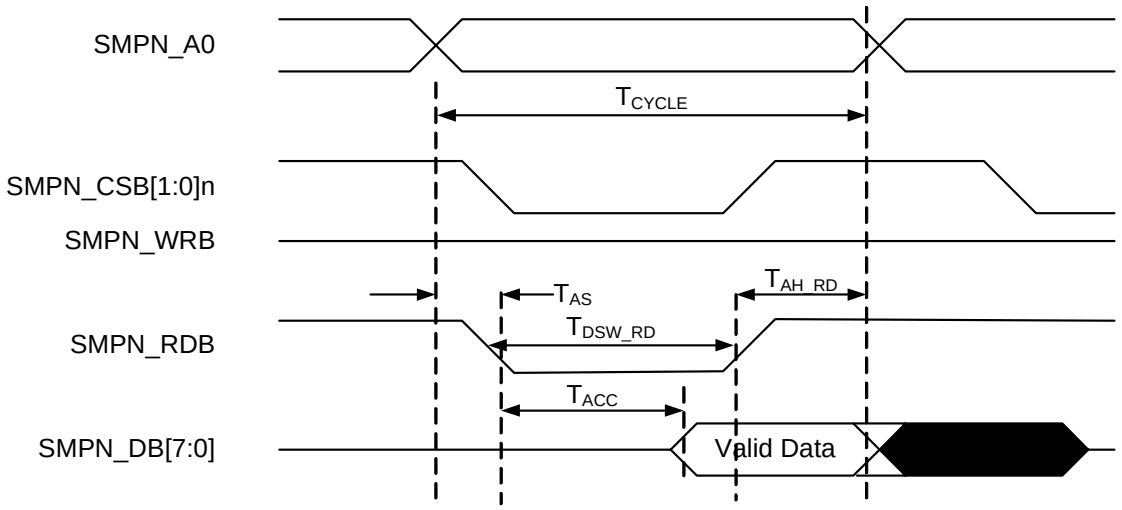


Figure 37: Smart Panel Interface 8-bit 8080-Series Parallel Mode Write Interface Protocol

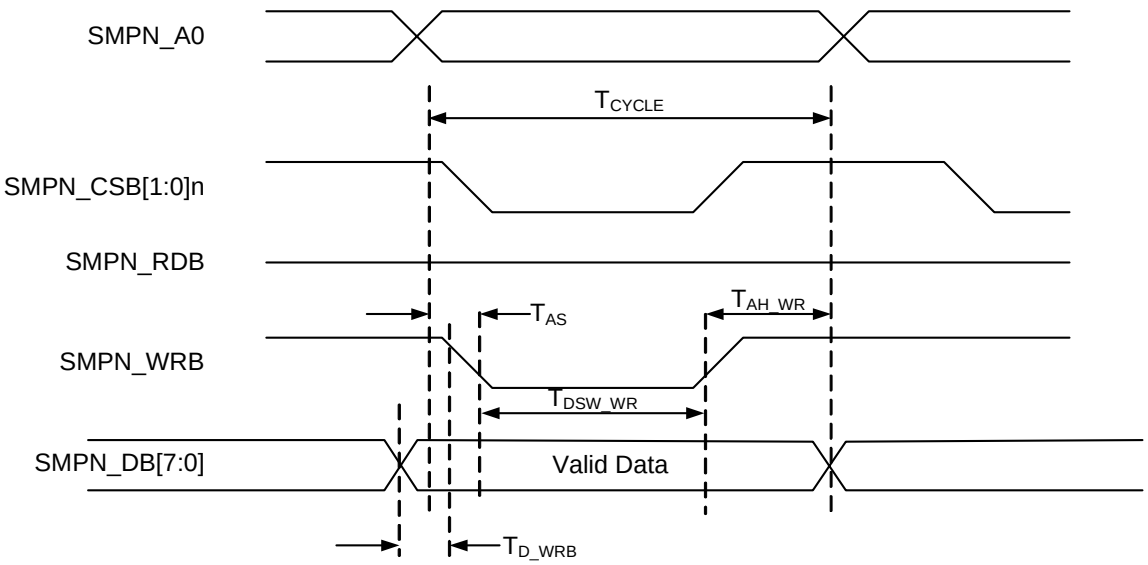


Figure 38: Smart Panel Interface 8-bit 6800-Series Parallel Mode Read Interface Protocol

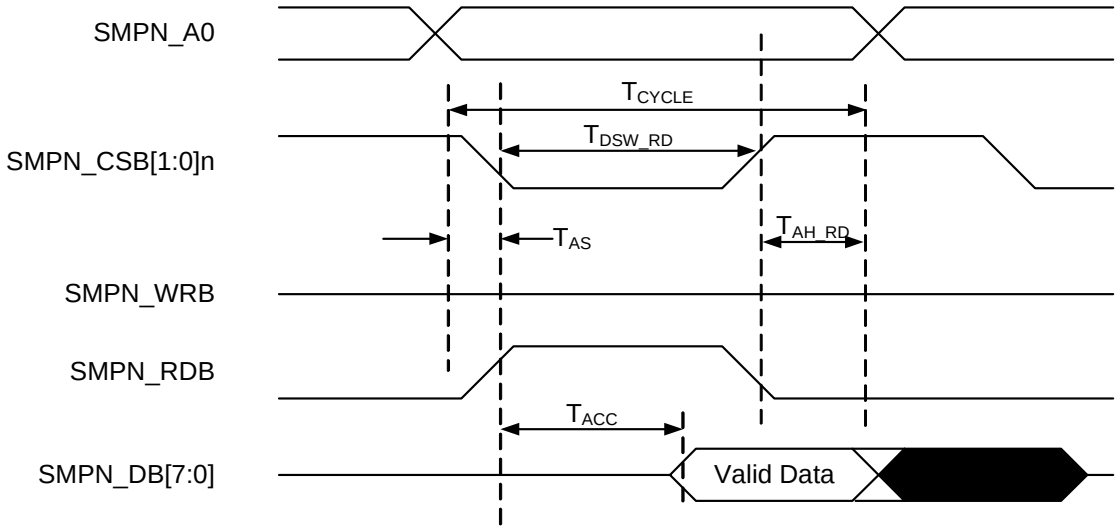


Figure 39: Smart Panel Interface 8-bit 6800-Series Parallel Mode Write Interface Protocol

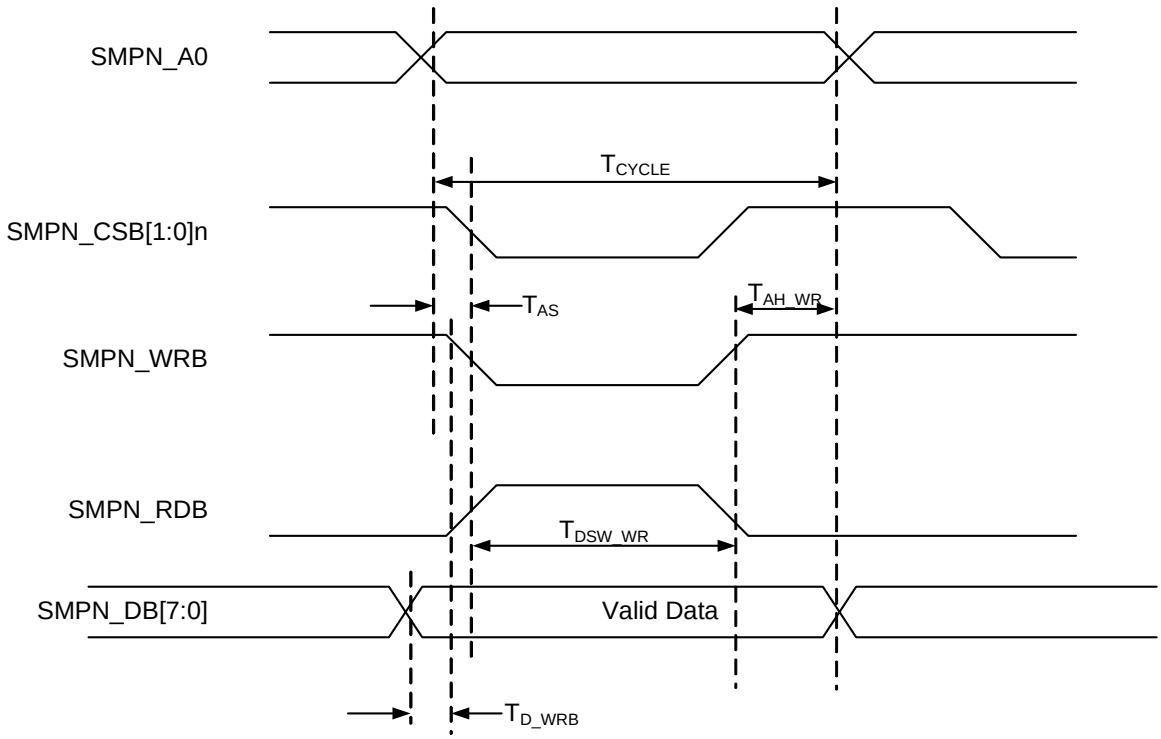
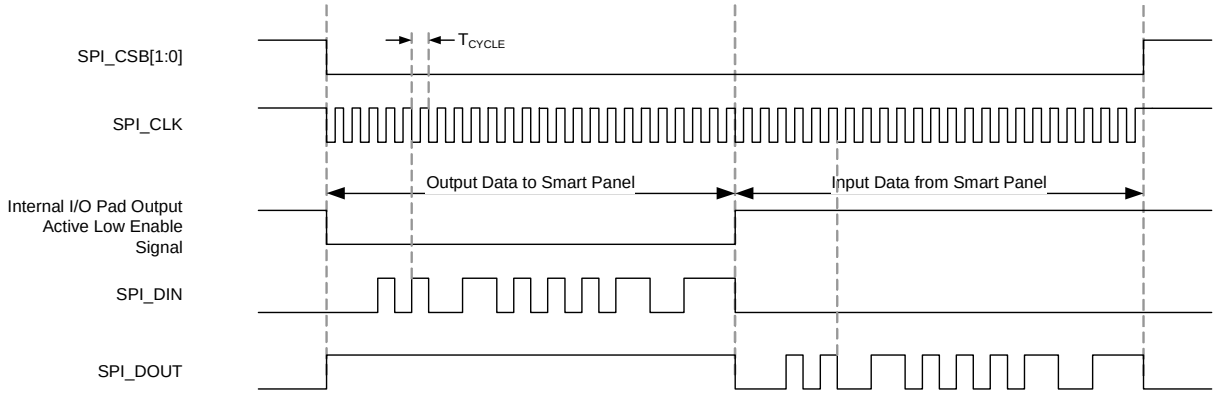


Figure 40: SPI Write/Read Protocol



The SPI_CLK Enable signal and Internal I/O Pad Output Active Low Enable Signal enable the I/O Pad.

Table 23: LCD Smart Panel Controller Timing

Symbol	Parameter	Min	Type	Max	Units
T_{AS}	Address setup time (A0)	—	Fixed 1	—	SCLK_SMPN cycles[1]
T_{DSW_RD}	Read strobe time	1	LCD_SPU_SMPN_CTRL[CFG_ISA_RXLOW]	16	SCLK_SMPN cycles[1]
T_{DSW_WR}	Write strobe time	1	LCD_SPU_SMPN_CTRL[CFG_ISA_TXLOW]	16	SCLK_SMPN cycles[1]
T_{AH_RD}	Read data hold time	1	LCD_SPU_SMPN_CTRL[CFG_ISA_RXHIGH]	16	SCLK_SMPN cycles[1]
T_{AH_WR}	Write data hold time	1	LCD_SPU_SMPN_CTRL[CFG_ISA_TXHIGH]	16	SCLK_SMPN cycles[1]
TD_WRB	Write data valid prior to SMPN_WRB	6	—	—	ns
T_{ACC}	Smart Panel read latency	—	—	20	ns
T_{CYCLE}	SPI_CLK frequency	—	LCD_SPI_CTRL[CFG_SCLKCNT]	70	MHz[2]
T_{CYCLE}	Read Cycle time	3	T_{AH_RD} + T_{DSW_RD} + 1 clock cycle	33	
T_{CYCLE}	Write Cycle time	3	T_{AH_WR} + T_{DSW_WR} + 1 clock cycle	33	

1. The panel clock source frequency is derived from one of three sources (ACLK, HCLK, 312 MHz (PLL1) or external LCD_PCLK) depending on the SCLK_SOURCE_SELECT, SCLK_AHB_AXI, and SCLK_INT_EXT fields in the LCD_CFG_SCLK_DIV register. The panel clock source is then divided using LCD_SCLK_DIV[CLK_INT_DIV] and LCD_SCLK_DIV[CLK_FRAC_DIV] to generate SCLK_SMPN. For more information on generating the SCLK_SMPN frequency refer to the LCD chapter in the *Marvell® Armada 16x Applications Processor Family Software Manual*.
2. LCD_SPU_SPI_CTRL[CFG_SCLKCNT] is used to divide PCLK to get SPI_CLK

7.5.2 LCD Dumb Panel Timing and Specifications

Figure 41 and Figure 42 show the horizontal and vertical dumb-panel timing diagrams. Refer to Table 24 for the registers used to program the LCD controller for dumb-panel operation.

Figure 41: Dumb LCD Panel Horizontal Timing

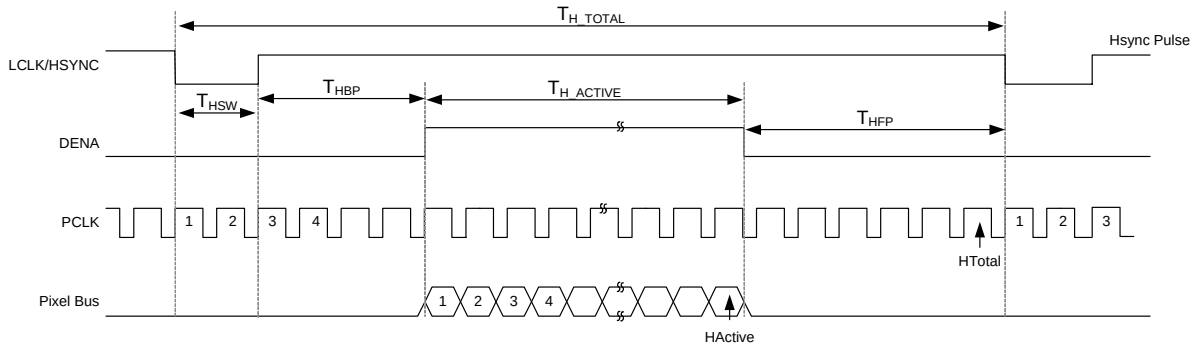


Figure 42: Dumb LCD Panel Vertical Timing

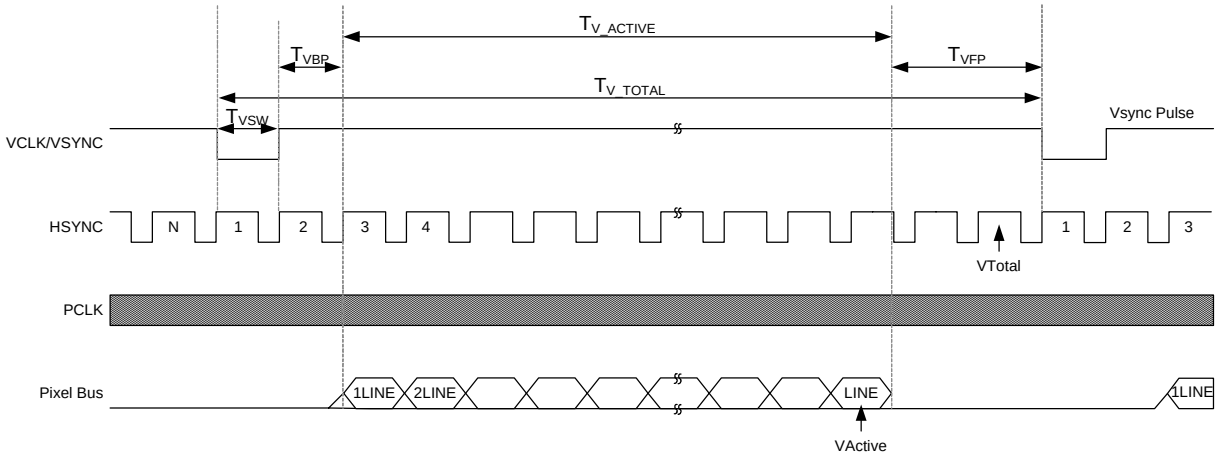


Table 24: LCD Dumb Panel Timing[1]

Symbol	Parameter	Min	Type	Max	Units	Notes
t_{PCLK}	PCLK period	—	—	70	MHz	
t_{CH}	PCLK high time	7	—	—	ns	
t_{CL}	PCLK low time	7	—	—	ns	
tDSU	Data Setup time	6	—	—	ns	
tDH	Data Hold time	—	—	5	ns	

Table 24: LCD Dumb Panel Timing[1] (Continued)

Symbol	Parameter	Min	Type	Max	Units	Notes
T_{HBP}	Horizontal back porch	0	LCD_SPU_H_PORCH[CFG_H_BACK_PORCH]	4096	PCLK cycles	2
T_{HFP}	Horizontal front porch	0	LCD_SPU_H_PORCH[CFG_H_FRONT_PORCH]	4096	PCLK cycles	2
T_{HSW}	Hsync pulse width	1	CFG_H_TOTAL – CFG_H_BACK_PORCH – CFG_H_ACTIVE – CFG_H_FRONT_PORCH	4096	PCLK cycles	2
T_{H_TOTAL}	Total horizontal pixels	1	LCD_SPU_V_H_TOTAL[CFG_H_TOTAL]	4096	Lines	
T_{H_ACTIVE}	Number of active horizontal lines	1	LCD_SPU_V_H_ACTIVE[CFG_H_ACTIVE]	4096	PCLK cycles	2,4
T_{VBP}	Vertical back porch	0	LCD_SPU_V_PORCH[CFG_V_BACK_PORCH]	4096	Lines	6
T_{VFP}	Vertical front porch	0	LCD_SPU_V_PORCH[CFG_V_FRONT_PORCH]	4096	Lines	7
T_{VSW}	Vsync pulse width	1	CFG_V_TOTAL – CFG_V_BACK_PORCH – CFG_V_ACTIVE– CFG_V_FRONT_PORCH	4096	Lines	3
T_{V_ACTIVE}	Panel Width	1	LCD_SPU_V_H_ACTIVE[CFG_V_ACTIVE]	4096	Lines	5
T_{V_TOTAL}	Total Vertical Lines	1	LCD_SPU_V_H_TOTAL[CFG_V_TOTAL]	4096	Lines	

Notes:
1. Pixel clock can be inverted to make its rising edge at the middle of pixel data cycle. It is always guaranteed setup and hold requirement.
2. The panel clock source frequency is derived from one of three sources (ACLK, HCLK, 312 MHz (PLL1) or external LCD_PCLK) depending on the SCLK_SOURCE_SELECT, SCLK_AHB_AXI, and SCLK_INT_EXT fields in the LCD_CFG_SCLK_DIV register. The panel clock source is then divided using LCD_SCLK_DIV[CLK_INT_DIV] and LCD_SCLK_DIV[CLK_FRAC_DIV] to generate PCLK. For more information on generating the PCLK frequency refer to the LCD chapter in the *Marvell® Armada 16x Applications Processor Family Software Manual*.
3. Vsync pulse can be configured as small as 1 cycle.
4. Sets the active horizontal screen display width for both Dumb Panel and Smart Panel.
5. Sets the active vertical screen display size for both Dumb Panel and Smart Panel.
6. VSYNC active edge at pixel count = TH_ACTIVE + 1.
7. VSYNC inactive edge at pixel count = TH_TOTAL + 1.

7.6 Quick Capture Camera Interface (CCIC) Timing Diagrams and Specifications

7.6.1 CCIC Parallel Interface Timing Requirements

Figure 43: Parallel Timing Diagram

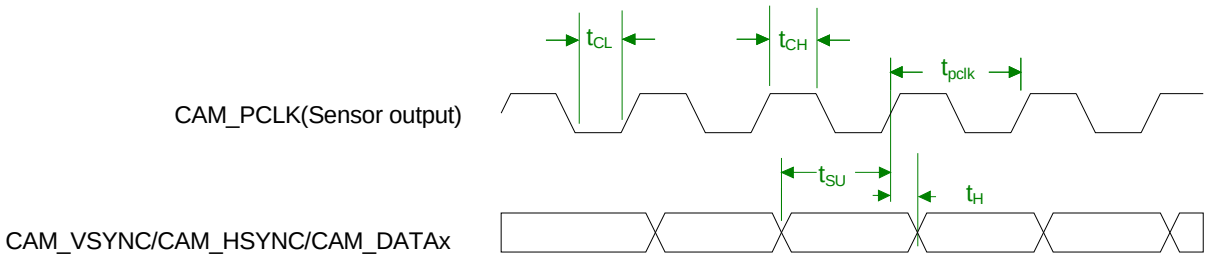


Table 25: CCIC Parallel Timing

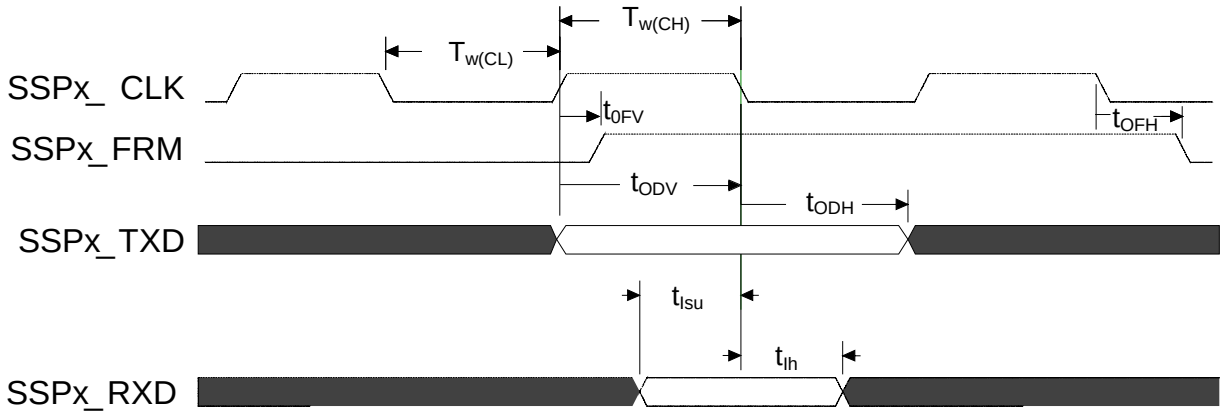
Symbol	Parameter	Min	Type	Max	Units	Notes
t_{PCLK}	PCLK period	0.1	—	78	MHz	
t_{SU}	Vsync/Hsync/Pixel Data setup	2.5	—	—	ns	
t_{H}	Vsync/Hsync/Pixel Data hold	1.5	—	—	ns	
t_{CH}	PCLK high time	6.41	—	—	ns	
t_{CL}	PCLK low time	6.41	—	—	ns	

7.7 SSP Timing Diagrams and Specifications

Figure 44 and Table 26 convey the SSP timing parameters with SSP in Master mode. The processor drives SSPx_CLK and SSPx_FRM when in Master mode. Figure 45 and Table 27 convey the SSP timing parameters with SSP in Slave mode. The processor receives SSPx_CLK and SSPx_FRM when in Slave mode.

SSP Master Mode Timing

Figure 44: SSP Master Mode Timing Diagram



1. SCLKDIR field in the SSP Control Register 1 (SSP_SSCR1) = 0x0
2. SFRMDIR field in the SSP Control Register 1 (SSP_SSCR1) = 0x0
3. The SPO and SPH fields in the SSP Control Register 1 (SSP_SSCR1) are used to determine the polarity of SSPx_CLK

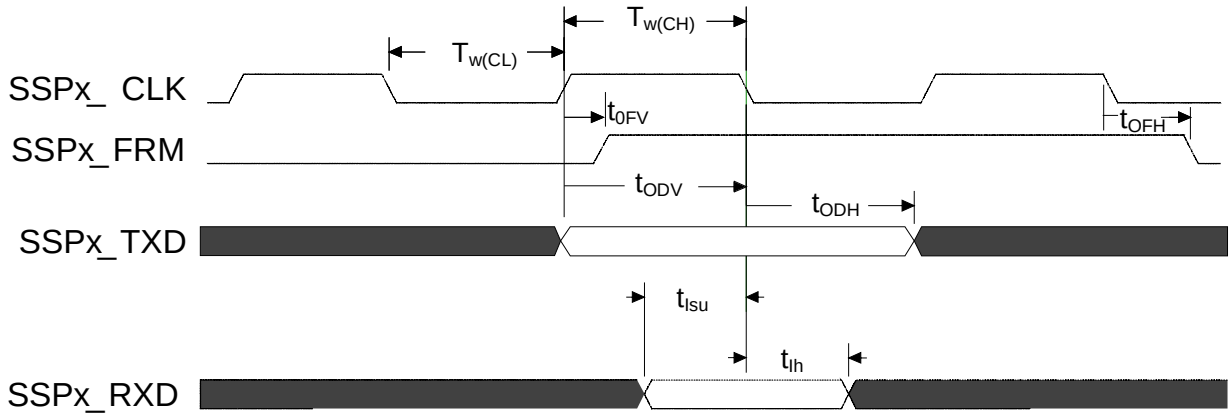
Table 26: SSP Master Mode Timing Specifications

Symbol	Description	Min	Max	Units
$t_{w(CH)}$	SSPx_SCLK pulse width high duration	9.6	—	ns
$t_{w(CL)}$	SSPx_SCLK pulse width low duration	9.6	—	ns
t_{ODV}	SSPx_TXD output valid prior to SSPx_CLK	1.1	—	ns
t_{ODH}	SSPx_TXD output hold time	7.6	—	ns
t_{OFH}	SSPx_FRM output hold time	6.9	—	ns
t_{OFV}	SSPx_FRM output valid prior to SSPx_CLK	0.6	—	ns
t_{Isu}	SSPx_RXD to SSPx_CLK setup time	0.6	—	ns
t_{Ih}	SSPx_CLK to SSPx_RXD hold time	14.9	—	ns

NOTE:
1. Timing values are based on 52 MHz SSPx_CLK frequency.
2. SSPx_SCLK is configure using the APBC_SSPx_CLK_RST[FNCLKSEL] and MPMU_ASYSDR and MPMU_SSPDR registers

7.7.1 SSP Slave Mode Timing

Figure 45: SSP Slave Mode Timing Definitions



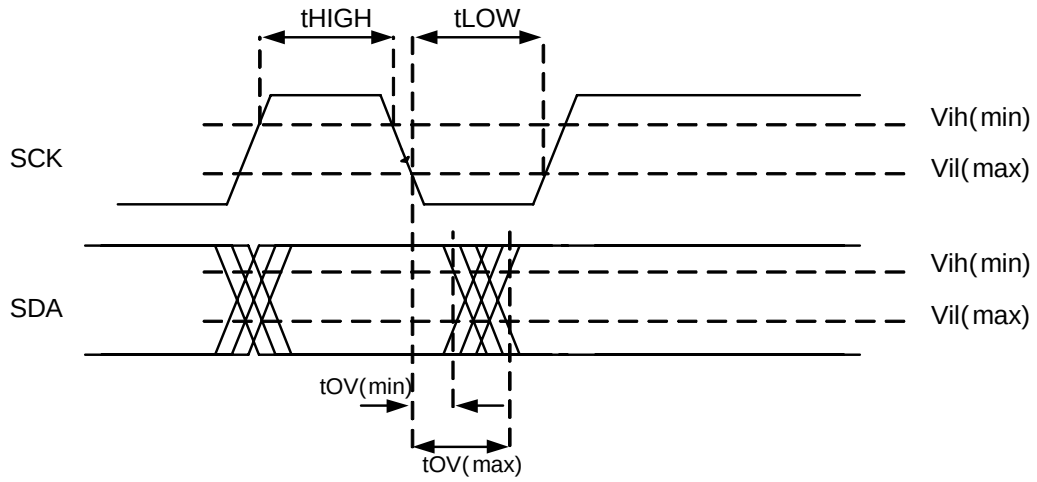
1. SCLKDIR field in the SSP Control Register 1 (SSP_SSCR1) = 0x1
2. SFRMDIR field in the SSP Control Register 1 (SSP_SSCR1) = 0x1
3. The SPO and SPH fields in the SSP Control Register 1 (SSP_SSCR1) are used to determine the polarity of SSPx_CLK

Table 27: SSP Slave Mode Timing Specifications

Symbol	Description	Min	Max	Units
$t_{w(CH)}$	SSPx_SCLK pulse width high duration	19.2	—	ns
$t_{w(CL)}$	SSPx_SCLK pulse width low duration	19.2	—	ns
t_{ODV}	SSPx_TXD output valid prior to SSPx_CLK	16.1	—	ns
t_{ODH}	SSPx_TXD output hold time	26.7	—	ns
t_{FH}	SSPx_CLK to SSPx_FRM hold time	19.3	—	ns
t_{FSU}	SSPx_FRM to SSPx_CLK setup time	12.6	—	ns
t_{Isu}	SSPx_RXD to SSPx_CLK setup time	13.2	—	ns
t_{Ih}	SSPx_CLK to SSPx_RXD hold time	21.54	—	ns
1. Timing values based on 26 MHz SSPx_CLK frequency				

7.8 TWSI Timing Diagrams and Specifications

Figure 46: TWSI Output Delay AC Timing Diagram



TWSI Input

Figure 47: TWSI Output Delay AC Timing Diagram

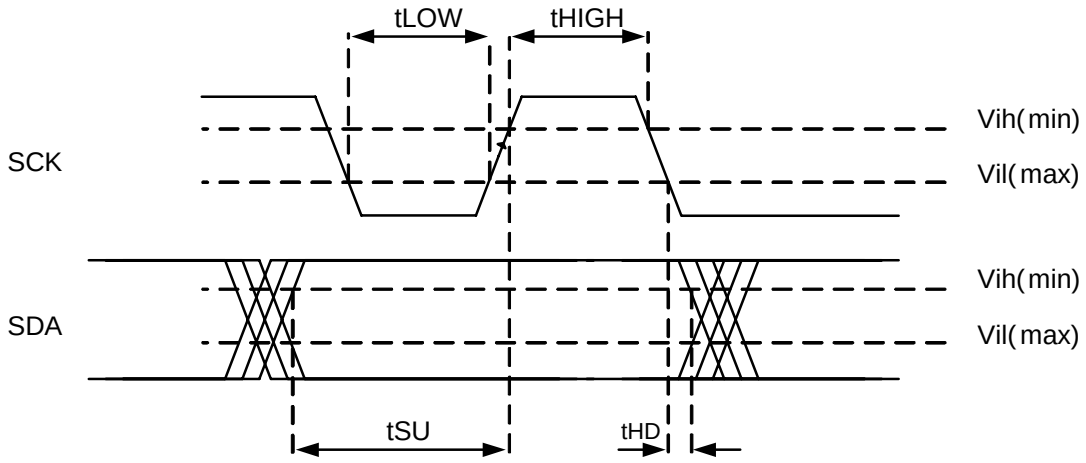


Table 28: TWSI Master AC Timing Table (Standard Mode 100 kHz)

Symbol	Description	Min	Max	Units	Notes
fCK	SCK clock frequency	—	100	kHz	-

Table 28: TWSI Master AC Timing Table (Standard Mode 100 kHz) (Continued)

Symbol	Description	Min	Max	Units	Notes
tLOW	SCK minimum low level width	0.47	—	tCK	1
tHIGH	SCK minimum high level width	0.40	—	tCK	1
tSU	SDA input setup time relative to SCK rising edge	250.0	—	ns	-
tHD	SDA input hold time relative to SCK falling edge	0.0	—	ns	3
tr	SDA and SCK rise time	—	1000.0	ns	1, 2
tf	SDA and SCK fall time	—	300.0	ns	1, 2
tOV	SDA output delay relative to SCK falling edge	0.0	0.4	tCK	1
	Notes: General comment: All values referred to VIH(min) and VIL(max) levels, unless otherwise specified. General comment: tCK = 1/fCK. 1. For all signals, the load is CL = 100 pF, and RL value can be 500 ohm to 8 kilohm. 2. Rise time measured from VIL(max) to VIH(min), fall time measured from VIH(min) to VIL(max). 3. For this parameter, the load is CL = 10 pF.				

Table 29: TWSI Master AC Timing Table (Fast Mode 400 kHz)

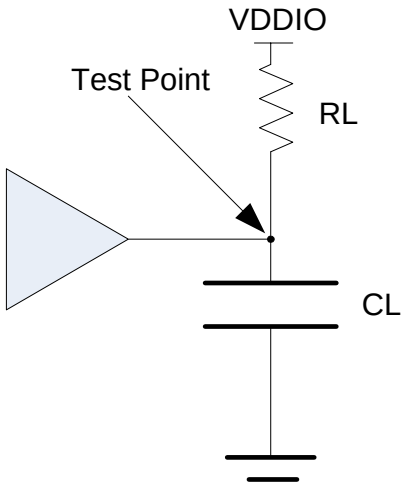
Symbol	Description	Min	Max	Units	Notes
fCK	SCK clock frequency	—	400	kHz	-
tLOW	SCK minimum low level width	0.52	—	tCK	1
tHIGH	SCK minimum high level width	0.24	—	tCK	1
tSU	SDA input setup time relative to SCK rising edge	100.0	—	ns	-
tHD	SDA input hold time relative to SCK falling edge	0.0	—	ns	3
tr	SDA and SCK rise time	20.0	300	ns	1, 2
tf	SDA and SCK fall time	20.0	300	ns	1, 2
tOV	SDA output delay relative to SCK falling edge	0.0	0.4	tCK	1
	Notes: General comment: All values referred to VIH(min) and VIL(max) levels, unless otherwise specified. General comment: tCK = 1/fCK. 1. For all signals, the load is CL = 100 pF, and RL value can be 500 ohm to 8 kilohm. 2. Rise time measured from VIL(max) to VIH(min), fall time measured from VIH(min) to VIL(max). 3. For this parameter, the load is CL = 10 pF.				

Table 30: TWSI Master AC Timing Table (high) speed 3.4 MHz)

Symbol	Description	Min	Max	Units	Notes
fCK	SCK clock frequency	—	3.4	MHz	-
tLOW	SCK minimum low level width	0.54	—	tCK	1
tHIGH	SCK minimum high level width	0.20	—	tCK	1
tSU	SDA input setup time relative to SCK rising edge	10.0	—	ns	-
tHD	SDA input hold time relative to SCK falling edge	0.0	—	ns	3
tr	SDA and SCK rise time	10.0	80.0	ns	1, 2
tf	SDA and SCK fall time	10.0	80.0	ns	1, 2
tOV	SDA output delay relative to SCK falling edge	0.0	0.4	tCK	1
	Notes: General comment: All values referred to VIH(min) and VIL(max) levels, unless otherwise specified. General comment: tCK = 1/fCK. 1. For all signals, the load is CL = 100 pF, and RL value can be 500 ohm to 8 kilohm. 2. Rise time measured from VIL(max) to VIH(min), fall time measured from VIH(min) to VIL(max). 3. For this parameter, the load is CL = 10 pF.				

7.8.1 TWSI Test Circuit

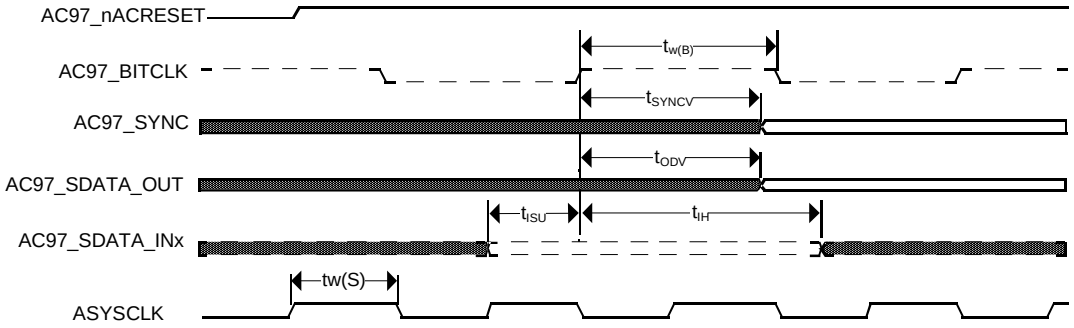
Figure 48: TWSI Test Circuit



7.9 AC'97 Timing Diagrams and Specifications

Figure 49 and Table 31 defines the AC'97 CODEC interface AC timing specifications.

Figure 49: AC'97 CODEC Timing Diagram



1. The MPMU Audio SYSCLK Dithering Divider Register (MPMU_ASYSDR) is used to select the frequency for ASYSCLK

Table 31: AC'97 CODEC Timing Specifications

Symbol	Parameter	Min	Max	Units	Notes
$t_{w(B)}$	AC97_BITCLK pulse width constraint	36	—	ns	
t_{SYNCV}	AC97_BITCLK high to AC97_SYNC valid delay	—	13	ns	1
t_{ODV}	AC97_BITCLK high to AC97_SDATA_OUT valid delay	—	11	ns	1
t_{ISU}	AC97_SDATA_INx to AC97_BITCLK setup time	3	—	ns	1
t_{IH}	AC97_BITCLK to AC97_SDATA_INx hold time	4	—	ns	1
$t_{w(S)}$	ASYSCLK pulse width delay	—	—	ns	

NOTE:
1. Transition time for input BITCLK is 2.5 ns.

7.10 JTAG Interface Timing Diagrams and Specifications

Refer to Table 32 for the timing specifications for Figure 50 and Figure 50

7.10.1 JTAG Interface Timing Diagrams

Figure 50: JTAG Interface Output Delay AC Timing Diagram

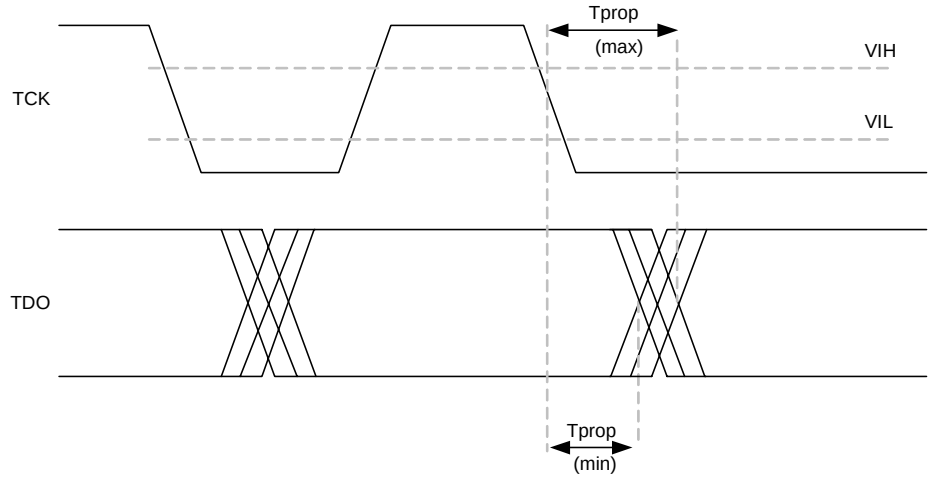
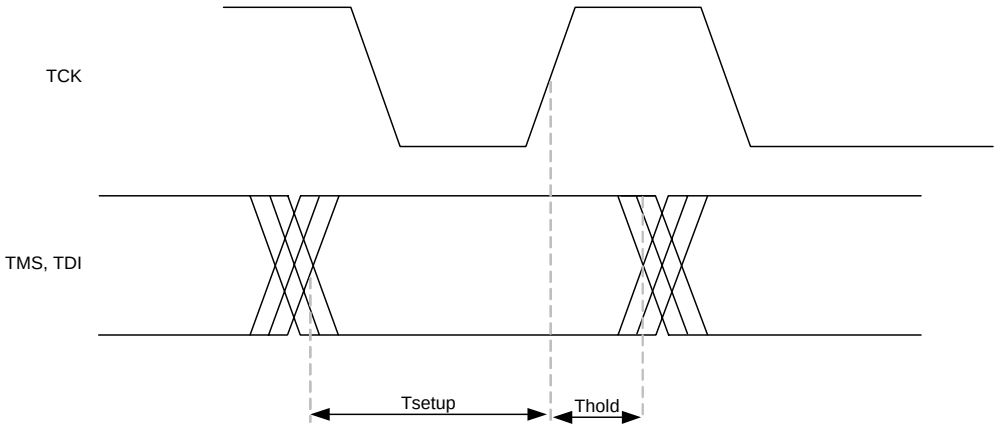


Figure 51: JTAG Interface Input AC Timing Diagram



7.10.2 JTAG Interface AC Timing Table

Table 32: JTAG Interface 10 MHz AC Timing[1]

Symbol	Description	Min	Type	Max	Units	Notes
fCK	TCK frequency	—	10	13.0	MHz	--
Tpw	TCK minimum pulse width	0.40	—	0.60	tCK	--

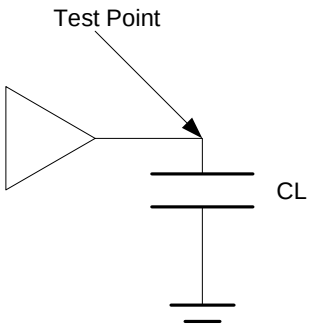
Table 32: JTAG Interface 10 MHz AC Timing[1] (Continued)

Symbol	Description	Min	Type	Max	Units	Notes
Sr/Sf	TCK rise/fall slew rate	0.50	—	—	V/ns	2
Trst	TRST_N active time	1.0	—	—	ms	--
Tsetup	TMS, TDI input setup relative to TCK rising edge	10.0	—	—	ns	--
Thold	TMS, TDI input hold relative to TCK rising edge	40.0	—	—	ns	--
Tprop	TCK falling edge to TDO output delay	1.0	—	20.0	ns	3

1. tCK = 1/fCK.
2. Defined from VIL to VIH for rise time and from VIH to VIL for fall time
3. For TDO signal, the load is CL = 10 pF.

7.10.3 JTAG Interface Test Circuit

Figure 52: JTAG Interface Test Circuit



7.11 USB 2.0 Timing Diagrams and Specifications

7.11.1 USB Interface Driver Waveforms

Figure 53: Low/Full Speed Data Signal Rise and Fall Time

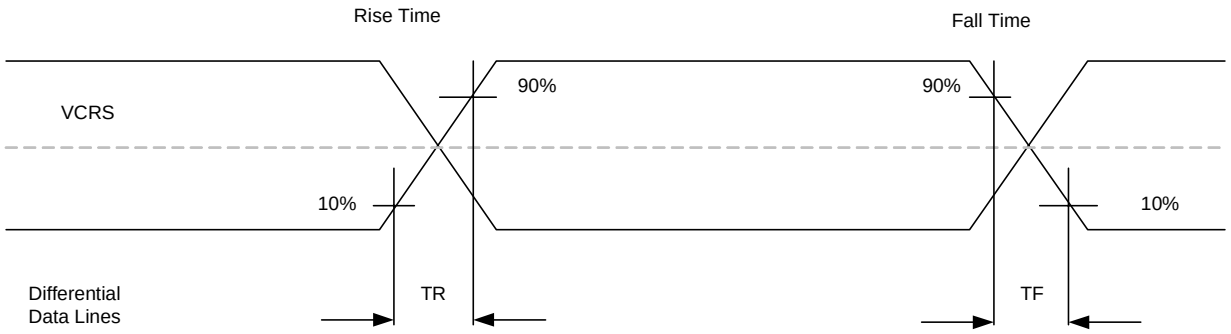


Figure 54: High Speed TX Eye Diagram Pattern Template

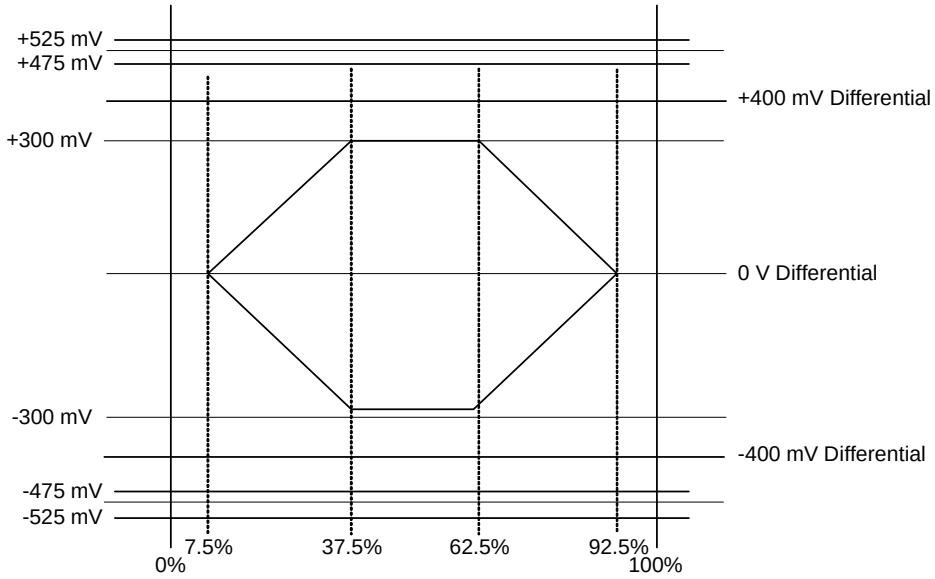
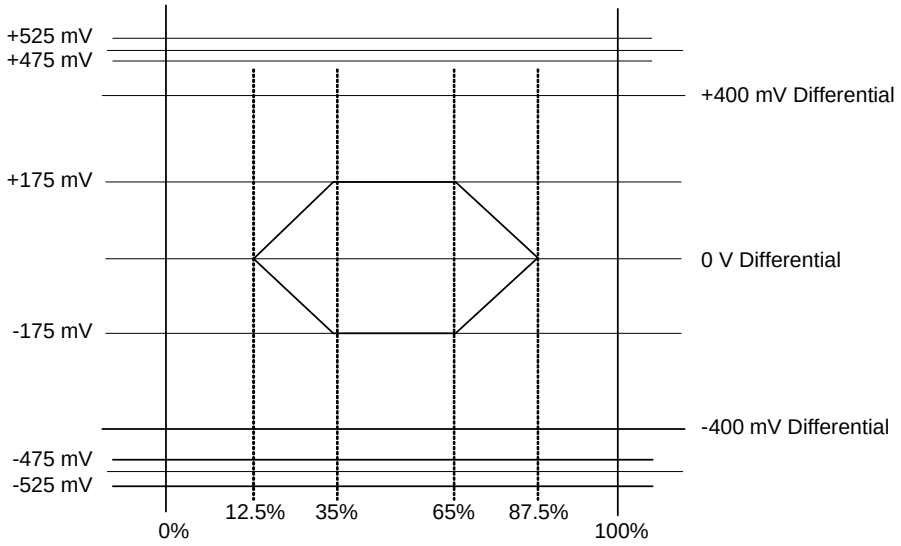


Figure 55: High Speed RX Eye Diagram Pattern Template



7.11.2 Differential Interface Electrical Characteristics

This section provides the reference clock, AC, and DC characteristics for the differential interface.

7.11.2.1 USB Driver and Receiver Characteristics

Table 33: USB Low Speed Driver and Receiver Characteristics[1]

Symbol	Description	Low Speed		Units	Notes
		Min	Max		
BR	Baud rate	1.5	—	Mbps	--
Bppm	Baud rate tolerance	-15000.0	15000.0	ppm	--
Driver Parameters					
VOH	Output single ended high	2.8	3.6	V	2
VOL	Output single ended low	0.0	0.3	V	3
VCRS	Output signal crossover voltage	1.3	2.0	V	4
TLR	Data fall time	75.0	300.0	ns	4,5
TLF	Data rise time	75.0	300.0	ns	4,5
TLRFM	Rise and fall time matching	80.0	125.0	%	--
TUDJ1	Source jitter total to next transition	-95.0	95.0	ns	5
TUDJ2	Source jitter total for paired transitions	-150.0	150.0	ns	6
Receiver Parameters					

Table 33: USB Low Speed Driver and Receiver Characteristics[1] (Continued)

Symbol	Description	Low Speed		Units	Notes
		Min	Max		
VIH	Input single ended high	2.0	—	V	--
VIL	Input single ended low	—	0.8	V	--
VDI	Differential input sensitivity	0.2	—	V	--

1. For more information, refer to *Universal Serial Bus Specification, Revision 2.0, April 2000*.
   The load is 100 ohm differential for these parameters, unless otherwise specified.
   To comply with the values presented in this table, refer to your local Marvell representative for register settings.
2. Defined with 1.425 kilohm pullup resistor to 3.6V.
3. Defined with 14.25 kilohm pulldown resistor to ground.
4. See Data Signal Rise and Fall Time waveform.
5. Defined from 10% to 90% for rise time and 90% to 10% for fall time.
6. Including frequency tolerance. Timing difference between the differential data signals.
   Defined at crossover point of differential data signals.

Table 34: USB Full Speed Driver and Receiver Characteristics[1]

Symbol	Description	Low Speed		Units	Notes
		Min	Max		
BR	Baud rate	12.0		Mbps	--
Bppm	Baud rate tolerance	-2500.0	2500.0	ppm	--
Driver Parameters					
VOH	Output single ended high	2.8	3.6	V	2
VOL	Output single ended low	0.0	0.3	V	3
VCRS	Output signal crossover voltage	1.3	2.0	V	4
TFR	Output rise time	4.0	20.0	ns	4,5
TFL	Output fall time	4.0	20.0	ns	4,5
TDJ1	Source jitter total to next transition	-3.5	3.5	ns	6, 7
TDJ2	Source jitter total for paired transitions	-4.0	4.0	ns	6,7
TFDEOP	Source jitter for differential transition to SE0 transition	-2.0	5.0	ns	--
Receiver Parameters					
VIH	Input single ended high	2.0	—	V	--
VIL	Input single ended low	—	0.8	V	--
VDI	Differential input sensitivity	0.2	—	V	--
tJR1	Receiver jitter to next transition	-18.5	18.5	ns	7

Table 34: USB Full Speed Driver and Receiver Characteristics[1] (Continued)

Symbol	Description	Low Speed		Units	Notes
		Min	Max		
tJR2	Receiver jitter for paired transitions	-9.0	9.0	ns	7

1. For more information, refer to *Universal Serial Bus Specification, Revision 2.0, April 2000*.
   The load is 100 ohm differential for these parameters, unless otherwise specified.
   To comply with the values presented in this table, refer to your local Marvell representative for register settings.
2. Defined with 1.425 kilohm pullup resistor to 3.6V.
3. Defined with 14.25 kilohm pulldown resistor to ground.
4. See Data Signal Rise and Fall Time waveform.
5. Defined from 10% to 90% for rise time and 90% to 10% for fall time.
6. Including frequency tolerance. Timing difference between the differential data signals.
   Defined at crossover point of differential data signals.
7. Defined at crossover point of differential data signals.

Table 35: USB High Speed Driver and Receiver Characteristics[1]

Symbol	Description	Low Speed		Units	Notes
		Min	Max		
BR	Baud rate	480.0		Mbps	--
Bppm		-500.0	500.0	ppm	--
Driver Parameters					
VHSOH	Data signaling high	360.0	440.0	mV	--
VHSOL	Data signaling low	-10.0	10.0	mV	--
THSR	Data rise time	500.0	—	ps	2
THSF	Data fall time	500.0	—	ps	2
	Data source jitter	See [3]			3
Receiver Parameters					
	Differential input signaling levels	See [4]			4
VHSCM	Data signaling common mode voltage range	-50.0	500.0	mV	--
	Receiver jitter tolerance	See [4]			4

1. For more information, refer to Universal Serial Bus Specification, Revision 2.0, April 2000.
The load is 100 ohm differential for these parameters, unless otherwise specified.
To comply with the values presented in this able, refer to your local Marvell representative for register settings.
2. Defined from 10% to 90% for rise time and 90% to 10% for fall time.
3. Source jitter specified by the TX eye diagram pattern template figure
4. Receiver jitter specified by the RX eye diagram pattern template figure.

7.12 PCI Express Specifications

Refer to Table 36 and Table 37 for PCIE output and input characteristics. For more information on PCIE timing requirements refer to the PCI Express Base Specification Revision 1.1 (http://www.pcisig.com/specifications/pciexpress/base).

7.12.1 PCIE Differential TX Output Electrical Characteristics

Table 36: PCI Express TX Output Electrical Specifications

Symbol	Parameter	Min	Type	Max	Units
UI	Unit Interval (UI)	399.88	400	400.12	ps
V_{TX_DIFFpp}	Differential Peak to Peak Output Voltage	0.800	—	1.2	V
$V_{TX\_DE\_RATIO}$	De-emphasized output voltage ratio	-3.0	-3.5	-4.0	dB
T_{TX_EYE}	Transmitter eye including all jitter sources	0.75	—	—	UI
$T_{TX\_EYE\_MEDIAN\_MAX\_JITTER}$	Maximum time between the jitter median and maximum deviation from the median	—	—	0.125	UI
T_{TX_RISE}, T_{TX_FALL}	D+/D- TX output rise/fall Time	0.125	—	—	UI
$V_{TX\_CM\_ACp}$	AC RMS common mode output voltage	—	—	20	mV
$V_{TX\_CM\_DC\_ACTIVE\_IDLE\_DELTA}$	Absolute Delta of DC Common Mode Voltage During L0 and electrical idle	0	—	100	mV
$V_{TX\_CM\_DC\_LINE\_DELTA}$	Absolute Delta of DC Common Mode Voltage between D+ and D-	0	—	25	mV
$V_{TX\_IDLE\_DIFFp}$	Electrical Idle Differential Peak Output Voltage	0	—	25	mV
$V_{TX\_RCV\_DETECT}$	The amount of voltage change allowed during Receiver Detection	—	—	600	mV
$V_{TX\_DC\_CM}$	The TX DC Common Mode Voltage	0	—	3.6	V
I_{TX_SHORT}	TX Short Circuit Current Limit		—	90	mA
$T_{TX\_IDLE\_MIN}$	Minimum time spent in Electrical Idle	50	—		UI
$T_{TX\_IDLE\_SET\_TO\_IDLE}$	Maximum time to transition to a valid Electrical Idle after sending an Electrical Idle ordered set	—	—	20	UI
$T_{TX\_IDLE\_TO\_DIFF\_DATA}$	Maximum time to transition to valid TX specifications after leaving an Electrical Idle condition	—	—	20	UI
RL_{TX_DIFF}	Differential Return Loss	10	—	—	dB
RL_{TX_CM}	Common Mode Return Loss	6	—	—	dB
$Z_{TX\_DIFF\_DC}$	DC Differential TX Impedance	80	100	120	Ohms
C_{TX}	AC Coupling Capacitor	75	100	200	nF
$T_{crosstalk}$	Crosstalk Random Timeout	0	—	1	ms

7.12.2 PCIE Differential RX Input Electrical Characteristics

Table 37: PCI Express RX Input Electrical Specifications

Symbol	Parameter	Min	Type	Max	Units
UI	Unit Interval (UI)	399.88	400	400.12	ps
V_{RX_DIFFpp}	Differential Peak to Peak Output Voltage	0.175	—	1.2	V
T_{RX_EYE}	Receiver eye including all jitter sources	0.4	—	—	UI
$T_{RX\_EYE\_MEDIAN\_MAX\_JITTER}$	Maximum time between the jitter median and maximum deviation from the median	—	—	0.3	UI

Table 37: PCI Express RX Input Electrical Specifications

Symbol	Parameter	Min	Type	Max	Units
$V_{RX\_CM\_ACp}$	AC RMS common mode output voltage	—	—	150	mV
RL_{RX_DIFF}	Differential Return Loss	10	—	—	dB
RL_{RX_CM}	Common Mode Return Loss	6	—	—	dB
$Z_{RX\_DIFF\_DC}$	DC Differential RX Impedance	80	100	120	Ohms
Z_{RX_DC}	RX DC input impedance	40	50	60	Ohms
$Z_{RX\_HIGH\_IMP\_DC}$	Power Down DC input impedance	200	—	—	kOhms
$V_{RX\_IDLE\_DET\_DIFFp}$	Electrical Idle detect threshold	65	—	175	mV
$T_{RX\_IDLE\_DET\_DIFF\_ENTERTIME}$	Unexpected electrical idle enter detect threshold integration time	—	—	10	ms
L_{RX_SKEW}	Total skew	—	—	20	ns

7.13 Ethernet MAC (MII) Timing Diagrams and Specifications

MII Tx Mode timing diagram is shown in Figure 56 and timing parameters are provided in Table 38. MII Rx Mode timing diagram is shown in Figure 57 and timing parameters are defined in Table 39. In Tx mode, the media access controller (MAC) receives TX_CLK from the Ethernet transceiver (PHY) and drives TX data and control signals. In Rx mode, the controller receives RX_CLK, data and control signals from the Ethernet transceiver.

MII Management interface timing diagram is shown in Figure 58 and timing values are defined in Table 40.

Figure 56: MII Tx Mode Interface Timing Diagrams

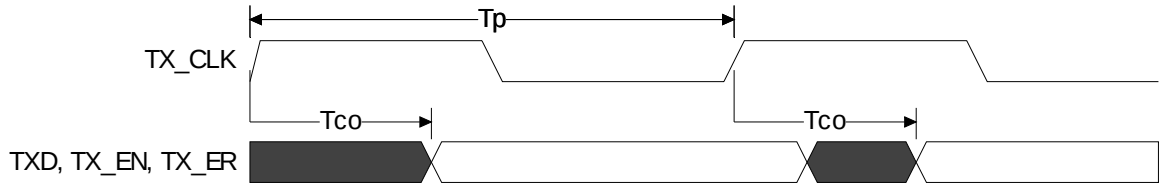


Table 38: MII Tx Mode Interface Timing Specifications

Symbol	Parameter	Min	Max	Unit	Notes
Tp	TX_CLK frequency	—	25	MHz	
Tco	TX_CLK in to TX data and control out	0	14	ns	1

NOTE:
1. Timing values are based on 30pf reference load.

Figure 57: MII Rx Model Interface Timing Diagrams

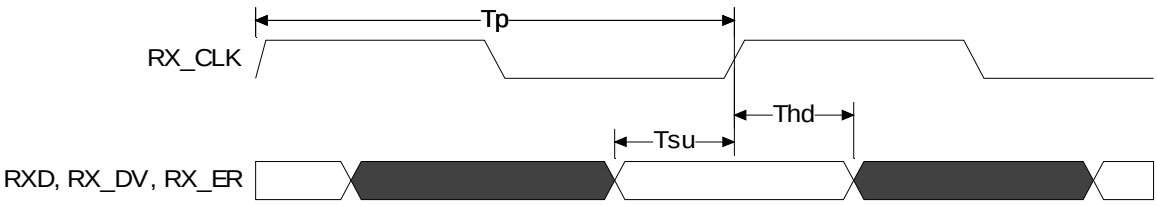


Table 39: MII Rx Mode Interface Timing Specifications

Symbol	Parameter	Min	Max	Unit	Notes
Tp	RX_CLK Frequency	—	25	MHz	
Tsu	Input setup time	6	—	ns	
Thd	Input hold time	4	—	ns	

Figure 58: MII Management Interface Timing Diagrams

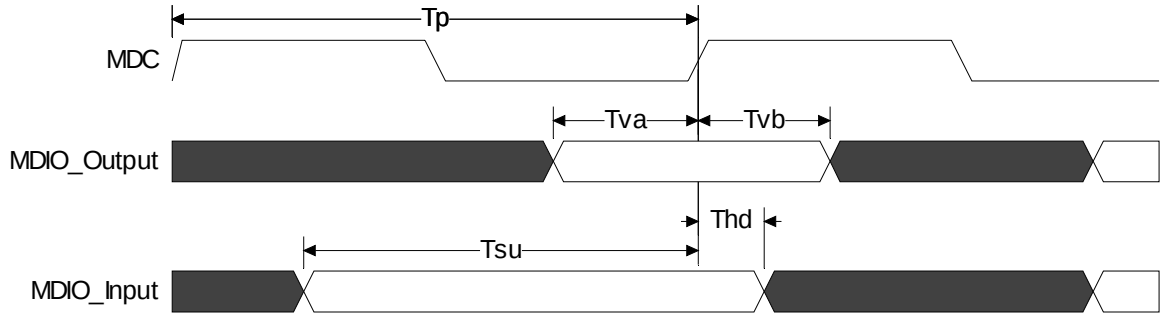


Table 40: MII Management Interface Timing Specifications

Symbol	Parameter	Min	Max	Unit	Notes
Tp	MDC Frequency	—	2.5	MHz	
Tva	MDIO output valid time before MDC rising	20	—	ns	
Tvb	MDIO output valid time after MDC rising	20	—	ns	
Tsu	MDIO input setup time	50	—	ns	

Table 40: MII Management Interface Timing Specifications (Continued)

Symbol	Parameter	Min	Max	Unit	Notes
Thd	MDIO input hold time	0	—	ns	

7.14 Powerup/Down Sequences

This section includes specifications for the following:

- Section 7.14.1, Power Up Timings
- Section 7.14.2, Powerdown Timings

Table 41: Terminology

Term	Description
VDD_M	ASIC DRAM IO power (1.8V nominal +/- 10%)
VDD_CORE	Core power (assume 1.0V nominal)
AVDD_USB	ASIC USB power including AVDD_OTG and AVDD_UHC (3.3V nominal)
AVDD5_USB	ASIC USB 5V power (5 V nominal)
VDD_OSC	Quiet 1.8V analog power for ASIC PLL/Crystal.
VDD_IOx	3.3/1.8V IO power Includes VDD_IO0, VDD_IO1, VDD_IO2, VDD_IO3, VDD_IO4
RESET_IN_N	External Master Reset In pin

7.14.1 Power Up Timings

The external voltage regulators and other power-on devices must provide the processor with a specific sequence of power and resets to ensure proper operation (see Figure 59 and Table 42).

7.14.1.1 Host Side PMIC USB Signals

- AVDD5_USB - Supply
  - Host Mode Only: Connect to 5V to supply a maximum of 10mA on USBVBUS. For higher current requirements, an external PMIC must be used to drive VBUS.
  - Device Mode Only: Not used; can remain floating.
  - OTG Mode: Connect to 5V to provide a maximum of 10mA on USBVBUS during session negation. For higher current requirements as external PMIC must be used to drive VBUS.

Note When the USBVBUS is driven from AVDD5_USB, the USBHPEN signal is pulled high (3.3V).

Caution When USBHPEN = 3.3V, do not supply both AVDD5_USB and USBVBUS with 5V.

- USBVBUS - Input/Output
  - Host Mode: USB power output (+5V@10mA) when USBHPEN = 3.3V
  - Device Mode: 5V VBUS input from host
  - OTG Mode: Input/Output to supply +5V during session negotiation
- USBHPEN - Output
  - Controls external power management chip to provide 5v power to VBUS
    a) OV: Does not drive VBUS
    b) 3.3V: Drives 5V power source on to VBUS

Note If the application does not need more than 10mA, float USBHPEN and connect AVDD5_USB to 5V power. VBUS is not driven inside the PHY.

Figure 59: Power-Up Reset Timing

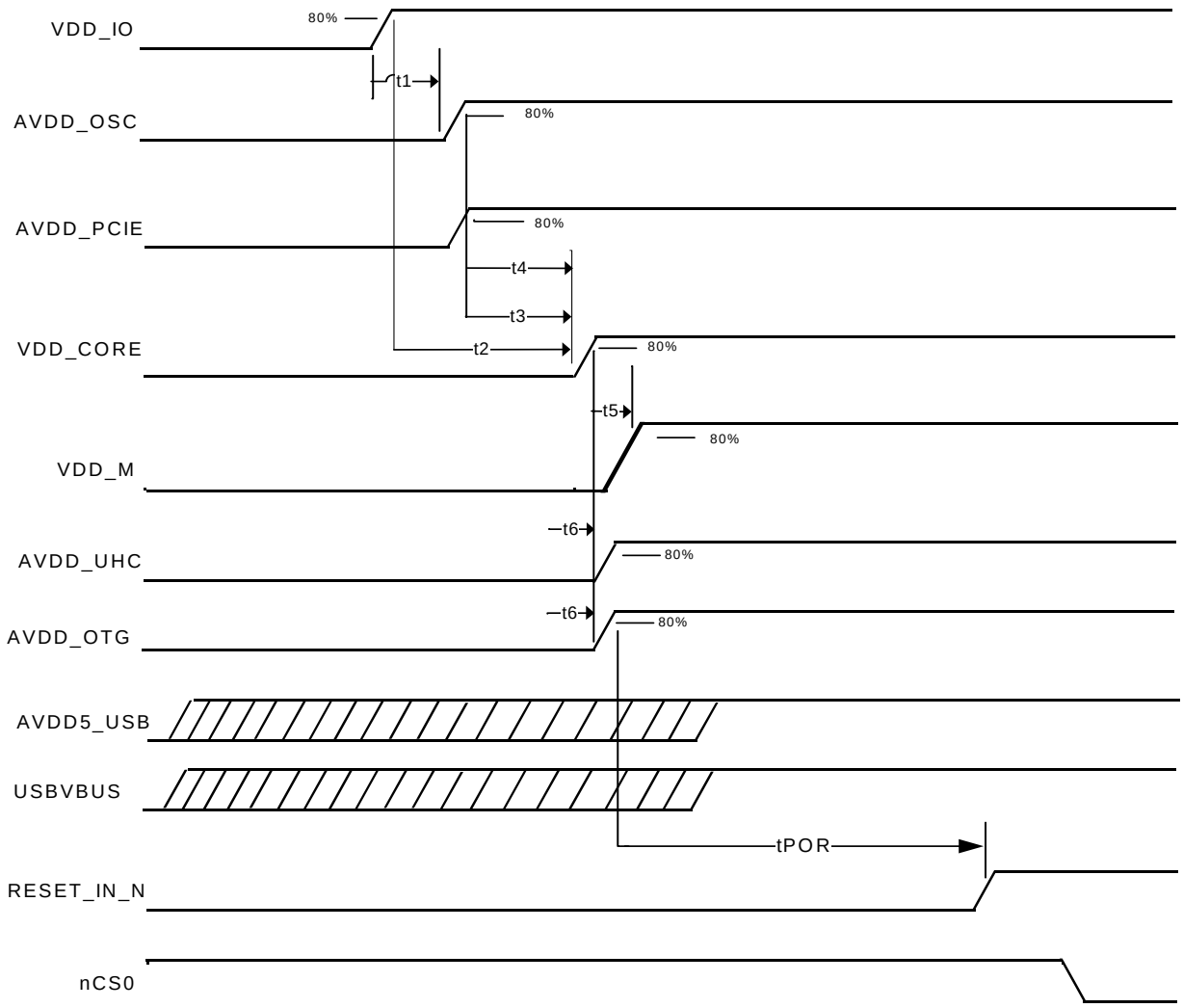


Table 42: Power-Up Timing Specifications

Symbol	Description	Min	Typical	Max	Units	Notes
t1	Delay from the start of the high voltage IO supplies ramp prior to AVDD_OSC ramp start.	0	—	—	µs	1
t2	Delay from VDD_IO prior to VDD_CORE ramp start	0	—	—	µs	2

Table 42: Power-Up Timing Specifications (Continued)

Symbol	Description	Min	Typical	Max	Units	Notes
t3	Delay from AVDD_OSC reaching 80% of its final value prior to VDD_CORE ramp start	0	—	—	µs	3
t4	Delay from AVDD_PCIE reaching 80% of its final value prior to VDD_CORE ramp start.	0	—	—	µs	4,5
t5	Delay from VDD_CORE reaching 80% of its final value prior to VDD_M reaching 80% of its final value	-500	300	—	µs	6, 7
t6	Delay from VDD_CORE reaching 80% of its final value prior to AVDD_UHC and AVDD_OTG ramp start	0	—	—	µs	8, 9
tPOR	Time required before de-asserting RESET_IN_N after AVDD_UHC and USB_OTG reach 80%.	153	—	—	µs	

1. VDD_IO and AVDD_OSC can be enabled at the same time.
2. VDD_IO must power to 80% prior to enabling VDD_CORE
3. AVDD_OSC must power to 80% prior to enabling VDD_CORE.
4. AVDD_PCIE must power to 80% prior to enabling VDD_CORE.
5. AVDD_PCIE includes AVDD_PCIE and AVDDT_PCIE.
6. VDD_M must not exceed VDD_CORE by more than 1.2V
7. Ideally VDD_CORE and VDD_M will ramp to 80% of their final value at the same time. Due to voltage level differences between VDD_M and VDD_CORE, VDD_M may reach 80% of its final value after VDD_CORE depending on the ramp rates for each supplies. To reduce the power up time keep the delay after VDD_CORE at a minimum.
8. Enable AVDD_UHC and AVDD_OTG after VDD_CORE reaches a minimum of 80% of its final value.
9. Do not power AVDD_UHC and AVDD_OTG prior to VDD_CORE
10. The AVDD5_USB supply can left on while the other supplies are powered off. Powering up AVDD5_USB is only required for USB OTG functionality when using host mode.
11. USBVBUS is not a power supply but is included in this diagram for completeness. USBVBUS can be supplied with 5V while the other supplies are turned off.

7.14.2 Powerdown Timings

When powering down the ARMADA 16x Applications Processor, all voltage rails can be removed simultaneously. Ideally, the power to VDD_M is removed prior to VDD_CORE. When the power to VDD_CORE is removed prior to removing VDD_M, refer to Table 43 for timing constraints between the voltage rails.

Figure 60: Powerdown Timing

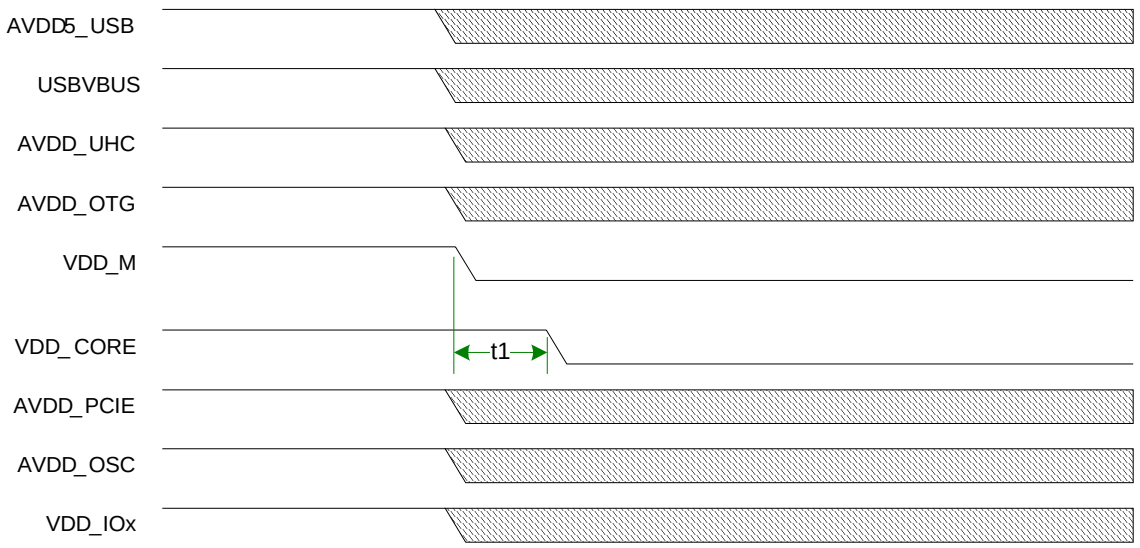


Table 43: Powerdown Timing Specifications

Symbol	Description	Min	Typical	Max	Units	Notes
t1	VDD_CORE to VDD_M	—	—	10	ms	2,3,4

1. AVDD5_USB can remain active while the other supplies are removed
2. VDD_M must not exceed VDD_CORE by more than 1.8V
3. The start of ramp down time when VDD_CORE is removed prior to VDD_M
4. When powering down VDD_CORE prior to VDD_M, VDD_M must not exceed VDD_CORE by 1.26V for a maximum of 200ms.
5. VDD_IO can remain active while the other supplies are removed. Recommended for Hibernate mode.

8 Design Guidelines and Checklist

This chapter discusses:

8.1 DDR Interface General Routing Guidelines

The basic routing rules for DDR devices on a PCB are shown as below. For specific guidelines, refer to the appropriate sections below.

8.1.1 General Rules:

- Ground Reference Routing for all signals
- DQ byte groups routed on the same layer

8.1.1.1 Data and QS Signals

- Signals within the same Data byte of must be routed to within +/-50 mils (1.27mm) of their respective QS signals. QS line length should be centered within their respective data groups and matched to within 0.05" (1.27mm). A Data byte consists of: 8 data lines (DQ), 1 data mask (DQM), 1 QS and 1 QS#.
- Data signals should be less than or equal to 3.0" (76.2mm) long.
- Whenever possible, the QS lines are to be ground guarded as GND-QS-QS#-GND.
- Data/DQM traces to have impedance of 50 ohms. DQS-DQS# to have differential 100-ohm traces.
- Signals within the same Data byte of must be routed to within +/-50mils (1.27mm) of their respective QS signals. QS line length should be centered within their respective data groups and matched to within 0.05" (1.27mm). A Data byte consists of: 8 data lines (DQ), 1 data mask (DQM), 1 QS and 1 QS#.
- Data and QS signals must be routed as stripline traces if possible
- Data signals should be less than or equal to 3.0" long. Longer lengths should be simulated for timing margins.
- Whenever possible, the QS lines are to be ground guarded as GND-QS-QS#-GND. If ground guarding is not possible, the spacing of QS, QS# to other signals should be at-least twice the minimum trace width
- Differential signals, QS and QS#, must be routed to a length within 0.025" (0.635mm) of each other.
- Data/DQM traces to have single ended impedance of 50 ohms.
- Differential signals, QS, QS#, must be routed with a differential impedance of about 100 ohms
- 8.QS, QS# traces to be terminated with a resistor placement on the controller side close to the pins. Use 1k ohm resistor from QS pin to gnd and 1k ohm resistor from QS# pin to VDDQ as close to the pins (controller side) as possible.

8.1.1.2 Address/Command Signals

- Address/Control lines to the same DRAM must be routed to within 0.5 inch of the clock signals and routed on the same layer.
- Address/Control lines need to have trace impedance of 50 ohms.
- Address/Control lines need to have a shunt termination of 50 ohms to VTT.
- Max length of stub (connecting from SDRAM pins to termination) should be less than 0.2" as close to the pins of dram as possible.
- CKE needs to have pulldown of 4.7k to gnd. There is no need to have a CKE termination to VTT.

8.1.1.3 Clock Signals

- Whenever possible, clock routing should be the Ground Guarded configuration for as long as possible.
- Differential clock signals, CLK and CLK# should be terminated at the end of the lines between them with a 100-ohm termination resistor.
- Differential clock signals, CLK and CLK#, must be routed to a length within 0.025" (0.635mm) of each other, and should be routed with at least a 2:1 spacing to each other.
- The differential impedance of CLK,CLK# traces should be 100 ohms.
- Clock signals (T0 length) should also be routed to within 0.5 inch of the Address/Command signals.
- Clock signals (T0 length) must be routed to be within 1.0" (+/-12.7mm) of their respective QS signals to the same dram, with CKs in the middle.
- Max length of stub (connecting from DRAM pins to termination) should be less than 0.1" as close to the pins of DRAM as possible.
- Whenever possible, clock routing should be the Ground Guarded configuration for as long as possible. If ground guarding is not possible, the spacing of CLK, CLK# to other signals should be at least thrice the minimum trace width.
- Differential Clock signals, CLK and CLK#, must be routed to a length within 0.025" (0.635mm) of each other.
- Clock signals should also be routed to within 0.5 inch of the Address/Command signals.
- CLK, CLK# traces to have single ended impedance of 50 ohms. Differential clock signals, CLK and CLK#, must be routed with at least a 2:1 spacing to each other. Spacing from CLK/CLK# to other signals should be 3 times trace width.
- Differential clock signals, CLK and CLK# should be terminated at the end of the lines between them with a 100 ohm termination resistor with a common mode (termination midpoint) capacitor of 1nF.
- Max length of stub (connecting from SDRAM pins to termination) should be less than 0.1" as close to the pins of DRAM as possible.

8.1.2 DDR Interface Detailed Routing Guidelines

For detailed routing guidelines refer to the *ARMADA 16x Applications Processor Family DDR Routing Guidelines* Application note.

8.2 EPD Controller Design Guidelines

This chapter describes:

- Section 8.2.4, “Source Driver Interface”
- Section 8.2.5, “Gate Driver Interface”
- Section 8.2.6, “Start Pulse Control”

8.2.1 Introduction

The EPD Controller (EPDC) is an IP block optimized for products using ElectroPhoretic Displays (EPDs). It enables an SoC solution with a direct connection to the EPD module. The EPD controller differentiates itself through

- High-level integration
- Presentation of complex content on EPDs
- Ease of software implementation
- Content security
- Significant power savings

Due to its intrinsic bi-stable nature, power is not required when there is no change to the display image. EPDs are reflective displays so backlighting is not necessary.

If an EPD display controller is in a typical EPD display system, it can drive an EPD panel through the source driver and gate driver chips.

Major EPDC features include:

- Frame resolution:
  - From SVGA (600x800) up to UXGA (1200x1600)
  - ~150 dpi A size sheet
- Partial and Parallel Update
- Capable of displaying videos and animations.
- Conventional software programming model
- Flexible interface to various EPD panels
- Elimination of the separate EPD SDRAM.
- Power management
- Faster update - Each pixel can detect its own waveform length and stops at the end. Shorter waveforms end sooner.
- Support content security though NDS secure IC.
- Appear as conventional Frame buffer.
- Host interrupt capability

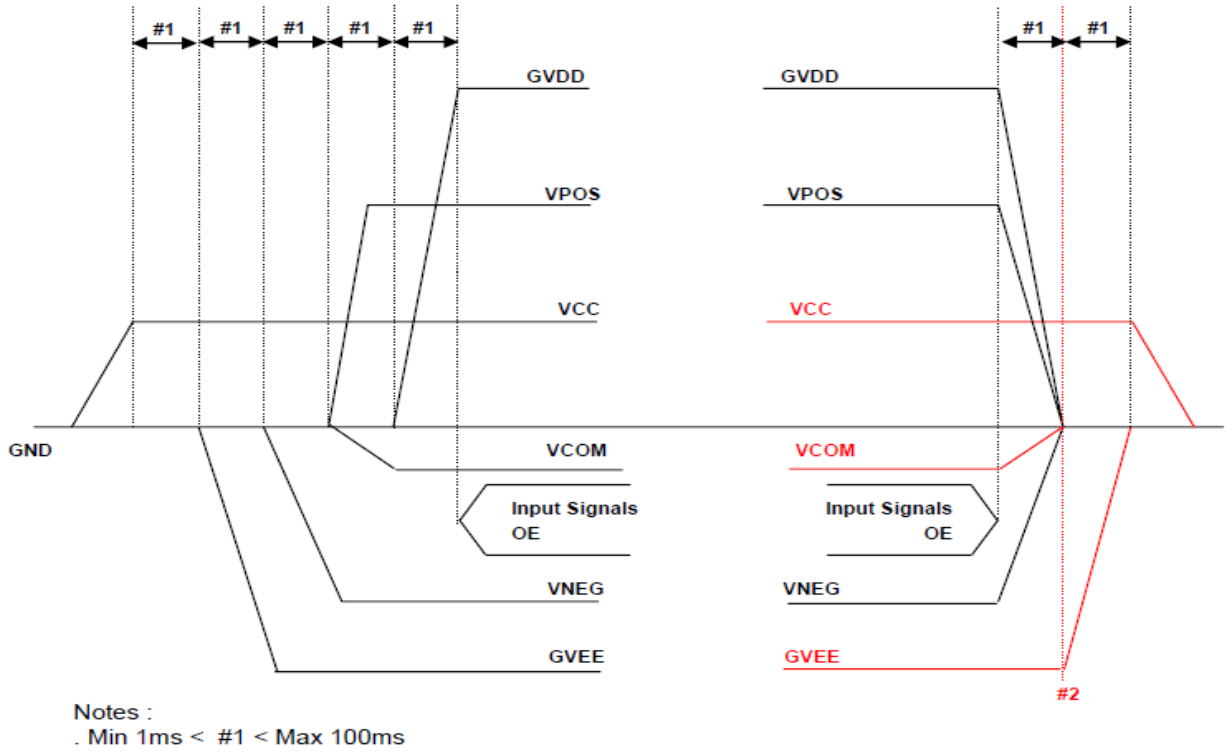
8.2.2 Panel Power Up Sequence

EPD panel power-up must follow a fixed sequence as described below and in Figure 61:

Power on sequence: VCC => GVEE => VNEG => VPOS => Input Signals: OE, GVDD

Power off sequence: Input Signals,OE => GVDD, VPOS, VNEG,VCOM => GVEE => VCC

Figure 61: Panel Power Sequence



The panel power supplies are controlled by the EPDC PWR[4:0] pins. PWR[4:0] timings are controlled by the POWER_[3:0] registers.

8.2.3 Display Common Power Signal

The PWRCOM signal controls the common driver output Vcom to the display panel. The signal is asserted during image updates; it is asserted when entering normal operation mode, and negated when exiting normal operation mode.

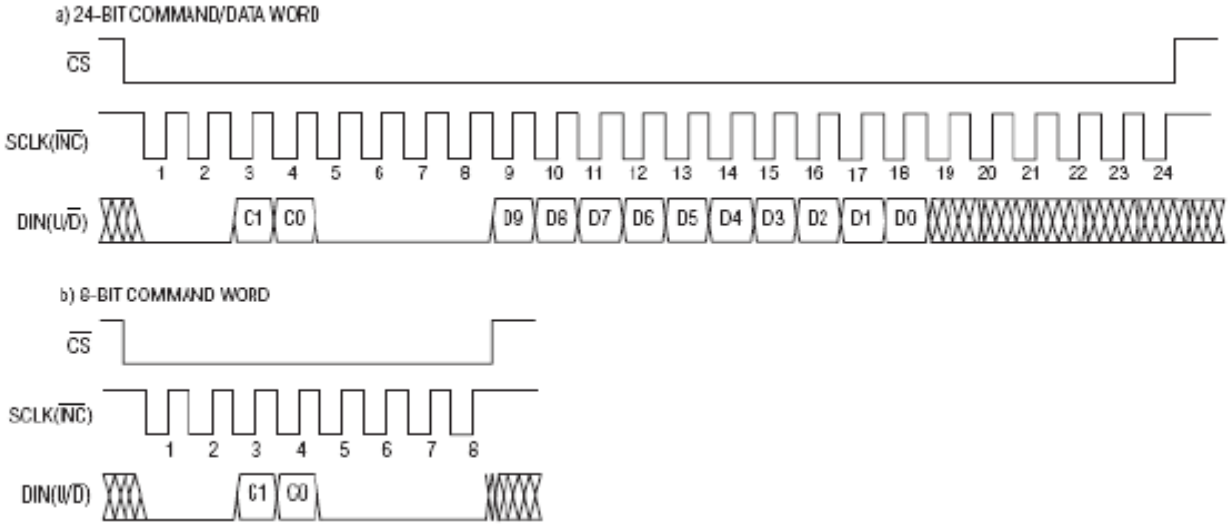
8.2.3.1 Vcom Setting by DPOT (Digital Potentiometer)

Vcom is the common voltage of the EPD panel, typically between -0.5V and -3.5V. Each EPD panel has a different Vcom voltage, therefore the EPDC must program a DPOT to drive the Vcom voltage.

A 10-bit value is used to program the DPOT in the following sequence (see Figure 62):

1. Assert the VCOM_VOLT[DPOT_CE_n] bit. Transmit an 8-bit "write wiper register" command to the DPOT.
2. Transmit a 10-bit voltage value to DPOT, followed by six "don't care" bits and then De-assert the VCOM_VOLT[DPOT_CE_n] bit.
3. Assert the VCOM_VOLT[DPOT_CE_n] bit. Transmit an 8-bit "copy wiper to NVRAM" command to the DPOT and then De-assert the VCOM_VOLT[DPOT_CE_n] bit.

Figure 62: DPOT Programming Sequence



With the EPDC, the VCOM_VOLT register is used for DPOT programming and is defined in Appendix A - Register Tables.

In hardware DPOT mode, the SCLK frequency should be PCLK divided by 64.

8.2.4 Source Driver Interface

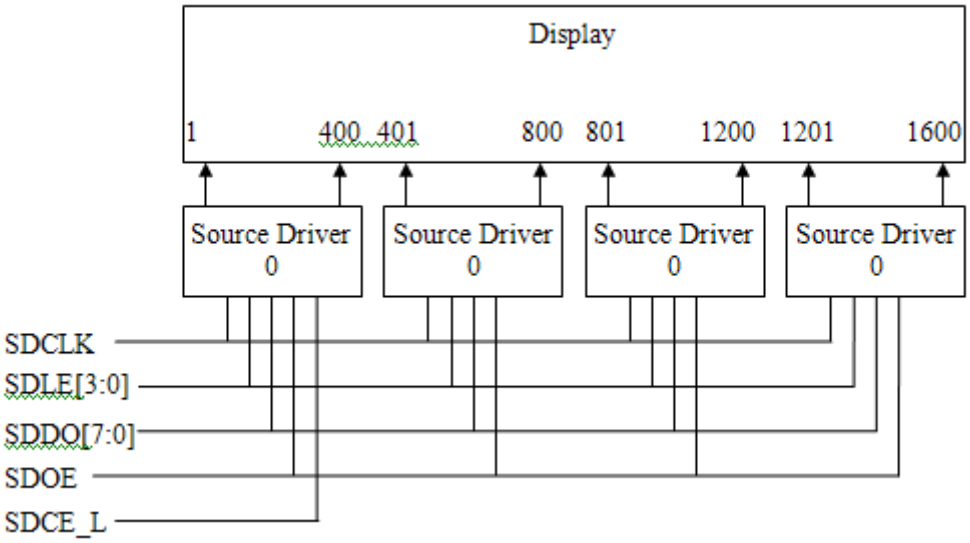
The EPDC output controller signals, SDDO[7:0], are connected to the source drivers. Currently each source driver can drive up to 400 columns. Therefore, as many as four source drivers are used for 1600 columns (see Figure 63). The source driver timing is shown in Figure 64.

The signals to the source driver are all outputs, as listed in Table 44.

Table 44: Source Driver Signals

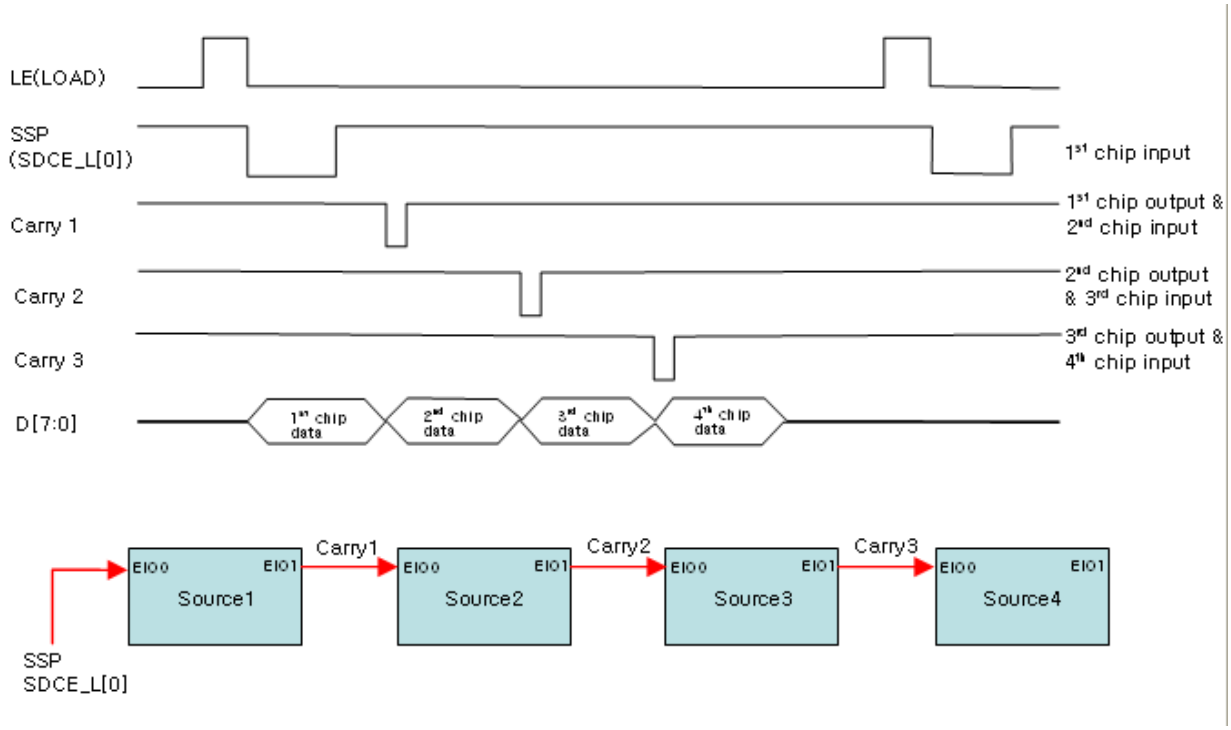
Signal	Description
SDCLK	Clock
SDLE[3:0]	Latch Enables
SDDO[7:0]	8-Bit Data Output
SDCE_L	Chip Enable
SEOE	Output Enable
SDSHR	Shift-right (for 6” panel)

Figure 63: Source Driver Connections



The EPDC uses the SDSHR pin to control the source driver data shifting direction.

Figure 64: Source Driver Timing



8.2.5 Gate Driver Interface

The gate driver turns on each panel row after the source drivers are filled with up to 1600 pixels split across up to four driver ICs.

The gate driver signals are all output, as listed in Table 45.

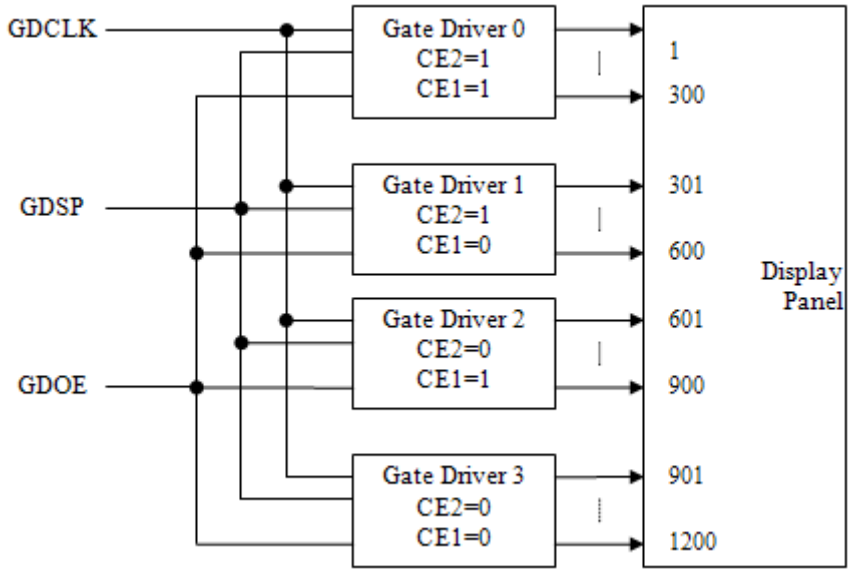
Table 45: Output Gate Driver Signals

Signal	Description
GDCLK	Clock
GDSP	Start Pulse
GDRL	Shift right/left (6” panel)

The GDRL pin controls gate driver shift up or down functionality.

The gate driver connections are shown in Figure 65.

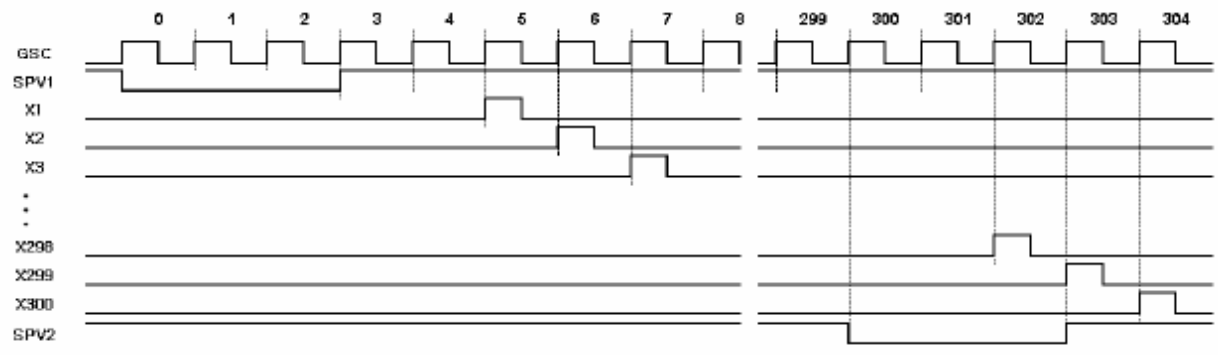
Figure 65: Gate Driver Connections



8.2.6 Start Pulse Control

The signal, GDSP, is the gate driver start-pulse signal. It determines the beginning of a frame scanning. The timing is shown in Figure 66.

Figure 66: Gate Driver Output Enable Timing



8.3 Schematic Checklist

Table 46 briefly describes requirements to add in schematics reviews. Refer to the various sections within this chapter for more information about these requirements.

Table 46: ARMADA 16x Applications Processor Family Schematic Checklist

✓	Signal Name	Recommended Connection	Recommended Value	Notes
		Clocks, Power and Reset Signals		
	RESET_IN_IN	Weak pull-up	4.7 - 10 kΩ to VDD_IO3	
	PXTAL_IN	Filtering capacitor	10 pF	3
	PXTAL_OUT	Filtering capacitor	10 pF	3
	A_ISET	Pulldown	6.04 kΩ ±1%	
	PXTAL_IN, PXTAL_OUT	External clock source	Connect 26 MHz clock to PXTAL_IN and leave PXTAL_OUT floating.	
		JTAG Interface		
	PRI_TCK	Pulldown	10 - 100 kΩ	
	PRI_TDI	Pullup	10 - 100 kΩ to VDD_IO3	1
	PRI_TMS	Pullup	10 - 100 kΩ to VDD_IO3	1
	PRI_TRST_N	Pullup	10 - 100 kΩ to VDD_IO3	
	JTAG_SEL	Pulldown	Pulldown to VSS	
		DDR SDRAM		
	CALPAD	Pulldown (for LPDDR1 or DDR2)	300 Ω ±1%	
	CALPAD	Pulldown (for DDR3)	240 Ω ±1%	
	SEC_CS_SEL	2nd Chip Select and DDR3 Enable	When using the second DDR chip select (nSDCS1) or DDR3, connect to VDD_IO3	6, 7
	nDDR_RESET	Connect to DDR3 device reset signal		3, 4
	nSDCS1	Connect to second DDR device Chip Select		3, 4
	ODT1	ODT for nSDCS1		3, 4
	SDCKE1	Clock Enable of nSDCS1		3, 4
	VREF	VDDQ +/-1%	Use separate VREF supplies for SOC and SDRAM	5
	SDCKE	Pulldown to GND	4.7 kΩ	6
	DQS<1:0>	Pulldown to GND	1 kΩ	7
	nDQS<1:0>	Pullup to VDD_M	1 kΩ	7, 5

Table 46: ARMADA 16x Applications Processor Family Schematic Checklist (Continued)

✓	Signal Name	Recommended Connection	Recommended Value	Notes
	Series Termination Resistors	Not Required		
	Shunt Termination to VTT	Required for address and control signals		
	NAND Flash Controller			
	ND_RnB<1:0>	Pullup to VDD_IO0	2.7kΩ - 4.7kΩ	
	Static Memory Controller			
	SMC_RDY	Pullup to VDD_IO0	2.7kΩ - 4.7kΩ	
	Compact Flash Controller			
	CF_nRESET	Connect to the hardware reset of the Compact Flash Card		8
	XD Controller			
	XD_RnB	Pullup to VDD_IO0	2.7kΩ - 4.7kΩ	
	SD/MMC Controller			
	MMCx_CMD	Pullup to MFP VDD_IOx supply	4.7kΩ - 10kΩ	9
	MMCx_DAT0	Pullup to MFP VDD_IOx supply	4.7kΩ - 10kΩ	10
	MMCx_DAT3	Pullup to MFP VDD_IOx supply	4.7kΩ - 10kΩ	11
	XD Controller			
	I2C_SDA, PWR_SDA	Pullup to MFP VDD_IOx supply	1.2kΩ - 4.7kΩ	
	I2C_SDA, PWR_SDA	Pullup to MFP VDD_IOx supply	1.2kΩ - 4.7kΩ	
	One-Wire Controller			
	One_wire	Pullup to MFP VDD_IOx supply	4.7kΩ	
	USB OTG Controller			
	AVDD5_USB	Connect to 5V@10mA when using host mode	Current limiting resistor needed to limit current to 10 mA.	
	USBVBUS	Connect to Host Controller VBUS	Current limiting resistor needed to limit current to 10 mA.	
	Ethernet Controller			
	MDIO	Pullup to MFP VDD_IOx supply	1.5kΩ	

Table 46: ARMADA 16x Applications Processor Family Schematic Checklist (Continued)

✓	Signal Name	Recommended Connection	Recommended Value	Notes
	RJ-45 Capacitor	Ensure at least 2kV voltage rating		
		PCI Express Controller		
	Routing	Dedicated clock pair for processor and connector / peripheral (no tee/daisy chain routing)		
	Differential pairs	PCIe 2.5GHz- 75..200nF AC blocking caps on all diff pairs		
		Multi-Function Pins		
	Unused Multi-Function Pins	Leave floating		
	Pullup/down resistors	Ensure external pull resistors match the internal pull resistor states		12, 13

NOTE:
1. Required for test logic reset sequence
2. Capacitor values depend on crystal requirements. Contact crystal manufacturer for correct capacitor values required for crystal accuracy and functionality.
3. SEC_CS_EN must be connected to the same voltage level as VDD_IO3 prior to using
4. Do Not connect to VSS when SEC_CS_EN is connected to VDD_IO3
5. Must be connected to the same power supply as Armada 16x Application Processor
6. Needed to allow DDR device to go into low power modes.
7. Place as close as possible to the DQS<1:0> pins.
8. Without this connection software cannot reset the CF card through the card register accesses
9. Response corruption will occur if the CMD signal does not rise fast enough when operating in open-drain mode during card initialation.
10. The DAT0 can float near GND incorrectly signaling a device BUSY status to the host controller.
11. The DAT3 can float near GND during CMD0 transmission which can incorrectly place some devices into SPI mode.
12. Check the pull state in the alternate function spreadsheet to verify internal pull states.
13. Pull resistors are only valid when the MFP is configured as an output

Note

Marvell's schematic review checklist does not replace a customer's in-house design review or substitute for training in design or Marvell architecture basics. Although Marvell makes a good faith effort to find potential design problems, the customer remains responsible for the success of their design. Marvell makes no claims or guarantees that the Marvell checklist will uncover all defects, or that the design will work. Neither does Marvell accept responsibility for any impact to the customer's project schedules.

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