Correction to "Graph Minor Approach for Application Mapping on CGRAs"

Liang Chen, Tulika Mitra
National University of Singapore
{chenliang, tulika}@comp.nus.edu.sg

Following the publication of the article "Graph Minor Approach for Application Mapping on CGRAs" [1] in the proceedings of the International Conference on Field Programmable Technology (ICFPT) 2012, we received correspondence [2] pointing to some inaccuracies in the article. With this correction, we would like to clarify some points that could otherwise be misconstrued.

In Section II, the sentence "However, none of these approaches attempt to share routes corresponding to different edges with the same source." should have been "However, sharing routes for different edges with the same source is not fully explored in most of these techniques."

Following the publication of [1], we were informed that although route sharing is not mentioned in the paper we referenced [3], brand DRESC includes route sharing. Mei's PhD thesis proposed and evaluated a simple route sharing algorithm. In [4], De Sutter et al. state that their proposed register sharing approach for register allocation in CGRAs need not be restricted to register files and can be used in other contexts. While route sharing through functional units is not explicitly highlighted in these articles, they did integrate such route sharing.

We note that our fundamental contribution is the formalization of the CGRA mapping problem with route sharing as a graph minor problem. This systematic approach of formally modeling the mapping problem and then designing the algorithm that exploits insights from the formalization is the main source of efficiency of our approach. The formalization also allows us to identify the optimal solution given enough compilation time. Following the correspondence, we integrated route sharing in our implementation of the simulated annealing (SA) algorithm [3] and graph minor still performs better than SA [5]. This confirms that the mapping quality is not only about route sharing, but whether the algorithm supports route sharing efficiently.

We would like to clarify that in the experimental evaluation section, we should have stressed that we re-implemented the simulated annealing (SA) based algorithm in [3] and the comparison was not against brand DRESC compiler. It would be more appropriate to replace all the references to "DRESC" with "DRESC-like" or "SA". The reported compilation times are representative for our re-implementation targeting a homogeneous 4x4 CGRA with no shared register files and not for brand DRESC on ADRES architecture with a central register file. For brand DRESC, the literature [3] presents faster compilation times on ADRES architecture.

The statement "As DRESC does not explicitly handle routing through register files and heterogeneous FUs..." should be removed. The routing through register files and heterogeneous FUs under DRESC framework has been addressed in [4].

We refer the readers to our technical report [5], which is an extended version of [1], for a more comprehensive treatment of the material including the correction and the clarification.

We thank the authors of the correspondence [2] for highlighting the inaccuracies and the Steering Committee of the ICFPT for giving us an opportunity to clarify the concerns through this correction.

REFERENCES

[1] L. Chen and T. Mitra, "Graph minor approach for application mapping on CGRAs," in *Proceedings of the International Conference on Field-Programmable Technology (ICFPT)*, 2012, pp. 285–292.
[2] B. De Sutter, "Private correspondence."
[3] B. Mei, S. Vernalde, D. Verkest, H. De Man, and R. Lauwereins, "Exploiting loop-level parallelism on coarse-grained reconfigurable architectures using modulo scheduling," in *Proceedings of the Design, Automation and Test in Europe Conference and Exhibition (DATE)*, 2003, pp. 296–301.
[4] B. De Sutter, P. Coene, T. V. Aa, and B. Mei, "Placement-and-routing-based register allocation for coarse-grained reconfigurable arrays," in *Proceedings of the ACM SIGPLAN-SIGBED Conference on Languages, Compilers, and Tools for Embedded Systems (LCTES)*, 2008, pp. 151–160.
[5] L. Chen and T. Mitra, "Graph minor approach for application mapping on CGRAs," School of Computing, National University of Singapore, Tech. Rep. TRB6/13, 2013.

978-1-4799-2198-0/13/$31.00 ©2013 IEEE