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T b B

j ȷﬀ ȷ

Analog Discovery 2™ Reference Manual

Revised September 14, 2015
This manual applies to the Analog Discovery 2 rev. C

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ﬆﬀ ﬀ

ﬆﬀ ﬀ ﬀ ﬀ ﬀ b ﬀ

ﬆﬀ ȷ ﬀ

ﬀ ﬀ b

ﬆﬀ B

B b i ﬀ ȷ

ǰ ȷ b ﬀ ȷ

ﬆﬀ ǰ b b ȷ i

ﬆﬀ ﬆﬀ b b b ﬀ ȷ ȷ

3 Arbitrary Waveform Generator 23

B B

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B K

B

B ȷ

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B b i ﬆﬆᵇ

ﬀ ﬆﬆᵇ

ﬀ bi ﬀ ﬆﬆȷﬀ

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ȷi ȷ b Tb ﬀ ﬀ ﬀ b

ȷi ȷ b K

T ﬀ ﬆﬆȷﬀ

ﬀ B b ᵇ ᵍ ﬀ

ﬀ ﬀ

ﬆﬀ B b ᵇ ᵍ ﬀ

ﬀ ﬃb ﬀ

Overview

[illegible]

The Analog Discovery 2.

- [illegible]
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- [illegible]
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- [illegible]
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- [illegible]
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- [illegible]
- [illegible]
- [illegible]

[illegible]

B b i ȷ ff ᵇ ȷ ff ffᵃ i ff ff b ȷ ff ff ᵇ st st b B b i ȷ ff ᵇ ff bȷ ȷ st ff ff b ff

- B ȷȷ ᵇ ff b ffᵃ ff b st ff ststᵇ b ff ff ᵇ ff ȷ ff ff st ff ff ff ststȷff ff st ff ff ffB b i ȷ ff ᵇ ff ȷ ff ff ff b ff st ff b ffB b i ȷ ff ᵇ
- ff ff ff ȷ ff b ff ff ji b ȷ st ff ff ff jb ȷȷ ᵇ
- K st ff ji b ȷ ff b b stff b ff ff stff b b ff i ff ff b
- ff ff ff ȷ ff b ȷ ff stff b b ff i ff ff b

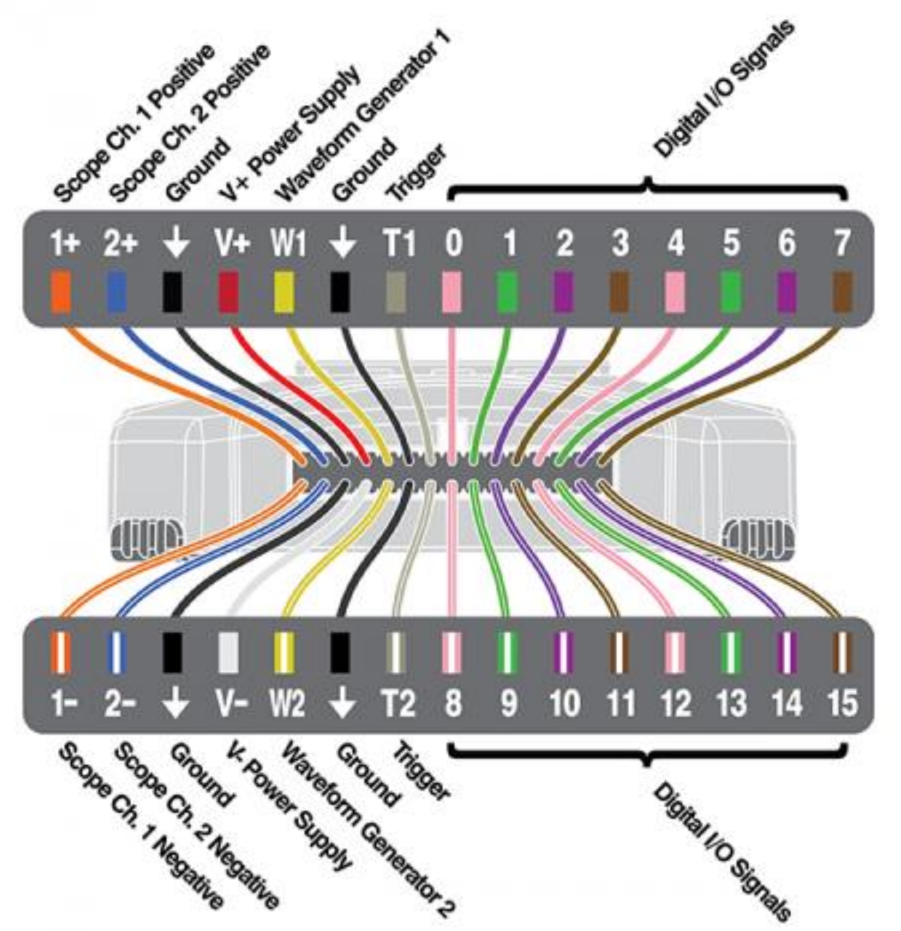

Scope Ch. 1 Positive
Scope Ch. 2 Positive
Ground
V+ Power Supply
Waveform Generator 1
Ground
Trigger
Digital I/O Signals
1+
2+
V+
W1
T1
0
1
2
3
4
5
6
7
1-
2-
V-
W2
T2
8
9
10
11
12
13
14
15
Scope Ch. 1 Negative
Scope Ch. 2 Negative
Ground
V- Power Supply
Waveform Generator 2
Ground
Trigger
Digital I/O Signals

Figure 1. Analog Discovery 2 pinout diagram.

1 Architectural Overview and Block Diagram

B b i ȷ ff ᵇ ji ff ff jbi b ȷ st ff ff ff ȷ ji ff ff ff ffB b i ȷ ff ᵇ ȷ ff ȷȷ ᵃ stb b T B stff ȷȷ b ᵇ ff O O ff ȷ ff ff b ff bststȷ b ȷ b b ȷ b ᵇ st i b ff ȷ ff ᵇ T B b b st ȷ b ji b ȷ ȷ ff ff ji ff ȷ stff ff b ȷ ȷ ff b ffb ff ff ȷ ff ff st i b ff ff T B ȷ ȷ ff ff ȷ ff ᵇ ȷ b ff ȷ ff T b ff b ff bststȷ b ȷ jb b ff ȷ ff b ff b ff ȷ ff T B b ff ȷ b ffB b i ȷ ff ᵇ ȷ ȷ i ff ȷ i stb b ff ff b ȷ ȷ i b b b b ff ȷ i b ȷ i b b

ji b ȷ ff **Analog Input** b b ff ff **Scope** ff ȷ ffᵃ ff ȷ ȷ b ff ffᵇ b ff ff b ff ff stff ji b ȷ ff **Analog Output** b b ff **AWG** ff B ȷ ffᵃ ff b ji b ȷ ff **Digital** ff b **D** ȷ ffᵃ b ff ȷ ff ff ff ᵇ ff ȷ ff ᵇ b b ff ff ff ȷ ȷ ȷ ff ff ffff

[illegible]

- [illegible] **Analog Inputs/Scope** [illegible]
  - **Input Divider and Gain Control** [illegible]
  - **Buffer** [illegible]
  - **Driver** [illegible]
  - **Scope Reference and Offset** [illegible]
  - **ADC** [illegible]
- [illegible] **Arbitrary Outputs/AWG** [illegible]
  - **DAC** [illegible]
  - **I/V** [illegible]
  - **Out** [illegible]
  - **Audio** [illegible]
- [illegible] **Oscillator** [illegible] **Clock Generator** [illegible]
- [illegible] **Digital I/O** [illegible]
- [illegible] **Power Supplies and Control** [illegible]
- [illegible] **USB Controller** [illegible]
- [illegible] **Calibration Memory** [illegible]

[illegible] **(4)** [illegible] **(3)** [illegible] *mux* [illegible] *in* [illegible] *P* [illegible] *N* [illegible] *diff* [illegible]

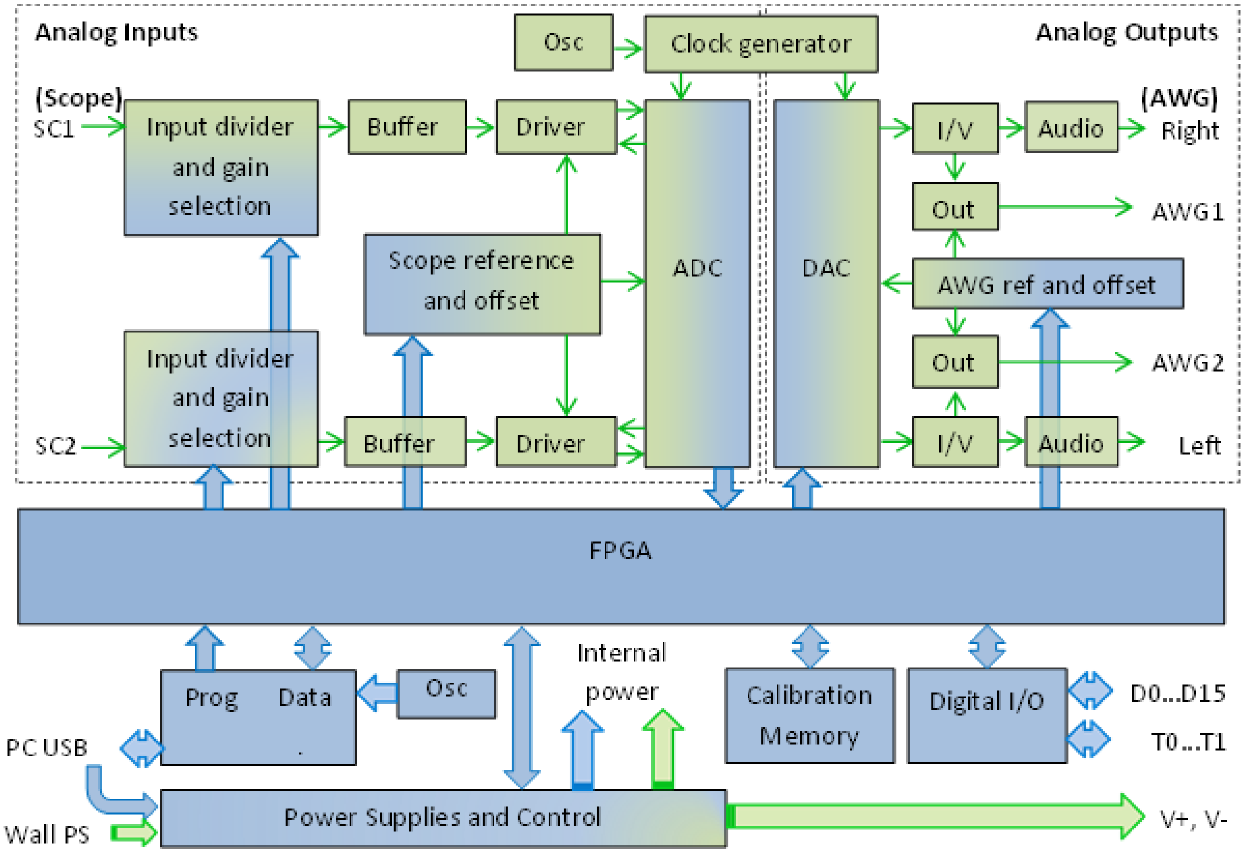

Analog Inputs
Osc
Clock generator
Analog Outputs
(Scope)
SC1
Input divider and gain selection
Buffer
Driver
ADC
DAC
I/V
Audio
(AWG)
Right
Out
AWG1
Scope reference and offset
AWG ref and offset
Out
AWG2
Input divider and gain selection
SC2
Buffer
Driver
I/V
Audio
Left
FPGA
Prog
Data
Osc
Internal power
Calibration Memory
Digital I/O
D0...D15
T0...T1
PC USB
Wall PS
Power Supplies and Control
V+, V-

Figure 2. Analog Discovery 2 block diagram.

2 Scope

Unlike traditional inexpensive scopes, the Analog Discovery 2 inputs are fully differential. However, a GND connection to the circuit under test is needed to provide a stable common mode voltage. The Analog Discovery 2 GND reference is connected to the USB GND. Depending on the PC powering scheme, and other PC connections (Ethernet, audio, etc. – which might also be grounded) the Analog Discovery 2 GND reference might be connected to the whole GND system and ultimately to the power network protection (earth ground). The circuit under test might also be connected to earth or possibly floating. For safety reasons, it is the user's responsibility to understand the powering and grounding scheme and make sure that there is a common GND reference between the Analog Discovery 2 and the circuit under test, and that the common mode and differential voltages do not exceed the limits shown in equation (1). Furthermore, for distortion-free measurements, the common mode and differential voltages need to fit into the linear range shown in Figs. 12 and 13. For those applications which scope GND cannot be the USB ground, a USB isolation solution, such as what is described in ADI's CN-0160 can be used; however, this will limit things to USB full speed (12 Mbps), and will impact the update rate (screen refresh rates, not sample rates) of the Analog Discovery 2.

2.1 Scope Input Divider and Gain Selection

Error! Reference source not found. ﬀ ﬆﬀ ȷ ﬆ ȷ ȷ ﬀ b i bȷ ﬀ ﬀ ȷ bi ﬀ

- b J g
- ﬆ ﬀb

ﬀO bJ J

$$\frac{V_{mux}}{V_{in}} = \frac{R_6}{R_1 + R_4 + R_6} = 0.019 \quad (3)$$

ﬀO bJ J ﬀ J ﬆ bi ﬀ

$$\left|V_{in\,diff}\right| = \left|V_{in\,P} - V_{in\,N}\right| < 50V \quad (4)$$

ﬀ ĳ bJ J

$$\frac{V_{mux}}{V_{in}} = \frac{R_4 + R_6}{R_1 + R_4 + R_6} = 0.212 \quad (5)$$

ﬀ ĳ bJ J ﬀ J ﬆ bi ﬀ

$$\left|V_{in\,diff}\right| = \left|V_{in\,P} - V_{in\,N}\right| < 7V \quad (6)$$

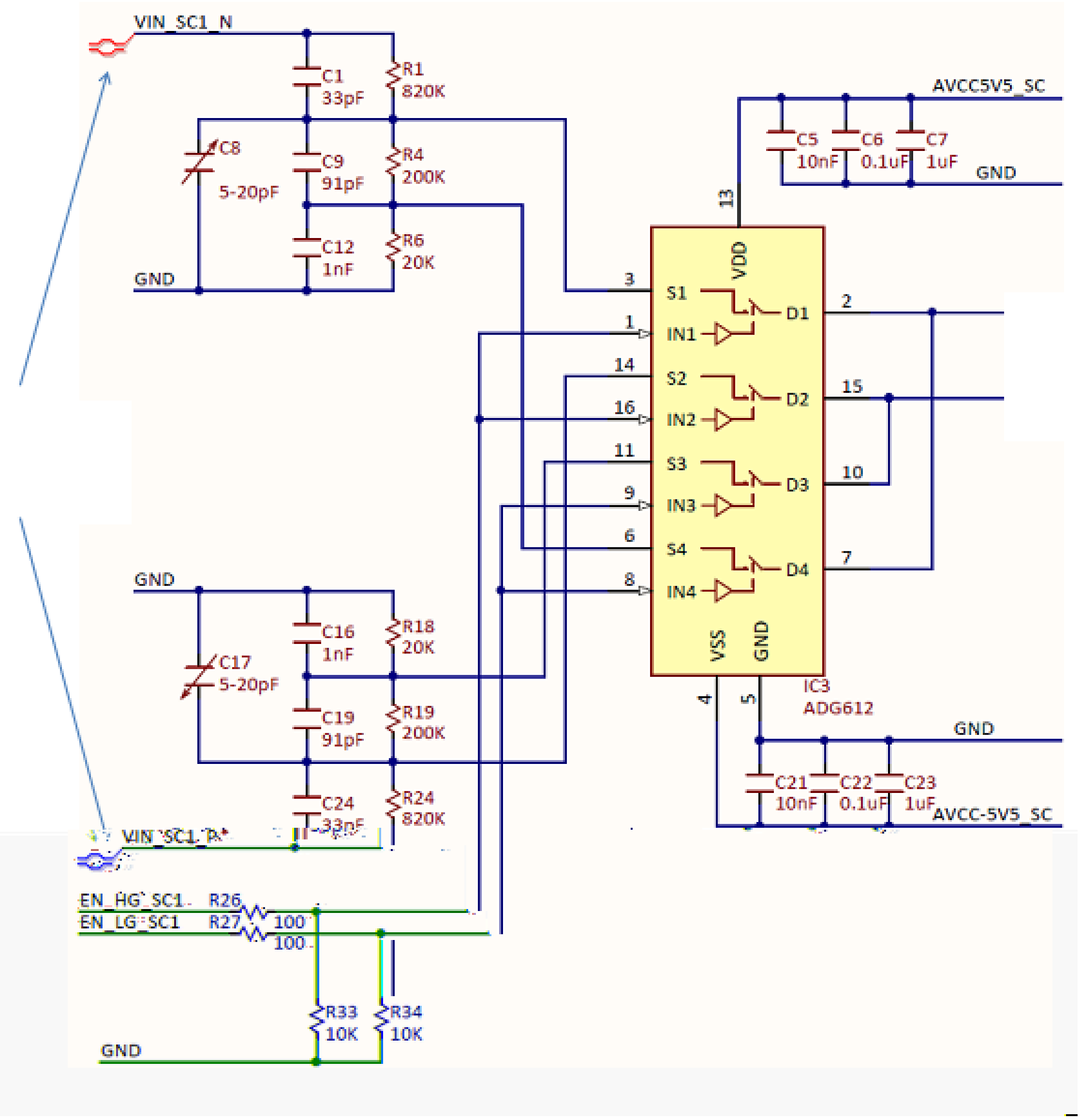

VIN_SC1_N
C1
33pF
R1
820K
C8
5-20pF
C9
91pF
R4
200K
C12
1nF
R6
20K
GND
AVCC5V5_SC
C5
10nF
C6
0.1uF
C7
1uF
GND
13
VDD
3
S1
D1
1
IN1
2
14
S2
D2
15
16
IN2
11
S3
D3
10
9
IN3
6
S4
D4
7
8
IN4
VSS
GND
4
5
IC3
ADG612
GND
C16
1nF
R18
20K
C17
5-20pF
C19
91pF
R19
200K
C24
33nF
R24
820K
GND
C21
10nF
C22
0.1uF
C23
1uF
AVCC-5V5_SC
VIN_SC1_P
EN_HG_SC1
EN_LG_SC1
R26
R27
100
100
R33
10K
R34
10K
GND

Figure 3. Input divider and gain selection.

2.2 Scope Buffer

B ȷ ff ȷ i ﬆB ﬆ bi ffﬆ ȷ ff ffᵇ ĳ ȷ ﬆff b ffb b ffȷ ﬆ ȷ ȷ ff ĳ ff

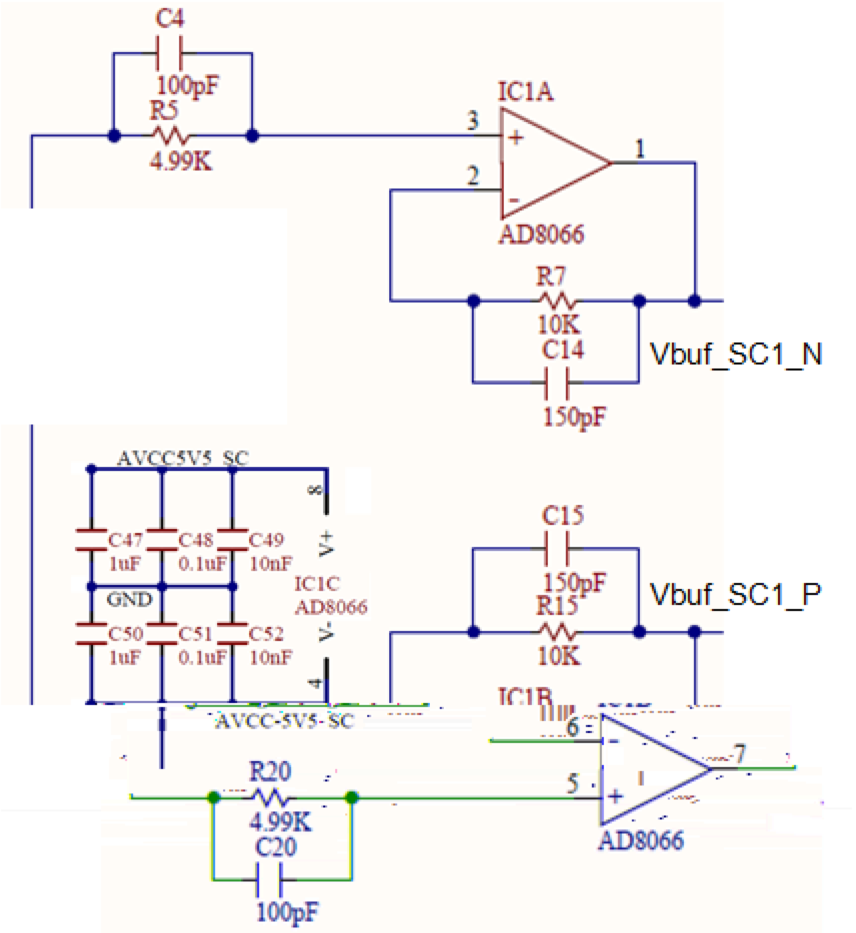

C4
100pF
R5
4.99K
IC1A
3
2
1
AD8066
R7
10K
C14
150pF
Vbuf_SC1_N
AVCC5V5_SC
8
V+
C47
1uF
C48
0.1uF
C49
10nF
GND
IC1C
AD8066
C50
1uF
C51
0.1uF
C52
10nF
V-
4
C15
150pF
R15
10K
Vbuf_SC1_P
IC1B
AVCC-5V5-SC
R20
4.99K
C20
100pF
6
5
7
AD8066

Figure 4. Scope buffer.

ff ff ffb ff ffB b ff

- ȷ ﬆ b ﬆȷ ȷff
- ﬆB ȷ ﬆ ȷb ff
- O
- ĳ ﬆfff ᵍ b ȷ
- ff b ff
- O ȷ ff ᵍ ᵍ B ᵍ ᵍ
- ȷ ff ﬆﬆᵇ bi ff b i ff
- bȷ bȷ ﬆ
- O ff bi ff bᵃ ȷ
- ᵃ ff ff ȷ ȷ ﬆff ȷ ȷ b ȷ
- ᵍ
- O ﬆ ff B b ﬆȷ ȷff ᵇ ﬆĳ b ﬆﬆᵇ ff
- b ﬆb bi ȷ i T

[illegible]

[illegible]

[illegible] $$-5.5V < V_{mux\,P}, V_{mux\,N} < 2.2V \tag{7}$$

[illegible] $$-5.38V < V_{buf\,P}, V_{buf\,N} < 5.4V \tag{8}$$

[illegible] $$\frac{V_{buf}}{V_{mux}} = 1 \tag{9}$$

2.3 Scope Reference and Offset

[illegible]

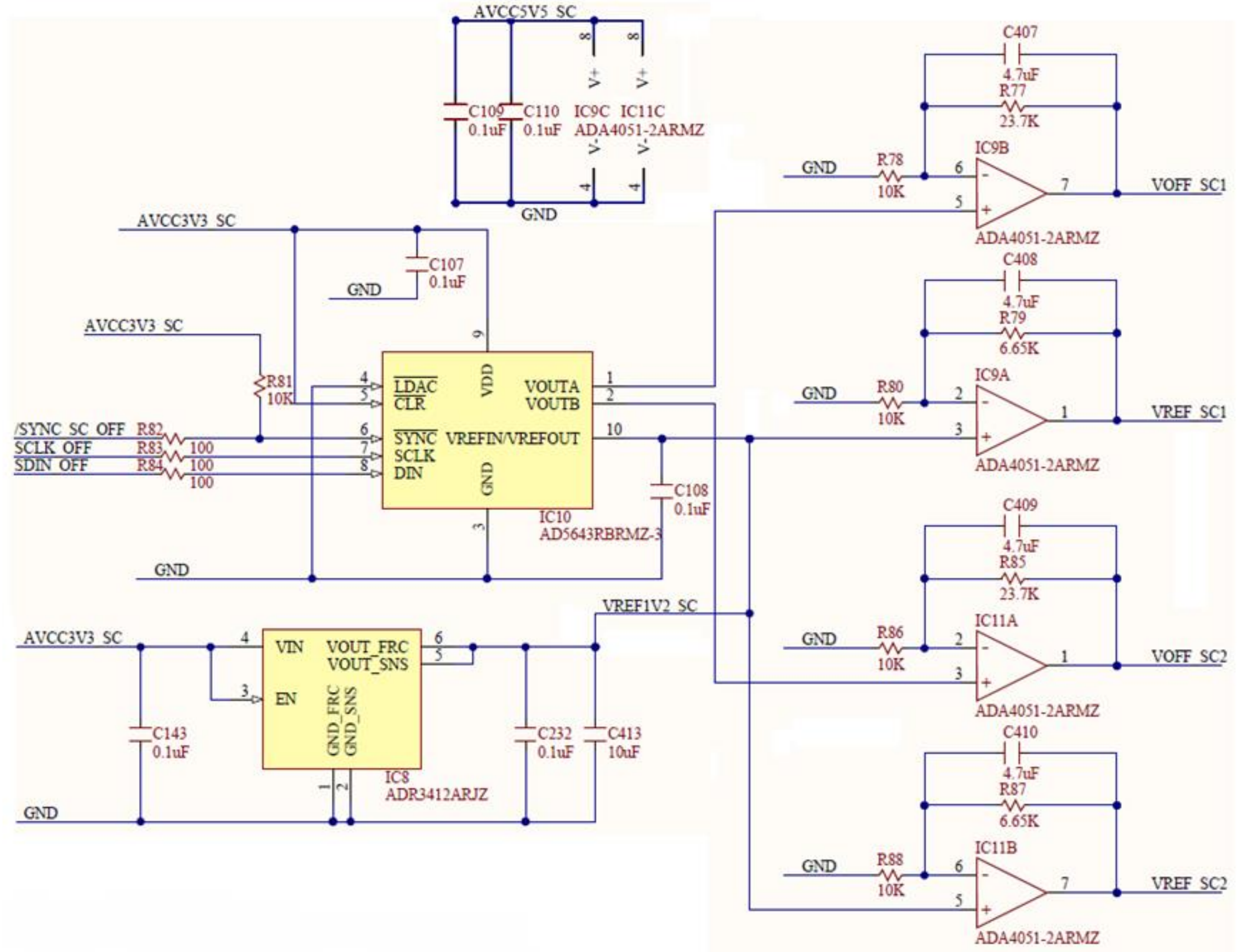

AVCC5V5_SC
C109
0.1uF
C110
0.1uF
IC9C IC11C
ADA4051-2ARMZ
V+
V-
8
4
GND
AVCC3V3_SC
C107
0.1uF
GND
AVCC3V3_SC
R81
10K
/SYNC_SC_OFF
SCLK_OFF
SDIN_OFF
R82
R83
R84
100
100
100
LDAC
CLR
SYNC
SCLK
DIN
VDD
GND
VOUTA
VOUTB
VREFIN/VREFOUT
IC10
AD5643RBRMZ-3
C108
0.1uF
GND
VREF1V2_SC
AVCC3V3_SC
VIN
EN
VOUT_FRC
VOUT_SNS
GND_FRC
GND_SNS
IC8
ADR3412ARJZ
C143
0.1uF
C232
0.1uF
C413
10uF
GND
C407
4.7uF
R77
23.7K
GND
R78
10K
IC9B
ADA4051-2ARMZ
VOFF_SC1
C408
4.7uF
R79
6.65K
GND
R80
10K
IC9A
ADA4051-2ARMZ
VREF_SC1
C409
4.7uF
R85
23.7K
GND
R86
10K
IC11A
ADA4051-2ARMZ
VOFF_SC2
C410
4.7uF
R87
6.65K
GND
R88
10K
IC11B
ADA4051-2ARMZ
VREF_SC2

Figure 5. Scope reference and offset.

B B J ﬆ ﬀ ĳ b b ᵇ bi ﬀ ﬀ ﬀ ﬀ ﬀ

- K J Ĳb b b ᵇ bª J
- O ﬀ ﬆﬀ b ﬀ ﬀ J Ĳﬀ ﬆﬆ
- O Ĳﬀ ﬀ ﬀ B bª J
- ﬆ J ﬀ ᵍ ᵍ ﬆ ﬆb ᵇ ﬆĳ b

B b J b B

- O ﬆ ﬀ b ﬀ b b B
- ﬆ ﬀ ﬆﬆᵇ
- ﬀ Ĳb J ﬀ b ﬀ ﬆ ᵍ

B B J ﬆ ﬀ ﬀ J bJ bJ J ﬆ ﬆ ﬆB ﬆ

- ﬀ ᵇ ﬆﬆᵇ ﬀ B ᵇ ﬆĳ b
- O ﬀ bi ﬀ bª J
- ﬀ bi ﬀ J
- ĳ T J J
- bJ bJ J ﬆ ﬆ
- J ᵇ i bJ b ﬀ

ﬀ ﬀ ﬀ ﬀ ﬀ bi ﬀ i ﬀ ﬀ b ﬀ ﬀ ﬆﬀ bi ﬀ b ﬀ

$$V_{ref\,SC} = V_{ref\,1V2} \cdot \left(1 + \frac{R_{79}}{R_{80}}\right) = 2V \qquad (10)$$

ﬀ ﬀ bi ﬀ ﬀ ﬆﬀ bi ﬀ b ﬀ

$$0 \le V_{off\,SC} = V_{out\,AD5643} \cdot \left(1 + \frac{R_{77}}{R_{78}}\right) < 4.044V \qquad (11)$$

2.4 Scope Driver

B B B J ﬀ ﬀb ﬀ

- b ĳ b b J ᵍ
- ª ﬀ ﬀᵇ b J J J b ᵍ b ᵍ
- O J ﬆ bi ﬀ J ﬀ ᵍ
- bª J ﬀ bi ﬀ
- ﬀ J i J ﬀ
- bJ bJ ﬆ
- B n b ﬀ ﬆ ﬀ bi ﬀ
- ﬀª J ﬀ ﬆ ﬀ ﬆﬆ Ĳﬀ O T
- b ﬆ ﬀ B

K **Error! Reference source not found.** J ﬀ

- J J i ﬀ J ﬀ ﬀ Ĳb J ﬆ ﬀ B J J ﬆﬀ b ﬀ ﬆ
- T J J i ﬀ ﬀ bi ﬀ ﬀ B
- B J i ﬀ ﬀ ﬀ J b ﬆ J J ﬀ ﬆﬀ J b b J b i ﬀ J bᵇ ﬀ b ﬀ ﬀ b ﬀ ﬀJ ﬀ ﬆ J J ﬀ ﬃ b J ﬀ

- B ﬆ ﬀ J ᵇ b ﬆĳ i ﬀ ﬆ ĳ b T ﬀ J J J ﬆ b J ﬀK J ﬆﬆJﬀ Jﬀ ﬀB J ﬆ ᵇ ﬆﬆ ﬀK B b ﬆ ĳ b b b b ﬆĳ i bi ﬀ ﬀ ᵇ J ﬀ

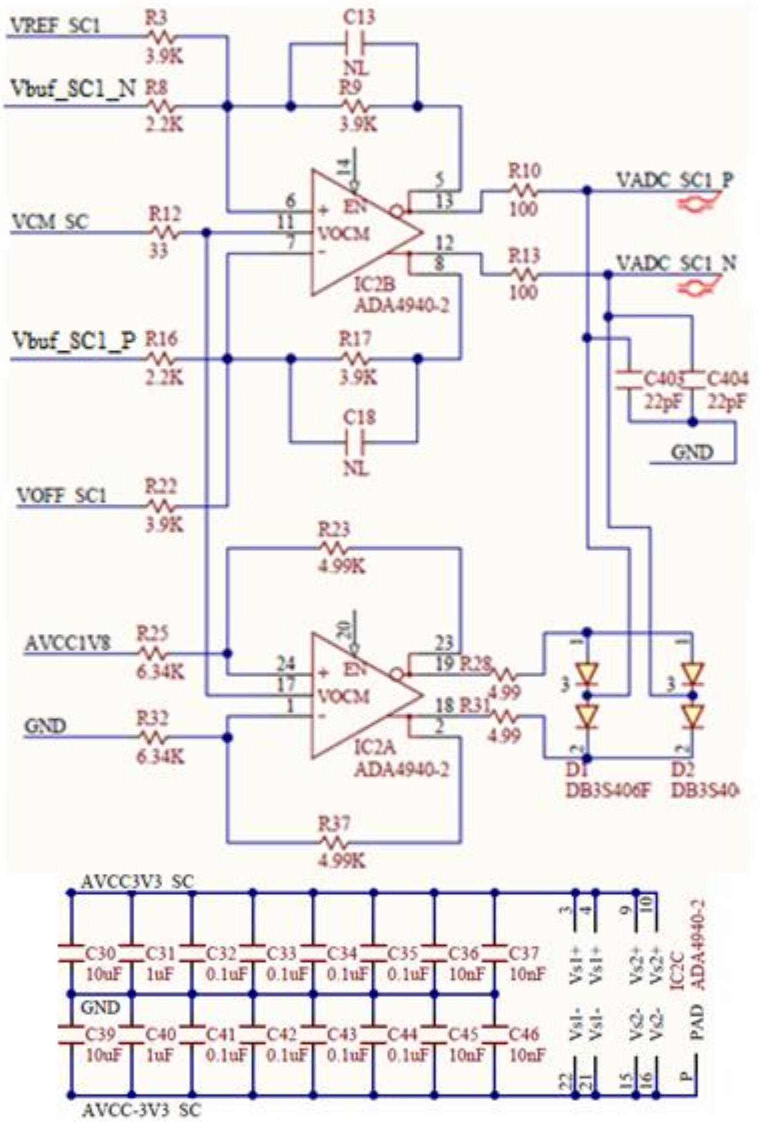

VREF_SC1
R3
3.9K
C13
NL
Vbuf_SC1_N
R8
2.2K
R9
3.9K
14
5
13
6
11
7
EN
VOCM
12
8
IC2B
ADA4940-2
R10
100
VADC_SC1_P
R13
100
VADC_SC1_N
VCM_SC
R12
33
Vbuf_SC1_P
R16
2.2K
R17
3.9K
C403
22pF
C404
22pF
GND
C18
NL
VOFF_SC1
R22
3.9K
R23
4.99K
AVCC1V8
R25
6.34K
20
24
17
1
23
19
R28
4.99
18
R31
4.99
2
IC2A
ADA4940-2
GND
R32
6.34K
R37
4.99K
D1
DB3S406F
D2
DB3S40
AVCC3V3_SC
C30
10uF
C31
1uF
C32
0.1uF
C33
0.1uF
C34
0.1uF
C35
0.1uF
C36
10nF
C37
10nF
C39
10uF
C40
1uF
C41
0.1uF
C42
0.1uF
C43
0.1uF
C44
0.1uF
C45
10nF
C46
10nF
Vs1+
Vs1+
Vs2+
Vs2+
Vs1-
Vs1-
Vs2-
Vs2-
PAD
IC2C
ADA4940-2
3
4
9
10
22
21
15
16
P
AVCC-3V3_SC

Figure 6. Scope driver.

B B J ﬆﬆJﬀ ﬀ ﬀ bi ﬀ b i ﬀJ

$$-3.5V < V_{+\,ADA4940} = V_{-\,ADA4940} < 2.1V \qquad (12)$$

ﬀ ĳ b bJ J

$$\frac{V_{ADC\,diff}}{V_{buf\,diff}} = \frac{R_9}{R_8} = \frac{R_{17}}{R_{16}} = 1.77 \qquad (13)$$

ﬀ ﬀ bJ J

$$\frac{V_{ADC\,diff}}{V_{offSC} - V_{refSC}} = \frac{R_9}{R_3} = \frac{R_{17}}{R_{22}} = 1 \qquad (14)$$

ﬀ ﬀ bJ J

$$\frac{V_{CM}}{\frac{V_{ADC\,P} + V_{ADC\,N}}{2}} = 1 \qquad (15)$$

ﬀ b ﬆĳ i bi ﬀ b ﬀ

$$V_{Out-IC2A} = V_{CM} - \frac{AVCC1V8}{2} \cdot \frac{R_{23}}{R_{25}} = 0.9V - \frac{1.8V}{2} \cdot \frac{4.99K}{6.34K} = 0.2V \qquad (16)$$

$$V_{Out+IC2A} = V_{CM} + \frac{AVCC1V8}{2}\cdot\frac{R_{23}}{R_{25}} = 0.9V + \frac{1.8V}{2}\cdot\frac{4.99K}{6.34K} = 1.6V \qquad (17)$$

[illegible]

$$-0.1V < V_{+\,ADA4940} = V_{-\,ADA4940} < 1.9V \qquad (18)$$

2.5 Clock Generator

[illegible]

[illegible]

[illegible]

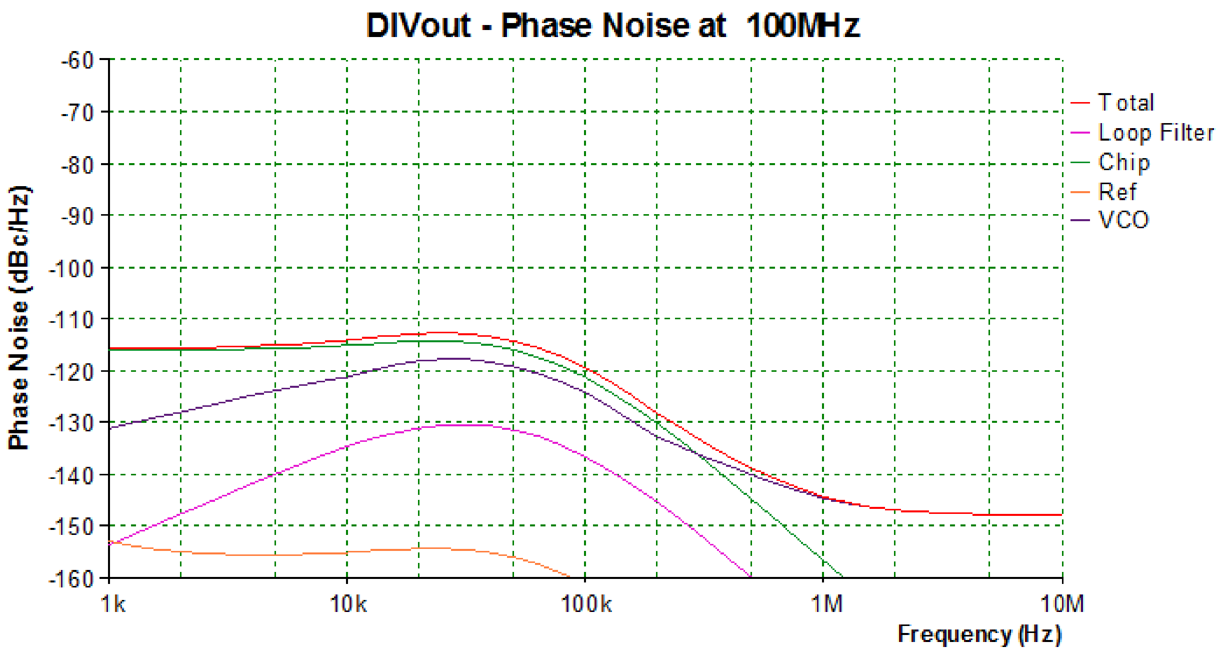


Figure 7. Phase noise figure for the clock generator.

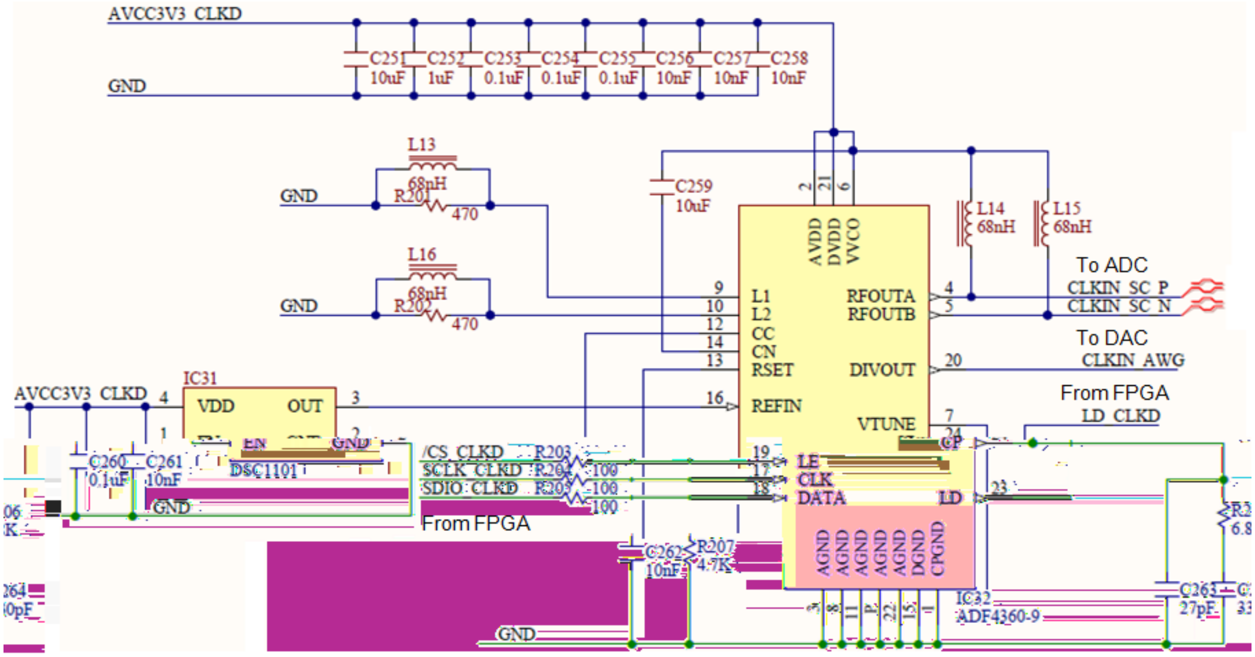

AVCC3V3_CLKD
GND
C251 10uF
C252 1uF
C253 0.1uF
C254 0.1uF
C255 0.1uF
C256 10nF
C257 10nF
C258 10nF
L13 68nH
R201 470
L16 68nH
R202 470
C259 10uF
L14 68nH
L15 68nH
AVDD
DVDD
VVCO
L1
L2
CC
CN
RSET
REFIN
RFOUTA
RFOUTB
DIVOUT
VTUNE
CP
LE
CLK
DATA
LD
AGND
DGND
CPGND
IC32
ADF4360-9
To ADC
CLKIN_SC_P
CLKIN_SC_N
To DAC
CLKIN_AWG
From FPGA
LD_CLKD
IC31
VDD
OUT
EN
GND
DSC1101
C260 0.1uF
C261 10nF
/CS_CLKD
SCLK_CLKD
SDIO_CLKD
R203
R204
R205
100
From FPGA
C262 10nF
R207 4.7K
C263 27pF
R2 6.8
C264 0pF

Figure 8. Clock generator.

2.6 Scope ADC

2.6.1 Analog Section

ffB b i j ff b ff b b b ff ji stffff st ff j T B B b i stb ff B b j ji ff

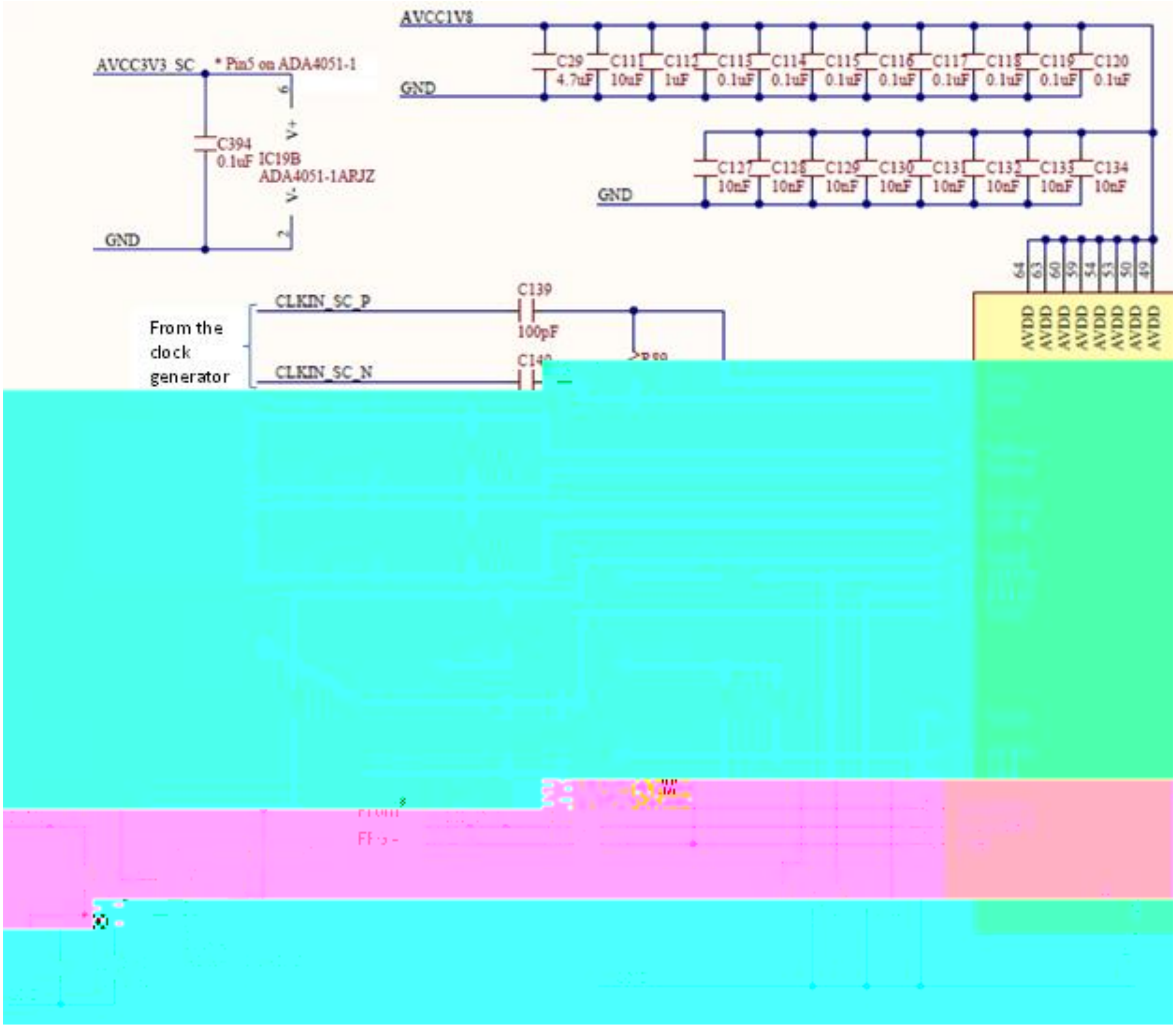

AVCC1V8
AVCC3V3_SC
* Pin5 on ADA4051-1
C29 4.7uF
C111 10uF
C112 1uF
C113 0.1uF
C114 0.1uF
C115 0.1uF
C116 0.1uF
C117 0.1uF
C118 0.1uF
C119 0.1uF
C120 0.1uF
GND
C394 0.1uF
IC19B ADA4051-1ARJZ
V+
V-
C127 10nF
C128 10nF
C129 10nF
C130 10nF
C131 10nF
C132 10nF
C133 10nF
C134 10nF
64 63 60 59 54 53 50 49
AVDD
From the clock generator
CLKIN_SC_P
CLKIN_SC_N
C139 100pF
C140

Figure 9. ADC - analog section.

ff ȷ ﬅ b ﬀb ff B

- g
- g
- O ﬅ ff b ff B ff T
- ȷ ff ff ȷb b b i ȷ ﬅ ȷ g b ȷ
- K b ﬅȷ i ff ff ȷff g
- ȷﬅ bi ff ff ff ff ffb b ﬅff b ȷ ȷ
- ﬅ ﬅ ȷ ff ff ȷb b b i ȷ ﬅ
- O O
- ff ȷb ﬅ ﬅ ȷ
- ff ȷ b b i b b ff ﬅff ff b b b
- ﬅ ȷ b b b ff b ȷ ȷg ff
- K ffi ff ȷ ﬅ ȷ ȷ ff
- b b ﬅ ȷﬅff ﬅ ȷ
- ȷ ȷ ff ff b ff ȷi ȷ b ff ﬅb ff i ff ff b ȷ
- ff i b b ȷ i ﬅ ff ff

- [illegible]

[illegible]

[illegible] $$-1V < V_{ADC\,diff} < 1V$$ (19)

2.6.2 Digital Section

[illegible]

[illegible]

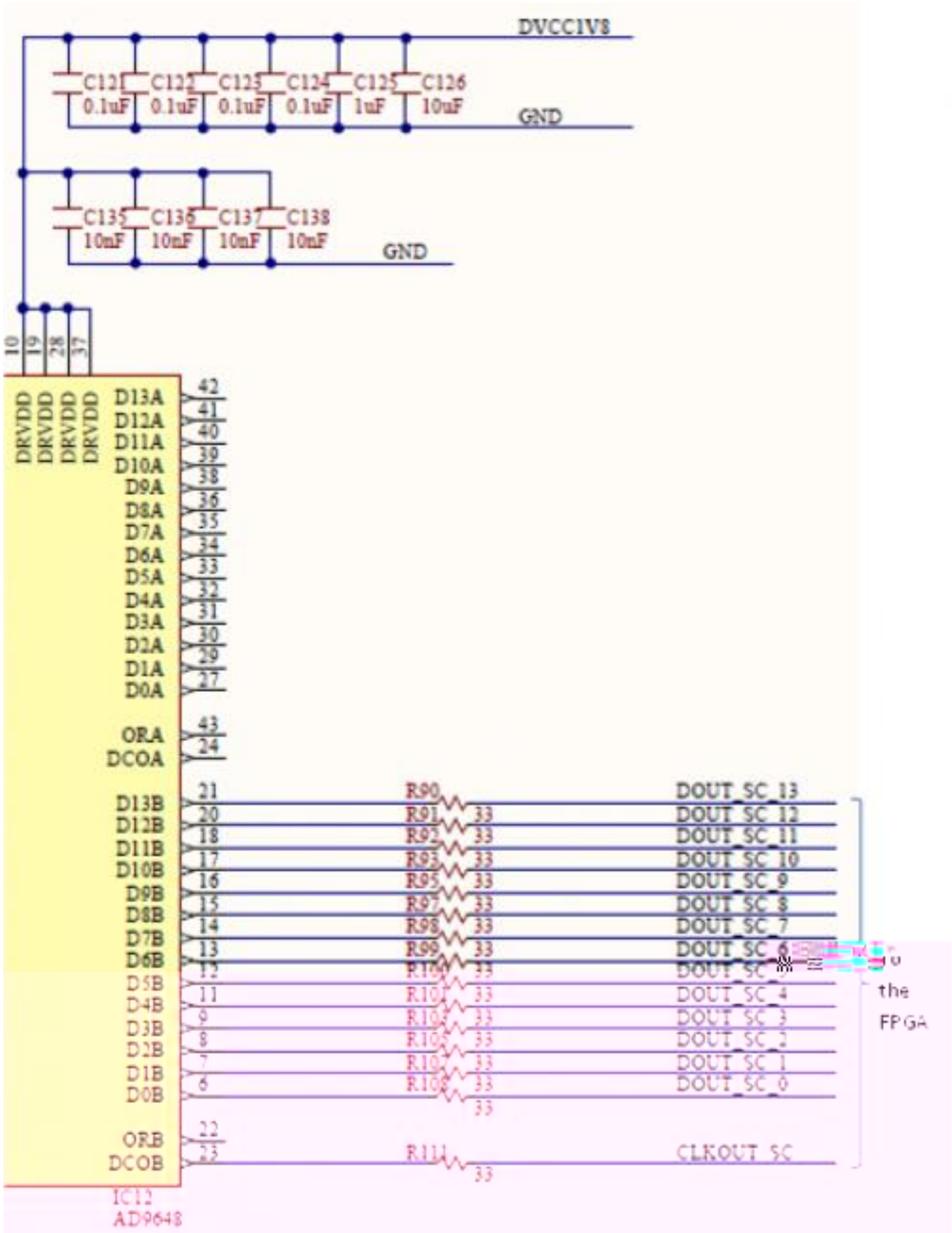

DVCC1V8
C121 0.1uF
C122 0.1uF
C123 0.1uF
C124 0.1uF
C125 1uF
C126 10uF
GND
C135 10nF
C136 10nF
C137 10nF
C138 10nF
GND
10
19
28
37
DRVDD
DRVDD
DRVDD
DRVDD
D13A 42
D12A 41
D11A 40
D10A 39
D9A 38
D8A 36
D7A 35
D6A 34
D5A 33
D4A 32
D3A 31
D2A 30
D1A 29
D0A 27
ORA 43
DCOA 24
D13B 21
D12B 20
D11B 18
D10B 17
D9B 16
D8B 15
D7B 14
D6B 13
D5B 12
D4B 11
D3B 9
D2B 8
D1B 7
D0B 6
ORB 22
DCOB 23
R90 33
R91 33
R92 33
R93 33
R95 33
R97 33
R98 33
R99 33
R100 33
R101 33
R102 33
R103 33
R104 33
R108 33
R111 33
DOUT_SC_13
DOUT_SC_12
DOUT_SC_11
DOUT_SC_10
DOUT_SC_9
DOUT_SC_8
DOUT_SC_7
DOUT_SC_6
DOUT_SC_5
DOUT_SC_4
DOUT_SC_3
DOUT_SC_2
DOUT_SC_1
DOUT_SC_0
CLKOUT_SC
to the FPGA
IC12
AD9648

Figure 10. ADC - digital section.

2.7 Scope Signal Scaling

ȷ ȷ i bȷ ﬀ b ȷ **(3) (5) (9) (13) (14)** b **(15)** ﬆ ﬀ ȷ bﬆ ﬀ ﬀ b ﬆﬀi bȷ b ﬀ

$$Low\ Gain = \frac{V_{ADC\ diff}}{V_{in\ diff}} = 0.034$$

$$High\ Gain = \frac{V_{ADC\ diff}}{V_{in\ diff}} = 0.375 \qquad (20)$$

ȷ ȷ i ﬀB ȷ ﬅ bi ﬀ b i ﬀ ȷ **(19)** ȷ V_{offsc} b ﬀ ȷ b i ﬀ **(11)** ﬅﬀ ﬀ ȷ b ﬅ ȷ ȷ b ﬀ ȷ b i ﬀȷ

$$at\ Low\ Gain:\ -30V < V_{in\ diff} < 28.6V$$

$$at\ High\ Gain:\ -2.7V < V_{in\ diff} < 2.6V \qquad (21)$$

ﬀ ﬅ ﬀ b ﬀ ﬀb ﬀ b b b ﬀ b ȷ b ȷ ᵇ ﬀ b i ﬀ ﬀ b ﬀ ﬅﬀ ȷ ȷﬀ

$$at\ Low\ Gain:\ -25V < V_{in\ diff} < 25V$$

$$at\ High\ Gain:\ -2.5V < V_{in\ diff} < 2.5V \qquad (22)$$

ﬀﬀ ﬀ ﬀ ﬀ ﬀ ȷ i ﬅﬀ ﬀ ȷ b ﬅ ȷ ȷ b ﬀ b b ﬀ **(10) (11)** b **(14)**

$$-2V < V_{offSC} - V_{refSC} < 2.044V \qquad (23)$$

ﬀ ﬀ ȷ b ﬅ ȷ ȷ ﬀ ȷ i ﬀ ﬀ ȷ b ﬀ ȷ b ᵇ ﬀ ﬅﬀ ﬀﬀ ﬀb ȷ ﬀ ﬀ ȷ b ﬀﬀ ﬀ ﬀ ᵇ $V_{off\ eq\ in}$ ⁸ â Ù Ù

$$at\ Low\ Gain:$$

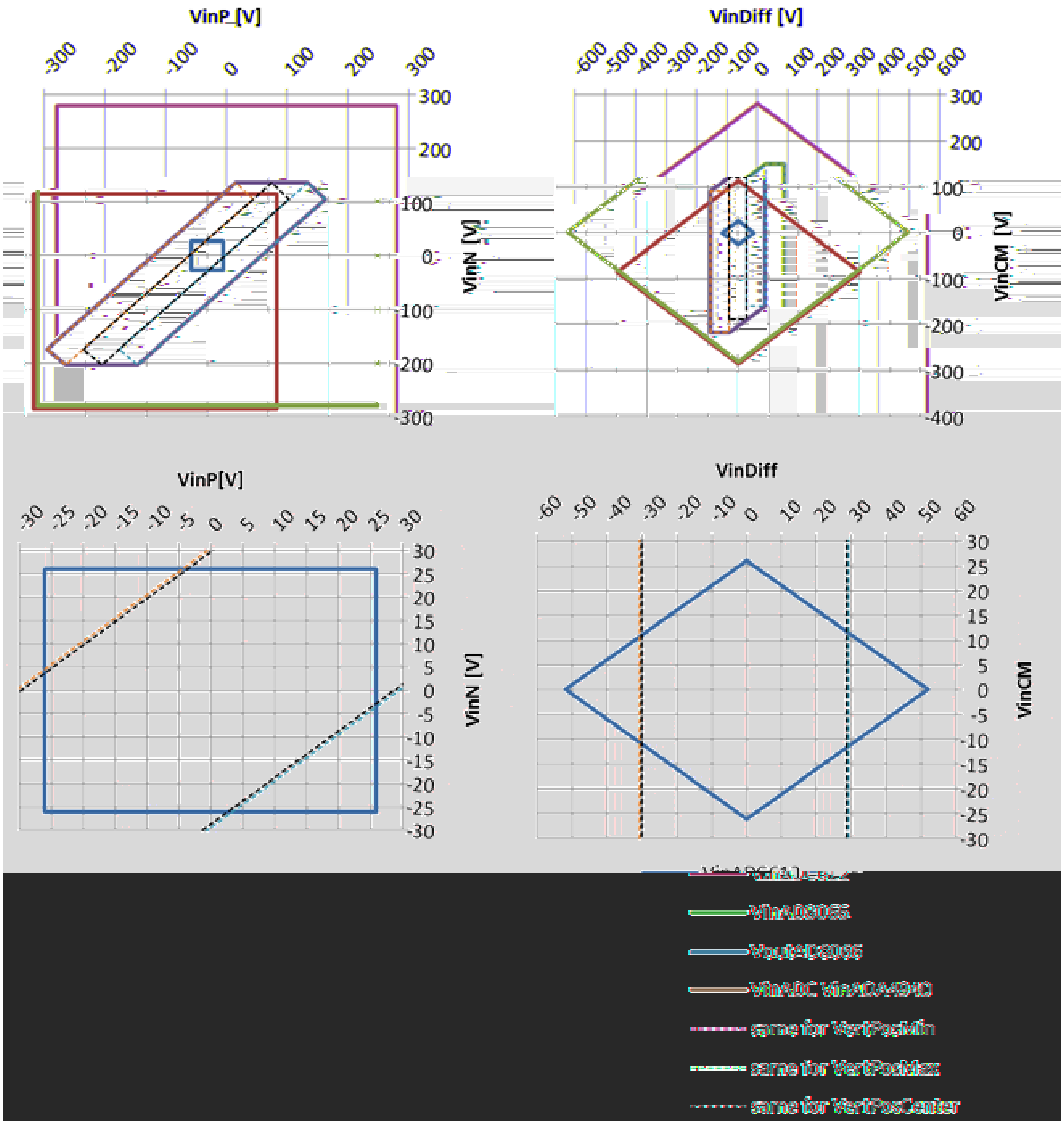


Figure 11. Scope input signal range.

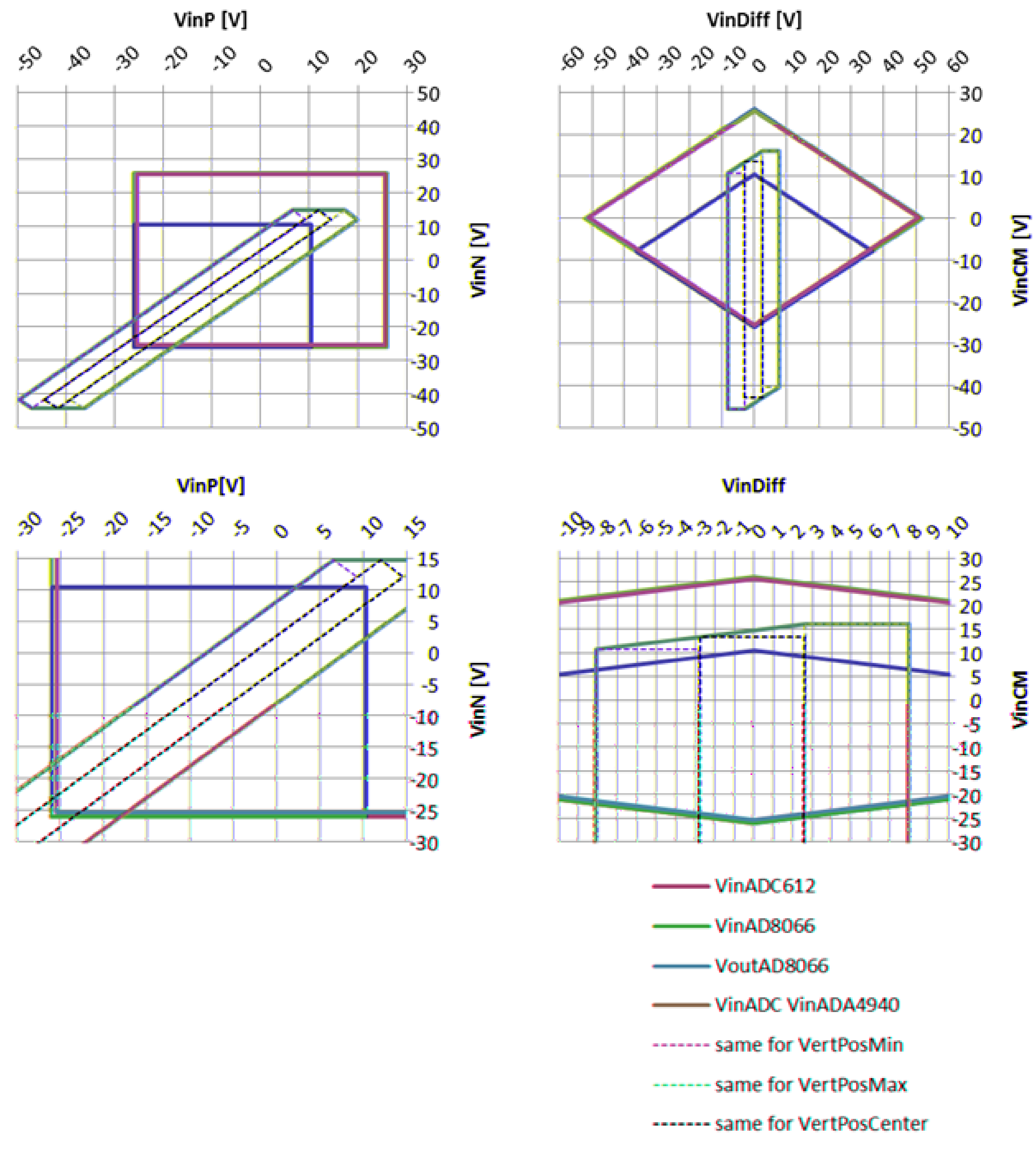


Figure 12. Scope input signal range.

ff b ff ff b i ff ffﬆ ff ff ff ȷ ﬆb b ffb ff ﬆff ffff ff ff b ff ffff b ff ff b i ff ȷ ffb ȷbi b ff ȷ ff ff ff ﬆ ff ff ȷ b ﬆ ȷ ȷ ff *VoffSc = 2.022V* ȷ ff b ȷ **(11)** ff ff ff ff ȷ ﬆb b ffb ff ff ȷ b ﬆ ȷ ȷ ȷ ff b ȷ *VoffSc = 4.044V* b ff ȷi ff ff ﬆ ff ȷ ȷ ffi b ȷ ff ff ȷ b ﬆ ȷ ȷ *VoffSc = 0V* B ȷ ff ff ȷb ff ff ȷ b ﬆ ȷ ȷ ȷ ﬆ ȷ ff ȷ i ff ȷ ﬆb b ff b ffb ȷ b b ff ff b i ff b ȷ ff ff ȷb ff ﬆ ȷ ȷ B ȷi b ȷ i ff i ȷ ff ff b ff ff b i ff ff ffff ff ȷ ﬆb b ff ȷ ﬆ bi ff b i ff b ȷ i ff B b b ff ffȷ ff b ff b b ff ȷ ȷ ffﬆ ff ff ff ff ﬆff ffff ȷ b ff ȷ ff b ȷ i ff ff

B ȷi b ffffﬆȷ i ȷ ȷ ff b ff ff b i ff ȷ i b ȷ ȷ ff ff ȷ ff ff ff ȷ b ȷ ȷ ȷ ff ff ȷb ff ȷ ȷ ȷ ff ȷi b ﬆb ffff ff ffi ff ff ȷi ff ȷ ff ȷ ȷ ȷ i ff ȷi b ȷ b b ȷ i ff

[illegible]

[illegible] V_{inP}, V_{inN} [illegible] **( )**

[illegible] **(7)** [illegible] **( )** [illegible]

$$-26\boldsymbol{V} < V_{\boldsymbol{inP}}, \boldsymbol{V_{inN}} < 10\boldsymbol{V}$$

(25)

[illegible]

$$-\boldsymbol{7.5V} < V_{\boldsymbol{inDiff}} < 7.5\boldsymbol{V}$$

(26)

[illegible]

[illegible]

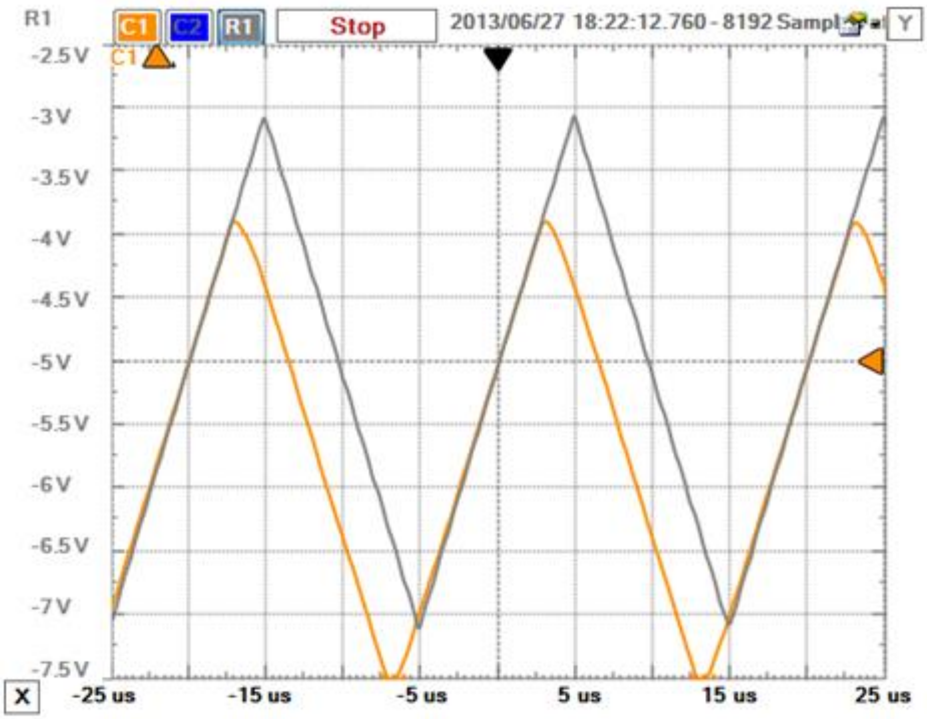


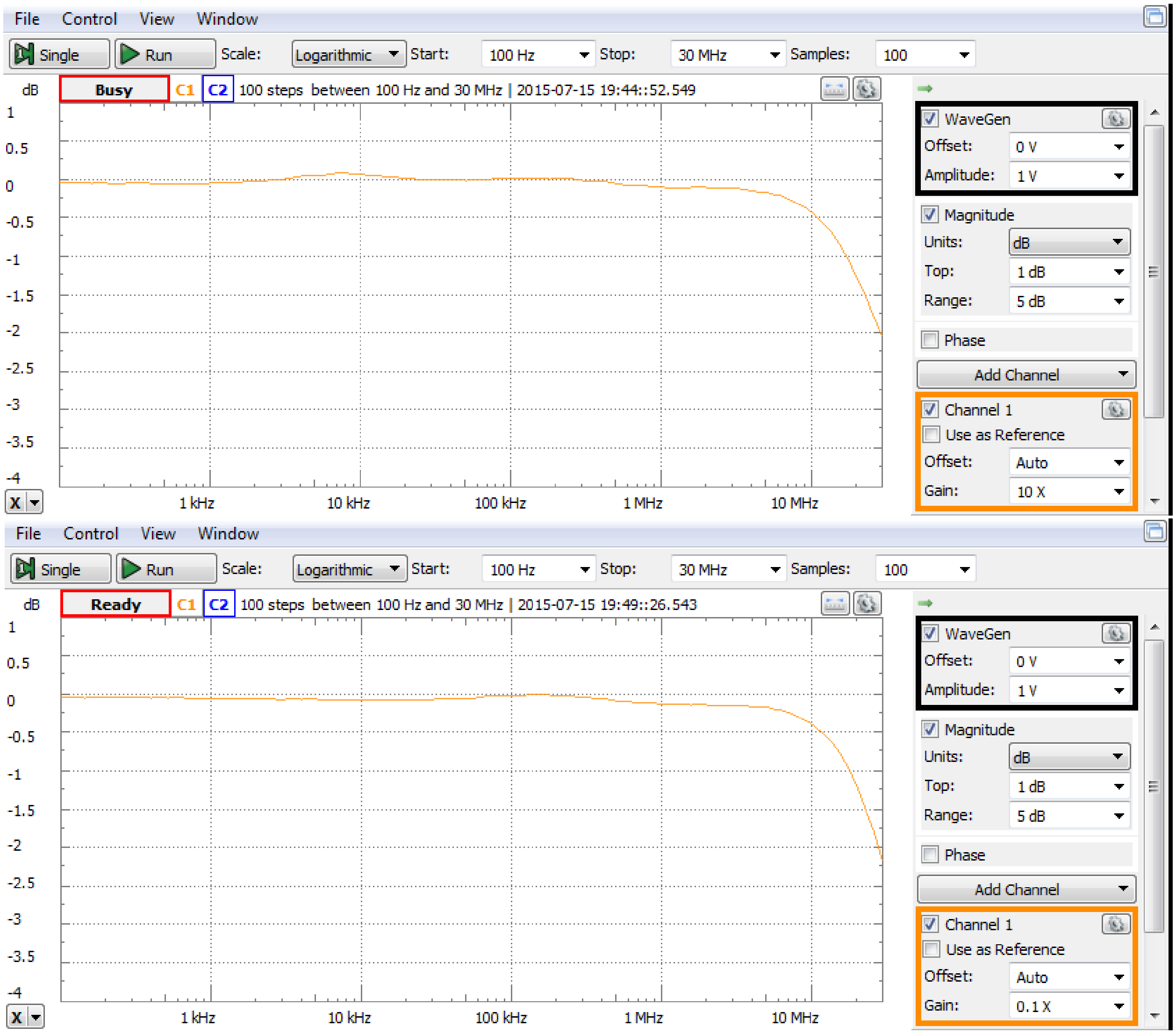
Figure 13. Common mode input voltage limitation.

2.8 Scope Spectral Characteristics

ﬁ ﬀ b ᵇﬆŋ b ﬆﬀ b b b ﬀȷ ȷ ﬀ ﬆﬀ B Bi ȷ ﬀ B ᵍ ȷ B ȷ b ᵇ b ﬀ ﬀ ﬀ b b ﬀ i ﬀ ﬀ b ﬀ ﬀ ȷ ﬆ ﬁ b ﬀ ﬁ b ﬀﬆ ᵍ ᵍ B bᵃ b ﬀ b b ﬁ ȷ ﬀ ȷ ﬀ ᵇ b bﬆ ﬀ ﬀ ﬀ ﬀ ﬀ ﬀ ȷ ﬆ ﬁ b ﬀ ȷ ﬀ ᵇ ȷ ﬆ

ﬀ ﬀ B b ᵇ ᵍ ﬀ b ﬀ ﬀ b ﬀ ﬀ b ﬀ ᵃ ﬀ b ﬀ b ȷ b ﬀ b ᵃ ﬁ i b ȷ ﬀ ﬆﬆﬀ ﬁ ﬀ b ᵃ i b ȷ ﬀ ﬀ ﬀ b ﬀ ﬀ b ȷ ȷ ᵍ ﬀ b ȷ ȷ ᵍ b ﬀ b ȷ ȷ ᵍ

ﬀ b b b ȷ ﬀ ȷ ȷ ȷ ȷ ﬀ ȷ ﬀ ȷ ﬀ ﬀ ᵇ B ﬀ ﬀ ᵇ ﬀ ﬆﬀ b ﬀ b ﬀ ﬀ ﬆﬀ b ﬆ ﬀ ᵇ b ȷ i b ﬀ bᵇ ﬁ b ﬀb ȷ i ȷ ﬀ ﬀ b ȷ ȷ b ﬆﬀ ȷ ȷ ﬀ b ﬀ ȷ ﬀ ﬀ ﬀ ﬀ ȷ ﬀ ﬀ ﬆﬀ ﬆﬀ b ﬆﬀ b ﬀ ﬀB b i ȷ ﬀ ᵇ ﬀᵃ ȷ ȷ ᵍ ﬀb ȷ i b b ᵍ ȷ ȷ b ﬁ b ȷ ȷ b b ﬀ ﬀ b bᵃ ᵍ ﬀb b b ᵍ ȷ ȷ b ﬁ b ȷ ȷ b b ﬀ ﬀ b bᵃ


File Control View Window

Single · Run · Scale: Logarithmic · Start: 100 Hz · Stop: 30 MHz · Samples: 100

Busy · C1 · C2 · 100 steps between 100 Hz and 30 MHz | 2015-07-15 19:44::52.549

WaveGen: ☑ · Offset: 0 V · Amplitude: 1 V

☑ Magnitude · Units: dB · Top: 1 dB · Range: 5 dB

☐ Phase

☑ Channel 1 · ☐ Use as Reference · Offset: Auto · Gain: 10 X

File Control View Window

Single · Run · Scale: Logarithmic · Start: 100 Hz · Stop: 30 MHz · Samples: 100

Ready · C1 · C2 · 100 steps between 100 Hz and 30 MHz | 2015-07-15 19:49::26.543

WaveGen: ☑ · Offset: 0 V · Amplitude: 1 V

☑ Magnitude · Units: dB · Top: 1 dB · Range: 5 dB

☐ Phase

☑ Channel 1 · ☐ Use as Reference · Offset: Auto · Gain: 0.1 X

Figure 14. Scope spectral characteristic diagram

- Low Gain (up)
- High Gain (down)

[illegible]

3 Arbitrary Waveform Generator

3.1 AWG DAC

[illegible]

- [illegible]
- [illegible]
- [illegible]
- [illegible]
- [illegible]
- [illegible]
- [illegible]
- [illegible]

[illegible]

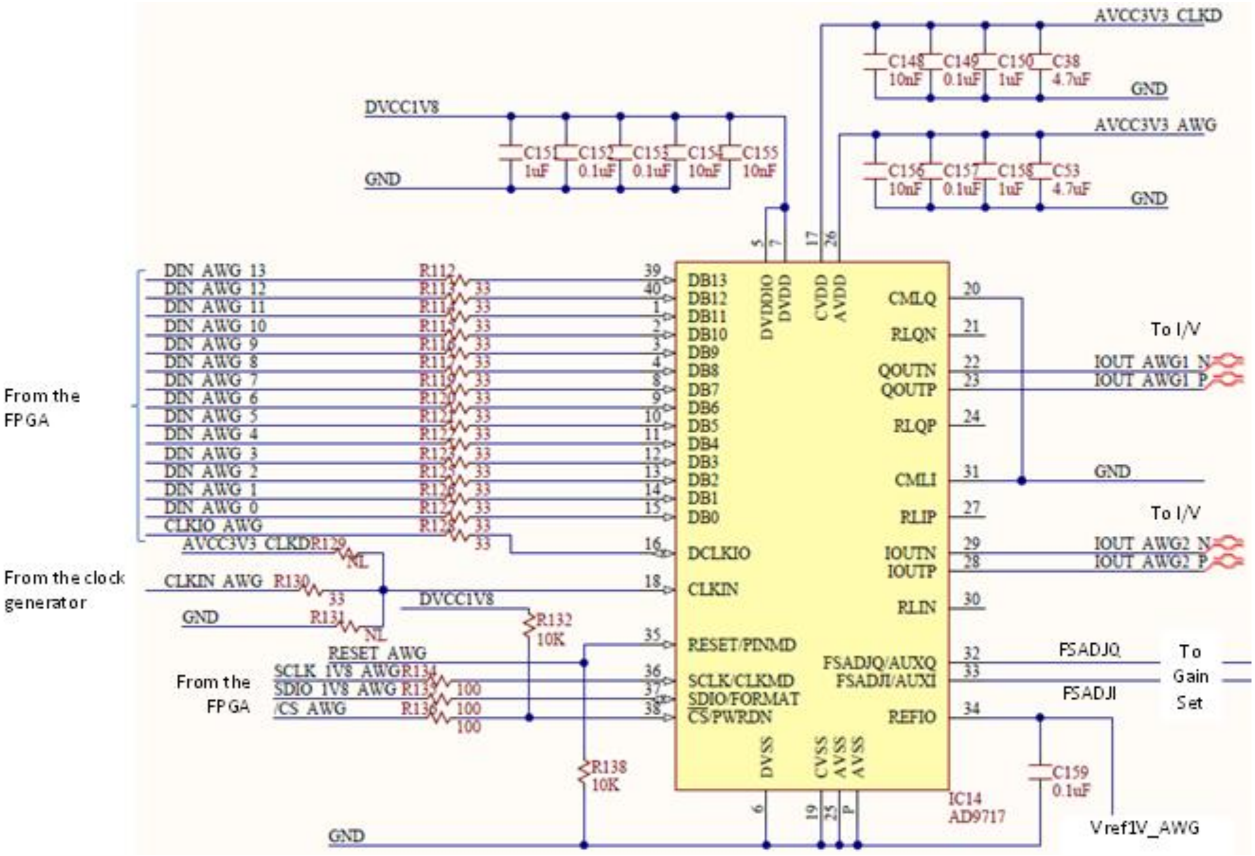

AVCC3V3_CLKD
C148 10nF
C149 0.1uF
C150 1uF
C38 4.7uF
GND
DVCC1V8
C151 1uF
C152 0.1uF
C153 0.1uF
C154 10nF
C155 10nF
GND
AVCC3V3_AWG
C156 10nF
C157 0.1uF
C158 1uF
C53 4.7uF
GND
From the FPGA
DIN_AWG_13
DIN_AWG_12
DIN_AWG_11
DIN_AWG_10
DIN_AWG_9
DIN_AWG_8
DIN_AWG_7
DIN_AWG_6
DIN_AWG_5
DIN_AWG_4
DIN_AWG_3
DIN_AWG_2
DIN_AWG_1
DIN_AWG_0
CLKIO_AWG
AVCC3V3_CLKD R129 NL
From the clock generator
CLKIN_AWG R130 33
GND R131 NL
DVCC1V8
R132 10K
RESET_AWG
From the FPGA
SCLK_1V8_AWG R134
SDIO_1V8_AWG R135 100
/CS_AWG R136 100
R138 10K
GND
DB13 DB12 DB11 DB10 DB9 DB8 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0
DCLKIO
CLKIN
RESET/PINMD
SCLK/CLKMD
SDIO/FORMAT
CS/PWRDN
DVDDIO DVDD CVDD AVDD
DVSS CVSS AVSS AVSS
CMLQ
RLQN
QOUTN
QOUTP
RLQP
CMLI
RLIP
IOUTN
IOUTP
RLIN
FSADJQ/AUXQ
FSADJI/AUXI
REFIO
IC14 AD9717
To I/V
IOUT_AWG1_N
IOUT_AWG1_P
GND
To I/V
IOUT_AWG2_N
IOUT_AWG2_P
FSADJQ
FSADJI
To Gain Set
C159 0.1uF
Vref1V_AWG

Figure 15. DAC.

ffB ffb ff

- b ȷ ᵍ
- ȷ i ff ﬆﬆᵇ ﬆff b ȷ
- O ff ȷ b ff ᵇ ﬆ b

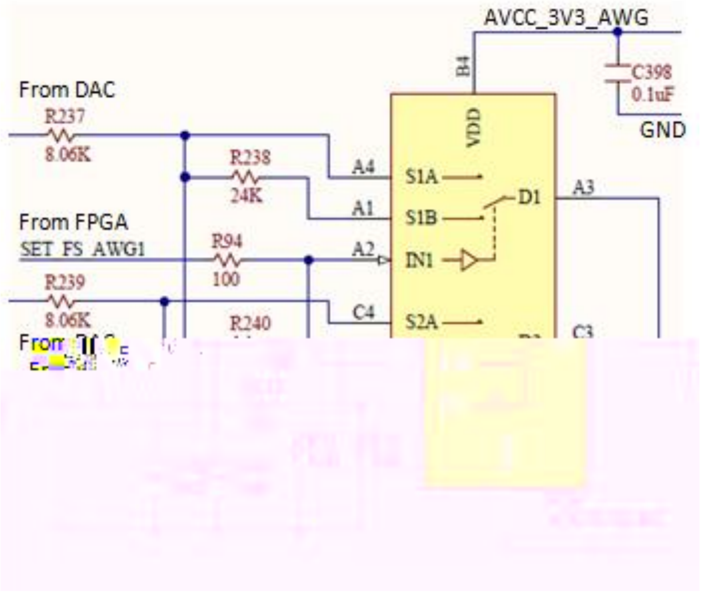

AVCC_3V3_AWG
B4
C398 0.1uF
GND
VDD
From DAC
R237 8.06K
R238 24K
A4
S1A
A1
S1B
D1
A3
From FPGA
SET_FS_AWG1
R94 100
A2
IN1
R239 8.06K
R240
C4
S2A
C3

Figure 16. DAC - gain set.

3.2 AWG Reference and Offset

B ȷ ȷi ff ff ff ff ff ff bi ff ffB ȷ i ff ff b ff ᵇ K B B B ȷ ȷ ff ff ȷ ȷ
ﬆ ȷ ff ff B

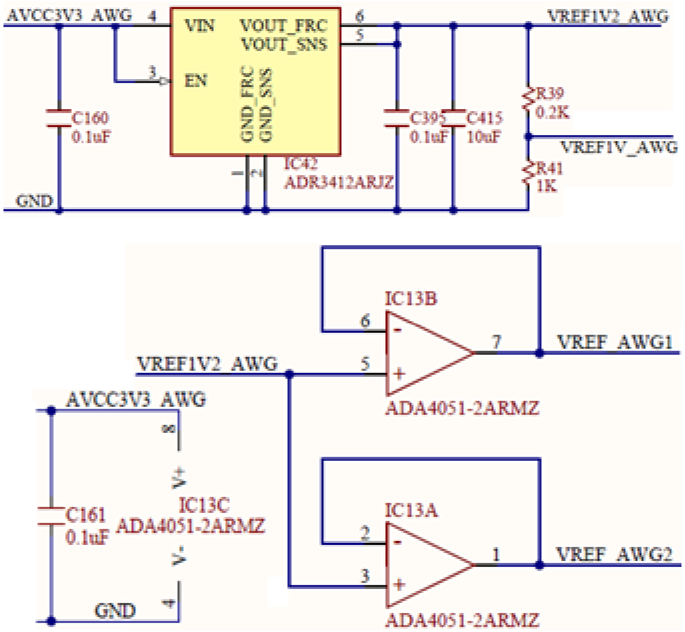

AVCC3V3_AWG
4
VIN
VOUT_FRC
VOUT_SNS
6
5
VREF1V2_AWG
3
EN
GND_FRC
GND_SNS
C160
0.1uF
C395
0.1uF
C415
10uF
R39
0.2K
VREF1V_AWG
R41
1K
IC42
ADR3412ARJZ
GND
IC13B
6
7
VREF_AWG1
VREF1V2_AWG
5
ADA4051-2ARMZ
AVCC3V3_AWG
8
V+
C161
0.1uF
IC13C
ADA4051-2ARMZ
V-
4
GND
IC13A
2
1
VREF_AWG2
3
ADA4051-2ARMZ

Figure 17. DAC - Reference voltages.

$$V_{ref1V\_AWG} = V_{ref1V2\_AWG} \cdot \frac{\mathbf{R_{41}}}{\mathbf{R_{39}} + \mathbf{R_{41}}} = 1V \tag{27}$$

ff ff ff ȷ b ffﬆ ȷ ff ffK bi ff b ȷ ȷ ȷ b ᵇ ffib B b ff ȷ ȷ ȷᵍff b

ff b ff B ﬆ ff ȷ

$$I_{outAWGFS} = 32 \cdot \frac{V_{ref1V\_AWG}}{\mathbf{R}_{set}} \tag{28}$$

ȷi bȷ

$$I_{outAWGFS\_HG} = 32 \cdot \frac{1V}{8\mathrm{k}\Omega} = 4mA \tag{29}$$

O bȷ

$$I_{outAWGFS\_HG} = 32 \cdot \frac{1V}{32\mathrm{k}\Omega} = 1mA \tag{30}$$

B B b ȷ b B i ff ff b ff ff ff bi ff b b ﬅ ff ffB ﬅ ĳ b ĳ ff ff b ff ȷ ȷ b i ff ff b ff b ff ff ff ff ﬅﬅȷff bi ff

- O ﬅ ff b ff b ȷ b B
- ﬅ ff ﬅﬅb
- ȷ b ff ĳ
- T ff ff ff ff b ff ȷ b ff ȷ ﬅ b b ȷ i ffB ȷ ﬅ ff

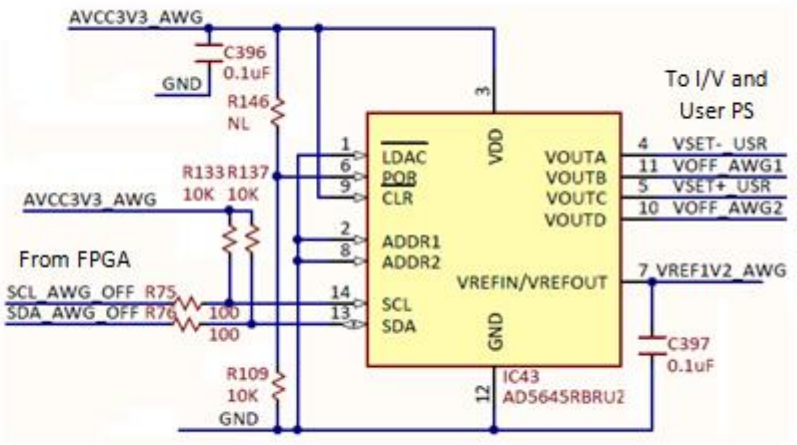

AVCC3V3_AWG
C396
0.1uF
GND
R146
NL
3
VDD
To I/V and
User PS
1
6
9
LDAC
POR
CLR
VOUTA
VOUTB
VOUTC
VOUTD
4 VSET-_USR
11 VOFF_AWG1
5 VSET+_USR
10 VOFF_AWG2
R133 R137
10K 10K
AVCC3V3_AWG
2
8
ADDR1
ADDR2
From FPGA
7 VREF1V2_AWG
VREFIN/VREFOUT
SCL_AWG_OFF R75
SDA_AWG_OFF R76
100
100
14
13
SCL
SDA
GND
C397
0.1uF
R109
10K
GND
12
IC43
AD5645RBRU2

Figure 18. DAC - Offset voltages.

ff b ff bi ff K ȷ

$$V_{offAWGFS} = V_{SET\_USRFS} = V_{ref1V2AWG} = 1.2V \quad (31)$$

4.3 AWG I/V

IC 15 in

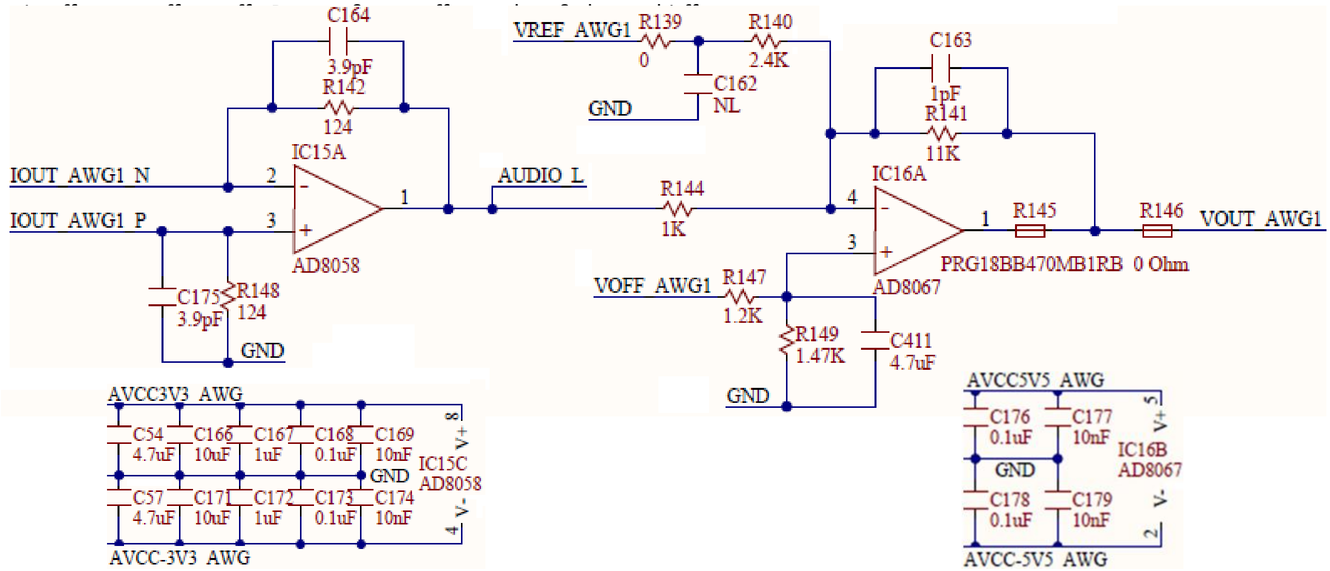

C164
3.9pF
R142
124
IC15A
IOUT_AWG1_N
IOUT_AWG1_P
2
3
1
AD8058
C175
3.9pF
R148
124
GND
AUDIO_L
VREF_AWG1
R139
0
R140
2.4K
C162
NL
GND
R144
1K
C163
1pF
R141
11K
IC16A
4
3
1
AD8067
R145
PRG18BB470MB1RB
R146
0 Ohm
VOUT_AWG1
VOFF_AWG1
R147
1.2K
R149
1.47K
C411
4.7uF
GND
AVCC3V3_AWG
C54 4.7uF
C166 10uF
C167 1uF
C168 0.1uF
C169 10nF
C57 4.7uF
C171 10uF
C172 1uF
C173 0.1uF
C174 10nF
GND
IC15C
AD8058
8 V+
4 V-
AVCC-3V3_AWG
AVCC5V5_AWG
C176 0.1uF
C177 10nF
GND
C178 0.1uF
C179 10nF
IC16B
AD8067
5 V+
2 V-
AVCC-5V5_AWG

Figure 19. AWG I/V and out.

K ﬅ b B ﬃb ﬀ

- O
- ᵍ b ȷ
- ﬀ b ﬀ
- bȷ b ﬀ ᵍ
- O ȷ ﬀ ᵍ
- O ﬅ ﬀ B b ﬅȷ ȷﬀ ᵇ ﬅ b
- O ȷ ȷ ᵍ O
- ȷ ﬀ ﬅﬅᵇ b i ﬀ
- b ﬅb bi ȷ i

$$V_{Audio} = I_{outAWGP} \cdot R_{148} - I_{outAWGN} \cdot R_{142} = \\ = (1 - 2 \cdot \{A_U\}) \cdot I_{outAWGFS} \cdot R_{142} = \{A_B\} \cdot I_{outAWGFS} \cdot R_{142} \tag{32}$$

ﬀ ﬀ

$$\{A_U\} = \frac{D}{2^N} \in [0 \ldots 1); \ -normalized\ unipolar\ DAC\ input\ number \\ \{A_B\} = (1 - 2 \cdot \{A_U\}) \in [-1 \ldots 1); \ -normalized\ bipolar\ DAC\ input\ number\ (binary\ offset) \\ D \in [0 \ldots 2^{14}) = [0 \ldots 2^{14} - 1]; \ -integer\ unipolar\ DAC\ input\ number \tag{33}$$

ﬀ bi ﬀ b i ﬀﬀᵃ ﬀ ﬀ ﬀﬀ

$$-V_{AudioFS} \le V_{Audio} < -V_{AudioFS} \tag{34}$$

ﬀ ﬀ ȷi bȷ ﬀ ﬅﬀ ȷ ﬀᵇ O bȷ

$$V_{AudioFS\_HG} = I_{outAWGFS\_HG} \cdot R_{142} = 496\text{mV} \\ V_{AudioFS\_LG} = I_{outAWGFS\_LG} \cdot R_{142} = 124\text{mV} \tag{35}$$

3.4 AWG Out

IC16 in

ȷi ﬀ ȷ ﬀ ﬅ bi ﬀ ﬀB B ﬃb ﬀ

- ȷ ﬅ ﬅB ȷ ﬅ ȷb ﬀ
- b ﬀ i bȷ ȷi bﬅb ȷ ȷ ﬀ O b
- ȷi ﬅﬀﬀ ᵍ
- ﬀ b ﬀ
- O ȷ ﬀ ᵍ B ᵍ
- O ﬀ bi ﬀ bᵃ
- bȷ bȷ ﬅ
- O ȷ ȷ ᵍ
- O ﬅ ﬀ B ᵇ ﬅȷ b ﬅﬅᵇ ﬀ

- O b ʂƀ biʝi

b ʝi ﬀʝ ʂƭﬀ b ﬀ ʝ ﬀʝ ﬀ ʝi b ʝ ﬀ ʝi ʝ ʂƚ K

$$\frac{1}{\mathbf{R}_{140}}+\frac{1}{\mathbf{R}_{141}}+\frac{1}{\mathbf{R}_{144}}=\frac{1}{\mathbf{R}_{147}}+\frac{1}{\mathbf{R}_{149}} \tag{36}$$

$$V_{outAWG}=-V_{Audio}\cdot\frac{\mathbf{R}_{141}}{\mathbf{R}_{144}}+\left(2\cdot V_{offAWG}-V_{ref1V2AWG}\right)\cdot\frac{\mathbf{R}_{141}}{\mathbf{R}_{140}} \tag{37}$$

ﬀ ʝ ﬀ ʝ ﬀ b ʝ **(37**

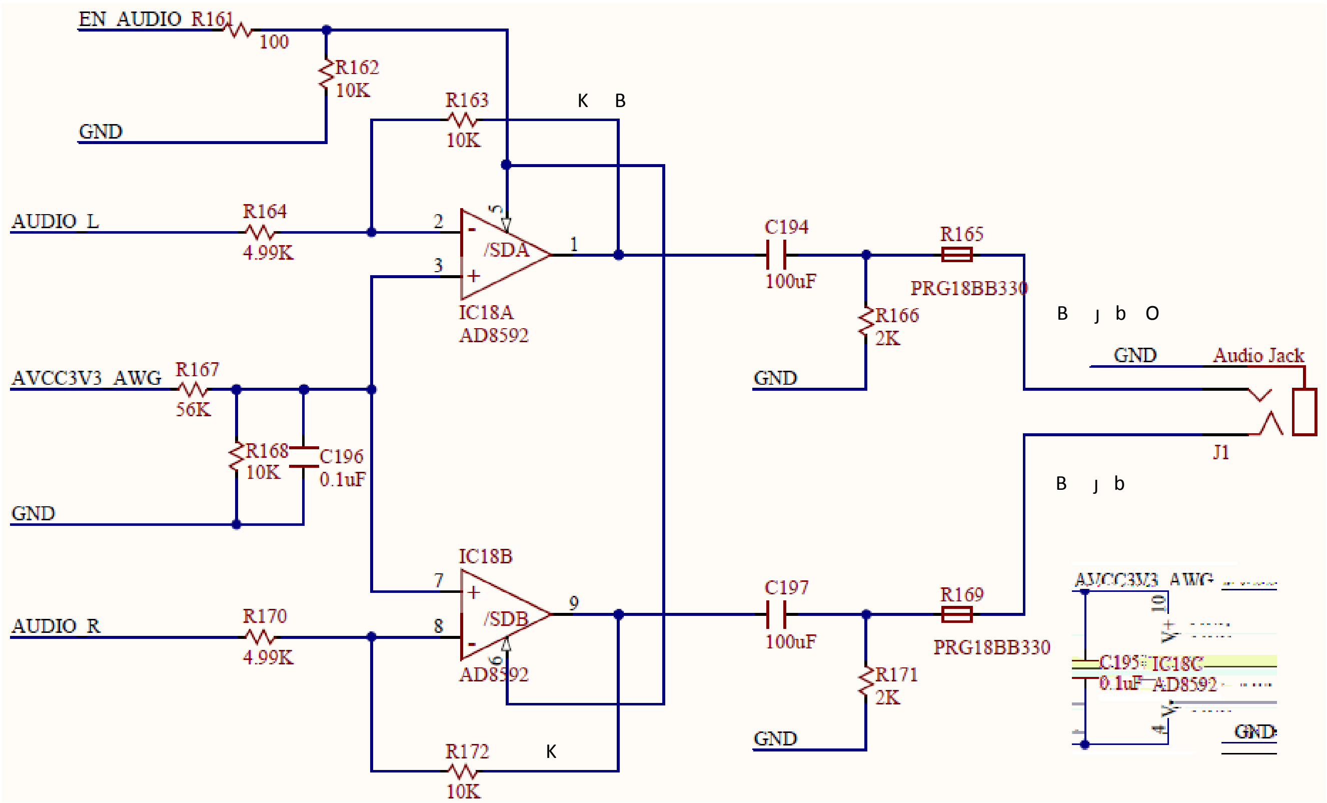
ff ȷ ff ȷ ff b ȷ **(41)** ȷ ffb ȷ ȷi b ff ff ff ȷ ff ff ﬆ ff ff ff ᵇ B ﬆȷ i

ffb ȷ ȷi b b i ffȷ

$$V_{AudioJack} = -2 \cdot V_{Audio}$$

$$-992mV < V_{AudioJack} < 992mV\ (High\ Gain)$$

$$-248mV < V_{AudioJack} < 248mV\ (Low\ Gain) \qquad (42)$$



EN_AUDIO
R161
100
R162
10K
GND
R163
10K
K B
AUDIO_L
R164
4.99K
2
3
5
/SDA
1
IC18A
AD8592
C194
100uF
R165
PRG18BB330
R166
2K
GND
B ȷ b O
GND
Audio Jack
J1
B ȷ b
AVCC3V3_AWG
R167
56K
R168
10K
C196
0.1uF
GND
IC18B
7
8
/SDB
9
6
AD8592
AUDIO_R
R170
4.99K
C197
100uF
R169
PRG18BB330
R171
2K
GND
R172
10K
K
AVCC3V3_AWG
10
V+
C195
0.1uF
IC18C
AD8592
V-
4
GND

Figure 20. Audio.

3.6 AWG Spectral Characteristics

ȷi ff ff ᵇ ﬆȷ b ﬆff b b b ff ȷ ȷ ffB K ff ȷ ffª ﬆff ȷ ff ȷ ȷ ff b bª b ffb b ȷi ȷ ff ȷ ff ᵇ b bﬆ ff ff ff ff ff ffB ȷi b ff ﬆff ȷ ﬆ ff ff ffª ﬆff ȷ ff b ff ȷ ff ffB b ff ff ff ﬆff ȷ ﬆ ȷb ffB b i ȷ ff ᵇ ȷ ff ȷ ff B b i ȷ ff ᵇ ﬆff b b ff b ȷ ff ff b ff ff ff ff ff ffª ﬆff ȷ ff b ff ff b ff ȷ b ﬆ ff ff ff ﬆff b b b ff ȷ ȷ ffB

ff ff B b ᵇ ᵍff ȷ b ȷ ff ȷ b ff ȷ ff ﬆff ᵇ ȷᵍff ȷi b ᵇ ff ȷ b b ȷ ȷ ȷ K b ff b ff B b ﬆff b ff b ﬆ ff ff ȷff b ff ff

ᵍ ᵍ ff ﬆff j ffᵇ j b ﬆj ffj ff ff b b ffj j j j j ffﬆ ff
b j j ᵍ j ff bᵃ b ffb ᵍ j ff j ff j

j jb ff ﬆff bi ff ffB ffᵃ ffff ff ff j ff ff ᵍ b j

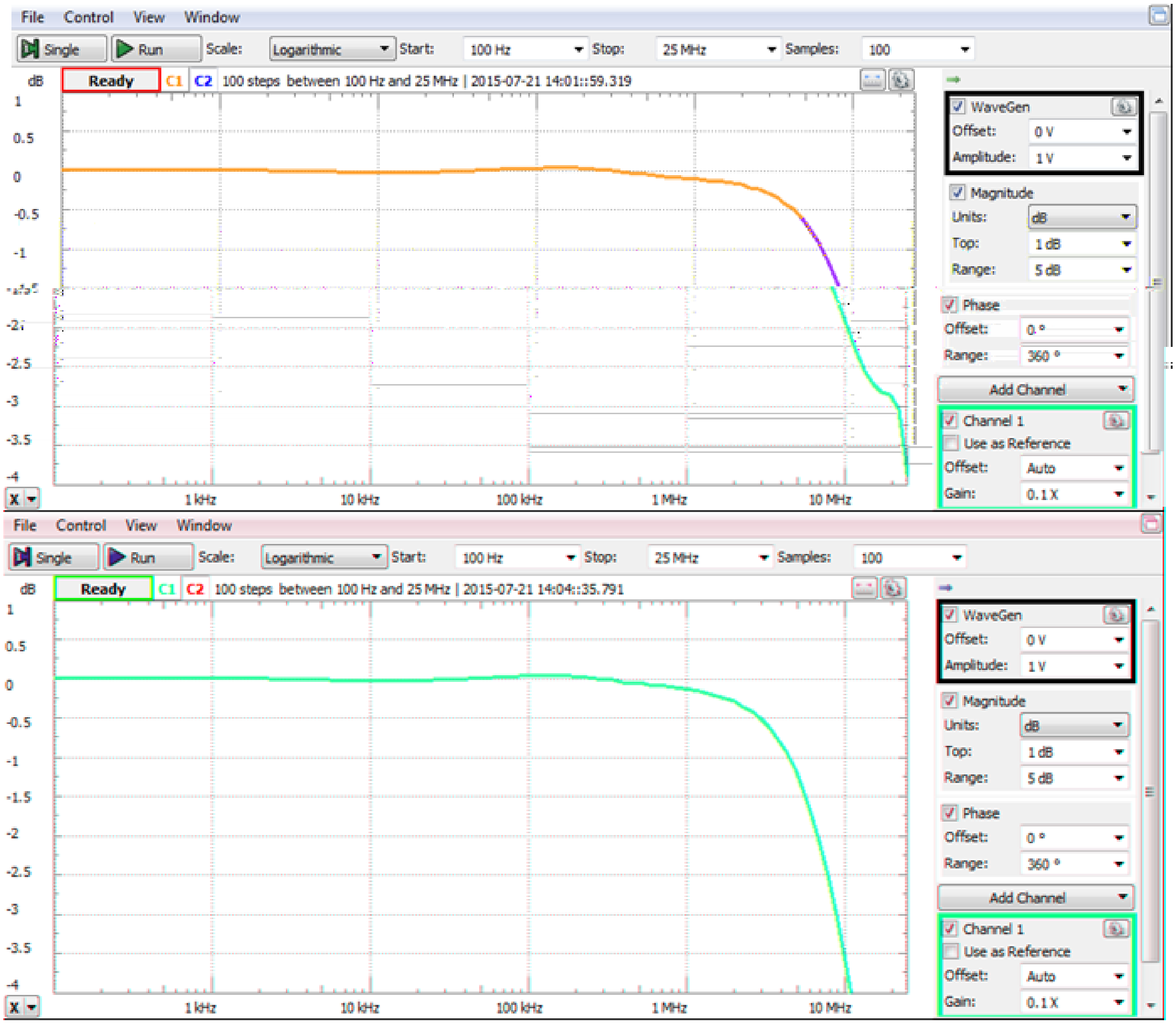

File Control View Window
Single Run Scale: Logarithmic Start: 100 Hz Stop: 25 MHz Samples: 100
dB Ready C1 C2 100 steps between 100 Hz and 25 MHz | 2015-07-21 14:01::59.319
1 0.5 0 -0.5 -1 -1.5 -2 -2.5 -3 -3.5 -4
X 1 kHz 10 kHz 100 kHz 1 MHz 10 MHz
WaveGen Offset: 0 V Amplitude: 1 V
Magnitude Units: dB Top: 1 dB Range: 5 dB
Phase Offset: 0 ° Range: 360 °
Add Channel
Channel 1 Use as Reference Offset: Auto Gain: 0.1 X
File Control View Window
Single Run Scale: Logarithmic Start: 100 Hz Stop: 25 MHz Samples: 100
dB Ready C1 C2 100 steps between 100 Hz and 25 MHz | 2015-07-21 14:04::35.791
1 0.5 0 -0.5 -1 -1.5 -2 -2.5 -3 -3.5 -4
X 1 kHz 10 kHz 100 kHz 1 MHz 10 MHz
WaveGen Offset: 0 V Amplitude: 1 V
Magnitude Units: dB Top: 1 dB Range: 5 dB
Phase Offset: 0 ° Range: 360 °
Add Channel
Channel 1 Use as Reference Offset: Auto Gain: 0.1 X

Figure 21. AWG spectral characteristic.

4 Calibration Memory

ffb b i j j ᵇ ff j ff j ﬆff j bﬆff j ff ﬆb j ffb b j ffffff j ﬆ ff ff b b ffff ﬆff ﬆb b ff ff ff j b ff bﬆb j b ff ff jb ff ff b ᵇﬆj b b ff b ff b ff ff ff b j j ﬆff j bﬆff j ff ᵇﬆj b b ff ﬆ ff ff b ff b ff B b ﬆff b ff ffB b i j ffᵇ j j jᵍff ff ffff ff ff ff ji ff

- ff j b bﬆb j j b ff j j b b b i ji b ﬆb
- bﬆb j j ff j ff b b j i ff ﬆff K ﬆ j j ff b bj ff ff j

ﬆ ji ff ﬆ ji j ff b K B ﬆb ji ᵇ b ff ff ff ff ff j ff bᵇ ff b ff b ffj ff ﬆff j ff ff

- [illegible]
- [illegible]
- [illegible]

[illegible]

[illegible]

5 Digital I/O

[illegible]

[illegible]

[illegible]

[illegible]

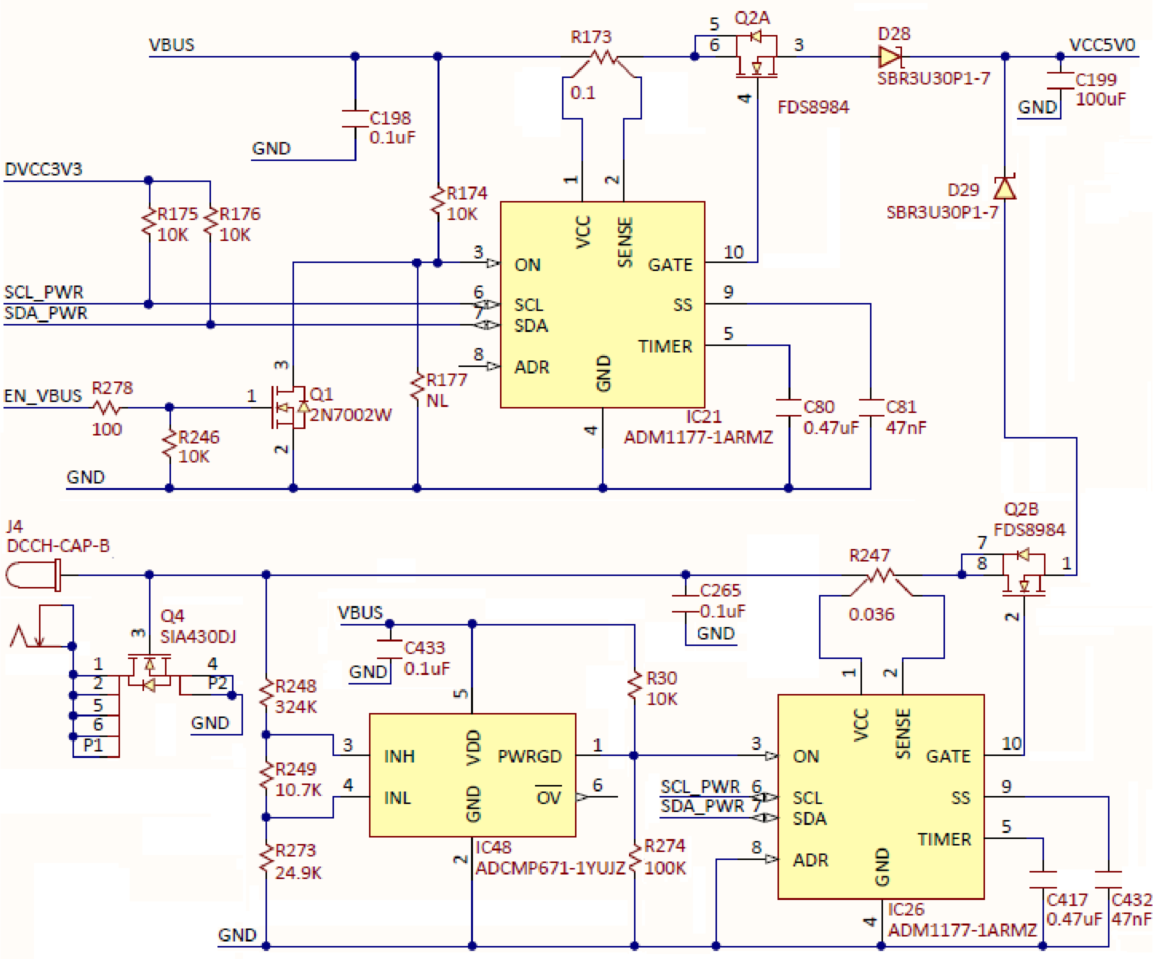

VBUS
R173
0.1
Q2A
FDS8984
D28
SBR3U30P1-7
VCC5V0
C199
100uF
GND
C198
0.1uF
DVCC3V3
R175
10K
R176
10K
R174
10K
D29
SBR3U30P1-7
VCC
SENSE
ON
GATE
SCL
SS
SDA
TIMER
ADR
GND
SCL_PWR
SDA_PWR
EN_VBUS
R278
100
Q1
2N7002W
R246
10K
R177
NL
IC21
ADM1177-1ARMZ
C80
0.47uF
C81
47nF
J4
DCCH-CAP-B
Q2B
R247
0.036
C265
0.1uF
Q4
SIA430DJ
P1
P2
C433
0.1uF
R248
324K
R249
10.7K
R273
24.9K
R30
10K
INH
INL
VDD
PWRGD
OV
IC48
ADCMP671-1YUJZ
R274
100K
IC26
ADM1177-1ARMZ
C417
0.47uF
C432
47nF

Figure 23. USB power control.

ff ffª ff b ﬅ ff ȷ ﬅ ȷ ﬅ ff ff bi bȷ ff ff ff bi ff ȷ b b ȷ i ﬅ ff ﬅﬅᵇ ȷ ffi b ȷ ff ﬅ b ȷ ᵇ ff b ﬅj ȷ ff ff ff ff ff ȷ ff ȷ ﬅ ff ff b ff ᵇ ȷ ff ᵇ ff b ff

- B b i ȷ ff ᵇ ff ff ff ﬅ b T ȷ b ff ff B
- ª ff b ﬅ ff ﬅﬅᵇ ȷ ffi b ȷ ff ﬅ b ȷ ᵇ ff b ﬅj b ȷ ffª ff ȷ ﬅj ff ff B

K ȷ b ff ff ffª ff b B ﬅb b b

B T ȷ b ȷ ﬅb b ȷ ff ȷ i ffb ff

- ȷ ȷ ȷ i ȷ ȷ ȷ ﬅ ff K
- K ȷ ȷ b ᵇ ȷ ȷ i bȷ ȷ ᵇ ﬅ ff K
- ff b
- ﬅﬅᵇ b i ff
- O ȷff ff ff B bª ȷ
- K ﬅ b i ff ȷ ff i
- K ff b ᵇ ff ff ȷ ᵇ ﬅj b
- O ȷ ﬅ ȷb ff B bª ȷ
- ﬅff bȷ ﬅ
- T ff i ȷ ȷ b ȷ ﬅ
- ff ȷi b ff ff bi ff ȷ ȷ b ȷ ﬅ

- O ŝƚ ȷff ffb ŝb bi ff

K ȷ ff T ŝƚ K ȷ i K ff ffᵃ ȷ ȷ ff b i ff

$$4.11V = 400mV \cdot \frac{R_{248} + R_{249} + R_{273}}{R_{249} + R_{273}} < V_{ext} < 400mV \cdot \frac{R_{248} + R_{249} + R_{273}}{R_{273}} = 5.76V \qquad (43)$$

ffB b i ȷ ffᵇ ffᵃ ȷ ȷ bȷ ŝƚ ff ȷ i ff **USB** b **External** ff ŝƚ b ᵇ ff **Racing OFF** **USB OFF** b **Racing** b ff ffᵃ ŝƚbȷ ff ff ff ff ĵi b ȷ ȷ b ȷ b ff ȷ ŝƚ b ff ff ff ff ff ff b ȷ

- **Racing OFF** ȷ ff ĵb ffᵇ b ff ff ff ff ff T B ȷ ŝƚ i b ff ȷ b ffᵃ ff b ŝƚ ff ŝŝƚᵇ ȷ b b ff b ȷ ff ĵi b i ff T K
- **USB OFF** ȷ ff ĵb ffᵇ b ff ff ff ff ff T B ȷ ŝƚ i b ff ȷ ffᵃ ff b ŝƚ ff ŝŝƚᵇ ȷ ȷ ȷ i b i ff T O
- **USB** b ff ŝƚ ff ȷ bȷ ff ff K K ff ffᵃ ff b ŝƚ ff ŝŝƚᵇ ȷ ffȷ ff ȷ ȷ i ff ĵi bi ff b i ff ff ŝƚ ff b bȷb ff ff ŝŝƚȷff ȷ ȷ ȷ ff
- **Racing** ff ffᵃ ff b ŝƚ ff ŝŝƚᵇ ȷ ȷ ff ĵi bi ff b i ff T K ff ff b ff ŝƚ ff T ff ff ȷ i b ȷ i ff T ff ff K b ᵃ ff b T ff ff K b ff ff ff ȷ ff bȷ ŝƚ ff b ff ff ŝŝƚᵇ b b ĵi ff bi ff b b b bᵃ ȷ bi ff ff ff ff b ȷ i ff ȷ ff ŝƚ b ᵇ ȷ ff ff ff T B ȷ ĵi ff b ȷ b ff ȷ ff b ff b ff ȷ i **Racing** ff ff ŝƚ ff b bȷb ff ff ŝŝƚȷff ȷ ȷ ȷ ff
- **External** ff ff ȷ ff ȷ ŝƚ ff ff b ffᵃ ff b ŝŝƚᵇ ĵb ff ff b K ffᵃ ȷ ȷ ff b i ff ᵇ ff b ȷ **(43)** T K b b ff b ffb ᵇ ŝŝƚff ff T ff ff K ff ff ŝŝƚȷff ff b ŝƚ ff ȷ ȷ b ff ȷ ffb ff B ffb ff ᵇ ȷ ȷ ȷ ŝŝƚȷff ff ȷ ff ff K

B T ff ff T B ȷ ŝƚ i b ff ȷ ȷ ff ŝƚ ff ȷ K ȷ ĵb ffB b i ȷ ffᵇ b ȷ **USB OFF** ff ff T O **Racing OFF** ff ff T K ff b ff b ff ȷ ĵi ff ff T B b ff ff ȷ ff ȷ **USB** **Racing** ff ffŝŝƚff ȷ i ŝƚ ff ff ff b ff ff ff ffᵃ ff b ŝŝƚᵇ bi ff ff T B ȷ ᵇ ȷ ff bi ff b ff ff ff ff ff ȷ i ff **Racing** ff T K b ff ff ff b ȷ ff K ȷ i ff T ff ff K ȷ ȷ i **External** ff

K ffᵃ ff b T ff ŝŝƚᵇ ȷ b b ff b ff b ff b ff b ff ff b ȷ ff ff ff ȷ ff ffŝƚ ffb ff ᵇ i **USB** **Racing** **External** ff ȷ i ȷ ff b ff b ff ff ffᵃ ffŝƚ ff ŝŝƚȷff i ff ff b bȷb ff ŝƚ ff

ff ff ff ȷ i ff ffᵃ ff b ŝƚ ff ŝŝƚᵇ ȷ i **External** ff ȷ ffb ff ᵇ ff ff ffffŝƚ ȷ i b ŝŝƚȷff ff ŝƚ ff T B i ff ŝƚ ff ff b ff ĵi b ȷ b b ff ff ȷ ff ŝƚ b ff ȷ ff i ȷ ȷ ffb ff **USB OFF** ff b ff ȷ ŝƚ ŝƚ ff ff ff ff ff ff ff ȷ ff ȷ ȷ ff ŝƚ i b ff T B B ff ȷ ff b ff ff ȷ ff **USB** ff

B B bŝƚ ff b ĵi ȷ b T ff ȷ ȷ b Tȷ ȷ ff ŝƚ ȷ ff ŝƚ ff ŝƚĵb ff ȷ i **USB** b **Racing** ff K ȷ ĵi ff

ff b b ffB ffb ff b ff

- b ff ȷ ff b ȷ ff ȷ b ff b

- ﬆﬆᵇ bi ﬀ
- T ﬀ ȷ ȷ ﬀ ﬀ ﬀb ﬆȷ ȷﬀ
- ȷ B ﬀ b bi ﬀ ﬀb
- B n b ﬀb b i ﬀ ȷ ȷ ȷ ȷ ȷ ﬀb ﬀ
- b b ﬀ bﬆ ﬀ ȷ ȷ ﬀ ﬀ
- b ﬀ ﬆ ﬀ ȷ ȷ ﬆﬀb b ﬀ
- B b ȷ ﬀ ᵇ b ﬀ b
- T i b b ﬀ bﬆ ȷ ȷ i ȷb K ﬆj
- b ﬆj ﬀ ﬀ ﬀ ﬀb n ﬀ b ﬆ i b ȷ i ȷ ȷ ȷb ﬀ b ﬆ b ﬀ
- K b ﬀ ﬆȷb ȷ ﬀ b ﬀ ᵍ bᵃ ȷ

ﬀ ﬀ b ﬀ ȷ **USB** **Racing** ﬀ K ȷ ȷ ﬀ ﬀ ﬀ ﬀ ﬆ

$$I_{limit} = \frac{100mV}{R_{173}} = \frac{100mV}{0.1\Omega} = 1A \qquad (44)$$

b bᵃ ȷ ȷ ﬀ

$$t_{fault} = 21.7[ms/\mu F] \cdot C_{80} = 21.7[ms/\mu F] \cdot 0.47\mu F = 10.2ms \qquad (45)$$

K ﬀ ﬀ ﬀ ﬀ b ﬀ I_{limit} ﬀ ﬀ t_{fault} K B B bﬆ ﬀ ᵇ ȷ ȷ ȷ ȷb ﬀ b ﬀ

$$t_{cool} = 550[ms/\mu F] \cdot C_{80} = 550\left[\frac{ms}{\mu F}\right] \cdot 0.47\mu F = 258.5ms \qquad (46)$$

b ȷ b ﬀ b bﬆ b ȷ ȷ ᵇ ȷ ȷ ﬀ ﬀ ﬆ

$$\frac{dI_{limit}}{dt} = \frac{10\mu A}{C_{81}} \cdot \frac{1}{10 \cdot R_{173}} = 212\frac{mA}{ms} \qquad (47)$$

K ﬀ ﬀ ﬆ ﬀ I_{limit} ﬀ ﬀ t_{fault} b ﬆﬀ b ȷ ﬃ ȷ

ȷ ȷb ᵇ K ȷ **Racing** **External** ﬀ ȷ ȷ ﬀ ﬀ ﬀ ﬀ ﬀᵃ ﬀ b ﬆ ﬀ ﬆﬆᵇ

$$I_{limit} = \frac{100mV}{R_{247}} = \frac{100mV}{0.036\Omega} = 2.78A \qquad (48)$$

t_{fault} b t_{cool} b ﬀ b ﬀb K b ﬀ ﬀ ﬆﬀ ȷ ȷ ȷ

$$\frac{dI_{limit}}{dt} = \frac{10\mu A}{C_{432}} \cdot \frac{1}{10 \cdot R_{247}} = 591\frac{mA}{ms} \qquad (49)$$

ﬀB b i ȷ ﬀ ᵇ ﬀ ﬆj b ﬀ ﬀ bi ﬀ ﬆ ﬀ ﬀ ﬀ bi ﬀ ȷ ﬀ ﬀ b ﬀ ﬆj ȷ ﬀ ȷ ﬀ ᵇ ﬀ ﬀᵃ ﬀ b ȷ ȷ ᵇ ȷ ȷ ﬀ ﬀ b ﬆ ﬀ ȷ i ﬀ ȷ ﬆ ﬆ b b ﬀ ȷ ȷ b ȷ i ﬀ b ﬀ ȷ ﬀ b ﬆ ﬀ ﬆﬆᵇ K ﬀ b ﬆ ﬀ ﬀ ﬀ ﬀ i ᵇ ȷ ȷ ﬀ b ﬀ ﬀ ﬀ ﬀ i ᵇ ﬀ ȷ ȷ ﬀ ȷ b ﬆ ﬀ ﬆﬆᵇ ﬀ ﬀ ﬀ ȷ ﬀ ﬀ ﬀb ﬀ ȷ ﬀ ȷ ﬀ ﬆ ﬀ ȷ ﬀ ȷ ﬀ ﬆ ﬀ b ȷ ff b ᵇ ff b ﬅ ff ȷ i ff ff i ᵇ b ȷ ff ff bȷ ȷ i ff bi ff b ff ff ȷ b b ff ȷ ȷ ff ﬅ ff ff T ﬅ bi bȷ b ȷ b ȷ

6.2 Analog Supply Control

ȷ i **USB** ff ff T B b ᵇ ffb K ff ff b ff i ﬅ ȷ b ᵇ ȷ ﬅb ᵇ ff bȷ ȷ ȷ ff ᵇ b B b ȷ i ȷ i ff ff b ff ff ffª ffff ȷ i B b ff ff K b b ff B ȷ ffb ff b ff ff ﬅ ff ȷ ȷ ff b ff bȷ ȷ ff ȷ ff ff ȷ i ff ff ﬅ ff ȷ b ff K B T ȷ ȷ ff b K ȷ ff ȷ b ȷ i ff b b i b ff ﬅ ff ﬅﬅ ȷ ff

B T bȷ ffb ff

- O
- O ȷ ﬅ bi ff b i ff
- i ȷ ﬅb ȷ ff ff b ff i ȷ
- ff ff ﬅff b ff ﬅ ff ȷ
- b b b ﬅȷ O T

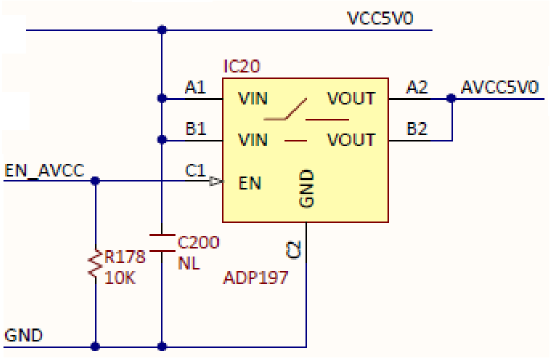


Figure 1. Analog supply control.

6.3 User Supply Control

K ȷ ȷ ff ff ﬅ ff b bȷ b ff ff ff ﬅﬅ ȷ ff B b ff ff ff ȷ bȷ ffb ff

- ﬅﬅ ᵇ bi ff
- b ff ȷ ff bi ff ﬅ ff ff ff ﬅﬅ ᵇ ﬅ ff ȷ
- b ff ȷ ff T b ff
- K ff ȷ ȷ ȷ i
- B n b ff ff ȷ ȷ
- b ff ȷ ȷ ȷ i
- B b ȷ ff ᵇ b ff b
- T i b b ff ff ȷ ȷ ȷ ff b ff ﬅff b ȷ i b ffb B
- T ff i b b ﬅ
- B b i ff bi ff b ff bi ff ﬅ ff ȷ
- ffb ª O T ﬅb bi ff
- ffb T ﬅb bi ff

K ȷ ȷ ff ff ff ᵇ ff ﬅ ff ﬅﬅ ȷ ff i ff ff ff b ff b ff b ff T B b i ff ff ȷ ȷ ffﬅff ȷ i ff ﬅ ff ff

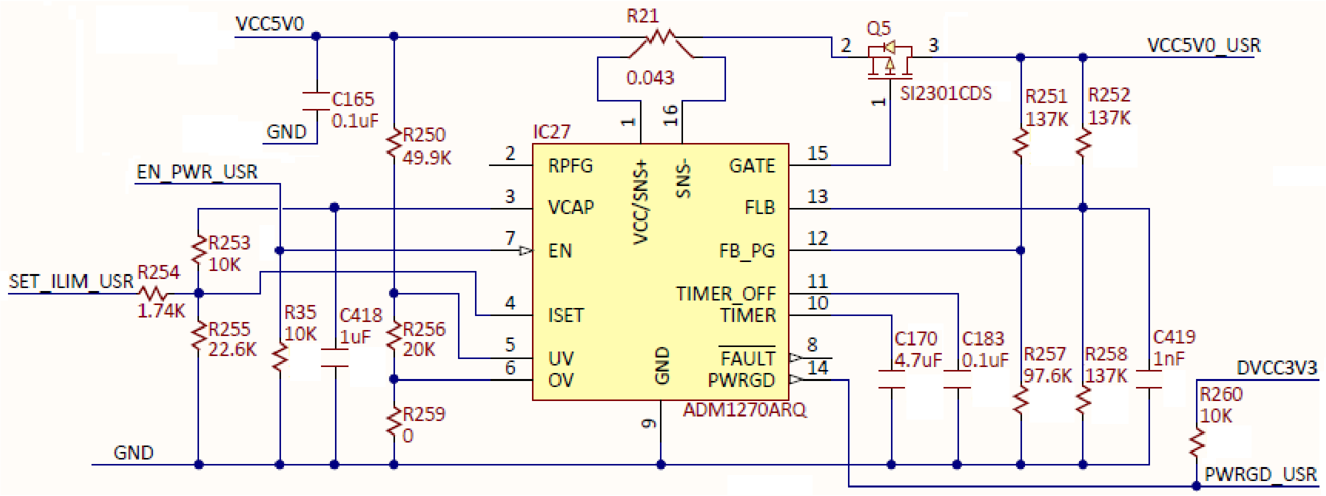
ȷ i **USB** b **Racing** ff KK ﬅȷ ȷ ȷ ff O ᵇ ff T B ff bi ff b ff K ﬅȷ K ȷ

$$V_{Iset} = \frac{\frac{V_{cap}}{R_{253}}}{\frac{1}{R_{253}} + \frac{1}{R_{254}} + \frac{1}{R_{255}}} = \frac{\frac{3.6V}{10k\Omega}}{\frac{1}{10k\Omega} + \frac{1}{1.74k\Omega} + \frac{1}{22.6k\Omega}} = 0.5V \qquad (50)$$

ﬅ ȷ ȷ ȷ ff K B ȷ ff ff ff
ff ﬅ b ﬅb ᵇ b ff ff ȷ ff bᵇ ff b ff b ffȷ ff ﬅff ȷ ff ff

ff ff j j j ff

$$I_{limit} = \frac{V_{Iset}}{40 \cdot R_{21}} = \frac{0.5V}{40 \cdot 0.043\Omega} = 290mA \qquad (51)$$



VCC5V0
R21
0.043
Q5
2
3
SI2301CDS
1
VCC5V0_USR
C165
0.1uF
GND
R250
49.9K
IC27
1
16
R251
137K
R252
137K
EN_PWR_USR
2
RPFG
3
VCAP
7
EN
4
ISET
5
UV
6
OV
VCC/SNS+
SNS-
GND
9
GATE
15
FLB
13
FB_PG
12
TIMER_OFF
11
TIMER
10
FAULT
8
PWRGD
14
ADM1270ARQ
R253
10K
SET_ILIM_USR
R254
1.74K
R255
22.6K
R35
10K
C418
1uF
R256
20K
R259
0
C170
4.7uF
C183
0.1uF
R257
97.6K
R258
137K
C419
1nF
DVCC3V3
R260
10K
PWRGD_USR
GND

Figure 25. User supplies control.

j i **External** b **OFF** ff KK ﬆj j j ff j ᵇ ff T B ff bi ffb ffK ﬆj K j

$$V_{Iset} = \frac{V_{cap} \cdot R_{255}}{R_{253} + R_{255}} = \frac{3.6V \cdot 22.6k\Omega}{10k\Omega + 22.6k\Omega} = 2.5V \qquad (52)$$

ff ff j j j ff

$$I_{limit} = \frac{V_{Iset}}{40 \cdot R_{21}} = \frac{2.5V}{40 \cdot 0.043\Omega} = 1.45A \qquad (53)$$

K b ff I_{limit} j b ff b bª j j ff

$$t_{fault} = 21.7[ms/\mu F] \cdot C_{170} = 21.7[ms/\mu F] \cdot 4.7\mu F = 102ms \qquad (54)$$

K ff ff ff ff b ff I_{limit} ff ff t_{fault} K B bﬆ ff ᵇ j j j jb ff b ff

$$t_{cool} = 550[ms/\mu F] \cdot C_{80} = 550[ms/\mu F] \cdot 4.7\mu F = 2.585s \qquad (55)$$

b j ff j b O b

K ff ff ﬆ ff I_{limit} ff ff t_{fault} b ﬆff b j ffi j

ff ff j j ff ᵇ ff b j **(51)** b **(53)** j b ff ᵇ ﬆ j j ffb ffi b j ff ff ﬆ ff ﬆﬆjff B ff j ff j i ff ff j jff ᵇ ff ff ﬆﬆᵇ bi ff b B j b bjb ff ff j ﬆﬆjff i ff ff j **USB Only** ff K **External** ff ff ff ﬆ ff j j ff j ff j ff ff bi ff ﬆﬆjff b ffª ﬆb j ff ff

6.4 User Voltage Supplies

[illegible]

- [illegible]
- [illegible]
- [illegible]
- [illegible]
- [illegible]
- [illegible]

[illegible]

[illegible]

$$V_{+IC46A} = \frac{\frac{V_{OUT+\_USR}}{R_{188}} + \frac{V_{SET+\_USR}}{R_{193}}}{\frac{1}{R_{188}} + \frac{1}{R_{193}}} = V_{-IC46A} = \frac{\frac{V_{FB}}{R_{266}}}{\frac{1}{R_{265}} + \frac{1}{R_{266}}} \qquad (56)$$

$$V_{+IC46B} = \frac{\frac{V_{OUT-\_USR}}{R_{187}} + \frac{V_{FB}}{R_{270}}}{\frac{1}{R_{187}} + \frac{1}{R_{270}}} = V_{-IC46B} = \frac{\frac{V_{SET-\_USR}}{R_{190}}}{\frac{1}{R_{72}} + \frac{1}{R_{190}}} \qquad (57)$$

[illegible]

$$\frac{1}{R_{188}} + \frac{1}{R_{193}} = \frac{1}{R_{265}} + \frac{1}{R_{266}} \qquad (58)$$

$$\frac{1}{R_{187}} + \frac{1}{R_{270}} = \frac{1}{R_{72}} + \frac{1}{R_{190}} \qquad (59)$$

[illegible]

$$V_{OUT+\_USR} = V_{FB} \cdot \frac{R_{188}}{R_{266}} - V_{SET+_{USR}} \cdot \frac{R_{188}}{R_{193}} = 5.33V - 4.87 \cdot V_{SET+\_USR} \qquad (60)$$

$$V_{OUT-\_USR} = -V_{FB} \cdot \frac{R_{187}}{R_{270}} + V_{SET-\_USR} \cdot \frac{R_{187}}{R_{190}} = -5.33V + 4.87 \cdot V_{SET-\_USR} \qquad (61)$$

[illegible]

$$V_{FB} = 1.235V\ typical \qquad (62)$$

[illegible]

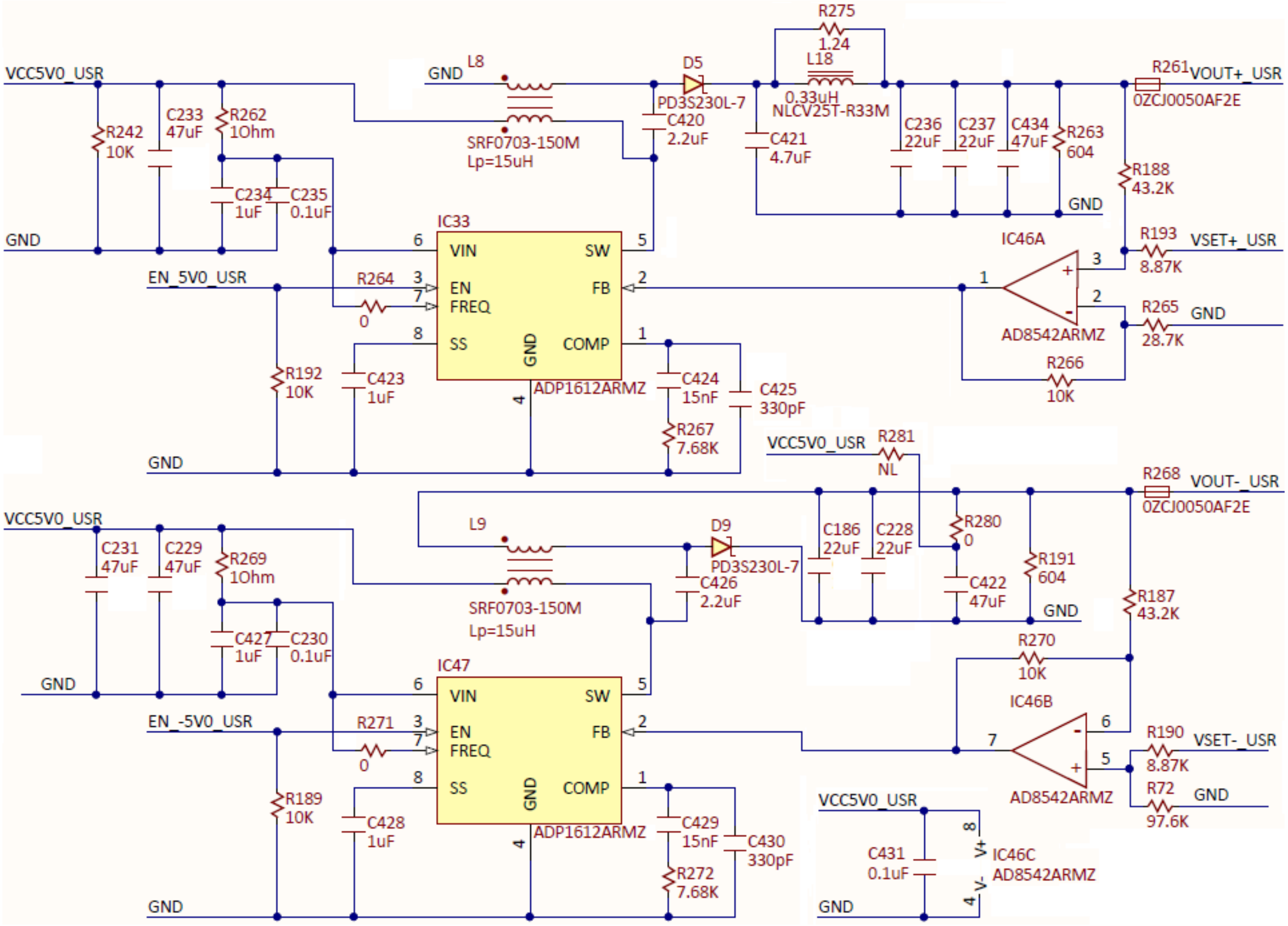
$$0 < V_{SET+\_USR}, V_{SET-\_USR} < 1.2V \qquad (63)$$

[illegible]

$$-0.51V \le V_{OUT+USR} < 5.33V \qquad (64)$$
$$0.51V \ge V_{OUT+USR} > -5.33V \qquad (65)$$

ff b i ȷ b ﬆff b ȷ i ff ﬆ ff ff b ff B ff b ȷ b ȷ ff b ff ᵇ b
ff b i ff ff ﬆff ȷ ffᵇ ff ﬆ bi ff ff b ff b ff b ff i b b ffff ȷ
ȷi b bi ff ȷi ffᵃ ȷ ȷ ȷi ȷ ȷ b ȷﬆﬆff

b ﬆﬆᵇ b ff ȷ b ff ᵇ ff T B



VCC5V0_USR
GND
L8
D5
R275
1.24
L18
0.33uH
NLCV25T-R33M
R261
VOUT+_USR
0ZCJ0050AF2E
PD3S230L-7
C420
2.2uF
C421
4.7uF
SRF0703-150M
Lp=15uH
R242
10K
C233
47uF
R262
10Ohm
C234
1uF
C235
0.1uF
C236
22uF
C237
22uF
C434
47uF
R263
604
R188
43.2K
IC33
VIN
SW
EN
FB
FREQ
SS
GND
COMP
ADP1612ARMZ
EN_5V0_USR
R264
0
R192
10K
C423
1uF
C424
15nF
C425
330pF
R267
7.68K
IC46A
AD8542ARMZ
R193
VSET+_USR
8.87K
R265
28.7K
R266
10K
R281
NL
R268
VOUT-_USR
L9
D9
C186
22uF
C228
22uF
R280
0
C422
47uF
R191
604
R187
43.2K
C231
47uF
C229
47uF
R269
10Ohm
C427
1uF
C230
0.1uF
C426
2.2uF
IC47
EN_-5V0_USR
R271
R189
10K
C428
1uF
C429
15nF
C430
330pF
R272
7.68K
R270
10K
IC46B
R190
VSET-_USR
8.87K
R72
97.6K
C431
0.1uF
IC46C
V+
V-

Figure 26. User power supplies.

6.5 Internal Power Supplies

6.5.1 Analog Supplies

B b i ﬆﬆ ȷff ffff b ff ffᵇ ȷﬆﬆff ﬆ ff ff ȷ ff ﬆ ȷ i ȷ b b i ȷi b ff ȷ ff ffb b ff
ff ȷ ff ff ff b ȷ ȷ i ȷ ȷ i ȷ ffb ffﬆb b ff ff ﬆ ff ﬆﬆ ȷff b i ff b ȷ b b i ȷ ȷ
b ȷ b

ff ȷi ff b ȷi ff b b i ﬆ ff ﬆﬆ ȷff b ff ȷ ﬆff ff ff b b B T ȷᵃ ff
ﬆ bi ff B ᵍ ffﬆ ff ff ȷ ff ﬆ bi ff ȷﬆﬆffb ff O
ȷ ff ȷ b ff b ff T ff ȷ ff ff ff

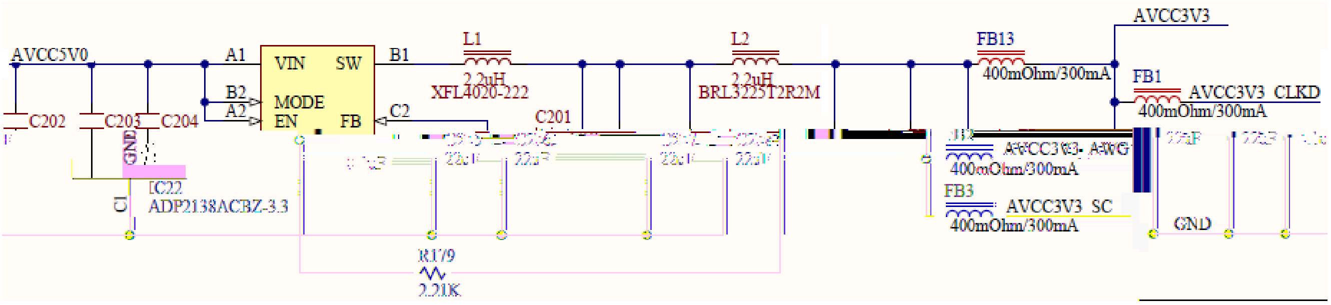

AVCC5V0
A1
VIN
SW
B1
B2
MODE
A2
EN
FB
C2
C202
C203
C204
GND
C1
IC22
ADP2138ACBZ-3.3
L1
2.2uH
XFL4020-222
C201
L2
2.2uH
BRL3225T2R2M
R179
2.21K
FB13
400mOhm/300mA
AVCC3V3
FB1
AVCC3V3_CLKD
400mOhm/300mA
AVCC3V3_AWG
400mOhm/300mA
FB3
AVCC3V3_SC
400mOhm/300mA
GND

Figure 27. 3.3V internal analog power supply.

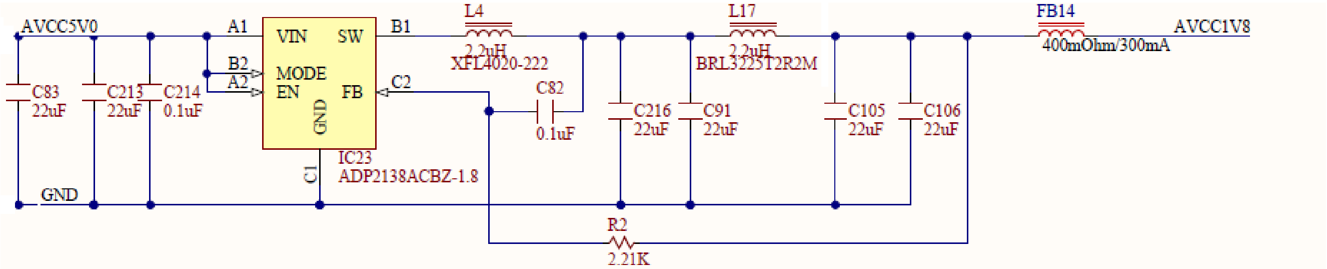

AVCC5V0
A1
VIN
SW
B1
B2
MODE
A2
EN
FB
C2
GND
C1
IC23
ADP2138ACBZ-1.8
C83
22uF
C213
22uF
C214
0.1uF
GND
L4
2.2uH
XFL4020-222
C82
0.1uF
L17
2.2uH
BRL3225T2R2M
C216
22uF
C91
22uF
C105
22uF
C106
22uF
R2
2.21K
FB14
400mOhm/300mA
AVCC1V8

Figure 28. 1.8V internal analog power supply.

- K ﬆ bi ﬀ
- Tﬀb ﬀ ȷ ȷﬀ ᵇ
- ᵍ ȷª ﬀ ﬀ ﬀ ᵇ ﬆﬀ b ȷ
- ﬀb O T ﬆb bi ﬀ
- b b b ȷ ﬀ b ȷﬀ ﬀ ﬆ ﬀ
- ᵇ ᵇ ﬀ ﬆ ﬀ
- K ﬀ b ᵇ ﬀ ȷ ȷﬀ ﬆﬀ b ȷ b b
- ﬀ ﬀ b b ﬀ b ﬆ ﬀ ȷ
- ﬀ T b b b ȷ T T ﬀ

ﬀ b b i ﬆ ﬀ ﬆﬆᵇ ȷi ﬀ ȷ ȷ ﬆﬀ ﬀ ﬀ ȷ ﬀB T ﬀﬆ ﬃ b ȷ b ȷ ﬀ ȷ i ȷi b ȷ ﬀﬀ b ﬆﬆ ȷ b ȷ ﬀB ﬀ ȷi ȷ i b K ﬀ ȷ i ȷ i ﬀB T b B T ﬀB T ﬀb ﬀ

- B bª ȷ b ﬀ
- ﬆ b b ᵇ ﬀ ﬀ ﬆﬀ b ﬀ b i ﬀ
- ᵍ ȷ ȷ i ﬀ ﬀ ᵇ
- ȷi ﬀ ȷ ȷﬀ ᵇ ﬆ
- ﬀ ﬀ b ȷ ﬀ ﬀ
- ﬆ bi ﬀ K
- B b ȷ T T ﬀ ȷ ȷ i
- K ﬃ b ﬀ ȷi ȷ ﬀ b bﬆ ȷ ﬀ
- K ﬀ b ﬆﬀ b ȷ b b
- ﬀ bi ﬀ O ﬀ ﬀ ﬆ ﬀ ȷ T b ﬀ b
- B bȷb ﬀ ȷ b b ﬀb ﬆb bi ﬀ

ff ﬅ bi ff ȷ ff ȷ b ffª ff b ff ȷ ȷ ȷ ff

$$\frac{R_{180}}{R_{181}} = \frac{-V_{out} - V_{ref}}{V_{ref}} \tag{66}$$

ȷ i $R_{181} = 10.2k\Omega$

$$R_{180} = \frac{3.3V - 0.8V}{0.8V} \cdot 10.2k\Omega = 31.87k\Omega \tag{67}$$

ff b b b ff ȷ $R_{180} = 31.6k\Omega$

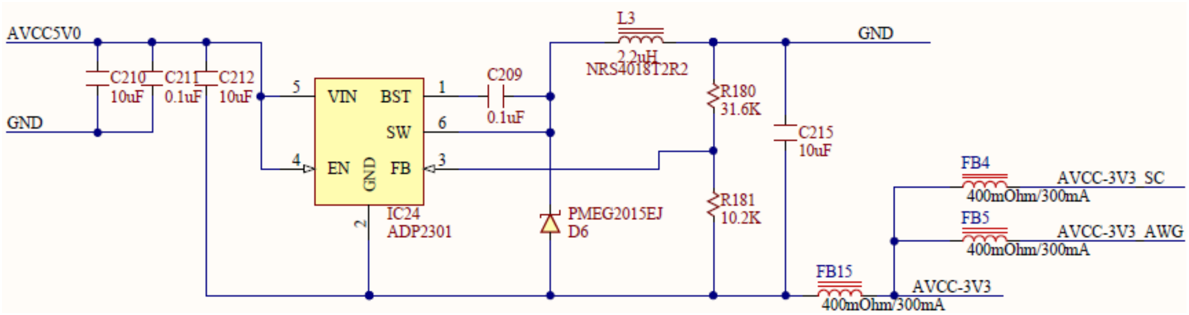

AVCC5V0
GND
C210
10uF
C211
0.1uF
C212
10uF
5
VIN
BST
SW
EN
FB
GND
4
1
6
3
2
IC24
ADP2301
C209
0.1uF
L3
2.2uH
NRS4018T2R2
GND
R180
31.6K
R181
10.2K
C215
10uF
PMEG2015EJ
D6
FB4
400mOhm/300mA
AVCC-3V3_SC
FB5
400mOhm/300mA
AVCC-3V3_AWG
FB15
400mOhm/300mA
AVCC-3V3

Figure 29. 3.3V internal analog power supply.

ff b ﬅﬅ ȷ ff ĳ ff b ff ffb ff ȷ b ffﬅ ȷ ﬅ i b ȷ b b ȷ i ff B T ffﬅ ﬅ ff ff ffﬅ ȷ b ff ff b ff ff ff ff b ff ȷ ȷ i ﬅ ȷ ff ffi b b ff ﬅ ȷ ȷ ff ffﬅ ȷ ﬅ ȷ ffi b ff ȷ ff ff ffi b ȷ ff ﬅ b ff ﬅ ȷ ȷ ff ff ȷ ȷ b b ffﬅ ff ff b ȷ ȷ ff ȷ ȷ b b ff b ff ffª ﬅff ff ﬅ ȷ ȷ ff b ffi b ȷ ff b ȷ

ff ﬅ ff ȷ b ffﬅ ȷ ȷ ȷ ȷ ff ȷ b ĳ ff ﬅ ȷﬅﬅ ff ff ȷ ȷﬅﬅ ff b b ȷ ȷ b ﬅ ȷ ff ȷ b ff ff ﬅ ȷ ȷ ff b ȷ

ff ȷ b ȷ ffff b ﬅﬅ ȷ b ȷ ff B B K ﬅ ff ﬅ i b ffb ȷ i ﬅ ȷ b ȷ b ȷ i ff K ﬅ bi ff

ff ȷ i ff ﬅ bi ff

$$\frac{R_{184}}{R_{185}} = \frac{V_{out} - V_{ref}}{V_{ref}} \tag{68}$$

ȷ i $R_{185} = 13.7k\Omega$

$$R_{184} = \frac{5.5V - 1.235V}{1.235V} \cdot 13.7k\Omega = 47.31k\Omega \tag{69}$$

ff b b b ff ȷ $R_{184} = 47.5k\Omega$

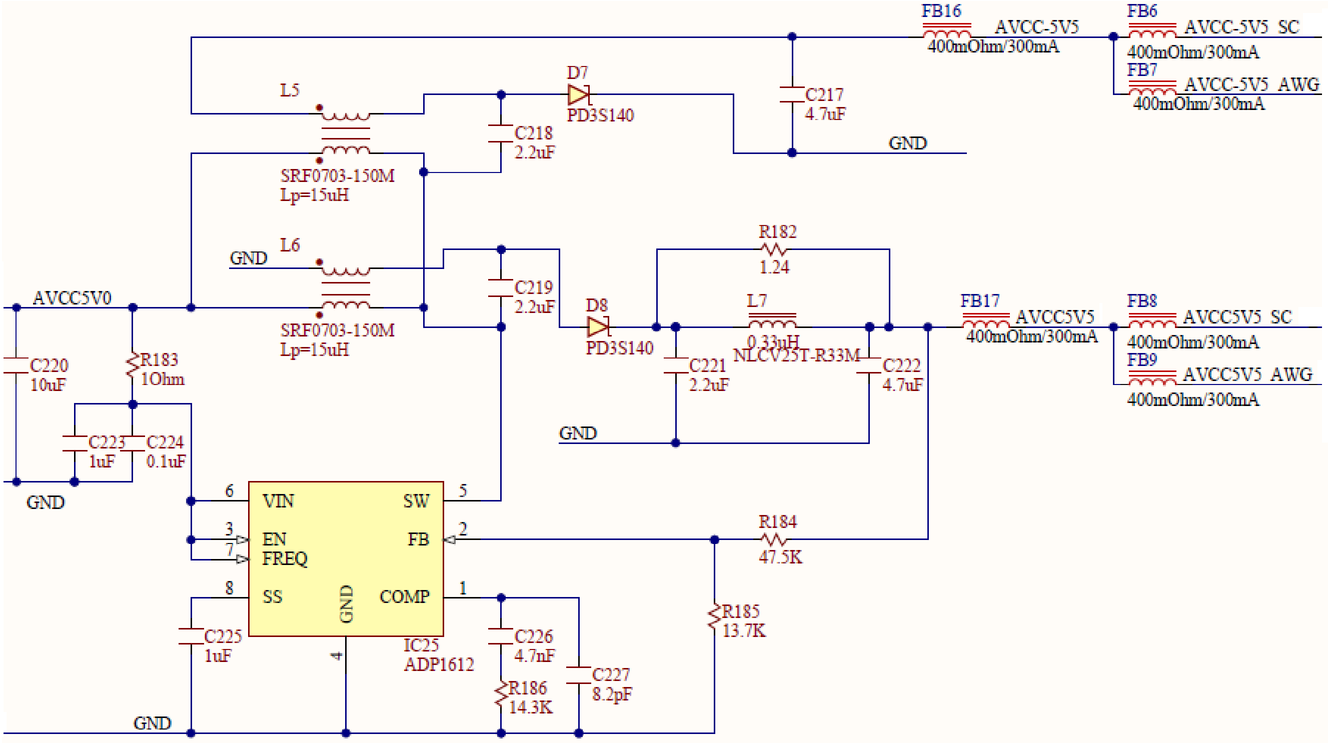

FB16
AVCC-5V5
400mOhm/300mA
FB6
AVCC-5V5_SC
400mOhm/300mA
FB7
AVCC-5V5_AWG
400mOhm/300mA
L5
D7
PD3S140
C217
4.7uF
C218
2.2uF
GND
SRF0703-150M
Lp=15uH
R182
1.24
L6
GND
C219
2.2uF
D8
PD3S140
L7
0.33uH
NLCV25T-R33M
C221
2.2uF
C222
4.7uF
FB17
AVCC5V5
400mOhm/300mA
FB8
AVCC5V5_SC
400mOhm/300mA
FB9
AVCC5V5_AWG
400mOhm/300mA
AVCC5V0
C220
10uF
R183
1Ohm
C223
1uF
C224
0.1uF
GND
VIN
SW
EN
FREQ
FB
SS
GND
COMP
IC25
ADP1612
R184
47.5K
R185
13.7K
C225
1uF
C226
4.7nF
R186
14.3K
C227
8.2pF
GND

Figure 31. ±5.5V internal analog supplies.

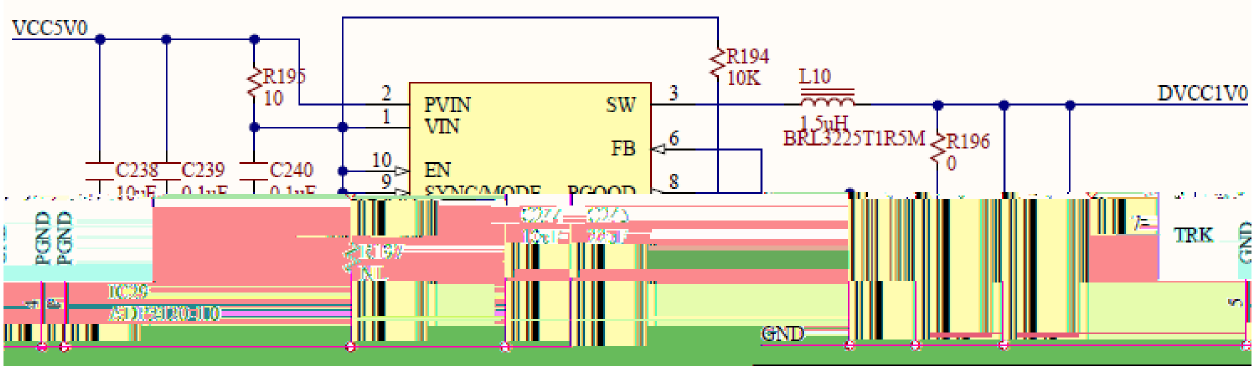

VCC5V0
R195
10
C238
10uF
C239
0.1uF
C240
0.1uF
PVIN
VIN
EN
SYNC/MODE
SW
FB
PGOOD
R194
10K
L10
1.5uH
BRL3225T1R5M
R196
0
DVCC1V0
PGND
PGND
IC29
ADP2120
TRK
GND
GND

Figure 32. 1V internal digital supply.

6.5.2 Digital Supplies

ff ji j b ﬆﬆᵇ ji ff j j ﬆff ff ff j ffB T K b b ʃᵃff ﬆ bi ff ﬆj b b ﬆ b b ᵇ j b ff j j b ff ff T B j ff b ﬆ ff ﬆﬆᵇ K b ffb ff

- B j ﬆ ff
- b j ffi b ff
- K ﬆ bi ff b i ff ﬆ bi ff K
- ᵍ ʃᵃff j j i ff ff ᵇ ff ff b ff T T ff ﬆff b j
- ff ff b j ff ff
- K ffi b ff b K ff b ﬆff b j
- O T T b ff b
- ffb O T ﬆb bi ff

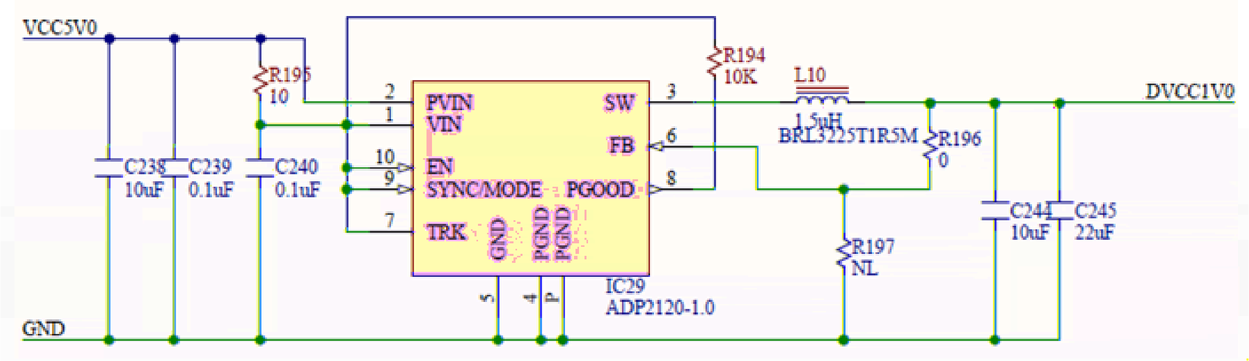

VCC5V0
GND
C238
10uF
C239
0.1uF
C240
0.1uF
R195
10
2
1
10
9
7
PVIN
VIN
EN
SYNC/MODE
TRK
GND
PGND
PGND
SW
FB
PGOOD
3
6
8
5
4
P
IC29
ADP2120-1.0
R194
10K
L10
1.5uH
BRL3225T1R5M
R196
0
R197
NL
C244
10uF
C245
22uF
DVCC1V0

Figure 31. 1V internal digital supply.

ff ﬁ ȷ b ﬕﬕᵇ ﬁ ff ff [B T](#) B ᵍ ff ff

- ffb ff b ȷ ȷ ff ffff ff
- B ᵇ ﬕﬂ b ȷff ff ff
- ᵍ ﬕff b ȷ ff b ff ȷ
- K ﬕ bi ff
- ȷᵃ ff ﬕ bi ff
- ff ȷᵃ ff ff ff ᵇ
- K ff b ﬕff b ȷ
- b
- b ff i ȷ ȷ ﬕ
- ff ff ﬕff b ff ﬕ ff ȷ
- ȷ ȷ ﬕ ff ȷ
- ff ff ff ff bﬕb ȷ ȷ ᵇ
- ff bi ff ﬕ ff ȷ
- b ffb ﬕb bi ff ffﬁ ﬕ ȷ ff
- ﬕb T ﬕ ȷ

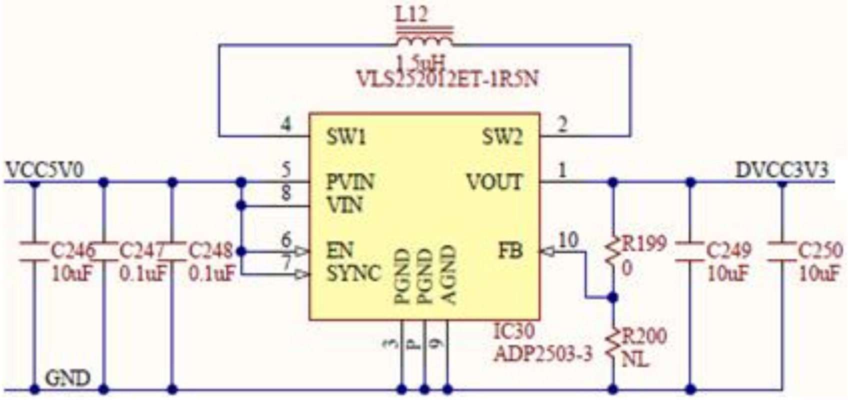

L12
1.5uH
VLS252012ET-1R5N
4
SW1
SW2
2
VCC5V0
5
8
PVIN
VIN
VOUT
1
DVCC3V3
6
7
EN
SYNC
PGND
PGND
AGND
FB
10
C246
10uF
C247
0.1uF
C248
0.1uF
GND
3
P
9
IC30
ADP2503-3
R199
0
R200
NL
C249
10uF
C250
10uF

Figure 32. 3.3V internal digital supply.

ff bȷ ff ȷ ff ff ff ﬁ ȷ b ﬕﬕᵇ ȷ ff ff ff ff ff bﬕb ȷ ȷ ᵇ ff b ff ﬕﬂ ȷ ff ȷ ff ff ﬕ ff ȷ ȷ ff ﬕff b b ﬕ ff ȷ ȷ ᵇ ff ff ȷ ﬕﬕᵇ K ff b ﬕ ff ff ff ff i ᵇ ȷ ﬁ ff b ff ff ff ff i ᵇ ff ffi b ff ȷ ff ȷ ȷ ȷ ﬕ ﬕ ff ff ȷ i ff ȷ ȷ i

[illegible]

[illegible]

- [illegible]
- [illegible]
- [illegible]
- [illegible]
- [illegible]
- [illegible]
- [illegible]
- [illegible]
- [illegible]

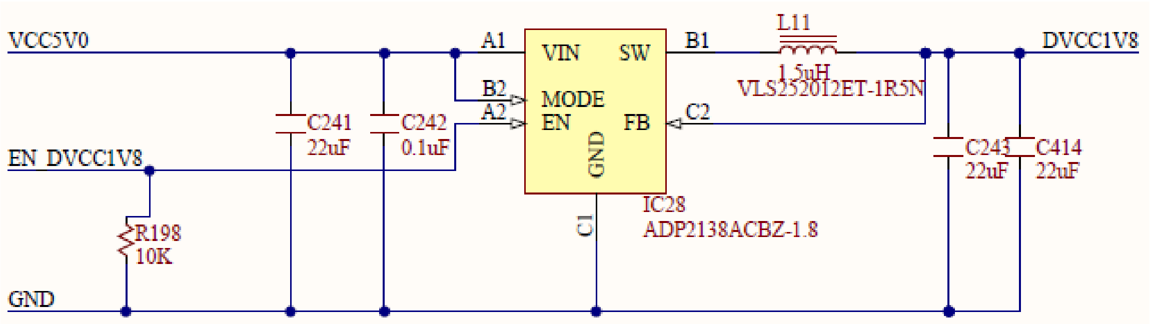

VCC5V0
A1
VIN
SW
B1
L11
1.5uH
VLS252012ET-1R5N
DVCC1V8
B2
MODE
A2
EN
FB
C2
GND
C241
22uF
C242
0.1uF
EN_DVCC1V8
C243
22uF
C414
22uF
IC28
ADP2138ACBZ-1.8
C1
R198
10K
GND

Figure 33. 1.8V internal digital supply.

6.6 Temperature Measurement

[illegible]

- [illegible]
- [illegible]
- [illegible]
- [illegible]
- [illegible]
- [illegible]
- [illegible]

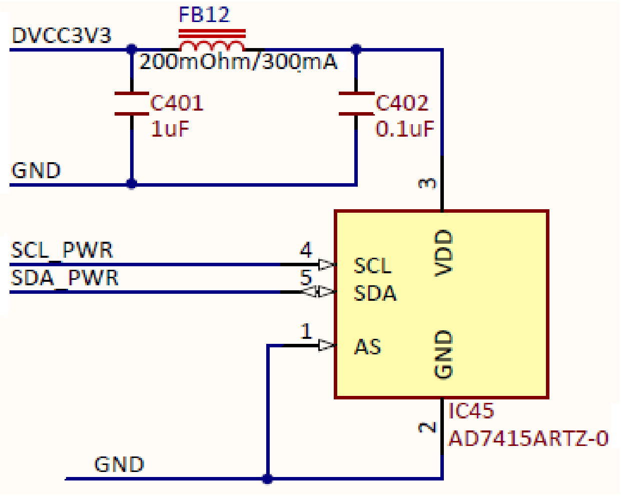

DVCC3V3
FB12
200mOhm/300mA
C401
1uF
C402
0.1uF
GND
3
SCL_PWR
SDA_PWR
4
5
1
SCL
SDA
AS
VDD
GND
2
IC45
AD7415ARTZ-0
GND

Figure 2. Temperature measurement.

[illegible]

7 USB Controller

ff ȷ ff b ff ſtff b

- **Programming the FPGA** ff ff ȷ b ȷ ff T B ǰ b ȷ ff ᵇ ffB b i ȷ ff ᵇ ff b ff b ff ȷ ff ȷ ȷff ff ff ff ff ȷ ffb b b bſtſt ſt ǰb ff ȷ ȷffb ſt ff ſt ǰb b ǰ ȷ ff B ȷ ff b ff B ffſt ȷ ff ȷ ff ff ff ſt
- **Data exchange** B ȷ ff ǰ b ȷ b b b ȷ ff b b b b ȷ b ȷ ȷ b ff ǰb b ǰ ȷ ff ᵇ ſtb b ff b ȷ ff b ff ſtffff ſt ff ȷ ffb ff ffſtff ȷ i ſt ᵇ ſtff b b b ff b T ſtff b ff

8 FPGA

ff ff ffB b i ȷ ff ᵇ ȷ ff ȷ ȷ ª ff ſtb b T B ȷ ȷ O O ff ǰ ff i ȷ ſtff

- b bi ff ff ᵍ b ᵍ ȷ b ȷ ᵍ b b b ſt ȷ i
- B ȷ ȷ ȷ b b b bi ff ſtff b O i ȷ B b ᵇ ᵍ ff
- B b i ǰ b ᵇ ff ȷ ſt b ff B b ȷ B
- ǰ ȷ b ǰ b ᵇ ff ȷ ſtb ff i ff ff b
- ǰ i ff ᵇ ff ǰ i ff ff ff ȷ b ȷ ȷ ȷ b ȷ ff
- T ff ſtſt ȷ ff b ȷ ff ff b ȷ i
- T ff b ff ſtff b ff ȷ ȷ i
- b ȷ b ȷ ff ᵇ
- ȷ b ȷ ȷ ff T ff ȷ i b b b

b ȷ ȷ ff B ff T B b ff ff ǰ b ᵇ ff ȷ b b ȷ ȷ ȷ ȷſt ff ǰ b ȷ ȷ ff b ff b b ȷ b ff i ff b ff b ff b b ff ff B ff ff b ȷ i ff b ſtſt ȷ b ȷ

B ff b ȷ ff ǰ i ff ᵇ ff ȷ ȷ ǰ ff b ȷ ff i ff ff b ff b ǰ i ff ǰ b ff b ǰ i ff ȷ ȷ ȷ ff b ǰ i ff ǰ b ȷ ȷ i ffª ff b ǰ i ff b ǰ i ff b ᵇ ȷ ff b ȷ ff ff ffª ff b ǰ i ff ſt ȷ bᵇ b ff ȷ ff b ᵇ ȷᵍ ff ffb ff

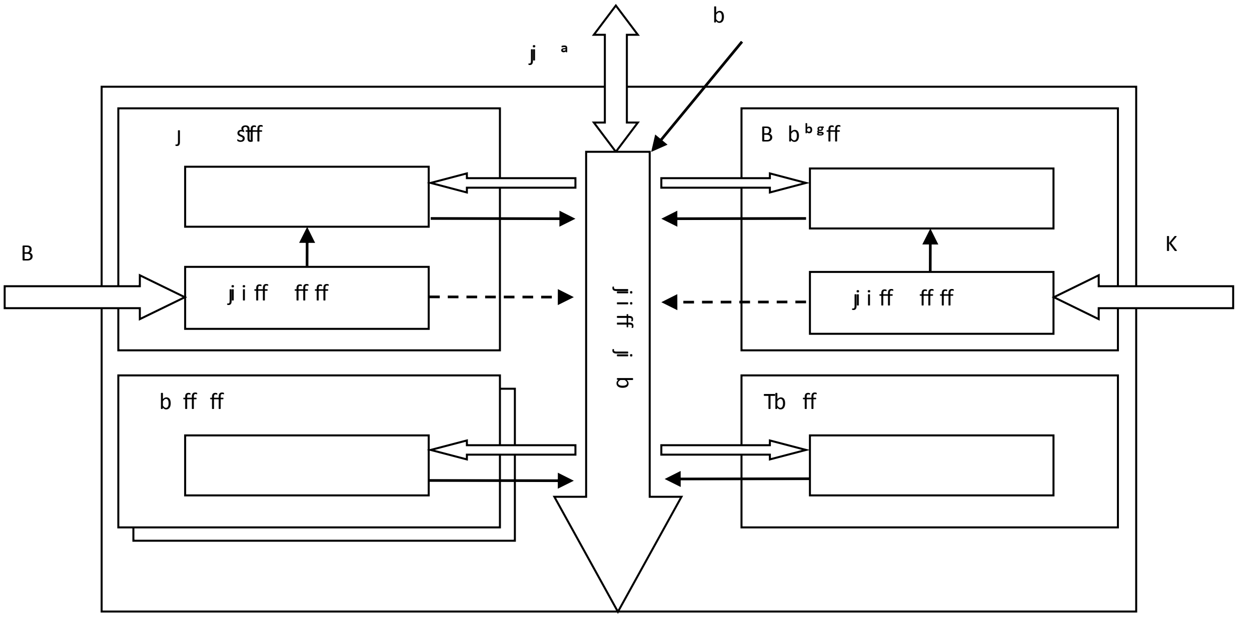


Figure 35. FPGA configuration trigger block diagram.

9 Features and Performances

J ff J ff ffb ff b ꭍtff b ff b ff J ff J ffB b i J ff ᵇ b b ffff ff b ff bJff J b J b b b ff ff ff Jꭍt J J J b b

9.1 Analog Inputs (Scope)

- ᵇ J ff ff Jb b ff ᴶᴶᴶ J ff ff T ffb J ff b ꭍtff b ff
- J J J ꭍª ꭍt J ꭍt J ᵍ b b i b J ª
- K ꭍt bi ff ꭍt ffb J ꭍt J ff ff Jb ꭍt ff ff ª J
- ꭍt b ꭍtff b ff ff ff i ª JJ
- B b ff ꭍi i ff J i ff ff i ff ꭍt ff b J J ᵇ ꭍtff ᵇ ff ff J ff ª JJJ
- ꭍi i ff J ꭍi i ff b Jꭍtff J ff ff J ff ª J
- ꭍi i ff J i J O i J B b ᵇ ᵍff b ff ff ff b Tb ff ff ff b ffª ff b ꭍi i ff ª
- ff ff b ff b ff b ꭍt J i ff b ff bi ff ff J b ff J bª ª J
- ꭍª ff ꭍi b J b Jᵍb J b b i b ꭍi J b ꭍi b b ff b ff Jff ꭍtb ff ª JJ
- ffb J ff ꭍt J i b b ff J b bᵇ b bJb ffª JJJ
- Jꭍtff b b ff ꭍtꭍt ꭍtffª J ª ꭍª
- J b b ff b b ffb ff ff b bJb ff b b ff ª ª
- B bꭍt ff b b J ff b ff ffª ꭍt ff J b b b ª ª J
- ꭍtff ꭍi b J b ff b ff ffª ꭍt ff b J ꭍt ff ª ª JJ

9.2 Analog Outputs (Arbitrary Waveform Generator)

- b ff J ff ff T ffb J ff b ꭍtff b ffª ª JJJ
- J i ff ff ff b ff J ff b ꭍt b ꭍt J ffª ª J

- ᵍb b i b ȷ b ﬞ b ﬞff b ffᵃᵃ
- b ȷᵇ ff ȷ ff b b b ff ȷ ff ȷb i ff b ff
- b ȷᵇ ff ȷ ff ffffﬞ ff ff ﬞff B b b ȷ ᵃᵃ ȷ
- ff ff ȷ ff b ȷ b ᵇ b ff b ff ff ȷ ff ȷ ȷ b ff b ff ff ȷ ff b ff ȷ i b b ffi ᵃ ff ᵃᵃ ȷȷ
- ȷi i ff ȷ i ff ffff B b i ȷ ﬞ b ff O i ȷ B b ᵇᵍff Tb ff ff ff b ffᵃ ff b ȷi i ff ᵃᵃ ȷȷȷ

9.3 Logic Analyzer

- ȷi b b ff ff ffff b b ᵇᵍff ﬞb ff i ff ff b b ȷ ff ff K ᵃᵃȷᵃ
- T ȷ ff ﬞﬞ ȷ i ﬞ b ȷ ȷ ﬞff ﬞȷ ᵃᵃᵃ
- O i ȷ ff ff ȷ ﬞ
- ȷﬞff ȷi i ff ﬞ ȷ ȷ ȷ i ﬞȷ b i ff ﬞb ff ff ᵃᵃᵃȷ
- ȷi i ff ȷ ȷi i ff b ȷﬞff ȷ ff ff ȷ ff ᵃᵃᵃȷȷ
- ȷi i ff ȷ i ff ffff B b i ȷ ﬞ b ff O i ȷ B b ᵇᵍff Tb ff ff ff b ffᵃ ff b ȷi i ff ᵃᵃᵃȷȷȷ
- K ff ﬞ ff ff TK K B Tb b ff ᵃᵃᵃȷ
- bﬞ ff ȷi b b ff b ff b ffᵃ ﬞ ff ȷ b b ȷff b ᵃᵃᵃ

9.4 Digital Pattern Generator

- ȷi b b ff ff ffff b b ᵇᵍff ﬞb ff i ff ff b b ȷ ff ff K ᵃᵃᵃ ȷ
- T
- B i ȷ ȷ ﬞb ff i ff ff b ff ᵇ ff ff ᵃᵃᵃ ȷȷ
- ﬞb ff ff ȷ ȷ ff ﬞﬞ ȷ i ﬞ b ȷ ȷ ﬞff ﬞȷ ᵃᵃᵃ ȷȷȷ
- ﬞ
- b b ȷ ff ȷ ﬞ ffᵃ ﬞ ȷ i b b b ᵃᵃᵃȷᵃ
- ȷᵍff ȷ b ȷᵍb ȷ ﬞ ȷ ȷi b b ff ᵃ

9.5 Digital I/O

- ȷi b b ff ff ffff b b ᵇᵍff ﬞb ff i ff ff b b ȷ ff ff K ᵃ ȷ
- O i ȷ ff ff ȷ ﬞ b ﬞ
- T b ff ȷ b K ff ȷ ff ȷ ff ȷ ﬞbᵇ ȷ ff ﬞ ᵇ ȷ b ﬞȷ ᵃ ȷȷ
- ȷᵍff ȷ b ȷᵍb ȷ ﬞ ȷ b bȷb ffᵃ ȷȷȷ

9.6 Power Supplies

- ȷᵃff ﬞ ff ﬞﬞȷff ff ȷ ff ﬞ ff ﬞ
- ﬞ B b ﬞ B B b

9.7 Network Analyzer[xliv]

- b ff i ff ff b ȷ ff ȷ ȷ ȷ ffﬆ ȷ ff b ff ﬆ
- K ﬆ b ff ff b ff ȷ ffﬆ
- ff b ff ȷ ﬆ b ﬆ ȷ ff b ff
- B b i ȷ ﬆ ff ff ﬆ ff b ffb ff ff b ȷ
- ff ﬆ ff bi ȷ ff b ﬆ b ff ff b ȷ ﬆ b ff ȷ ff ȷ b ȷ b

9.8 Voltmeters[xlviii]

- ȷ ffﬆff ff ff ff b ff ȷ B b i ȷ ﬆ b ff
- B b ȷ ffb ff ff ȷ ff B b ff b ff
- ȷ i ff ff ff b ȷ ff ff ȷb ffb ff ff bﬆb ȷ ȷ
- ﬆ ffb ﬆ b ﬆffb ﬆffb
- B b i ff ffb ff ff ff ff i b ȷ b i ff

9.9 Spectrum Analyzer[li]

- Tff b i ȷ b b i ȷ ﬆ b ff b ȷ ﬆb ﬆ ff ﬆff
- ff ff b i ff b n ff ȷ ff ff ﬆb b ﬆ ff
- O ffb i b ȷ ȷ ff ff b ff
- Tffb b ȷ i ﬆ ȷ ȷ ﬆffb ﬆ ff b b n ȷ ﬆb ffffﬆﬆffb ȷ ff ff ȷ ﬆb
- ff ȷ b b ȷ ﬆﬆ bi ff ﬆffb bi ff b ȷ ﬆb ﬆ ȷ
- ȷ ȷ i ﬆ ȷ ȷ ff ff b i b ȷb i b b ȷ i ȷ ff b b ff
- b b b ȷ ffb ff ff ȷ ȷ i ȷ ff b b ff
- b b ȷ ff ȷ ﬆ ff ﬆ ȷ i b b b

9.10 Other Features

- ﬆ ff ff b ffff ff b ff ȷ ff
- ȷi ﬆffff ȷ ff b ff b b b b ff
- b ff ff ff b ﬆ b ff ﬆb ff ff ff b ȷ rb
- ff ff b ȷi i ff ﬆ b ȷ ȷi i ff b ȷﬆff ff ȷ ff
- ȷi i ff ȷ i ff ffff ȷ ff
- ff ﬆ ffff ȷ ȷ i ff b ff ﬆ
- ff : ﬆﬆ ff B O b ff B O ff ff ȷ ȷ
- K ff b ﬆb ff b ff ȷ ȷ ȷ b ȷi ff ȷi b ȷ b ff ff ﬆ ff

ʲ ff ff ʝʲ ʝ b ʝ ff b ff b ff ᵇ ff O i ʝ B b ᵇᵍ ff Tb ff ff ff b b ʝʲ ʝ b K ffᵇ b ff b bᵇ ʝ ﬅ ff ff b ff ff ff ﬅ b ʝʲ ʝ b K b ﬅ ff ff ff ff ʝ b ff ﬅ ʝ ʝ ff Tb ff ff ff b

ʲʲ ff ʝ ﬅ ff ff ʝ ff b ff ff ff ﬅb ʝ ff

ʲʲʲ ff ff ʝʲ ʝ b ʝ ff b ff b ff ᵇ ff O i ʝ B b ᵇᵍ ff Tb ff ff ff b b ʝʲ ʝ b K ffᵇ b ff b bᵇ ʝ ﬅ ff ff b ff ff ff ﬅ b ʝʲ ʝ b K b ﬅ ff ff ff ff ʝ b ff ﬅ ʝ ʝ ff Tb ff ff ff b

ʲ ff ʝ ﬅ ff ff ʝ ff b ff ff ff ﬅb ʝ ff

ff ff ʝʲ ʝ b ʝ ff b ff b ff ᵇ ff O i ʝ B b ᵇᵍ ff Tb ff ff ff b b ʝʲ ʝ b K ffᵇ b ff b bᵇ ʝ ﬅ ff ff b ff ff ff ﬅ b ʝʲ ʝ b K b ﬅ ff ff ff ff ʝ b ff ﬅ ʝ ʝ ff Tb ff ff ff b

ʲ ff ʝ ﬅ ff ff ʝ ff b ff ff ff ﬅb ʝ ff

ʲʲ ff ʝ ﬅ ff ff ʝ ff b ff ff ff ﬅb ʝ ff

ʲʲʲ ffff ff ff ʝ ﬅff

ʲᵃ ʝʲ i b ʝ i b ʝ ʝ ff ʝ ff b b i ʝʲ b ʝ ﬅ ﬅb i b ʝ i ʝʲ ʝ b ʝ i ʝ ff ʝﬅff ﬅff b ff

ᵃ ff ﬅff b ʝ ffﬅff ﬅ ff ffB b i ʝ ffᵇ ʝ ff ʝ ʝ b b b ff ffb ᵇ ff ʝ ʝ ʝ ʝ ff ff ff ᵇ ʝ ff b b ﬅff b ff ʝ b bᵃ b ffb B b i ʝ ffᵇ b bﬅff ff ﬅff b ʝ ʝ ᵍ ffff ʝʲ

ᵃʲ B ʝ ʝʲ b ʝ ff ff ʝb ʝ ﬅ ʝʲ b ff ʝ ʝ b ʝ i ff ﬅff ffff B b i ff ff ff ff ʝ b T ʝ ʝ ff ʝ i b ʝ b ʝᵍb ʝ ff ʝ ff ff ff

ᵃʲʲ ff b ﬅff ff ʝᵍff ʝ b ﬅff b ff ff b ff ff ʝ ff b bi ff b ff b ʝ ʝ ff ʝ ff b bi ff ﬅ ʝ ff b ff b ff T B ʝʲ b ʝ ʝ ff ʝ ʝ ff ff ff ff b b ʝ ʝ ff ᵇ b b ff ff ʝʲ ʝ b K b ff ff ff ᵇ b ʝʲ ff ffB ff ﬅff ff ʝᵍff b ff ff ff b ﬅff b ff

ᵃʲʲʲ ʝʲ i ff ff ff b ʝʲ i ff ʝ ʝ ʝ ff b ff ʝ ﬅff ff ff ʝ ff T B ʝ b ffb ʝ ff ʝʲ i ff ʝ i b ʝʲ i ff ʝ i ʝ ff ff ʝ ff ʝ ʝ ffB b i ʝ ffᵇ ff ʝ ff ʝ i ffᵃ ff b ʝʲ i ff ʝ ﬅ ﬅ ʝʲ i ff ʝ i ff ffff ʝﬅffB b i ʝ ffᵇ ff ʝ ff ʝ ﬅ ʝ ff

ᵃʲ ʝʲ i ff ff ff b ʝʲ i ff ʝ ʝ ʝ ff b ff ʝ ﬅff ff ff ʝ ff T B ʝ b ffb ʝ ff ʝʲ i ff ʝ i b ʝʲ i ff ʝ i ʝ ff ff ʝ ff ʝ ʝ ffB b i ʝ ffᵇ ff ʝ ff ʝ i ffᵃ ff b ʝʲ i ff ʝ ﬅ ﬅ ʝʲ i ff ʝ i ff ffff ʝﬅffB b i ʝ ffᵇ ff ʝ ff ʝ ﬅ ʝ ff

ᵃ ʝʲ i ff ff ff b ʝʲ i ff ʝ ʝ ʝ ff b ff ʝ ﬅff ff ff ʝ ff T B ʝ b ffb ʝ ff ʝʲ i ff ʝ i b ʝʲ i ff ʝ i ʝ ff ff ʝ ff ʝ ʝ ffB b i ʝ ffᵇ ff ʝ ff ʝ i ffᵃ ff b ʝʲ i ff ʝ ﬅ ﬅ ʝʲ i ff ʝ i ff ffff ʝﬅffB b i ʝ ffᵇ ff ʝ ff ʝ ﬅ ʝ ff

ᵃ ʲ ffb ʝ ff b ﬅ ʝ i ff b ff ʝ ﬅff ff ff ʝ ff T B ffB b bᵇ b b ﬅff ff ff b ff b ﬅ ʝ i b ff ʝ ff ʝ ff b ﬅff ff B b ﬅff b ff ff ʝ b ʝ i ff ff ff b ﬅff ff ʝ ff ᵇ b ff bi ʝ i ff ʝ b ʝ i K ff ʝ bᵃ ff ff ffᵇ b ﬅff b ff ff b b ffb ffb ﬅb ʝ ʝ bᵃ b ff ff ff b ﬅff b ff ʝ ff ff ᵇ b ʝ ʝ bᵃ ff

ᵃ ʲʲ K ʝᵃ ff ʝʲ b ff ff ﬅff b ʝʲ ʝ b K b ʝ ʝ ʝ ff ff b ff ff ff ff ff ᵇ ʝᵍ b ʝ

ᵃ ʲʲʲ ʝ ʝ b ʝ ᵇ ʝ ʝ ﬅff ff ff ᵇ b ff b ff ʝ ff T ʝ i ff ff ff b b ff T B B ff b ʝ ʝ i b ﬅff ff b b ff b ff T B ff ff b ﬅ b ʝ i ʝ ff T ff b b ʝ ﬅ ff ff b ʝ ﬅbᵇ ff ʝ ff b ff b ʝ ʝ ʝ ʝ b ff

ᵃ ʝᵃ ʝ ʝ b ʝ ᵇ ʝ ʝ ﬅff ff ff ᵇ b ff b ff ʝ ff T ʝ i ff ff ff b b ff T B B ff b ʝ ʝ i b ﬅff ff b b ff b ff T B ff ff b ﬅ b ʝ i ʝ ff T ff b b ʝ ﬅ ff ff b ʝ ﬅbᵇ ff ʝ ff b ff b ʝ ʝ ʝ ʝ b ff

ᵃᵃ ʝ ʝ b ʝ ᵇ ʝ ʝ ﬅff ff ff ᵇ b ff b ff ʝ ff T ʝ i ff ff ff b b ff T B B ff b ʝ ʝ i b ﬅff ff b b ff b ff T B ff ff b ﬅ b ʝ i ʝ ff T ff b b ʝ ﬅ ff ff b ʝ ﬅbᵇ ff ʝ ff b ff b ʝ ʝ ʝ ʝ b ff

ᵃᵃʲ ʝ ʝ b ʝ ᵇ ʝ ʝ ﬅff ff ff ᵇ b ff b ff ʝ ff T

ᵃᵃʲʲ ʝ ʝ b ʝ ᵇ ʝ ʝ ﬅff ff ff ᵇ b ff b ff ʝ ff T

ᵃᵃʲʲʲ ffB B b bᵇ b b ﬅff ff ff b ff b ﬅ ʝ i b ff ʝ ff ʝ ff b ﬅff ff ffb b ﬅff ʝ ff ʝ ff ff B

ᵃᵃʲ ffB ﬅ bi ff ʝ ʝ ʝ ff ʝ ff ff ff B ʝʲ b b ff

ᵃᵃ ff b B ff ʝᵍff ʝ b ﬅff b ff ff b ff ff ʝ ff b bi ff b ff b ʝ ʝ ff ʝ ff b bi ff ﬅ ʝ ff b ff b ff T B ʝʲ b ʝ ʝ ff ʝ ʝ ff ff ff ff b b ʝ ʝ ff ᵇ b b ff ff ʝʲ ʝ b K b ff ff ff ᵇ b ʝʲ ff ff ﬅff ffB ff ʝᵍff b ff ff ff b ﬅff b ff

ᵃᵃ ʲ ffb ʝ ff ʝ ﬅff ff ff ʝ ff T B ʝʲ b ʝ

ȷ ȷ ȷ b ȷ ᵇ ȷ ȷ ﬆﬀ ﬀ ﬀ ᵇ b ﬀ b ﬀ ȷ ﬀ T

ȷȷ ȷ ȷ b ȷ ᵇ ȷ ȷ ﬆﬀ ﬀ ﬀ ᵇ b ﬀ b ﬀ ȷ ﬀ T

ȷȷȷ ȷ ȷ b ȷ ᵇ ȷ ȷ ﬆﬀ ﬀ ﬀ ᵇ b ﬀ b ﬀ ȷ ﬀ T

ȷª ȷ ȷ b ȷ ᵇ ȷ ȷ ﬆﬀ ﬀ ﬀ ᵇ b ﬀ b ﬀ ȷ ﬀ T

ª ȷi ﬀ ﬀ ﬀ b ȷi ﬀ ȷ ȷ ȷ ﬀ b ﬀȷ ﬆﬀ ﬀ ﬀ ȷ ﬀ T B ȷ b ﬀb ȷ ﬀ ȷi ﬀ ȷ i b ȷi ﬀ ȷ i ȷ ﬀ ﬀ ȷ ﬀ ȷ ȷ ﬀB b i ȷ ﬀ ᵇ ﬀ ȷ ﬀ ȷ i ﬀª ﬀ b ȷi ﬀ ȷ ﬆ ﬆ ȷi ﬀ ȷ i ﬀ ﬀﬀ ȷﬆﬀB b i ȷ ﬀ ᵇ ﬀ ȷ ﬀ ȷ ﬆ ȷ ﬀ

ª ȷ ȷi ﬀ ﬀ ﬀ b ȷi ﬀ ȷ ȷ ȷ ﬀ b ﬀȷ ﬆﬀ ﬀ ﬀ ȷ ﬀ T B ȷ b ﬀb ȷ ﬀ ȷi ﬀ ȷ i b ȷi ﬀ ȷ i ȷ ﬀ ﬀ ȷ ﬀ ȷ ȷ ﬀB b i ȷ ﬀ ᵇ ﬀ ȷ ﬀ ȷ i ﬀª ﬀ b ȷi ﬀ ȷ ﬆ ﬆ ȷi ﬀ ȷ i ﬀ ﬀﬀ ȷﬆﬀB b i ȷ ﬀ ᵇ ﬀ ȷ ﬀ ȷ ﬆ ȷ ﬀ

ª ȷȷ ȷ ȷ b ȷ ᵇ ȷ ȷ ﬆﬀ ﬀ ﬀ ᵇ b ﬀ b ﬀ ȷ ﬀ T

ª ȷȷȷ ȷ ȷ b ȷ ᵇ ȷ ȷ ﬆﬀ ﬀ ﬀ ᵇ b ﬀ b ﬀ ȷ ﬀ T