INVITED PAPER

The Promise of Nanomagnetics and Spintronics for Future Logic and Universal Memory

This paper provides an overview of basic principles associated with representing information in the form of magnetic polarization; spin-based memory and logic devices are reviewed.

By Stuart A. Wolf, Jiwei Lu, Mircea R. Stan, *Senior Member IEEE*, Eugene Chen, *Senior Member IEEE*, and Daryl M. Treger

ABSTRACT | This paper is both a review of some recent developments in the utilization of magnetism for applications to logic and memory and a description of some new innovations in nanomagnetics and spintronics. Nanomagnetics is primarily based on the magnetic interactions, while spintronics is primarily concerned with devices that utilize spin polarized currents. With the end of complementary metal–oxide–semiconductor (CMOS) in sight, nanomagnetics can provide a new paradigm for information process using the principles of magnetic quantum cellular automata (MQCA). This paper will review and describe these principles and then introduce a new nonlithographic method of producing reconfigurable arrays of MQCAs and/or storage bits that can be configured electrically. Furthermore, this paper will provide a brief description of magnetoresistive random access memory (MRAM), the first mainstream spintronic nonvolatile random access memory and project how far its successor spin transfer torque random access memory (STT-RAM) can go to provide a truly universal memory that can in principle replace most, if not all, semiconductor memories in the near future. For completeness, a description of an all-metal logic architecture based on magnetoresistive structures (transpinnor) will be described as well as some approaches to logic using magnetic tunnel junctions (MTJs).

KEYWORDS | Magnetic cellular automata (MCA); magnetoresistive random access memory (MRAM); reconfigurable array of magnetic automata (RAMA); spin transfer torque random access memory (STT-RAM)

I. INTRODUCTION

Both nanomagnetics and spintronics utilize spin or magnetism to provide new ways to store and process information; nanomagnetics is based mainly on magnetic interactions between nanomagnets, while spintronics is primarily associated with the utilization of spin polarized currents in memory and logic devices. With the end of complementary metal–oxide–semiconductor (CMOS) in sight, nanomagnetics can provide a new paradigm for information process using the principles of magnetic quantum cellular automata (MQCAs). MQCAs are described in the next section, where a new method of fabricating MQCAs that are fully reconfigurable is proposed. These reconfigurable arrays can also be prepared as independent storage bits and by virtue of an extremely regular structure, both for logic and memory, may be amenable to very cost-effective polymeric self-assembly manufacturing methods that can complement, and perhaps eventually replace, the expensive, top down lithographic techniques currently used to produce semiconductor logic and memory. In addition, a brief description of magnetoresistive random access memory (MRAM) will be presented. MRAM is the first mainstream spintronic nonvolatile random access memory. A recent successor to MRAM that uses a novel

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S. A. Wolf is with the Department of Materials Science and Engineering and the Department of Physics, University of Virginia, Charlottesville, VA 22904 USA (e-mail: saw6b@virginia.edu).
J. Lu is with the Department of Materials Science and Engineering, University of Virginia, Charlottesville, VA 22904 USA (e-mail: jl5tk@virginia.edu).
M. R. Stan is with the Department of Electrical and Computer Engineering, University of Virginia, Charlottesville, VA 22904 USA (e-mail: mircea@virginia.edu).
E. Chen is with Grandis Inc., Milpitas, CA 95035 USA (e-mail: eugene.chen@grandisinc.com).
D. M. Treger is with Strategic Analysis, Inc., Farmington Hills, MI 48331 USA (e-mail: treged@earthlink.net).
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method of writing the bits will also be described; spin transfer torque random access memory (STT-RAM) can go much further to provide a truly universal memory that can in principle replace most, if not all, semiconductor memories in the near future, and its performance will be estimated and compared with more conventional memories below. Finally some novel logic architectures based on magnetoresistive devices will be described. These are the transpinnor, which is an all-metal-based architecture, and a logic structure based on magnetic tunnel junctions (MTJs).

II. NANOMAGNETIC LOGIC: MQCA AND RAMA

Modern electronics is charge based where electronic charge is used to encode digital information (binary bits 0 and 1). However, this paradigm has a fundamental shortcoming. Charge is a scalar quantity, and only has magnitude. Therefore, logic levels must be demarcated by a difference in the *magnitude* of charge. For example, more charge stored in a device could signify the logic bit 0 and less charge could signify the logic bit 1. Or presence of charge could signify the logic bit 0 and absence could signify the bit 1. This is the approach adopted in the metal–oxide–semiconductor field-effect transistor (MOSFET). When the channel is full of charge, the transistor is "on" and could encode the bit 0. When the channel is depleted of charge, the transistor is "off" and could encode bit 1. Switching between logic levels requires changing the magnitude of charge in the device, which invariably involves current flow and an associated I^2R Joule dissipation ($I =$ current and $R =$ resistance in the path of the current). This dissipation is unavoidable in any charge-based electronics.

Spin, on the other hand, is a *pseudovector* (spinnor) that has a fixed magnitude, but a variable direction (or polarization) and whose rotations are governed by the Pauli spin matrices. By placing an electron in a magnetic field, we can make its spin polarization bistable (only polarizations parallel and antiparallel to the field are allowed eigenstates). These two polarizations can encode the logic bit 0 and 1. Switching between logic levels will then require merely flipping the spin, without physically moving the charge in space and causing a current flow. This can potentially reduce energy dissipation significantly since the I^2R loss is eliminated. The energy dissipated during a spin flip (logic switching event) is the energy difference between the two bistable polarization states which are separated by the Zeeman energy $g\mu_B B$. This energy can be made less than the thermal energy k_BT without causing too many unwanted random spin flips and bit errors, because spin couples very weakly with phonons and as a result, spin split levels are not broadened by $\sim k_BT$. If that were not the case, electron spin resonance experiments could never be carried out at room temperature where the spin splitting energy is only few tens of μeV (tens of gigahertz frequency), while the room temperature k_BT is 25 meV. Because of this weak phonon coupling, spins can also be maintained out of equilibrium for long durations. As a result, the energy dissipated during a switching event can be less than the Landauer–Shannon limit of $k_BTln(1/p)$ ($p =$ bit error probability) since the latter result is derived on the basis of equilibrium thermodynamics [1], [2].

The idea of spin-based computing, where Boolean logic gates are realized with interacting single electron spins, is quite old [3], [4] and is the progenitor of spin-based quantum computing. This paradigm, known as single spin logic, is extremely energy efficient (it can reach the Landauer–Shannon limit of $k_BTln(1/p)$ [5]), but requires low-temperature operation ($\sim$1 K) because of the current state of semiconductor technology. More recently, the idea of implementing Boolean logic gates with magnetic dots interacting via dipole–dipole interactions has gained ground. In a ferromagnetic dot, $\sim 10^4$ spins act in unison like a giant classical spin. When the grain has shape anisotropy, the magnetization direction becomes bistable and can encode logic bits 0 and 1 [6]. Logic gates are realized in the same way as single spin logic. This paradigm can work at room temperature and Boolean logic gates have been demonstrated. It has been termed MQCA [7].

A very important result is that the energy dissipated in switching the magnetization of a dot containing $\sim 10^4$ spins is *not* 10^4 times the switching energy of a single spin, but only about 35 times the switching energy of a single spin [8]. This happens because of the interactions between the spins that significantly reduce the number of degrees of freedom thus reducing the switching energy, etc. In the end, the energy dissipated in switching a magnetic grain is $2\ Ku_2V$ where Ku_2 is the anisotropy per unit volume and V is the volume of the magnetic grain. For a dot of size $(5\ \text{nm})^3$ this energy has been estimated as 0.8 eV [9]. This energy is about 32 k_BT at room temperature, whereas present-day transistors dissipate about $5 \times 10^4\ k_BT$ at room temperature [10]. Magnetic logic is therefore capable of reducing energy dissipation by three orders of magnitude. Our ideas for magnetic logic have their foundations in these early ideas, but go well beyond these implementations by placing the magnetic bits in arrays in which the dots can be electrically addressed individually (not with charge currents, but with electric fields) and the magnetism in the dots can be gated and clocked electrically without having strongly varying magnetic fields.

A. MQCA

Quantum cellular automata (QCAs) were initially proposed by D. Tougaw and C. Lent at the University of Notre Dame, Notre Dame, IN [11]. The computation is based on Coulomb interactions of the electrons confined in quantum dots (QDs). A typical QCA cell design as shown in Fig. 1 [11] contains four QDs and the two electrons hopping among the QDs. Due to the Coulomb repulsion, the electrons occupy one of the two diagonal configurations which correspond to the bistable ground state representing logic "0" and "1". With an external perturbation (input), the

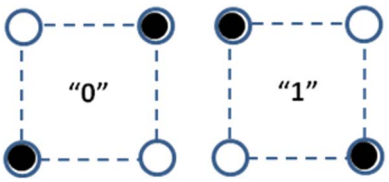

Fig. 1. *Schematic of QCA cells. The open circles represent the QD and the solid ones are electrons. The Coulomb blockade between two electrons results in two configurations of electrons in diagonal QDs representing logic "0" and "1."*

cell can switch between the ground states in a highly nonlinear and abrupt manner. The information transmission can be realized by "binary wires" which are composed of linear arrays of cells that are coupled via the Coulomb interactions. The QCA cell has been experimentally demonstrated in 1997 [12] followed by the logic gate [13]. However, these demonstrations were performed at subkelvin temperatures due to the weak strength of the Coulomb interaction ($\sim k_B \times$ 1 K). In order to operate QCA at room temperature, the scale of QD and QCA cell needs to be extremely small ($\sim$2 nm) [12], which remains a challenge to the current technology.

MQCAs on the other hand function based on the dipolar interactions between nanomagnetics. However, it is the exchange interaction among spins inside one ferromagnetic dot that can transform the dot ($\sim$100 nm) into one single classical spin which then can be coded as "0" or "1" based on the spin direction, e.g., up versus down. Cowburn *et al.* [7] first demonstrated a room temperature MQCA using a chain of ferromagnetic circular dots. Later, the group at the University of Notre Dame developed the MQCA using noncircular dots and showed the magnetic switching of MQCA wires with the assistance of an external magnetic field (the clocking field) [14], while Fig. 2 illustrates the schematics of MQCA cells and wires developed by Bernstein *et al.* [14]. Similar to the QCA, the switching between the ground states in MQCA is adiabatic. The clocking field helps to align the magnetization along the hard axis of MQCA dots and once it is removed, the spins in the dots relax into the ground state set by the initial input without falling into metastable states. A logic gate based on the majority voting function has been also demonstrated in 2006 [15].

MQCA is scalable to rather small dimensions and the scaling limit is the thermal fluctuation limit of about 40 kT which translates to a nanomagnet size of about 5 nm^3 for a typical ferromagnet. Below the critical size, the spins in the ferromagnetic dots can randomly flip direction due to thermal fluctuations. However, the spin state can be stable for $\sim$1 ms even below the superparamagnetism limit, which is long enough to allow some information processes [16]. The size scaling also reduces the number of spins in the dots which in turn increases the switching speed of the ferromagnetic domain.

One disadvantage of MQCA is its relatively low speed in comparison to a conventional CMOS device. The bottleneck is the precession speed of the domains in response to the dipolar interaction with neighboring nanomagnets. These speeds are typically of the order of nanoseconds [14]. This limits the top speed of MQCA. In addition, the interface between MQCA and conventional integrated circuits is also complicated owning to the information conversion between the charge and the spin. A recent review by Orlov *et al.* presents a more detailed discussion and an outlook of these issues [17].

B. Reconfigurable Array of Magnetic Automata (RAMA)

This section describes the development of a novel self-assembled thin-film array of *magnetic nanopillars* that can be configured into a MQCA architecture [18]. These nanopillars are located at the intersections of a very large and regular cross-point structure with wires below the nanopillars running one way, and wires on the top running perpendicular to the wires below, as illustrated in Fig. 3. The nanopillars are magnetized and the selection and geometry of the ferromagnet ensure that the magnetic moments of the nanopilllars point either up or down, perpendicular to the substrate. It has already been demonstrated that a random array of up and down polarized ferromagnetic pillars ($CoFe_2O_4$) embedded in a ferroelectric or multiferroic matrix (e.g., $BiFeO_3$) can have their magnetizations rotated from being perpendicular to the pillar (and the film) surface to being in-the-plane of the film with the application of a modest electric field [19]. These structures can be fabricated using polymeric self-assembly methods for both the nanopillars in the matrix [20], [21] and for the crossbar nanowires [22]. We can position the ferromagnetic nanopillars so that they couple

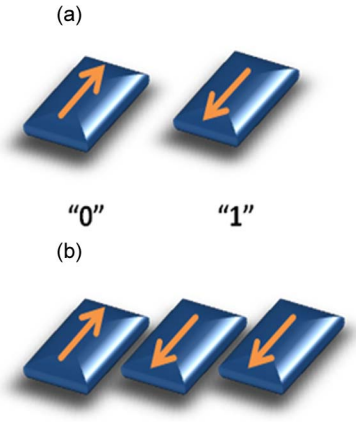

Fig. 2. *(a) Schematic of elongated ferromagnetic dots: the size of dot is small enough to maintain a single ferromagnetic domain and the direction of magnetization presents either "1" or "0"; (b) schematic of a section of MQCA wire. The adjacent dots are coupled antiferromagnetically, i.e., the opposite magnetization direction.*

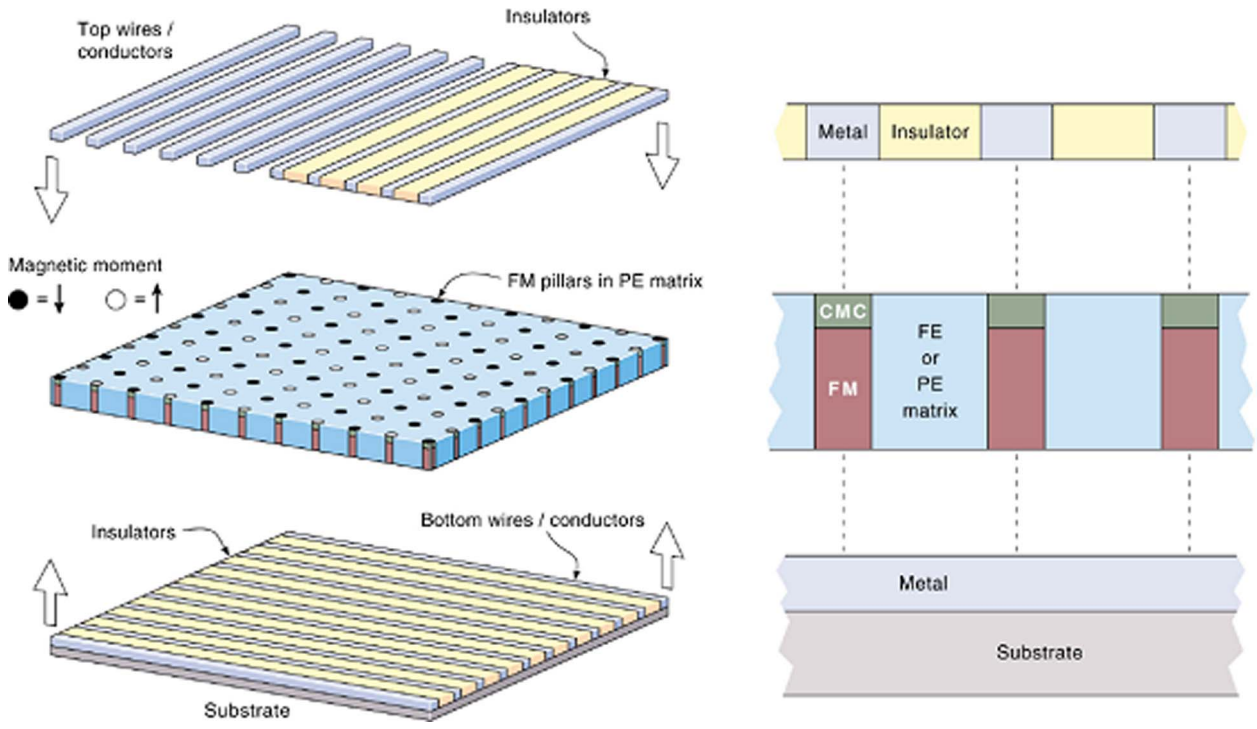

Fig. 3. ***Method of constructing the logic array.***

antiferromagnetically. A key to making RAMA work is the ability to prepare large, very regular arrays of nanopillars arranged in a square pattern. Large square arrays templated by triblock terpolymers [21] have recently been demonstrated.

The proposed logic array is similar to an MQCA and works in the following fashion. We design our array so that the ferromagnetic pillars couple antiferromagnetically through their dipolar exchange and thus there are two stable configurations of the array, with each magnet being oppositely magnetized for the two configurations. Similar to QCA, each bit consists of four pillars in a square with two corners polarized up and two down, as illustrated in Fig. 4. This arrangement provides stability for the bit as opposed to using a single pillar as well as allowing us to map the logic gates unto existing gate designs for QCA. A sample gate (inverter gate) is also illustrated in Fig. 4. The unique

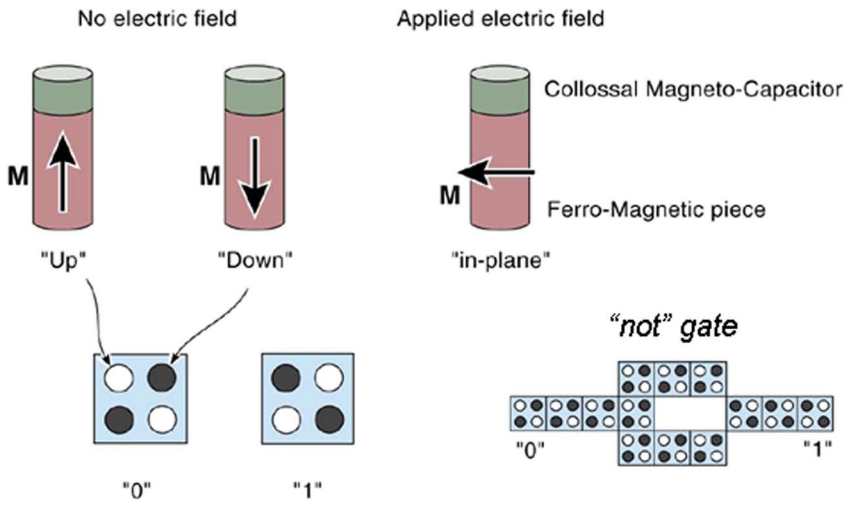

Fig. 4. ***An illustration of the four-pillar bit pattern and a sample gate, i.e., the inverter ("not gate").***

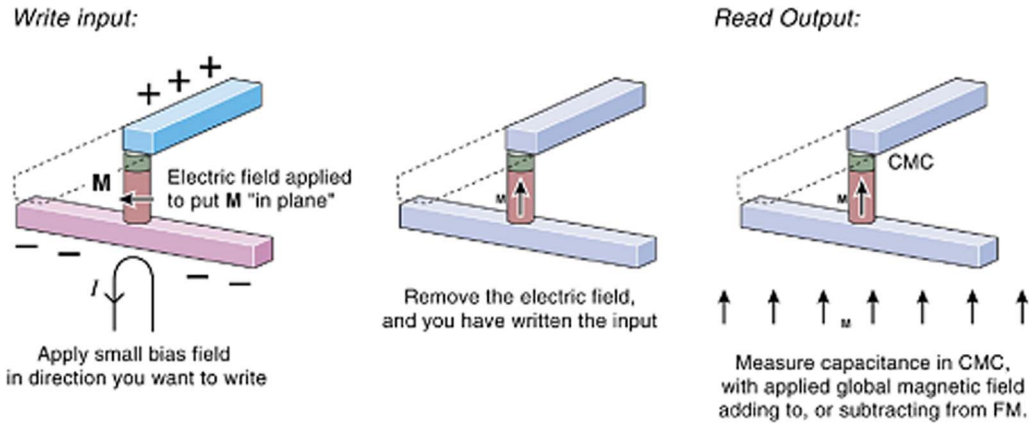

Fig. 5. ***Illustration of the writing and the reading of the bits.***

features of RAMA consist of the way the array is configured by using the interaction of the ferromagnetic pillars with the ferroelectric matrix and the sole use of electric fields for configuration, input, output, and operation of the array.

The two states of this bit can be represented by the state of the left uppermost corner, which could be up or down and the other magnets would adjust accordingly. Any pattern of such bits can be formed in the array by disabling unwanted pillars in the following fashion: electric fields are applied to the interface between the pillars (bits) and the surrounding ferroelectric material using the cross bar of wires, column by column. The strain on the interface will cause the easy axis of the pillars to be rotated 90°, from perpendicular to the surface of the array (out-of-plane), to parallel to the surface (in-plane). A gate pattern can then be imposed on the array by disabling all of the unnecessary pillars, e.g., the inverter gate illustrated in Fig. 4. Because of the hysteresis of the polarization in the ferroelectric, the remnant polarization will keep the easy axis in-plane until a small reverse electric field (the coercive field) is applied. The only reason to reactivate the pillars with the small reverse electric field would be to create a new gate pattern, i.e., reconfigure the array.

Gate operations would be initiated by applying an electric field to the left uppermost corner of the input bit which would rotate its magnetization in plane. This is also illustrated in Fig. 4. A very small magnetic field from a small wire loop above the array can be applied either up or down as the electric field is slightly reversed from the corner pillar, and thus this bit will be written and the magnetic information will then propagate through the MQCA as in any other MQCA. In fact the array can be clocked by using the electric fields to gate the propagation of the spin flips by selectively weakening the magnetization in the dots reducing the barrier to rotation from out-of-plane to in-plane. *No magnetic fields* are required for the clocking, only synchronized electric fields.

The output bits can be read using either an inductive method utilizing a pickup loop over the output bits, using a capacitive method (as shown in Fig. 5) or an MTJ method. (See a detailed discussion in [18].)

Of course, these RAMA arrays can also function well as large memory arrays since the bits are nonvolatile and can be individually addressed. In this case, one may want to deactivate half of the pillars (alternate ones) so that the remaining pillars are not coupled to their neighbors, and thus can be individually written with another layer of wires on top. If just a memory is desired then the pillars can be spaced so that they couple very weakly and then all of the pillars can be utilized for storage. This would provide a very dense array of nonvolatile random access memory.

The projected performance and the device parameters of RAMA based on $CoFe_2O_4$ nanopillars embedded in a ferroelectric matrix ($BiFeO_3$ or $BaTiO_3$) are listed in Table 1 in comparison with the end-of-road CMOS.

III. SPINTRONICS

A. MRAM Memory

MRAM is based on the concept of using the direction of magnetization to store information, and magnetoresistance (variation in resistance with magnetization) as information readout. It was originally invented in the late 1980s to replace bulky and heavy plated wire radiation hard memories [23]. The basic memory cell is a dual stripe of anisotropic magnetoresistive (AMR) layers separated by a nonmagnetic spacer. AMR materials were also used in the read head of magnetic recording hard disk drives (HDD). AMR is a change in the resistance of ferromagnetic conductors depending on the angle between the magnetization and the current. The magnitude of this effect is only about 2% for the most common magnetostriction-free NiFe or NiFeCo alloys suitable for device applications. The low resistance of metallic AMR thin-film

Table 1 Projected Device Parameters of RAMA

Device	CMOS ca. 2020	RAMA
Operation method	**Ballistic Charge**	Magnetic exchange (Dipolar)
Fabrication method	**Photolithography**	Polymeric self-assembly
Cost	**High**	Low
Cell size	**100 nm**	20
Bit density	**10^{10} cm^{-3}**	~10^{11}
Switching energy	**5 aJ/op**	0.01 aJ/op
Speed	**0.1 ps**	<1 ns
Non-volatility (No stand-by power)	**NO**	YES
RT operation	**YES**	YES
CMOS compatibility	--	YES

memory elements and low magnetoresistance resulted in an AMR–MRAM memory architecture that required the connection of a large number of memory elements in series with a large pass transistor, hence the read signal was further degraded. MRAM was a niche nonvolatile (i.e., retains memory when power is off) memory device for specialty radiation hard application when it was first invented, with dimensions larger than 1 μm.

The advancement of the MRAM technology benefited greatly from the rapid improvements and revolutionary discoveries in magnetoresistive materials fueled by the need to enhance magnetic recording areal density.

In the late 1980s, giant magnetoresistance (GMR) was discovered [24], [25]. It was immediately realized that this not only had the potential to enhance the performance of HDD, but also would improve MRAM read performances. The simplest form of GMR films consist of two magnetic layers separated by a Cu spacer, and had a magnetoresistance (MR) ratio of 6% initially and later more than 10% with improvements. New MRAM storage cells using spin valves [26] and pseudospin valves [27], [28] were proposed. The memory states were defined by the magnetization direction of the free layer being either parallel or antiparallel to that of the pinned or hard magnetic layer. No magnetic fields were required during read operation for these new memory modes. The all-metallic thin films still required many elements to be connected in series with a pass transistor, which degraded the read signal and speed.

In the early 1990s, higher tunnel magnetoresistance (TMR) was discovered in MTJ materials [29], [30]. While many efforts were directed at adapting MTJs for HDD read head applications for higher areal density, a few pioneering groups [31], [32], partially funded by the U.S. Defense Advanced Research Projects Agency (DARPA), were pursuing MTJ materials for MRAM applications. The resistance of MTJ material is easily tunable by varying the tunnel barrier thickness to match the impedance of the semiconductor isolation devices, so it enabled, for the first time, one MTJ element and one transistor bit cell (1TMTJ) architecture, as shown in Fig. 6. The magnetoresistance of an MTJ (TMR ratio) is much higher than for GMR material, and the read signal of MTJ-based MRAM is greatly improved as a result. Read speed in the range of 10 ns became feasible as a consequence of the improved signal levels.

The writing of standard MRAM is accomplished by flowing orthogonal currents to produce the required orthogonal magnetic fields at the cell at their cross point. The writing current required per line is on the order of 5–10 mA or larger: a very large pass transistor is required to control the pulsing of this large current. The only feasible option to minimize memory chip footprint is to share this large write current over many rows or columns of cells. The bits at the cross points get written, but the bits that experience half of the writing field under just one current line are "half-selected." The magnetic switching fields of a single free layer bits depend sensitively on the exact bit shapes since shape anisotropy is the main contributor to the free layer magnetic anisotropy, and have a large variation in a large memory array. As a result, some bits may experience half-select disturb switching problems. This was one of the key problems blocking the development of MRAM memory products. A new storage mode using a synthetic antiferromagnetic (SAF) free layer was invented and resulted in a rotational switching of the free layer with a greatly enhanced writing operational window [33]. Other inventions, such as the addition of oxygen

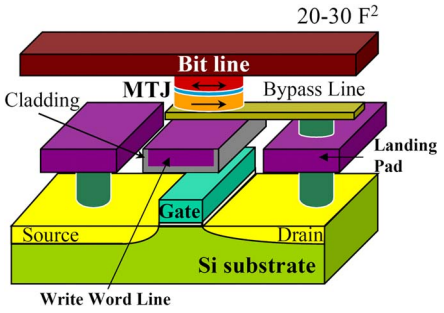

Fig. 6. *Schematic drawing for MRAM.*

gas during etch to solve MTJ shorting problems and metal line cladding to reduce write current and provide partial stray magnetic field shielding, greatly improved MRAM chip performances and expedited its productization [34].

A MRAM chip product prototype was announced in 2003 and the first ever MRAM commercial products started to ship in 2006 [35]. The manufacturability of MTJ devices as memory bits was proven in these nonvolatile MRAM products, having high read and write speeds (tens of nanoseconds) and nearly unlimited endurance.

Today 180- and 90-nm standalone MRAM products are finding more and more applications in various areas where their unique features of being nonvolatile fast and of unlimited endurances are vital: satellite applications, automotive data recorders, industrial controls, etc. Efforts are ongoing to scale MRAM technology to 65 nm for both standalone and embedded applications.

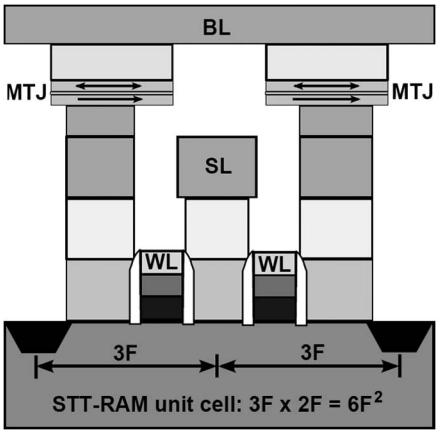

Fig. 7. *STT-RAM memory cell cross-sectional sketch. BL stands for bit line, SL stands for sense line, and WL stands for word line.*

B. STT-RAM Memory

STT-RAM stands for spin transfer torque random access memory. It utilizes a spin polarized current to directly switch the magnetization of a nanomagnet. It was theoretically predicted in 1996, and first demonstrated in metallic spin valve thin films with critical switching current density (J_{c0}) $> 10^7 \sim 10^8$ A/cm^2 [36]–[41], which is too high for practical memory devices. Grandis reported the first STT switching in an MTJ with J_{c0} less than 10^7 A/cm^2 [42]. Grandis also demonstrated STT switching in MgO barrier MTJ devices with J_{c0} in the 1 to 5×10^6 A/cm^2 range and TMR $> 150\%$ [43].

The STT switching technique brings significant advantages to magnetic random access memory (MRAM). In STT-RAM, the half select disturb problem of conventional field writing MRAM was avoided because the writing currents only flow to the cells being written. STT-RAM enables MRAM scalability beyond 65 nm by reducing write current more than 10$\times$ in a 1-T (transistor)/1-MTJ memory cell architecture such as the one shown in Fig. 7. It also leads to simpler memory architecture and manufacturing than conventional MRAM.

A viable new memory technology must demonstrate a clear path to migrate to smaller and denser memory size with lower power consumption as the underlying CMOS logic technology scales down as predicted by the International Technology Roadmap for Semiconductors (ITRS) roadmap. One of the major drawbacks of conventional MRAM has been the increase of switching current as the technology scales down. STT-RAM solves this switching current problem by applying the spin polarized current vertically through the MTJ element. Whether the nanomagnet switches is determined roughly by the current density; therefore, as the CMOS technology scales down, and the area of the MTJ element decreases, the total current decreases, as shown in Fig. 8.

Advances in J_{c0} reduction have been fast and steady, and along with the obvious advantages of STT-RAM, they have driven continued increases in STT-RAM R&D activities. SONY Corporation demonstrated for the first time a 180-nm logic STT-RAM test chip in 2005 at the International Electron Devices Meeting (IEDM) [44], and Hitachi and Tohoku University demonstrated a circuit design for a 2-Mb STT-RAM chip in 2007 at the International Solid-State Circuits Conference (ISSCC) using a 200-nm CMOS process [45]. These early STT-RAM demonstrations used large transistor nodes (130–180 nm) and smaller MTJ sizes (90-nm width), for their larger drive currents to switch a smaller MTJ element. Recently, 50-nm perpendicular MTJ dots were reported to have very low STT writing current [46], and 45-nm CMOS platform was used for an embedded STT-RAM test chip using in-plane MTJ films [47]. For the first time, MTJ-materials-based memory devices are being developed at the same advanced nodes as mainstream semiconductor memories [44].

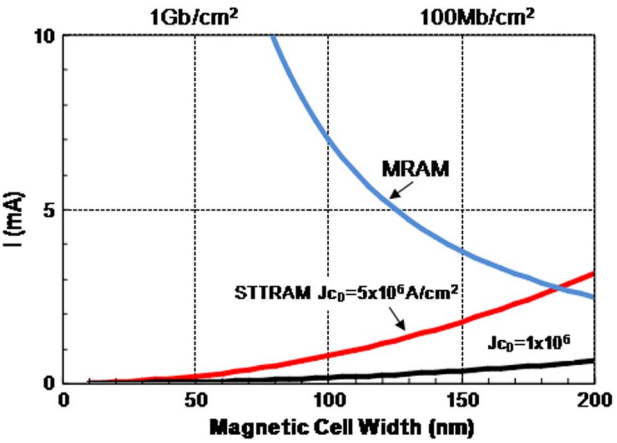

Fig. 8. *Comparison of writing current scaling trends between MRAM and STT-RAM.*

One of the key issues of STT-RAM technology has always been the reduction of the STT writing current of the MTJ storage element while maintaining sufficient thermal stability for adequate data retention and minimal write/read error rates [48]. Thermal stability of the storage layer in an MTJ not only affects STT-RAM memory cell standby data retention, but also it affects the write current distribution and hence write error rate, and read disturb error rate. A key figure of merit for STT writing, [STT critical writing current I_{c0} divided by the thermal stability factor (Δ)] was proposed [46] to compare various types of MTJ materials. Equations for I_{c0}/Δ for various types of MTJ materials can be found in [44]. This parameter offers a standardized way to compare results from various groups and from various MTJ materials (e.g., in-plane MTJ versus perpendicular MTJ). Since low thermal stability MTJ devices tend to have lower STT writing currents, thus it will be misleading to compare STT writing currents between devices having different thermal stability factors.

To switch the free layer magnetization in a conventional in-plane MTJ device, a spin polarized current is applied, and the free layer magnetization starts precessing around the direction of the total effective field. The magnetization has to overcome a very large out-of-plane demagnetizing field before it can switch to the opposite direction. The out-of-plane demagnetizing field does not contribute to the thermal stability of the in-plane free layer, yet it causes the STT writing current to be much higher, thus making the ratio of writing current over Δ higher. Perpendicular MTJs (PMTJ) for STT-RAM had been investigated to solve this problem [49], [50]. Indeed very low STT writing current was demonstrated at reasonably high thermal stability factor [46]. Perpendicular magnetic materials have been extensively studied for HDD hard disk application as a recording media. This type of material is capable of having a very high magnetic anisotropy field arising from the atomic properties of these materials. No shape anisotropy is required, and circular shaped bits can be used, which simplifies the manufacturing process. Sizes below even 10 nm are expected to have enough thermal stability due to the high anisotropy field ($>$ 2 Tesla) in some of these materials. The main challenges of making PMTJ work for STT-RAM are how to make these materials compatible with the MgO tunnel barrier, yielding high TMR ratio and spin transfer efficiency, and decreasing their damping constants for lower STT writing currents.

Another promising approach in solving the high out-of-plane demagnetizing field of conventional in-plane MTJ devices is to induce strong perpendicular anisotropy in the in-plane free layer material through material engineering, to the degree that it nearly cancels the demagnetizing field, so that the in-plane magnetization of the free layer can easily rotate out-of-plane and switch to the opposite in-plane direction [48]. Shape anisotropy will still be needed to achieve adequate thermal stability.

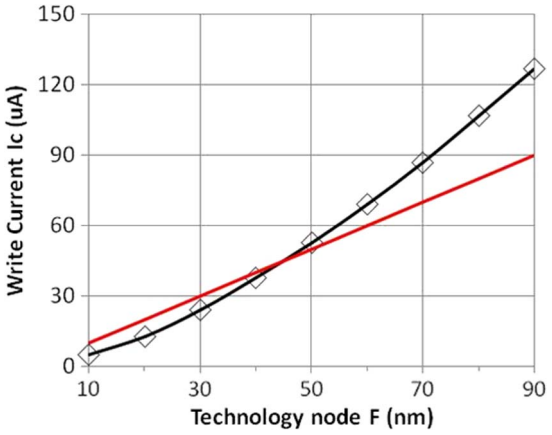

Fig. 9. *Simulation study of scaling with size F for in-plane DMTJ devices. The line without symbols is the drive current of a typical 6 F^2 transistor.*

Today the lowest STT critical writing current density reported with reasonable storage thermal stability ($>$ 40) was about 1 to 2 $\times$ 10^6 A/cm^2 for in-plane MTJ materials [48] and around 2 $\times$ 10^6 A/cm^2 for PMTJ materials [46]. Because in-plane MTJ elements need an aspect ratio of more than 2 to 3, and PMTJ simply uses a circular shape, total STT writing currents are comparable. As shown in Fig. 9, such write current levels enable the design of smaller than 8 F^2 STT-RAM memory cells.

At the present time, high TMR ratio $>$ 150% and low RA ($<$ 10 $\Omega\mu$m^2) seem to be achieved by various groups using in-plane MTJ materials. In the case of PMTJ materials, on the other hand, it seems hard to achieve these transport performances. More work is needed in this area.

Future STT-RAM architectures employing cross-point architecture and multiple ($>$ 4) storage states per bit can effectively lower the memory cell size to 2–4 F^2 range to compete with storage class memories such as Flash.

The switching of an MTJ free layer using STT is intrinsically capable of being completed in less than 1 ns, if the writing current amplitude is large enough. A typical writing current dependence on writing current pulse width is shown in Fig. 10 for an in-plane MTJ elliptical element with a size of 90 nm $\times$ 180 nm. It can be seen that there is tradeoff between writing speed and the current level required, which scales with the size of the transistor or memory cell size.

The read operation of STT-RAM is very similar to conventional field writing MRAM, even though MTJ based on AlO_x tunnel barrier, with much lower TMR ratio ($\sim$25%), supports a read access time of 30 ns. STT-RAM uses MgO barrier-based MTJ having a TMR ratio greater than 120%. Circuit simulation showed that 2–5-ns read access time is possible with even 2–5 μA read current differential. Unlike MRAM, STT-RAM has a read current disturb switching issue. This can be minimized by controlling the read current level and designing the bit with proper thermal stability [48].

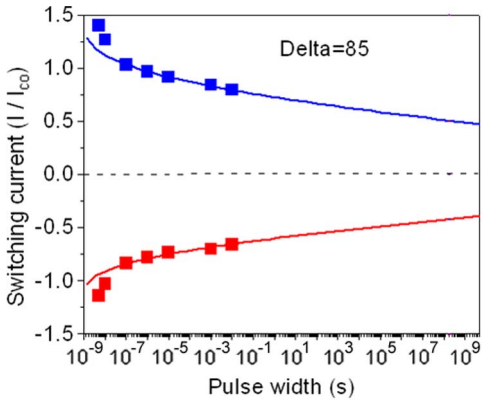

Fig. 10. *Experimental pulse width dependences of STT writing current from Grandis in-plane MTJ devices. Positive current is for parallel to antiparallel switching, and negative current is for antiparallel to parallel switching. Lines are drawn as guides to the eye.*

Write endurance test results beyond $1E + 12$ cycles are shown in Fig. 11, where no degradation is seen in the performances of the MTJ bits. Demonstration of more than $1E + 13$ cycles (10 ns equivalent) has been reported in literature [44].

In summary, STT-RAM retains the major benefits of MRAM of being a fast and nonvolatile memory with no known wear-out mechanism, and unlimited endurance; and extends the scalability to sub-10-nm nodes. For the first time, STT-RAM is being demonstrated at a leading edge CMOS node like other mainstream semiconductor memories.

C. STT-RAM Potential Applications

Currently, mainstream existing semiconductor memory technologies like SRAM, DRAM, and Flash are greatly challenged beyond 45 nm. SRAM has high power consumption, and its leakage power increasing 10× with each technology node. DRAM needs constant refreshing. Its refresh current keeps increasing, and it is becoming harder to maintain the minimum capacitance needed. Flash memory has limited endurance, high write power, very slow write speed, and multilevel cell and aggressive scaling leading to reduced performance and complicated controller.

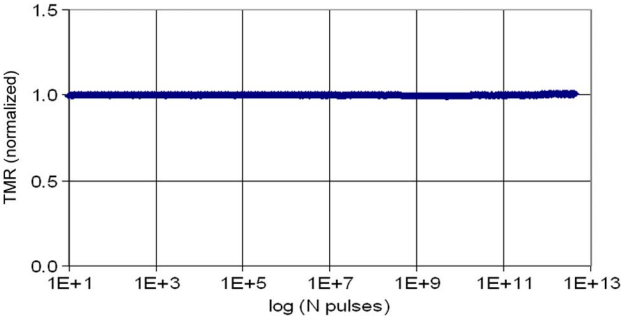

Fig. 11. *Normalized TMR ratio of an MTJ bit is shown versus repeated writing cycles.*

Power consumption in both mobile and data center applications is an increasingly serious issue. Incorporating STT-RAM in mobile applications can dramatically reduce standby power; and it was estimated that replacing DRAM with STT-RAM in data centers can reduce power by up to 75%.

Memory performance is fast becoming the key bottleneck that limits system performance, and critical applications are becoming more data-centric, and less compute-centric. Instant-on is becoming a requirement for many applications.

These problems create an opening for an alternative high-speed, nonvolatile random access memory. The basic requirements are capable of operating at high read and write speeds of 10–30 ns, and having nearly unlimited endurances. Main alternative nonvolatile memories that industry has been pursing are phase change memory (PRAM) and resistive change memory (RRAM). These not only lack the endurances required for a working memory, but also operates slower than the required 10–30 ns for both read and write operations. STT-RAM has the potential to meet both the endurance and speed requirements. STT-RAM will enable new instant on mobile applications for consumer and mission critical applications. These applications are expected to drive the next boom of the semiconductor industry.

A comparison chart of major memory technologies is shown in Table 2.

As the STT-RAM technology matures, and cell size is reduced below 4 F^2 using cross-point architecture and multistates per cell, STT-RAM may also work as a replacement for storage class memory such as Flash.

D. MTJ Based Logic Circuits

The main attraction of MTJs for logic is the *nonvolatile* aspect, which allows in principle for zero-leakage and instant-on operation. There are several ways to approach the design of logic circuits based on MTJs, but essentially those can be divided into two categories: one in which the MTJs are arranged and function as 2-D *memory arrays*, and another in which the MTJs are used as *individual switches*, either in series/parallel configurations to provide logic functionality, or as register replacement devices.

MTJ memory arrays for logic use the concept of look-up tables (LUTs) as in several types of field-programmable gate arrays (FPGAs) like the ones originally pioneered by Xilinx [51] and later adopted by most other FPGA manufacturers [52]. The truth table for any Boolean function can be directly stored in a LUT, with the address lines for the LUT acting as logic inputs; thus for each input combination, the corresponding minterm stored in the LUT is being activated depending on the stored truth table value. Any MRAM or STTRAM structure can be used for logic as a LUT; the only difficulty coming from all the peripheral circuitry needed for reliable operation. MTJs are passive

Table 2 Memory Technology Performance Comparison Chart (Source: Grandis)

	SRAM	DRAM	Flash (NOR)	Flash (NAND)	FeRAM	MRAM	PRAM	STT-RAM
Non-volatile	No	No	Yes	Yes	Yes	Yes	Yes	Yes
Cell size (F^2)	50–120	6–10	10	5	15–34	16–40	6–12	6–20
Read time (ns)	1–100	30	10	50	20–80	3–20	20–50	2–20
Write / Erase time (ns)	1–100	50 / 50	1 µs / 10 ms	1 ms / 0.1 ms	50 / 50	3–20	50 / 120	2–20
Endurance	10^{16}	10^{16}	10^{5}	10^{5}	10^{12}	$>10^{15}$	10^{10}	$>10^{15}$
Write power	Low	Low	Very high	Very high	Low	High	Low	Low
Other power consumption	Current leakage	Refresh current	None	None	None	None	None	None
High voltage required	No	2 V	6–8 V	16–20 V	2–3 V	3 V	1.5–3 V	<1.5 V
	Existing products						*Prototype*	

devices, so for robust operation, there is always a need for additional circuitry with gain (typically CMOS) at least at the periphery (e.g., inputs, outputs, clocking, etc.) [53], and typically as selection devices in one-transistor-one-MTJ (1T1MTJ) configurations [48], although, at least in principle, simpler one-diode-one-MTJ (1D1MTJ) in cross-point architectures is desirable [54]. As the area of the array grows as the square of the number of rows or columns, while the periphery grows only linearly with the number of rows/columns, the larger the memory array the less important the overhead for the periphery becomes. This can be a problem though for LUT operations because if the LUTs become too large there is a higher likelihood of resources remaining unused (for example, for SRAM-based FPGAs the optimum LUT size is between 16 and 64, i.e., 4–6 inputs [55]; such a MRAM array would be dominated by the periphery, especially the read sense amp). The main advantage of the LUT-style logic is though that it can work even with poor TMR ratios; if a memory is feasible, then a LUT-based logic is also feasible.

If higher TMR ratios (500%–1000%) become feasible as predicted by theory [56], then non-LUT MTJ-based logic becomes possible. For example, programmable logic arrays (PLAs) would consist of two separate 2-D cross-point 1D1MTJ arrays in a two-level logic configuration, the so-called AND and OR planes [57], in which the state of more than one MTJ can contribute to the output function, by being connected either in series, or more likely in parallel (this is quite similar to the case of the two flavors of flash memory, NAND—series, and NOR—parallel). Unlike a LUT that implements logic functions based on the nonminimized function truth table, a PLA can take advantage of two-level logic minimization to reduce the circuit complexity. In either case, both LUT- and PLA-based logic circuits would use MTJs "statically" in the sense that each MTJ would be programmed once when the circuit is first *configured*, and would stay that way until a reconfiguration is necessary; also, both LUT- and PLA-based logic would have a clear demarcation between the MTJ array and the CMOS peripheral circuitry.

There have also been proposals for tightly integrated CMOS/MTJ hybrid circuits, in which the MTJ devices are an integral part of the CMOS circuit functionality, as they are switched on and off during regular operation [58]–[62]. In some of these *fine-grained* CMOS/MTJ hybrid circuits, the MTJ is generally used as a register replacement device while the actual logic function uses regular CMOS transistor networks. In other such schemes, there have been proposals to use more complicated structures, with multiple wire passing currents of different values that can switch an MTJ that will represent the output of a logic function depending on the wire configuration and the current values [63]. In that case, the logic function is essentially a majority logic gate that has as special cases many of the useful Boolean functions [53]; unfortunately, for most of these proposed schemes, the focus was on feasibility, no comprehensive study being performed to compare the metrics (area, power, performance) with competing solutions.

E. Transpinnor

A transpinnor is based on a GMR structure. A prototype transpinnor was proposed and demonstrated by Barna *et al.* [64]. It consists of a bridge of four spin valves and a current stripline that could exert magnetic fields to

spin valves. Without any external fields, the bridge is balanced, therefore there is no output. When a current flows in the stripline, an external H field is generated, and if the H field is large enough, it will switch the resistance states of the spin valve. As a result, the bridge is no longer balanced and there is an output. The output is proportional to the GMR as well as the resistance (size) of spin valves.

If two current strip lines are used, the transpinnor can be used as a logic gate. The concept is to adjust the parameters of spin valves as a function of the external fields generated by the two striplines. For example, to make an OR gate, the output is turned on when the current in either input is sufficient enough to switch the resistance of the spin valves.

Transpinnors can also be used for amplifiers, memories, analog-to-digital (A–D) converters, etc. However, there is a lack of advancements up to date. It is largely due to the small GMR (typically $< 10\%$) of spin valves so that the output is highly dependent on the size of the spin valves which is not in favor of scaling. In addition, each transpinnor requires four spin valves that also limits the circuitry density significantly.

IV. SUMMARY AND CONCLUSION

As the CMOS roadmap's end draws closer, nanomagnetics and spintronics can provide a new paradigm for information processing. There are many more ideas for using spin and magnetism for information processing than we can discuss in this review and projection. We have selected those devices that we were asked to discuss and that we are most familiar with. Rather than restate what has already been discussed, we would like to provide the reader with the following take-home messages.

1) We can implement Boolean logic gates with magnetic dots interacting via dipole–dipole interactions (MQCAs) that are capable of reducing energy dissipation by three orders of magnitude compared to present-day transistors.
2) Reconfigurable arrays of MQCAs can be prepared as independent storage bits with an extremely regular structure that can be used for memory and logic functions. The RAMA concept uses a novel self-assembled thin-film array of magnetic nanopillars and nanowires that have very unique and multifunctional properties.
3) MRAM was the first mainstream commercial spintronic nonvolatile random access memory. It is based on using current produced magnetic fields for writing the information and the concept of using the direction of magnetization to store information, and magnetoresistance changes due to spin polarized currents as information readout.
4) STT-RAM, the successor to MRAM, can go much further to provide a truly universal memory that can in principle replace most, if not all, semiconductor memories in the near future. It utilizes a spin polarized current to directly switch the magnetization of a nanomagnet. The STT switching technique brings significant advantages to MRAM: for the first time, MTJ-materials-based memory devices are being developed at the same advanced nodes as mainstream semiconductor memories.
5) Novel logic architectures based on magnetoresistive devices are also very possible.
6) The transpinnor, which is an all-metal-based architecture, is based on a GMR structure and can be used as a logic gate, as well as for amplifiers, memories, A–D converters, etc. Development of these devices lags behind that of MRAM and STT-RAM.

Based on the advancements in these materials and devices, the promise of the use of nanomagnetics and spintronics for future logic and universal memory is at hand. ■

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ABOUT THE AUTHORS

Stuart A. Wolf received the A.B. degree in physics from Columbia College, New York, in 1964 and the M.S. and Ph.D. degrees in physics from Rutgers—The State University of New Jersey, New Brunswick, in 1966 and 1969, respectively.

He is currently the Director of the University of Virginia Institute for Nanoscale and Quantum Scientific and Technological Advanced Research (nanoSTAR), Charlottesville, and is a Professor at the Materials Science and Engineering Department as well as the Physics Department. He was previously a Program Manager at the U.S. Defense Advanced Research Projects Agency (DARPA) and a Senior Scientist at the Naval Research Laboratory. At DARPA, he conceived and initiated many projects on functional materials that pushed the frontiers of materials science for electronics including the spintronics memory project, the quantum information project (QuIST), and the frequency agile materials for electronics (FAME) project. At the University of Virginia, he is continuing to push the frontiers in spintronics and quantum information science. His group utilizes the spin degree of freedom in novel oxide heterostructures that will utilize spin torgue and electric fields to manipulate the magnetism in nanomagnetic heterostructures. He is also contributing to the development of a new spintronic logic structure based on controlling the magnetism in coupled magnetic nanodots. He was a Research Associate at Case Western Reserve University (1970–1973) and a Visiting Scholar at the University of California at Los Angeles (1981–1982). He has authored or coauthored two books, over 300 articles, and has edited numerous conference proceedings.

Dr. Wolf is a Fellow of the American Physical Society (APS, 1984), and was a Divisional Councilor for the Condensed Matter Division (1990–1991) and for the Forum on Industrial and Applied Physics (1993–1996).

Jiwei Lu received the B.E. and M.E. degrees in materials science and engineering from Tsinghua University, Beijing, China, in 1999 and 2001, respectively, and the Ph.D. degree in materials science from the University of California, Santa Barbara, in 2006.

He is currently a Research Assistant Professor at the Department of Materials Science and Engineering, University of Virginia, Charlottesville. His research is in the development of novel materials and structures which can be utilized as nonvolatile memory, reconfigurable logic, and very sensitive magnetic sensors. His graduate research was centered on structure–property relationships of electric field tunable dielectric thin films, including strontium titanate and bismuth zinc niobate pyrochlores for microwave applications.

Dr. Lu is a member of the American Physics Society and the Materials Research Society.

Mircea R. Stan (Senior Member, IEEE) received the diploma in electronics and communications from the Politechnica University, Bucharest, Romania, in 1984 and the M.S. and Ph.D. degrees in electrical and computer engineering from the University of Massachusetts at Amherst, Amherst, in 1994 and 1996, respectively.

Since 1996, he has been with the Charles L. Brown Department of Electrical and Computer Engineering, University of Virginia, Charlottesville, where he is now a Professor. He is teaching and doing research in the areas of high-performance and low-power very large scale integration (VLSI), temperature-aware circuits and architecture, embedded systems, and nanoelectronics. He has more than eight years of industrial experience, was a visiting scholar at the University of California at Berkeley, in 2004–2005, a visiting faculty member with IBM in 2000, and with Intel in 2002 and 1999.

Dr. Stan received the National Science Foundation (NSF) CAREER Award in 1997 and was coauthor on Best Paper Awards at the 2008 International Symposium on Quality Electronic Design (ISQED), the 2006 Great Lakes Symposium on Very Large Scale Integration (GLSVLSI), the 2003 International Symposium on Computer Architecture (ISCA), and Workshop on Self-Healing, Adaptive, and self-MANaged Systems (SHAMAN) 2002. He was the Chair of the VLSI Systems and Applications Technical Committee (VSA-TC) of the IEEE Circuits and Systems (CAS) Society for 2006–2007, the General Chair for the 2006 International Symposium on Low Power Electronics and Design (ISLPED) and for the 2004 GLSVLSI, the Technical Program Chair for the 2007 International ICST Conference on Nano-Networks (NanoNets) and the 2005 ISLPED, on technical committees for numerous conferences, and an Associate Editor for the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I from 2004 to 2007 and for the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS from 2001 to 2003. He also was a distinguished lecturer for the IEEE Solid-State Circuits Society (SSCS) from 2007 to 2008, and for the IEEE CAS Society from 2004 to 2005. He is a member of the Association for Computing Machinery (ACM), the Institution of Engineering and Technology (IET), USENIX: The Advanced Computing Systems Assocation, Eta Kappa Nu, Phi Kappa Phi, and Sigma Xi.

Eugene Chen (Senior Member, IEEE) received the Ph.D. degree in physics from the University of Minnesota, Minneapolis, in 1992.

He is an Engineering Director at Grandis, Inc., Milpitas, CA, where he is the Principal Investigator of the U.S. Defense Advanced Research Projects Agency (DARPA) and the National Institute of Standards and Technology Advanced Technology Program (NIST-ATP) sponsored projects to develop spin transfer torque random access memory (STT-RAM) universal memory technology. Previously, he had worked on magnetoresistive random access memory (MRAM) technologies at Cypress Semiconductor, Motorola, and NVE Corporation. He has achieved 53 issued U.S. patents and 28 published papers on MRAM, sensor, magnetic material, device, and processing technologies.

Daryl M. Treger received the B.S. degree in chemical engineering from the University of Buffalo, Buffalo, NY.

He is a Program Manager and a member of the technical staff at Strategic Analysis, Inc., Farmington Hills, MI. He performs analytical and engineering work for the U.S. Defense Advanced Research Projects Agency (DARPA) Defense Science Office (DSO) and Microelectronics Technology Office (MTO). He is involved in programs including those in spintronics, nonvolatile magnetic memory, multiferroic and magnetoelectronics, low-frequency uncooled magnetic sensors, frequency tunable materials and devices, thermoelectric materials, and superconductivity.