Letters

Suppression of Row Hammer Effect by Doping Profile Modification in Saddle-Fin Array Devices for Sub-30-nm DRAM Technology

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***Abstract*—The row hammer effect has become a reliability issue that cannot be ignored in sub-30-nm dynamic random-access memory (DRAM) products because of the narrow isolation spacing between the array devices. Improving the row hammer effect via fabrication process optimization is first proposed in this paper. An additional phosphorus (P) implantation with energy and dosage modification applied in the common source area between two adjacent buried word lines of the access devices and energy adjustment of the well implantation are applied to provide a doping profile modification in the array device. With the proper implantation setting of the high energy and 2X dosage in the additional P implantation, a localized shielding effect from the electric field by a depletion effect could be used to reduce the chances of hammering gate-induced electrons in the channel leaking to the adjacent access device. This proposed mechanism could be supported by the experimental results of the doping profile. Therefore, the row hammer effect can be suppressed by up to 30% in normalized fail bit counts. This proposed methodology could be used in future generations to suppress the row hammer effect in DRAMs.**

***Index Terms*—Row hammer, implantation, DRAM.**

I. Introduction

Scaling down the access device is one of the driving forces in DRAM technology to provide higher data storage ability in the same size memory chip by increasing the device density. Conventional plenary access devices cannot be used in sub-50 nm technology nodes in DRAMs because of the unacceptable leakage from the short channel effect (SCE) [1], [2]. To minimize the leakage issues, a three-dimensional (3D) device structure of a recess channel with an extended distance between source and drain is presented [3], [4]. To maintain the current drivability, a fin-curved gate area, which is called a saddle-fin (S-Fin) device, is further designed in the recess channel [5], [6]. Even a buried word line (WL) of the access device is proposed to provide a smaller step height difference for better yield of cell capacity during fabrication [7]. Meanwhile, the unit area of the DRAM cell is also shrinking from 6 F^2 to 4 F^2, which provides a smaller spacing between access devices and a stronger coupling effect between neighboring transistors and word lines [8], [9]. As mentioned in previous studies, a coupling effect could introduce an electromagnetic coupling force between cells and increase the sub-threshold leakage current [10], [11]. This behavior of the increase of leakage in the access devices of adjacent rows (victim rows) by frequent activation on a given row is called row hammering [12]. The worsening of device operation failures by a row hammer effect could be because of access frequency and refresh interval [12]. To our knowledge, previous studies related to the row hammer effect have mainly focused on DRAM testing flow optimization [11], [12]. No improvement to the row hammer effect via fabrication process modification has been presented to date. In this study, the doping profile of the access device, optimized by additional phosphorus implantation and well implantation in 3× nm DRAM technology node to suppress the row hammer effect, is presented. A new mechanism for suppressing the row hammer effect is also proposed with the support of a scanning spreading resistance microscope (SSRM) and technology computer aided design (TCAD) simulation data.

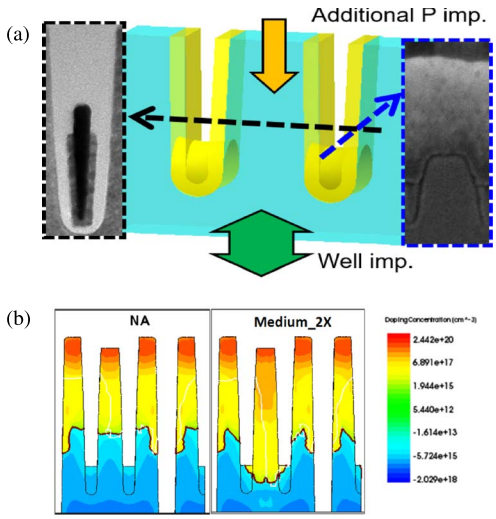

Fig. 1. (a) Schematic representation and TEM cross sections of the X- and Y-axes of the S-Fin device. The fin height for the channel width and the recess channel for the channel length of the S-Fin device are shown in the TEM image of the X- and Y-axes. (b) TCAD simulation for the doping profile of the access device without and with additional P implantation of high energy and 2X dosage.

II. Experiments

Fig. 1 shows a 3D schematic representation of the S-Fin device in the 3×-nm DRAM technology processed at Inotera Memory Inc., Taiwan. As shown in the inset of Fig. 1, the saddle shape of the array device channel and the recess channel are responsible for a relatively large channel width for a high drive current and a relatively large channel length for a decreased number of SCEs, respectively. The critical dimensions of the active area, the recess channel, and the gate area are all defined using ArF immersion photolithography. After the

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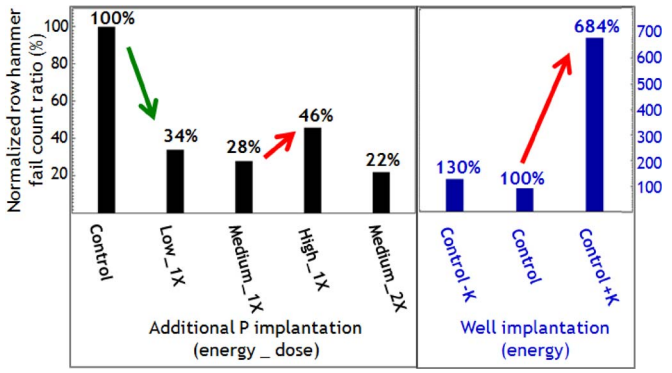

Fig. 2. Normalized fail bit counts of standard row hammer test in wafers without and with different conditions of (a) additional P implantation and (b) well implantation of 3× nm DRAM technology. The row hammer fail bit count can be reduced more by the energy of additional P implantation than by dosage. The behavior of the row hammer effect impacted by the energy of well implantation supports the blocking effect of the depletion junction.

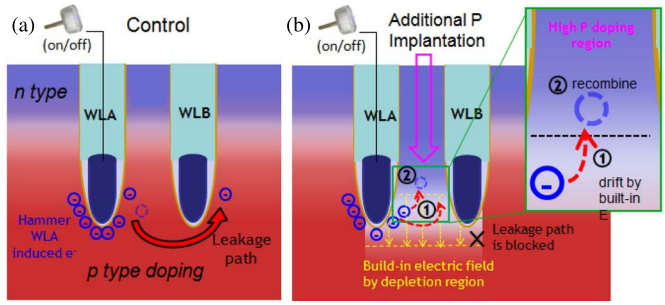

Fig. 3. Hypothesis for the improvement of the row hammer effect in a recess channel device with additional P implantation. (a) WLA is hammered frequently; electrons generated by the on–off interval could be attracted toward WLB (adjacent WL) by the high potential level. (b) With additional P implantation, the depletion region goes to down side with a built-in electrical field, which could make induced electrons from WLA drift to the common bit line and then recombine in a very short period. The original leakage path could be blocked, producing a reduced row hammer effect.

processes of shallow trench isolation, a silicon active area is formed. After the recess channel patterning and etching, the gate oxide is grown using low-pressure wet oxidation. The energy of the well implantation is adjusted with +/− K eV compared to the control sample. After well and S/D implantation, the experimental condition, i.e., an additional P implantation through the epitaxial silicon layer only in the area between adjacent word lines that are defined by an additional mask, is implemented, with different energies of low, medium, and high levels and different dosages of 1X and 2X. The P doping profile in the S/D area of the silicon bulk is verified by the TCAD simulation, as shown in Fig. 1(b). The gate-stack structure with poly-Si, TiN, WN, and W layers is fabricated as the buried word line. Based on the simulation results in Fig. 1(b), it is clearly observed that junction depletion moves to the deeper Si area after the additional P implantation. This location is close to the high electric field in the bottom corner of the buried word line. The stacked cell capacitance with a high-dielectric insulator is fabricated on the bottom TiN conductive electrode. After all processes are completed, the experimental wafers are tested for the row hammer fail bit counts with 4-Gbit chips using a standard wafer-level test program and electrical characterization on a test element group of 30 array transistors connected in parallel. To confirm the effective doping profile of the S-Fin device, product wafers from both the control and experimental groups were sliced for investigation by SSRM with a resolution of 1 nm.

III. Results and Discussion

Fig. 2(a) presents normalized fail bit counts of row hammer testing for wafers without and with different energy and dosage of additional P implantation. With an increase in energy from the low to the medium level, the normalized fail bit count can be further reduced to 28%. However, the normalized fail bit count in the group with high energy is increased to 46% of the control group. This could be from the doping profile that is already outside the coupling area or from the leakage path. With double dosage (2X) of P implantation in the medium energy level, the row hammer fail bit count can have an additional reduction of 6%. The lowest normalized fail bit count that can be achieved is only 22% of the control group. To determine the mechanism of row hammer improvements more precisely, the energy of the well implantation is also adjusted to investigate the row hammer effect. As shown in Fig. 2(b), the energy of well implantation is modified with control −K and control +K eV from the control group, respectively. In the −K and +K groups, the normalized fail bit count is increased to 130% and 684%, respectively, compared to the control group. The behavior of energy modification of both the additional P implantation and both well implantation on the row hammer effect could be concluded to be the effect of the PN junction. With proper energy of the additional P implantation and well implantation, both the depletion width and location help the blocking of the leakage path. In other words, the depth and width of the junction depletion play an important role in suppressing the row hammer effect. A higher dosage of additional P implantation could lead to fewer induced electrons and a slightly wider depletion width of the p-type layer formed by well implantation, which would result in fewer induced carriers and less of a leakage path by a better blocking effect from the depletion width. Both factors could help suppress the row hammer effect. To confirm this, an effective resistance check on the cross section of the access device from the wafer without and with additional P implantation is investigated. The junction depth is approximately 10 nm deeper in the wafer with additional P implantation, as measured by the distance between the point of the highest resistance and the point of lowest resistance at the metal-Si interface. Further, no clear difference occurs in the drain-to-source current versus gate-to-source voltage (Ids-Vgs) curve of the access devices in key tests between wafers without and with additional P implantation. The threshold voltage (V_T), subthreshold swing (SS), drive current (Ids) and retention fail bit counts are almost comparable in static data of the experimental wafers.

The mechanism of the row hammer effect could be due to frequently induced electrons in WLA that then leak to WLB to disturb the storage state, as shown in Fig. 3(a). As shown in Fig. 3(b), with a deeper and heavier junction because of the additional P implantation of medium energy, less charge can be generated by the frequently active word line. Further, induced electrons could easily drift to a common bit line by and then recombine in the high n-type doping area. The leakage path to WLB is blocked by the built-in electric field of this depletion area.

IV. Conclusion

The row hammer effect is a notable reliability issue for the current DRAM products and their future generations. A process methodology and its working mechanism are proposed to suppress the row hammer effect. A 78% reduction of the row hammer fail bit count is achieved by this proposed additional P implantation process and junction depth optimization. Based on this concept, more robust access devices with immunity to the row hammer effect could be fabricated in the sub 3×-nm DRAM technology node.

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