Engineering Science and Technology, an International Journal 19 (2016) 1503–1513

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Engineering Science and Technology, an International Journal

journal homepage: www.elsevier.com/locate/jestch

Review

Spintronics: A contemporary review of emerging electronics devices

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ARTICLE INFO

Article history:
Received 19 August 2015
Revised 2 May 2016
Accepted 2 May 2016
Available online 20 May 2016

Keywords:
Spin valve
GMR
MTJ
FTJ
Spin-FET
Spin-MOSFET

ABSTRACT

Spintronics is a new field of research exploiting the influence of electron spin on the electrical conduction (or current is spin dependent). The major problem is the realization and fabrication of spintronics based devices. To meet the objective scientific community is developing the novel kind of materials that relies on magnetism instead of flow of current through electron. This paper illustrates and reviews one of the emerging technologies known as spintronics by putting few low power computing techniques altogether based on spintronics to provide a basic and meaningful understanding to the reader. The challenges of spintronics devices that has to meet for the success of electronics future are summarized.

Contents

1. Introduction

As the channel length is keep on reducing, downsizing the channel length has become a major concern [1]. The expected gate length in future is 5 nm, because of that, off leakage current will be too high for the entire chip (ITRS map 2008) [2]. However, there are various techniques to reduce the off chip power in which double gate-metal oxide semiconductor field effect transistor (DG-MOSFET), fin-field effect transistor (fin-FET) and Si-nanowire MOSFET are the most promising one [3]. Dual material surrounding gate (DMSG) MOSFET is also another approach to improve the carrier transport efficiency and reduce the short channel effects by employing gate material engineering [4]. Carbon nanotube field effect transistor (CNTFET) is another feasible nanodevice similar

http://dx.doi.org/10.1016/j.jestch.2016.05.002
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in structure and successor of complementary metal oxide semiconductor (CMOS) technology. It has higher performance, transconductance and lower power consumption etc. than conventional CMOS technology. A lot of logics have been developed using these methods [5]. The problem with all above mentioned logics are volatility. Spin logics are the emerging one, which improves the battery life by consuming less power from portable devices to large data centers [6] and are non-volatile in nature.

Two diversified field of low power spintronics technologies are the active and passive devices. Here, few low power spintronics technologies of active devices like spin valve, giant magneto resistance (GMR), magnetic tunnel junction (MTJ), ferroelectric tunnel junction (FTJ) and domain wall (DW) in magnetic nanowires have been discussed. The other two domains of technologies under passive devices are monolithic and hybrid technologies. In monolithic spintronics the data storage and data communication is done by spin only (for example single spin logic (SSL)). SSL is a novel type of computer technology proposed in 1994 and popular due to bistable spin states of the electrons in quantum dots. This technology forms the SSL using quantum dots, magnetic field and electrons altogether. To understand the monolithic technologies one example of SSL, a universal logic NAND gate and its realization is discussed. In hybrid spintronics the data storage and data communication is done by charge only (either electron or hole), but its effect is augmented by the presence of spin. Spin plays a secondary role and influences how charge stores or manipulate information [7]. It has been shown in the literature that hybrid spintronics do not really show the significant advantages over the traditional bipolar junction transistor (BJT) or MOSFET based transistor [8]. The reason for that, the logic '0' or logic '1' is still decided whether the transistor is on or off. If the current flows from drain (D) to source (S) logic '1', or if no current logic '0' will be considered. To understand the hybrid technologies, an example of theoretically developed spin-FET and spin-MOSFET is addressed. In spin-MOSFET, graphene is used due to its low spin orbit interaction in the channel region which has shown interesting effects on conventional electronics. It has opened the way of "beyond CMOS" to develop the spin only logic circuits. These circuits consume less power than conventional CMOS.

Spintronics is one of the emerging technology which has extended the Moore's law and industry is trying to put more than Moore. Any technology can replace the current world of electronics if it reduces any one of the very large scale integration (VLSI) cost functions like area, power consumption and speed etc. Fortunately, spintronics can reduce heat dissipation significantly. In charge based device to switch from logic '0' to logic '1' the magnitude of the charge must be changed in the active region of the device due to which current flows from S to D. It is not possible with charge based electronics to reduce the power (or heat) dissipation, since charge is a scalar quantity and the presence or absence of charge gives logic '1' or logic '0'.

Spin unlike charge is a pseudo vector quantity which has a fixed magnitude of $h/4\pi$ with a variable polarization. If an electron is placed in magnetic field it can have more than two states but in digital only two bits 0 and 1 can be encoded, rest all cases are not required here and only these two states will have eigen states. These states can be achieved with a polarization parallel and antiparallel to the field which encode logic 1 and logic 0 respectively. In that case switching is accomplished by flipping the polarization of spin without any change in flow of current as that was the case in hybrid spintronics. This may result in significant energy saving. However, there is still some energy dissipated in flipping the spin but it will be of the order of $g\mu_B B$, where g is Lande factor, μ_B is the Bohr magnetron and B is the magnetic field required to keep the spin polarization bistable. The term $g\mu_B B$ can be reduced by lowering B, but it may cause more random bit flips. However, bit flip errors can be handled up to an extent by error correcting codes up to a certain extent [9,10].

To understand the charge particle behavior in metal, first I would like to discuss the relation between energy and density of states of metal. The spin polarization has been calculated theoretically by the below given relation [7,11,12],

$$P_n = \frac{n_\uparrow - n_\downarrow}{n_\uparrow + n_\downarrow} \tag{1}$$

If $n_\downarrow = 0$; $P_n = 1$ in this case only majority spins are there and the spin polarization is 100%. Such materials are known as ferromagnetic half metals or heusler alloys with 100% spin polarization. Heusler alloys (or half metals) are ferromagnetic metal alloys based on a heusler phase [13]. One example of half metals is strontium doped lanthanum manganate (LSMO), well known for its colossal magneto resistive behavior and has 100% spin polarization at low temperature (0 K), but it is difficult to achieve 100% spin polarization for spintronics devices and a lot of argument are there in the literature [14]. LSMO materials also show a sharp transition from metal to insulator at transition temperature. If $n_\uparrow = 0$; $P_n = -1$, if $n_\uparrow = n_\downarrow$; $P_n = 0$ (only for paramagnetic or normal metal). These three cases has been shown in Fig. 1, using Stoner-Wohlfarth (SW) model of ferromagnet [15,16]. Later people used this simplest SW model and did further modification to understand the physics of magnetization of digital magnetic storage like floppies, hard disk and magnetic tapes. The E-K diagram has been shown in Fig. 2. The up (↑) and down (↓) spins related energy is calculated by the Eq. (2) or (3) [7],

$$E_\uparrow = \frac{h^2}{4\pi^2 m_0} K^2 \tag{2}$$

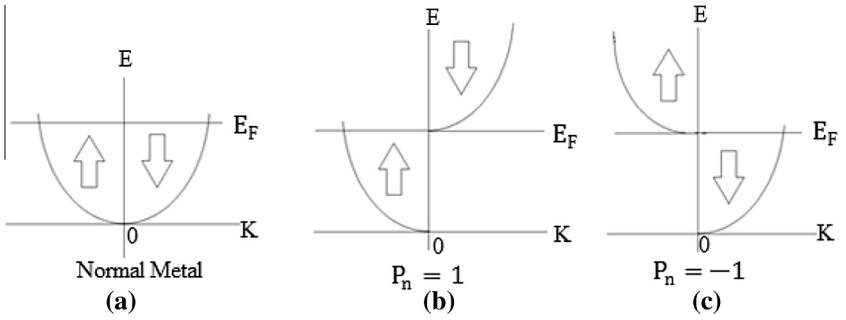


Fig. 1. Energy level (E-K) diagram using SW model (a) In normal metal both up spin and down spin are equal (b) if $n_\downarrow = 0$, and $n_\uparrow$ is 100% spin polarized has $P_n = 1$ (c) here $n_\uparrow = 0$, and $n_\downarrow$ is 100% spin polarized has $P_n = -1$ [11,12].

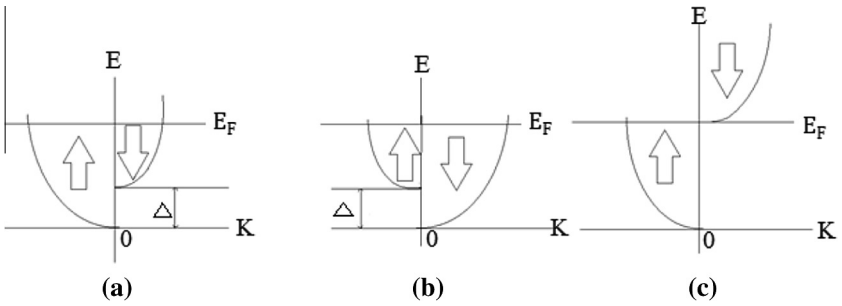


Fig. 2. (a) and (b) contains both up (↑) and down (↓) spin while fig. (c) represents E-K diagram for half metallic ferromagnet at absolute 0 K. Here, below E_F only the energy levels with up (↑) spin are occupied while above E_F all the energy levels are occupied with down spin (↓) only [7,12].

$$E_{\downarrow} = \frac{h^2}{4\pi^2 m_0} K^2 + \Delta. \quad (3)$$

Here Δ denotes shift in either of the energy level of up (↑) or down (↓) spins. In all the above mentioned cases the fermi level is above the bottom of both the sub bands, but in case if it is well below the bottom of both the sub bands then Boltzmann statistics can be replaced by the Fermi–Dirac (FD) statistics.

Another young emerging area of spintronics is organic spintronics, which is in great progress, both experiment and theory [17,18]. Organic spintronics is the area of research in which organic electronics (developed based on organic materials) is combined with spintronics. The advantage of using organic materials is that they are cheap, light weight, chemically interactive, and mechanically flexible, while the addition of the concept of spintronics allows the non-volatility in device [17,18]. The discovery of organic spintronics is the outcome of an attempt to improve the efficiency of OLED [19]. OLED is well-known area of research and a lot of examples using these concepts has already been fabricated and are available in the market. Few examples of those are flat TV screen, mobile phone displays, bill boards and computer displays [20–23] etc. As the field of spintronics is still growing, this review cannot be the final word for spintronics based devices. Instead it is a comprehensive reference for those who like to explore more in this area of research. Here, I have categorized all the devices and tried to understand their structure and operation using fundamental physics.

2. Low power spintronics technologies

This section describes active, passive, OLED and organic spintronics based devices.

2.1. Active devices

In the Section 2.1, few spintronics technologies of active devices like spin valve, GMR, MTJ, FTJ, DW in magnetic nanowires has been discussed [7,24].

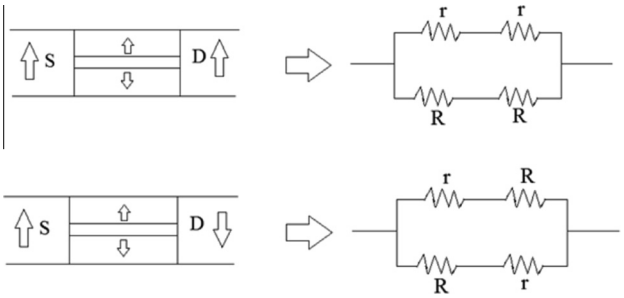


Fig. 4. Parallel and antiparallel spin valve using Mott's resistor model [30,32].

2.1.1. Spin valve

Spin valves were first developed in 1991 [25], later on it did a revolutionary change in the industry of magnetic sensor, read head of hard disks and magnetic random access memory (MRAM). Few articles in which spin valve is used to develop the magnetic sensor [26–28] and prototype magnetic read head of hard disks has been reported in literature timely [29]. The effect of GMR can be analyzed using a repetitive structure of spin valve in either current in plane (CIP) or current perpendicular to plane (CPP) form [7,24]. GMR has been discussed in the subsequent section. From the Fig. 3(a and b) if the S, D region is replaced with magnetic material and channel is replaced by non-magnetic material (or metallic like Cu) than the structure can be think of a spin valve as shown in Fig. 3(c). The structure can be built either horizontally or vertically. In the Fig. 3(c), I have represented the vertical structure (CIP geometry).

Generally spin valve structure consists of four layers. Free layer- the first sensing layer of ferromagnetic material at top. Spacer layer- the second layer of non-magnetic material which separates free and fixed layer. Pinned layer- the third layer of magnetic materials known as fixed layer. Exchange layer- the fourth layer of antiferromagnetic materials that fixes the magnetic orientation of pinned layer (Fig. 3(c)).

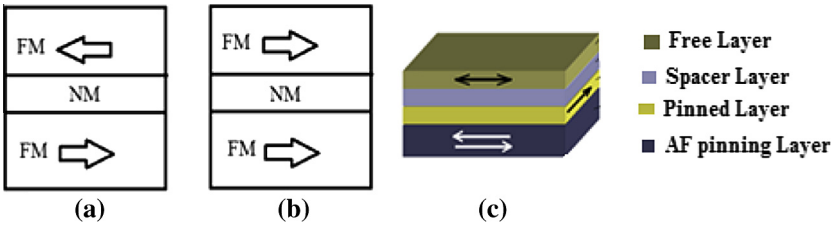


Fig. 3. (a) Represents antiparallel resistance while (b) represents parallel resistance. (c) Schematic of a simple 4 layer spin valve structure. Basic experimental fact is antiparallel resistance is always larger than parallel resistance [24].

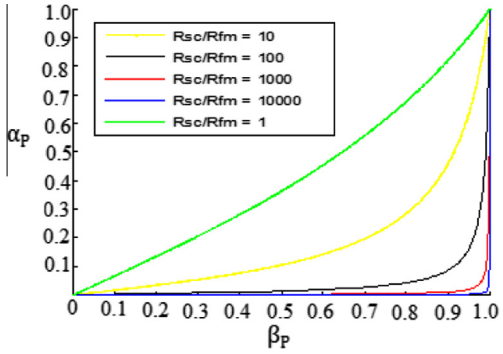


Fig. 5. Plot α_p vs β_p with $\left(\frac{R_{sc}}{R_{fm}}\right)$ variation from 1 to 10,000 [7,32].

Sir Neville Mott first presented a simple two current model to understand the spin valve operation [30,31]. It has been verified experimentally that there is a difference in resistance when the magnetizations are either parallel or antiparallel (Fig. 4). From Fig. 3, it is clear that a spin valve consists of two ferromagnetic layers (for example Co, Fe) separated by ultra-thin layer of non-magnetic material of size about 1 nm. A sufficient biased voltage is applied between the electrodes and the electron can tunnel through the non-magnetic region. Tunneling magnetoresistive (TMR) effect is a consequence of spin dependent tunneling. In spin valve the tunneling current depends on the relative orientation of magnetizations of the two magnetic layers which can be changed by applying the magnetic field. The effect by which electron tunnel through one end to another end is a quantum mechanical effect and is known as TMR effect. TMR is calculated by Eq. (4),

$$\text{TMR} = \frac{R_{AP} - R_P}{R_P},\ \text{here } R_{AP} = \frac{R+r}{2} \text{and } R_P \approx 2r \tag{4}$$

R, r is the resistance when channel and contact spin are in antiparallel and parallel direction respectively. Here R is more than r. Other useful factors are junction magneto resistance (JMR) and spin conductance ratio (SCR). JMR is same as that of TMR but calculated with respect to R_{AP}. These are defined as,

$$\text{JMR} = \frac{R_{AP} - R_P}{R_{AP}};\ \text{SCR} = \frac{G_P - G_{AP}}{G_P + G_{AP}} \tag{5}$$

A relation has been established by neglecting the effect of channel between spin polarizations conductivity in the ferromagnet (β_p) with polarization of the spin current (α_p) and is given by Eq. (1.5) mentioned in Appendix A [7,32]. A plot between α_p vs β_p has been drawn by varying, $\frac{\text{Resistance of ferromagnetic layer}}{\text{Resistance of semiconducting layer}}\left(\frac{R_{fm}}{R_{sc}}\right)$ ratio from 1 to 10,000 (Fig. 5). The following observations has been made from the graph,

(1) It is quite clear from the graph that α_p obtained its highest value 1, if the spin.
(2) polarization in the ferromagnet β_p is 100%, which shows half metals are the best spin injectors and detectors.
(3) In actual spin valve term $\left(\frac{R_{fm}}{R_{sc}}\right) \rightarrow 10^{-4}$, leading to very low spin polarization in semiconductor.
(4) But for significant spin in semiconductor, $\left(\frac{R_{fm}}{R_{sc}}\right) \approx 1$ is required i.e. $R_{fm} \approx R_{sc}$; but it seems difficult to achieve and known as a popular resistance mismatch problem.
(5) Another case if $R_{fm} \gg R_{sc}$; α_p approaches β_p but resistance of metal cannot be lesser than semiconductor.

Few more analysis has been made by considering the effect of the NM layer (paramagnetic layer), which was neglected above. NM layer plays a major role because all the mixing of the spin and spin relaxation happen here. A spin valve is again described by the resistor network model by considering the effect of channel. A relation for TMR has been established in appendix (A) and is given by Eq. (1.6). In the Eq. (1.7), $\text{MR} = \frac{R_{AP}-R_P}{R_P} = \left(\frac{\Delta R}{R_P}\right)$; is plotted with β_p for different values of $\frac{R_{sc}}{R_{fm}}$ from 1 to 1000 [7] (Fig. 6). From Eq. (1.7), $\text{MR} \propto \left(\frac{R_{fm}}{R_{sc}}\right)^2$, if $\frac{R_{fm}}{R_{sc}} \approx 10^{-4}$ and $\beta_p = 0.3$–0.5 as required for normal metallic ferromagnets (not for half metals); it will be impossible to detect MR in experiment due to the large difference in conductivities between non-magnetic semiconductor layers and metallic ferromagnetic contacts (because of $\frac{\Delta R}{R_P} \rightarrow$ very small), [7] (Fig. 6).

2.1.2. GMR

GMR is a quantum mechanical effect observed in thin film structures formed by alternating FM and NM layers. Fe/Cr or Co/Cu material can be used for making the GMR structure. When a magnetic field is applied, the thickness of NM layer is chosen such that there is a change in the direction of magnetization in another layer which reflects a huge change in resistance. That's why the effect is called GMR, a large change in electrical resistance in presence of a magnetic field [33–35]. Baibich et al. represented the GMR of Fe/Cr magnetic superlattices by varying the magnetic field, thickness of NM (Cr) layer and by varying the number of superlattice structure [34]. They reported a large change in resistance or resistivity by applying the small magnetic field as shown in Fig. 7, which has a wide application in designing MRAM memories and magnetic read heads, biosensor and MEMS device etc. A lot of

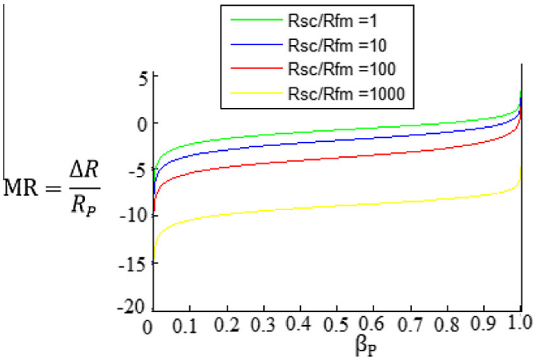


Fig. 6. $MR = \frac{\Delta R}{R_P}$ vs β_p for different values of $\left(\frac{R_{sc}}{R_{fm}}\right)$ from 1 to 1000. For the values on y axis the log of the base 10 has been taken [7,32].

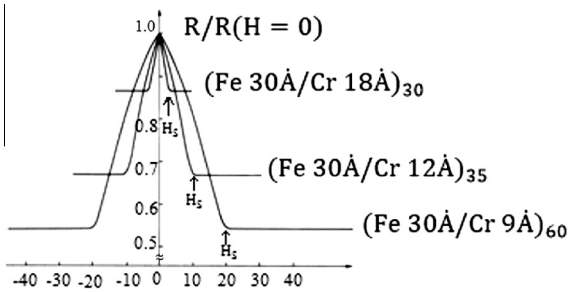


Fig. 7. Magnetic field dependent resistivity of three Fe, Cr superlattices at 4.2 K. The current and applied magnetic field are along the same [110] axis in CIP configuration as shown in below Fig. 9 (a). A sample of the work that led to the 2007 Nobel Prize [34].

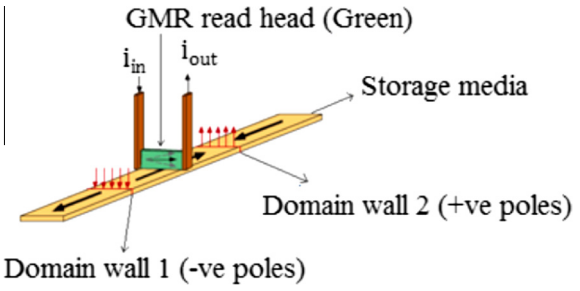


Fig. 8. A schematic representation of GMR read head that passes over the storage media [11].

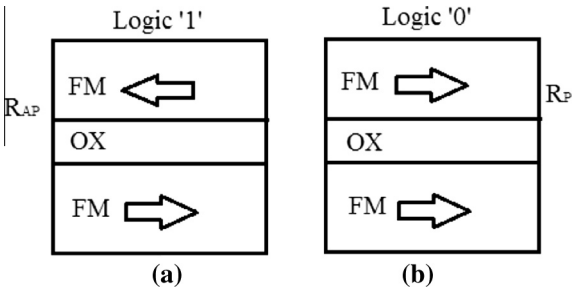


Fig. 10. Schematic of the MTJ nano-pillars. Here below layer is fixed while top layer is a free layer. An oxide layer of thickness ≈nm is sandwiched between FM layers. These structures may have CPP or CIP geometries [7,24,40].

experiments have been carried out using polarized neutron reflectometry (PNR) tool which clearly illustrates Fe/Cr superlattices that led to GMR effect [36] but PNR has some limitations also [37].

First magnetic sensor using GMR was released in 1994 [38], later IBM produced the first GMR read heads for reading data stored in magnetic hard disks [11,39]. The first GMR based RAM chips were produced by Honeywell in 1997. Today GMR based read heads are frequently used in laptops/computers, iPods, CD/DVD player and other portable devices. In 21st century, TMR based read heads began to displace GMR based read heads. MRAM chips based on TMR devices are now marketed by several companies, such as Freescale, SanDisk etc. The impact of GMR/TMR technology is rapidly growing and has now become a billion dollars industry.

A simple schematic representation of magnetic read head has been shown in Fig. 8. The logical value is stored as '0' or '1' in storage media and wherever these two regions meet a DW form (around 10–100 nm depending on the material used in the media). The uncompensated magnetic field generated in the vicinity of the DW may extend or enter into the media. When the two heads of the magnetic field meet uncompensated positive poles generated and extended out of the media while two tails of the magnetic field create −ve poles and magnetic field lines sink on it. Thus when GMR read head (Green color) passes over a positive and negative DW, magnetic field direction pushes up and down respectively as shown in Fig. 8. The measured resistance of GMR element thus increases for antialigned metal layers while decrease for aligned layers. The best design for GMR read head is one in which a small changes in magnetic field can give maximum rate of change in resistance or high GMR value. In GMR read heads, changes in resistance 1% per oersted has been observed [11].

The superlattice of GMR can be made of two ways, either in CPP [40] or in CIP geometry [24] (Fig. 9). The mechanisms of both CPP and CIP geometry are same. CPP is easy for theoretical calculation but difficult to realize experimentally due to very small thickness of NM (∼nm) layer as compare to FM (∼cm) layer. The resistance of multilayer in CPP geometry is extremely low and therefore sophisticated experimental techniques are required to measure, that's why CIP configuration is preferred over the CPP configuration.

2.1.3. MTJ

MTJ is a tunnel junction used for logic and memory applications, which combines magnetism, electronics and promises high read/write speed, non-volatility, infinite endurance [41] etc. MTJ nano-pillars are one of the important devices of spintronics. An MTJ nano-pillar consist of two ferromagnet separated by an ultra-thin layer of oxide (insulating layer of around nm) (Fig. 10). Here the NM (Cu or Cr) layer used in spin valve is replaced by a very thin barrier layer of oxide Al_2O_3 or Mgo. TMR for MTJ is also defined by the relative orientation of parallel resistance (R_p) and antiparallel (R_{AP}) resistance and is calculated from Eq. (4). For practical application one of the layers is pinned and known as the reference layer while other magnetic layer store a binary state based on the relative orientation of the two FM layers. In recent research TMR ratio was found more than 604% by using the MGO oxide barrier and this allows MTJ as excellent candidate for sensor design [42]. Today there are various ways to improve MTJ in which few are, perfect choice of material, scalability, energy efficiency, reliability, power consumption and area etc. A number of approaches like thermally assisted switching (TAS) and spin transfer torque (STT) are investigated but both of them either suffer the power or reliability issues. A compact model of MTJ switched by TAS and STT has been reported in literature [43]. This improves data reliability, power efficiency and performance etc. The advantage of MTJ is that it can be easily integrated with CMOS circuits. Based on hybrid combination of CMOS and MTJ, NV memory (magnetic flip-flop [44]) and NV logic have been developed [45].

2.1.4. FTJ

The concept of FTJ was proposed by Esaki early in 1971 [46] but the fabrication was achieved recently [47], because it is a challenging task to retain stable ferroelectric polarization on ultra-thin layer that is made of few unit cells. FTJ is a tunnel junction

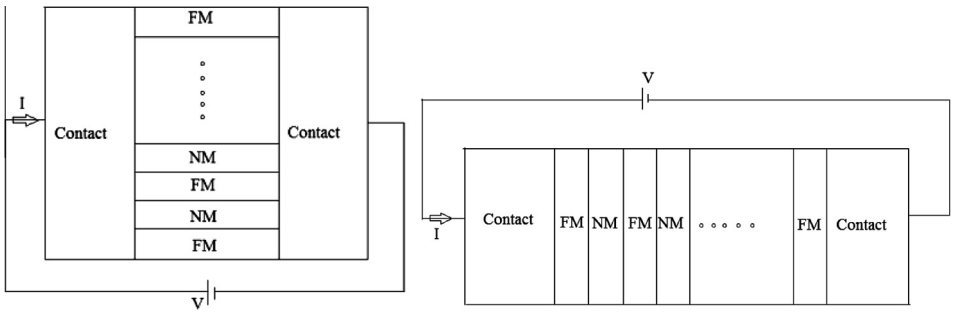


Fig. 9. (a) CIP geometry (b) CPP geometry [24,40].

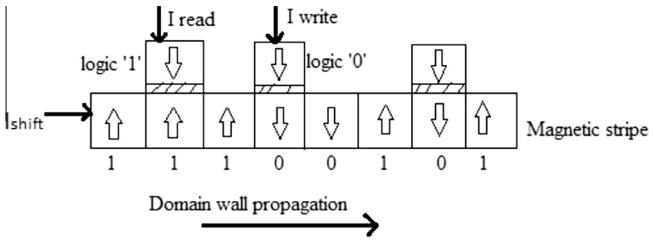


Fig. 11. Schematic of the current induced DW which has two write and read head MTJ0 and MTJ1 and one magnetic nanostripe. I_{write} injects the data in magnetic stripe using any of the method of the STT or TAS approach, I_{shift} induces DW motion along the magnetic stripe and I_{read} detects the magnetization direction through TMR effect [53].

composed of two different metal electrodes and an ultra-thin layer of ferroelectric sandwich between them. Due to the rapid progress in the nano-fabrication the critical thickness of ferroelectric thin film has been shrink to ~2 nm [48]. It is a voltage controlled device and the electrical resistance of FTJ strongly depends on the orientation of the electric polarization. When the electric field is applied across the thin ferroelectric layer, spontaneous ferroelectric polarization takes place that give rise to two logic states (high or low) with polarization pointing either up or down. Switching the ferroelectric polarization gives a change in tunnel resistance and this phenomenon is known as tunneling electro resistance (TER) (It is a ratio of high resistance to low resistance). An external voltage larger than threshold is required to switch polarization orientation of ferroelectric barrier. There are at least 3 mechanisms reported, which produce TER effect [49]. Wang et al. reported the first physics based compact model of FTJ nanopillar using Co/BTO (2 nm)/LSMO (30 nm) for memory and logic design [50]. FTJ has high OFF/ON resistance ratio, fast operation speed, low write power, non-destructive read out etc. FTJ has many advantages over MTJ [48,51] as given below.

(i) TER ratio is found ~100 at room temperature, while TMR ratio of MTJ is usually less than 4.
(ii) The write power and resistance area product for FTJ is $\sim 1 \times 10^4$ A/cm^{-2} and ~30 KΩμm^2 respectively, while for MTJ it is $>1 \times 10^6$ A/cm^{-2} and ~10Ωμm^2 respectively, allowing low power consumption.
(iii) The speed of writing is in nanoseconds that can enable it for high speed computation.

2.1.5. DW in magnetic nanowires

DW motion in magnetic nanowire has been used to develop various logic gates like NOT gate, AND gate and magnetic shift register [52] etc. The logic state is non-volatile and consumes zero standby power to keep the computing results. The major problem with these devices are their low operating speed (<100 kHz) and the generation of magnetic field with CMOS circuits. The Fig. 11 represents the current induced magnetic DW motion to generate the magnetic field [53]. It works on the basis of MTJ nanopillars of CoFeB/MgO/CoFeB as discussed above. A magnetic stripe of CoFeB is used to store the value of logic '0' and logic '1'. When the two fields are antiparallel, resistance is high and it reads logic '1', while, when two magnetic fields are parallel, resistance is low and it reads logic '0'.

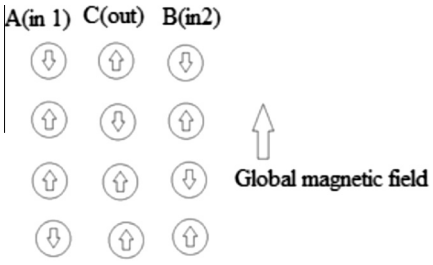
2.2. Passive devices

Here, I have discussed the two separate domains of spintronics, monolithic and hybrid spintronics. In monolithic spintronics only SSL, while in hybrid spintronics the charge carrier in addition with spin has been considered [7,24].

2.2.1. Monolithic spintronics (eg. SSL using 2 i/p NAND gate)

The SSL logic is made of by combining electrons, quantum dots and magnetic field. The SSL logic is popular due to the stable state of the spin of the electron. In this logic, current does not flow using charge while it flows using spin. Spin has both magnitude and polarization. The polarization can be made bistable by placing the electron in DC magnetic field, and then let the system relax to the thermodynamic ground state. The logic output C will set up to a polarization as that of NAND gate truth table. Here the switching of the device happens by flipping the state. So there is no power dissipation like I^2R as in case of conventional devices. To have an understanding of the SSL, I have taken example of 2 i/p NAND gate, by which any combinational or sequential logic can be implemented [7,54–56]. An estimate of energy dissipated during switching of this gate is only 21 kT which is small compared to nanoscale transistor. A nanoscale transistor dissipate about 40,000–50,000 kT during switching [57]. Any logic can be developed by placing the quantum dots in a 2D array and correct pin configuration of input and output. Many researchers have come up with logic gates like NAND gate [7,57], ALU [54], adders [58] etc. and a joint collaboration of universities is trying to come up with SSL based processors in future [59].

2.2.1.1. Single spin boolean logic of 2 i/p NAND gate. Consider a linear array of 3 electrons A, B and C containing the quantum dots. From Fig. 12, wave functions of nearest neighbor A and C, B and C overlap and they will have exchange interaction coupling. Here A (in1), B (in2) are two inputs and C (out) is the output spin of the NAND gate. Polarization parallel to the magnetic field corresponds to logic '1' and antiparallel to magnetic field comprises logic '0'. When the spin polarizations of the input A and B are made to confirm the desired bit inputs and the system is allowed to relax to the ground state, the spin polarizations in C always represent the output. The input signal can travel to different node using clock pad. The advantage of using this interaction is unidirectional transmission of the signal which makes the structure pipelined to achieve the high speed with a cost of clock latency. To read and write the input



A(in1)	C (out)	B (in2)
0	1	0
1	0	1
1	1	0
0	1	1

Fig. 12. An array of 3 spin polarized single electrons, each housed in a quantum dot, realizes the NAND gate when the entire array is placed in a static magnetic field and allowed to relax to the thermodynamic ground state [7,55,60].

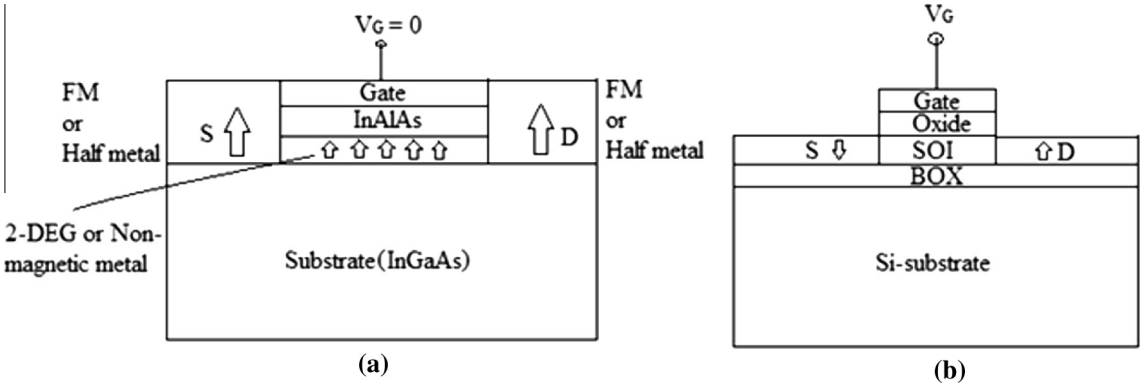


Fig. 13. Schematic representation of Spin-FET and Spin-MOSFET (a) the arrow indicates the direction of magnetization of the S and D contacts. V_G is the gate voltage. When V_G is zero the injected spins which are transmitted through the 2-DEG layer reach at the collector with the same polarization. When $V_G >> 0$ the precession of the electrons is controlled with electric filed (b) here S, D region have opposite direction of magnetization and does not require spin precession of spin polarized electrons in the channel [7,53,61].

and output pin various methods are used in which one of them is, spin polarized scanning tunneling microscope (SPSTM) [7,55,60].

2.2.2. Hybrid spintronics (spin-FET and spin-MOSFET)

Datta Das proposed the first spin polarized transistor known as spin-FET in 1990 using the concept of spin transistor [61]. It is also known as electro optic modulator. The first Datta Das spin-FET is not yet fabricated completely, but theoretically proven and has one of the most advanced application of spintronics technology. Later wide variety of spin transistor based on various operating principles have been reported. Spin transistor has been designed with same analogy of conventional MOSFET, which consists mainly three terminals (excluding bulk); S, D regions and channel between them is controlled by the gate. A schematic of spin-FET has been shown in Fig. 13(a). In these devices channel is made of non-magnetic layer (or 2 dimensional electron system with strong spin orbit interaction) which is used for transmitting the spin polarized electrons from S to D.

The spin tranjection in the channel plays a crucial role. Initially the device is ON, while by applying electric field through gate, strong Rashba spin orbit interaction is set up and spin precesses around the magnetic field. The spin of every electron precesses by the same amount. The angel of precession is given by $\varnothing \propto m^* E_y L$; where m^* the effective mass of electron, E_y vertical component of applied electric field and L is the channel length. When applied gate voltage is $V_G = 0$, the spins do not precess ($E_y = 0$; $\varnothing = 0$) so that every electron arriving at the D has its spin polarized parallel to the D magnetization. Thus a maximum I_{ds} (D to S current) or high conductance (G_{on}) is achieved. This analogy is same as a constructive interference between the waves with phase of $\varnothing = 2n\pi$ (here n is an integer from 0, 1, 2...).

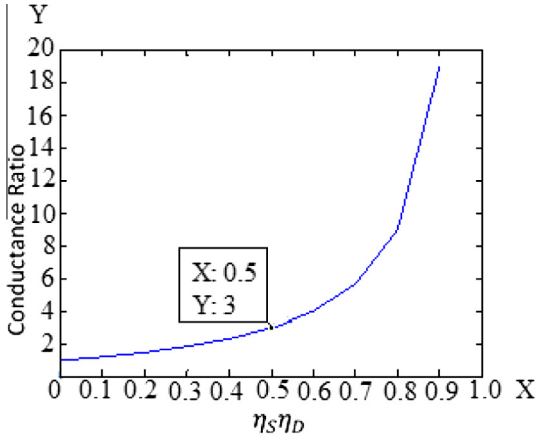


Fig. 14. Conductance ratio vs ($\eta_S\eta_D$), If $\eta_S = \eta_D = 70\%$ [60], conductance ratio ≈3 [7].

A electron can be assumed as a particle with spin ↑ or ↓. When V_G is applied, it causes Rashba spin–orbit interaction in the channel (Fig. 13a). It is given by $B_{Rashba} \propto E_y v_x \hat{z}$; here electrons are moving in x direction with velocity v_x and E_y is the vertical component of applied gate electric field along y axis. The direction of B_{Rashba} (spin independent magnetic field) is along z direction. As the electron travels to D the Larmor precession is in the X–Y plane and the Larmor frequency is given by [7,61],

$$\frac{d\varnothing}{dt} = \omega(\text{Larmor frequency}) \propto m^* E_y v_x \tag{6}$$

While spatial rate of spin precession is given by $\frac{d\varnothing}{dx} \propto m^* E_y$. Spatial rate of spin precession depends on E_y but independent of carrier velocity. Spin of every electron precess by exactly the same angle as it travels from S to D. When $V_G \gg 0$; there is strong spin orbit interaction and I_{ds} (D to S current) ≈0 or low conductance (G_{off}) is achieved. This analogy is same as destructive interference of two waves of same frequency with phase $\varnothing = (2n + 1)\pi$ (here n is a integer from 0, 1, 2....). The ratio of ON to OFF conductance of this transistor is given by [61],

$$\frac{G_{on}}{G_{off}} = \frac{1 + \eta_S\eta_D}{1 - \eta_S\eta_D} \tag{7}$$

Here η_S is the spin injection efficiency at the S and η_D is the spin detection efficiency at the D. The conductance ratio obtained from Eq. (7) for $\eta_S = \eta_D = 70\%$ is ≈3 which is quite small (Fig. 14). It means that the leakage current in the OFF state is very huge. It is at least one third of ON current, if the spin injection/detection efficiencies are 70%, 90% at room temperature [62] and low temperature [63] respectively. Much effort is going on to improve the spin injection and detection efficiency for ferromagnet/paramagnet interfaces [64]. To achieve a higher conductance ratio of order $\approx 10^5$, the spin injection and detection efficiency have $La_{0.7}Sr_{0.3}MnO_3$ to be 99.9995% [7]. Another major problem with spin-FET is the conductivity mismatch between the S/D and transmitting layer. The problem of conductivity mismatch may be solved to a certain extent using heusler alloys (or half metals) in S/D region and a semimetallic heusler alloy as the transmitting layer but it is difficult to achieve experimentally.

Spin-MOSFET requires no spin precession of spin polarized electrons in the channel. So, a material of low spin orbit interaction can

be used in the channel region of spin-MOSFET as shown in Fig. 13 (b). One magical material developed recently that may be used for transport is single layer atom graphene which holds ultra-high mobility and very low spin orbit interaction [65,66]. By using both spin-FET and spin-MOSFET full spin computing systems can be realized to achieve ultra-low power operations.

2.3. OLED and organic spintronics

In OLED a large portion of electrons and holes form triplet spin states instead of singlet spin states, which limits the light emission efficiency. The first result in this field was published in 2002 in which the spin polarized electrons inject from colossal magnetoresistance manganite $La_{0.7}Sr_{0.3}MnO_3$ electrode into an organic compound layer of sexithienyl (T_6, a prototypical organic semiconductors (OSC)). The spin diffusion length of T_6 was about 200 nm at room temperature [19,67]. Later other group of people observed the spin valve effect in a hybrid inorganic–organic device [68]. A small variation in magnetic field produces the variation in the intrinsic resistance of OSC which is termed as organic magneto resistance (OMAR) [69]. These results confirmed the potential of OSC for spintronics. Tris(8-hydroxyquinoline)aluminium(III) abbreviated as Alq_3, is one of the organic material widely investigated for OLED and spintronics device application due to its high carrier mobility and have readily apparent functional properties [18,19]. A vertical structure of Co/Alq_3/LSMO known as organic spin valve was fabricated in 2004, where (Alq_3) layer of 100–200 nm was deposited as a spin transport OSC layer on $La_{0.7}Sr_{0.3}MnO_3$ substrate, covered by a 3.5 nm thick Co film on top. A sizeable OMAR of 40% was observed at 11 K temperature [68]. A variation was observed in OMAR using Alq_3 and other OSC layer with the same structure of type Co/Alq_3/LSMO [70,71].

The reason for this variation was due to interface property between FM electrode and OSC interface properties, which can be induced by material intrinsic properties, interface interactions and even different fabrication conditions [72]. The low spin orbital coupling and weak hyperfine structure contribute to long relaxation time in organic materials, which provide sufficient time to manipulate the logic [18,23]. Being the above mentioned advantages the OSC's have disadvantage of low mobility and complex transport properties. Even after that organic material is the obvious choice for spintronics devices [18,23]. There are some other factors such as paramagnetic impurities which may also induce spin scattering and cause change in spin relaxation time. Another issue is contacting the organic materials. The organic materials are fragile and special microelectronics technique is required for fabrication. Since spin injection and detection takes place at the interface between FM electrode and OSC, the quality of interface is also a crucial issue [17,18].

Spin valve is one of the most studied prototype device of organic spintronics based devices [17]. The architecture of organic

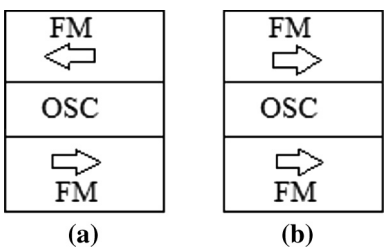


Fig. 15. Schematic representation of an organic spin valve. Two ferromagnetic (FM) contacts (magnetization denoted by arrows) are separated by organic semiconductor (OSC) layer. These FM contact may be made of organic or inorganic FM material [18].

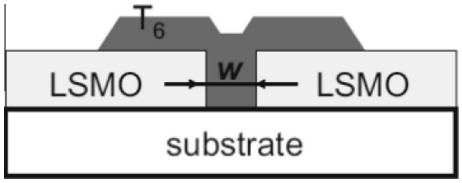


Fig. 16. Cross section view of hybrid LSMO/T6/LSMO junction where w is the separation between electrodes [67].

spintronics based spin valve is same as that of Fig. 3(c). It is made of two FM contacts act as spin injector and detector with different coercive fields are separated by a channel of organic material (Fig. 15). It is a hybrid spintronics device since inorganic (FM contacts) and organic (NM spacer) materials have been used to develop the device (Fig. 16). If the FM contacts are also made of organic materials then it is known as organic monolithic spintronics devices. A lot of hybrid spintronics devices in which FM contacts of inorganic material with organic active interlayers have been investigated, while a complete organic monolithic spintronics devices have not been realized so far [18,23].

3. Conclusion

This article deals with few low power technology of spintronics. All the techniques discussed in this article have been divided in active and passive devices category. Particularly, I addressed on spin valve (Two FM layers separated by NM layer of metal like Cu), their repeated extension (superlattice) known as GMR (alternating FM and NM layers), the two very popular structure of the tunnel junctions MTJ (two FM layer separated by thin insulating layer of oxide), FTJ (two different metal electrode separated by ultra-thin layer of ferroelectric), and DW in magnetic nanowires under the category of active devices. Non-volatility provided by spintronics technique has been used to develop the NV logic. Hybrid CMOS/MTJ, CMOS/FTJ, CMOS/DW are the few emerging techniques which has been used to develop the basic NV logic gates and NV memory etc. Passive spintronics covers specifically the monolithic and hybrid spintronics. In monolithic spintronics an example of SSL using 2 i/p NAND gate has been reviewed from literature. The SSL provide the least power dissipation, scalability and higher performances compare to conventional devices. The estimation of power observed shows a large difference between SSL logic and power dissipated in transistor based gates. The hybrid spintronics has covered the two important topics spin-FET and spin-MOSFET.

OLED is a well-known area and a lot more examples of fabricated OLED are in use since last ten years, while the first organic spintronics device has been reported in 1998, and from then onwards, there are still a number of issues to be tackled like ferromagnetic-organic interface, different microfabrication techniques than the conventional one, reliable contacts etc. Organic spintronics is a vast area of research where physics, chemistry and electronics engineering inevitably meet and hence a joint venture of learned and skilled people is required to overcome the above mentioned issues.

The realization of spintronics based devices is a challenging task and required precise techniques for fabrication. There is a lot of scope for many technology (discussed here) to improve and intense investigation is required to come up with more and more prototypes. To develop those prototype, a sound knowledge of material science and the physics behind it, is required. Some kind of modeling language (like Verilog-A) is required to get the behavior model of these prototypes, then integration of those models with CMOS technology is done using CAD tools. One of the tool

developed by the industry is Cadence which is user friendly and most of the CMOS/MTJ, CMOS/FTJ models have been verified using these techniques. However, engineers have come up with this idea already more than a decade, but still there is a large gap between theoretically predicted models by using different material (showing the improvement in characteristics like performance, power consumption etc.) and prototype models used by the industry. So intense and joint investigation of academia -industry is required to fill this gap.

Appendix A

A.1

Most of the equations are rederived from the book [7] to get the feel of the topics covered in this article. From Fig. 4, R is the resistance when channel and contact spin are in opposite direction, r is the resistance when the channel and contact spin are in parallel. Initially the channel effect has been neglected. The parallel resistance is given by $R_P = 2r \| 2R \approx 2r$ if $R \to \infty$, while the antiparallel resistance is $R_{AP} = (r+R) \| (R+r) \approx \frac{R+r}{2}$ (Fig. 4). It is an experimentally proven fact that antiparallel resistance (R_{AP}) will be more than parallel resistance (R_P). The value of the TMR has been calculated by Eq. (4).

$$\mathrm{TMR} = \left(\frac{R_{AP}}{R_P} - 1\right) = \frac{(r+R)^2}{2 \times 2Rr} - 1 = \frac{1}{1 - \left(\frac{R-r}{R+r}\right)^2} - 1 = \left(\frac{P^2}{1-P^2}\right) \tag{1.1}$$

Here $P = \frac{R-r}{R+r}$ is the polarization of the magnet, it also tells how effective the magnet is. The same calculation can be carried out for MTJ by replacing the non-magnetic channel (or paramagnetic material) with insulator but in that case TMR for MTJ is $\left(\frac{2P^2}{1-P^2}\right)$. From Drude's model of electrical conduction, $R = \rho l/A$; $\rho \propto 1/\sigma$ and $\rho \propto n$ for metal and semiconductor, here n is the electron density. Let $R_{fm\uparrow}$, $R_{fm\downarrow}$ are up spin and down spin resistance of the ferromagnetic metal, $R_{sc\uparrow}$ and are up spin and down spin resistance of paramagnetic semi conducting layer respectively, spin polarization conductivity (β_p) in the ferromagnet (by assuming the mobility of up spin, down spin electrons are equal) can be calculated from Eq. (1),

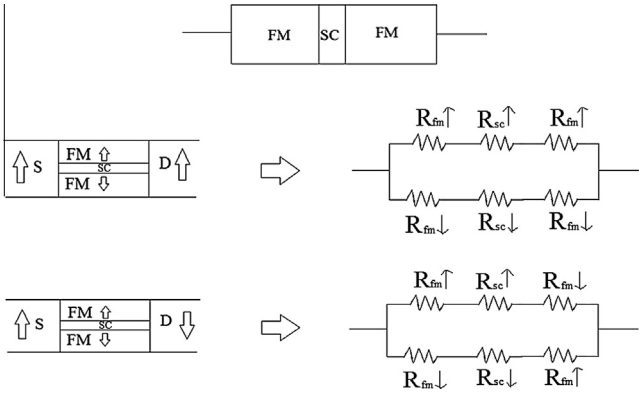


Fig. A1. Parallel and antiparallel spin valve by taking into account the non-magnetic layer between two ferromagnetic contacts [32]. The overall resistance for parallel configuration $R_p = \frac{(2R_{fm\uparrow}+2R_{sc})(2R_{fm\downarrow}+2R_{sc})}{2R_{fm\uparrow}+2R_{fm\downarrow}+4R_{sc}}$ and antiparallel configuration $R_{AP} = \frac{R_{fm\uparrow}+R_{fm\downarrow}+2R_{sc}}{2}$ is calculated by assuming $R_{sc\uparrow} = R_{sc\downarrow} = 2R_{sc}$ (since in paramagnetic semiconductor both up and down spins are equal in number, here $R_{sc} = \rho_{sc} l/A$; ρ_{sc} is the resistivity of the semiconductor, l is the separation between the contacts and A is the cross-sectional area of the contacts).

$$\beta_p = \frac{\sigma_\uparrow - \sigma_\downarrow}{\sigma_\uparrow + \sigma_\downarrow} \tag{1.2}$$

Another important factor is the spin current injection efficiency (α_p) [32] which can be written in terms of both up and down resistance of the channel (From Fig. A1, the antiparallel resistance of both the channel are equal and is given by $R_\uparrow = R_\downarrow = R_{fm\uparrow} + R_{sc\uparrow} + R_{fm\downarrow}$). The up spin and down spin resistance of the ferromagnetic metal can be rewrite in terms of β_p $R_{fm\uparrow} = \frac{2R_{fm}}{1+\beta_p}$ and $R_{fm\downarrow} = \frac{2R_{fm}}{1-\beta_p}$. If $R_\uparrow \propto 1/\sigma_\uparrow$, from Eq. (1.2),

$$\alpha_p = \frac{R_\downarrow - R_\uparrow}{R_\uparrow + R_\downarrow} \tag{1.3}$$

If $\beta_p = 100\%$; $R_{fm\downarrow} \to \infty$ which indicates the completeness of up spin and complete absence of down spin in the ferromagnet or half metallic ferromagnet (see the band diagram Fig. 1). If $\beta_p = 0\%$; $R_{fm\downarrow} = R_{fm\uparrow}$ means up and down spin are equal in number ($n_\uparrow = n_\downarrow$). So spin polarization $P_n = 0$ from Eq. (1), So ferromagnetic material will behave as normal metal or paramagnetic semiconductor. The value of α_p for antiparallel resistance is 0, while for parallel configuration (Fig. A1), $R_\uparrow = 2R_{fm\uparrow} + R_{sc\uparrow}$; $R_\downarrow = 2R_{fm\downarrow} + R_{sc\downarrow}$. Now α_p can be calculated for parallel configuration from Eq. (1.3) as,

$$\alpha_p = \frac{2(R_{fm\downarrow} - R_{fm\uparrow})}{2(R_{fm\uparrow} + R_{fm\downarrow}) + 4R_{sc}} \tag{1.4}$$

Now putting the values of $R_{fm\uparrow}$ and $R_{fm\downarrow}$ in Eq. (1.4),

$$\alpha_p = \beta_p \left(\frac{R_{fm}}{R_{sc}}\right) \frac{2}{[2\left(\frac{R_{fm}}{R_{sc}}\right) + (1-\beta_P^2)]} \tag{1.5}$$

Another useful factors TMR and MR are calculated from Eqs. (4) and (5),

$$\mathrm{The\ TMR} = \frac{R_{AP} - R_P}{R_P} = \frac{(R_{fm\uparrow} - R_{fm\downarrow})^2}{4(R_{fm\uparrow} + R_{sc})(R_{fm\downarrow} + R_{sc})}, \tag{1.6}$$

$$\mathrm{MR} = \frac{\Delta R}{R_P} = \left(\frac{\beta_P^2}{1-\beta_P^2}\right)\left(\frac{R_{fm}}{R_{sc}}\right)^2 \left[\frac{4}{4\left(\frac{R_{fm}}{R_{sc}}\right)^2 + 4\left(\frac{R_{fm}}{R_{sc}}\right) + (1-\beta_P^2)}\right] \tag{1.7}$$

A.2. code for Figs. 5, 6 and 14

Fig. 5, Plot α_p vs β_p for different values $\frac{R_{sc}}{R_{fm}}$ from 1 to 10,000.

```
x = [0:0.001:1];
y = [0:0.001:1];
u = [0:0.001:1];
v = [0:0.001:1];
p = [0:0.001:1];
q = [0:0.001:1];
r = [0:0.001:1];
s = [0:0.001:1];
w = [0:0.001:1];
z = [0:0.001:1];
y = (2*x)./(3-x.^2);
u = (2*v)./(12–10*v.^2);
p = (2*q)./(102–100*q.^2);
r = (2*s)./(1002–1000*s.^2);
w = (2*z)./(10,002–10,000*z.^2);
figure; hold on;
```

plot(x,y,'g'); plot (v,u,'y'); plot (q,p,'k'); plot (s,r,'r'); plot (z,w,'b')

Fig. 6, Plot $\mathrm{MR} = \frac{\Delta R}{R_P}$ vs β_p for different values of $\frac{R_{sc}}{R_{fm}}$ from 1 to 1000.

```
x = 0:0.0001:1;
v = x;
z = 0:0.0001:1;
p = 0:0.0001:1;
y = 4*(x.^2)./(9–10*(x.^2)+x.^4);
u = 4*(v.^2)./(144–244*(v.^2)+100*(v.^4));
w = 4*(z.^2)./(10,404–20,404*(z.^2)+10,000*(z.^4));
q = 4*(p.^2)./(1000004004–1001004004*(z.^2)+1,000,000*(z.
^4));
figure;
```

hold on; plot (x,log10(y), 'g'); plot (v,log10(u),'b'); plot (z,log10 (w),'r'); plot (p,log10(q),'y');

Fig. 14, Plot conductance ratio vs $(\eta_S \eta_D)$.

```
x = 0:0.1:1;
y = (1 + x)./(1-x);
plot(x,y);
```

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