INVITED PAPER

Spin-Transistor Electronics: An Overview and Outlook

Spin transistors are new devices that unite ordinary transistors with the functions of magnetoresistive devices to realize nonvolatile information storage and reconfigurable output characteristics.

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ABSTRACT | Spin transistors are a new concept device that unites an ordinary transistor with the useful functions of a spin (magnetoresistive) device. They are expected to be a building block for novel integrated circuits employing spin degrees of freedom. The interesting features of spin transistors are nonvolatile information storage and reconfigurable output characteristics: these are very useful and suitable functionalities for various new integrated circuit architectures that are inaccessible to ordinary transistor circuits. This article reviews the current status and outlook of spin transistors from the viewpoint of integrated circuit applications. The device structure, operating principle, performance, and features of various spin transistors are discussed. The fundamental and key phenomena/technologies for spin injection, transport, and manipulation in semiconductors and the integrated circuit applications of spin transistors to nonvolatile logic and reconfigurable logic are also described.

KEYWORDS | CMOS integrated circuits; half-metallic feromagnet; magnetoresistance; nonvolatile logic; power-gating architecture; programmable logic; spin transistor; spin transport; spintronics

I. INTRODUCTION

Dramatic progress in the present integrated electronics has been powered by the miniaturization of transistors and the high degree of device integration [1]–[3], since the size reduction and large-scale integration of transistors provide improvements in integrated circuit performance including reliability and production cost. Metal–oxide–semiconductor field-effect transistors (MOSFETs) and complementary MOS (CMOS) devices (hereafter, both are referred to as MOS devices) based on sophisticated Si technology are a fundamental building block for mainstream integrated circuits, and they play an essential role as "technology drivers" in the current electronics. This is, of course, due to the excellent scalability and integration ability of MOS devices. The rapid and continual progress in the scaled-down technology of MOS devices (that is, the so-called scaling) is known as Moore's law [4]–[6]. However, the scaling of preproduction MOS devices has already reached a physical limit of several nanometers [7], [8], indicating the end of scaling in the near future. In such extremely scaled-down devices, leakage currents induced by quantum mechanical phenomena, various parasitic elements, and variability in device characteristics give raise to serious performance degradation problems. In addition, the production cost including facility investment becomes huge. These mean that the effect of scaling weakens for nanometer-scale MOS devices. Therefore, scaling-independent technologies for improving device/circuit performance have attracted considerable attention.

In highly interconnected integrated circuits, the high current drivability of the transistors is very important for the circuit performance, since the circuit speed is dominated by charging/discharging of the load capacitance. Therefore, the operating speed and operating principle of the individual transistors hardly affect the circuit speed, as long as they exhibit high current drivability. In addition, the high current drivability is also indispensable for other performance indices of the integrated circuits, such as low (dynamic) power dissipation. From these viewpoints, a great deal of effort has been made to achieve much higher current drivability for MOS devices so far. Therefore, it has been explored that new channel structures, such as fin,

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nanowire, and other three-dimensional structures, and new channel materials with a high carrier mobility, such as strained Si, Ge, III-V compound semiconductors, and grapheme, are introduced into MOS devices [9]–[21]. An effect equivalent to scaling can be substantially achieved by introducing new channel structures/materials without scaling, which is sometimes called the "more Moore" approach or the "extended CMOS" concept [22]. It should be noted that the operating principle of extended CMOS devices is the same as that of ordinary MOS devices, although the channel structure and material of extended CMOS devices are replacing conventional ones.

Introduction of new functionality, such as quantum effects and spin-related phenomena, into integrated circuits is also expected to be an alternative approach instead of the scaling. By introducing new functionality, the transistor performance itself would not become superior to conventional MOS devices. However, there exists a possibility for improving the circuit performance by employing new circuit architectures based on newly added functionality. In order to achieve such new architectures, a new MOS device with the desired functionalities must be realized. One approach is a combination of a MOS device with a so-called functional device at the circuit level. In many cases, functional devices have no characteristics (in particular, high current drivability) suitable to integrated circuits, except for new functionalities. Therefore, they should be used in combination with MOS devices. For example, this approach was examined in quantum effect devices. A quantum effect transistor consisting of an ordinary field-effect transistor (FET) and a resonant tunnel device was demonstrated [23], [24].

Another approach is the device-level integration of a MOS device and a functional device with a hybrid structure. Several functional MOS devices that contain the structure of two-terminal functional devices in their device structure have been proposed so far, such as a Josephson junction [25], [26], a Esaki diode [27], a resonant tunnel device [28], [29] and a magnetic tunnel junction [30]–[32]. The important features of functional MOS devices, except for newly added functionalities, could be high current drivability and exponentially steep ON/OFF switching of MOS devices, which would be inaccessible to any other functional device. The paradigm shift from device scaling to the introduction of new functionalities to MOS devices could become an important route to future integrated electronics technology. Note that an electronic device based on new physical phenomena and/or new state variables is called a beyond-CMOS device, and new devices uniting a beyond-CMOS element with an ordinary MOS device are referred to as the "nonconventional extended CMOS" [22].

The aim of recently emerging spintronics (spin electronics) research is to manipulate spin degrees of freedom in solid state devices and provide new concepts for future electronics and photonics employing spin degrees of freedom [33]–[40]. One of the most attractive research directions is to control charge and spin transport phenomena in active electronic devices, i.e., spin transistors. Spin transistors are a new type of concept device that unites an ordinary transistor with the useful functions of a spin (magnetoresistive) device. The interesting features of spin transistors are nonvolatile information storage and reconfigurable output characteristics, which are very useful and suitable functionalities for future high-performance integrated circuit architectures such as nonvolatile logic (e.g., nonvolatile power-gating systems) and reconfigurable logic (e.g., nonvolatile field programmable gate arrays). Following the first proposal of the spin transistor concept by Datta and Das [41] and Johnson [42], [43], a wide variety of spin transistors based on various operating principles have been proposed so far.

In this article, we present the current status and outlook of spin transistors. After a brief review of the fundamental and key phenomena/technologies for spin transistors in Section II, the device structure, operating principle, and features of various spin transistors are described in Sections III, IV, and V, in which we focus on potential-effect spin transistors in the Section III and field-effect spin transistors in Sections IV and V. Finally, integrated circuit applications of spin transistors, including nonvolatile logic and reconfigurable logic systems that are the most suitable applications of spin transistors, are presented in Section VI.

II. FUNDAMENTALS OF SPIN TRANSISTORS

A. Two-Terminal Magnetoresistive Devices

Two-terminal magnetoresistive devices are a basic building block of spin transistors. After the discovery of the giant magnetoresistance (GMR) effect in ferromagnetic/nonmagnetic metal multilayers [44], [45], magnetoresistive devices have received considerable attention [46]–[49]. Here, we briefly review two-terminal magnetoresistive devices from the viewpoint of their application to spin transistors. Their magnetoresistive memory (MRAM) applications were reviewed in [50]–[55]. Fig. 1 schematically shows the structures and typical current–voltage (I–V) characteristics of two-terminal magnetoresistive devices. Spin valve (SV) devices consist of at least two ferromagnetic metal (FM) layers separated by an ultrathin nonmagnetic metal (NM) spacer layer, as shown in Fig. 1(a). They are classified into current-in-plane (CIP) and current-perpendicular-to-plane (CPP) geometries, and CPP-SVs have been applied to spin transistors. Ferromagnetic transition metals and their related alloys, including full-Heusler alloys, have been applied to the ferromagnetic layers, and nonmagnetic transition metals and other nonmagnetic metals have been used for the spacer layer. Magnetic tunnel junctions (MTJs) have a device structure

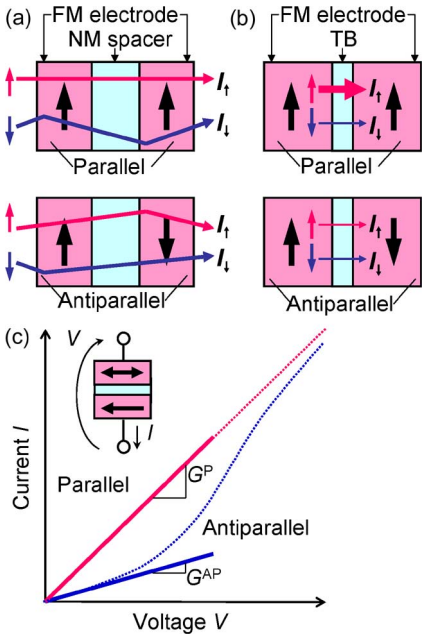


Fig. 1. *Schematic representations of (a) CPP-SV and (b) MTJ devices. (c) current–voltage characteristics of these devices. FM, NM, and TB represent ferromagnetic metal, nonmagnetic metal, and tunnel barrier, respectively.*

similar to SVs, however the metallic spacer in the SVs is replaced by an insulating tunnel barrier (TB) layer, as shown in Fig. 1(b). The MTJ technology was initially developed by the invention of the AlO_x tunnel barrier [56]–[58], and its subsequent dramatic progress has been due to the development of MgO tunnel barriers [59]–[64]. Furthermore, half-metallic ferromagnet electrodes using full-Heusler alloys have also had a great impact on the MTJ technology [65].

SVs and MTJs are designed to establish two relative magnetization configurations of parallel and antiparallel alignments. The electrical conductance of both the devices depends on the magnetization configuration. SVs and MTJs exhibit qualitatively the same features in spite of different mechanisms, i.e., a high conductance is achieved in parallel magnetization and it becomes low in antiparallel magnetization, as schematically shown by solid lines in Fig. 1(c). This phenomenon can be attributed to spin dependent scattering for SVs and to spin-dependent tunneling for MTJs, which is sometimes called the spin valve effect for SVs and the tunneling magnetoresistance (TMR) effect for MTJs. The magnetoresistance ratio is defined by $\gamma_{MR} = (G^P - G^{AP})/G^{AP}$ that is a measure of magnetoresistive devices, where G^P and G^{AP} represent the electrical conductance in the parallel and antiparallel magnetization configurations, respectively. Note that the I–V characteristics of the magnetoresistive devices well-reflect the feature of their device structures, and the γ_{MR} value often depends on a bias voltage. In the case of MTJs, it is known that the I–V characteristics show a nonlinear behavior and γ_{MR} decreases with increasing bias voltage, as schematically shown by the dashed curves in Fig. 1(c). The γ_{MR} of MTJs is much higher than that of SVs. In contrast, the resistivity of SVs is much lower than that of MTJs, which is caused by a difference in the resistivity between the metallic spacer layer and the insulating tunnel barrier.

The spin-filter effect that enables the selective propagation of carriers depending on their spin orientation is also useful for magnetoresistive devices. Fig. 2 shows the basic structure of two-terminal spin-filter devices. Ferromagnetic tunnel barriers [Fig. 2(a)], using a ferromagnetic insulator (FI), and ferromagnetic pn junctions [Fig. 2(b)], using a ferromagnetic semiconductor (FS), can act as spin filters [66], [67] based on the spin-dependent tunnel barrier and the spin-dependent built-in potential, respectively. By installing a ferromagnetic electrode as a spin injector or a spin detector to these spin-filter devices, magnetization-configuration-dependent I–V characteristics can be obtained, i.e., they act as a magnetoresistive device.

In order to establish the parallel and antiparallel magnetization configurations of magnetoresistive devices, exchange bias induced by antiferromagnets is commonly used [68], [69]. When an antiferromagnet/ferromagnet-layered structure is cooled with a magnetic field from a temperature above the Neel temperature of the antiferromagnet layer (that is lower than the Curie temperature of the ferromagnet layer), an magnetic anisotropy, the so-called exchange bias, is induced in the structure. The resulting hysteresis loop of the antiferromagnet/ferromagnet system is shifted along the field axis (generally in the opposite direction to the applied field during the cooling) by the anisotropy, which is referred to as the "pinning" of the ferromagnet layer. When one of two ferromagnetic layers in a magnetoresistive device is sufficiently pinned (which is called the pinned layer), the parallel and antiparallel configurations can be easily formed by magnetization switching of the other ferromagnetic layer (which is called the free layer), since the magnetization of the

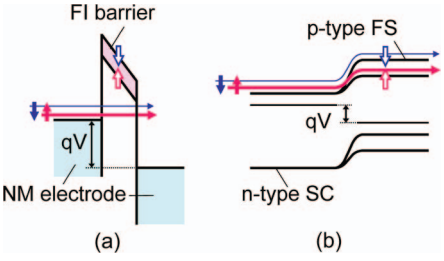


Fig. 2. *Schematic representations of the spin-filter effect in (a) ferromagnetic tunnel barrier and (b) ferromagnetic pn junction. FI, FS, and SC represent ferromagnetic insulator, ferromagnetic semiconductor, and semiconductor, respectively.*

pinned layer cannot be switched by the magnetic field for the magnetization reversal of the free layer. Note that a shape magnetic anisotropy of ferromagnet films is often used in laboratory experiments for generating different coercivities in ferromagnetic electrodes in magnetoresistive devices, which is also useful for achieving the formation of the parallel and antiparallel configurations.

Attractive functionalities of two-terminal magnetoresistive devices for integrated circuit applications are nonvolatile information storage based on the magnetization configuration and reconfigurable output characteristics depending on it. Therefore, these devices are promising not only for nonvolatile memory but also for new logic circuits using the nonvolatile and reconfigurable features. However, the two-terminal magnetoresistive devices would not be suitable for logic circuits when they used as logic elements, since they are a passive device. Of course, logic circuits can be configured by using two-terminal passive devices. Nevertheless, these devices have no following functions that are strongly required for logic circuits: high current drivability for high-speed and low-power operations and for sufficient fan-out, amplification capability for the restoration of attenuating signal, sufficient cutoff behavior for low standby power, and sufficient isolation behavior between input and output. (Note that the isolation behavior is required for logic devices, since the unidirectional propagation of a logic signal from input and output is crucial for logic circuits.) Therefore, three-terminal transistor-type magnetoresistive devices, that is, spin transistors, are attractive. Spin transistors are a new concept device that unites an ordinary transistor with the useful functions of a two-terminal magnetoresistive device, which is realized by the device-level integration of these devices with a hybrid structure. Several ordinary potential-effect transistors (PETs) and FETs are applied to spin transistors as their basic device structure, as described in this paper. It is worth noting that ordinary transistors (such as MOSFETs) used in present integrated electronics completely satisfy the above-described requirements.

Another way to use two-terminal passive magnetoresistive devices in logic circuits is in a circuit-level combination of magnetoresistive devices with CMOS circuits. Although this method is not necessarily ideal, there is the advantage that the present MRAM technology can be applied to spin transistors, as also discussed in this paper.

B. Spin Injection and the Conductivity Mismatch Problem

In the case of spin injection from an ordinary ferromagnet (i.e., a ferromagnetic metal) to a semiconductor through the ohmic junction, a high efficiency spin injection can hardly be achieved, which is known as the conductivity (or impedance) mismatch problem [70]–[73]. This originates from the fact of the large difference in electrical conductivity between a ferromagnetic metal and a semiconductor, as shown below. Although the resistance of the spacer layer is not taken into account in CPP-SV devices as shown in Fig. 1(a), it becomes problematic when the spacer layer belongs to a semiconductor. In general, the conductivity mismatch problem is treated by using electrochemical potential for spin-up and spin-down electrons [70], [71]. Here, we introduce a simple resistance network model [70], [71] for qualitative understanding. In the resistance network model, a ferromagnet can be expressed by a parallel circuit of two different resistances that represent the majority and minority spin channels of the ferromagnet. This circuit model can show the current spin-polarization of the ferromagnet. In a similar fashion, a semiconductor is expressible by a parallel circuit of two resistances of the same magnitude for spin-up and spin-down electrons. Fig. 3(a) shows the resistance network model of a ferromagnet (FM1)/semiconductor (SC)/ferromagnet (FM2) junction in the parallel magnetization configuration, where it is assumed that the FM1/SC and SC/FM2 junctions are ohmic, and that spin flip in the SC region can be eliminated. $R_{\mathrm{FM}}^{\mathrm{maj}}$ and $R_{\mathrm{FM}}^{\mathrm{min}}$ $(> R_{\mathrm{FM}}^{\mathrm{maj}})$ represent the resistances for the majority and minority spin channels in FM1 and FM2, respectively, and R_{SC} represents the

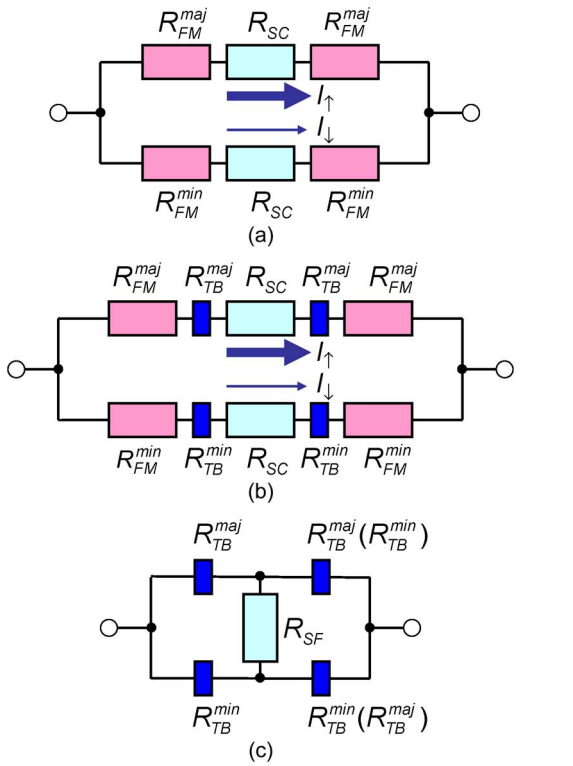


Fig. 3. *Resistor network model for an FM/SC/FM junction. (a) Equivalent circuit for parallel magnetization. (b) Equivalent circuit with interface resistance for parallel magnetization. (c) Equivalent circuit for parallel magnetization in the case of high interface resistance. The parentheses represent the equivalent circuit for antiparallel magnetization.*

resistance for the spin-up and spin-down channels in SC (both are equal). Here, the majority spin of FM1 is assumed to be the spin-up. The conductivity mismatch problem can be understood by treating the currents of the spin-up and spin-down channels in the parallel magnetization configuration. When the resistance of SC is comparable with that of FM1 and FM2, the combined resistances for the spin-up and spin-down channels are different. The resulting current for the spin-up channel is higher than that for the spin-down channel. Therefore, the total current that flows in this structure is spin-polarized. When R_{SC} is much higher than $R_{\mathrm{FM}}^{\mathrm{maj}}$ and $R_{\mathrm{FM}}^{\mathrm{min}}$, which is an actual case, the situation is quite different. In this case, $R_{\mathrm{FM}}^{\mathrm{maj}}$ and $R_{\mathrm{FM}}^{\mathrm{min}}$ can be neglected, and the voltage drop is caused entirely in the SC region. Therefore, the spin-dependent resistances ($R_{\mathrm{FM}}^{\mathrm{maj}}$ and $R_{\mathrm{FM}}^{\mathrm{min}}$) of FM1 and FM2 have no effect on the currents in the spin-up and spin-down channels, i.e., the currents are determined by spin-independent R_{SC}, and thus the total current cannot be spin-polarized. This phenomenon is referred to as the conductivity mismatch problem.

In order to evade the conductivity mismatch problem, it was proposed to add tunnel barriers (TB1 and TB2) at the interfaces of the FM1/SC and SC/FM2 junctions instead of the ohmic contacts [72], as shown in Fig. 3(b). The tunnel barriers can be formed by placing an ultrathin insulator at the interfaces, and also by using a ferromagnetic metal/semiconductor Schottky junction. The contact resistance (tunnel resistance) of such a tunnel barrier would be spin-dependent, owing to the effect of the ferromagnetic electrode. Fig. 3(b) shows the equivalent circuit of a FM1/TB1/SC/TB2/FM2 junction including the effect of the spin-dependent tunnel resistance, where $R_{\mathrm{TB}}^{\mathrm{maj}}[R_{\mathrm{TB}}^{\mathrm{min}}(> R_{\mathrm{TB}}^{\mathrm{maj}})]$ represents the tunnel resistance of TB1 and TB2 for the majority [minority] spin channel. When $R_{\mathrm{TB}}^{\mathrm{maj}}$ and $R_{\mathrm{TB}}^{\mathrm{min}}$ are comparable with R_{SC} or, more preferably, higher than R_{SC}, the combined resistances for the spin-up and spin-down channels become sufficiently different. Therefore, the total current passing through this structure is spin-polarized by introducing the tunnel barriers at the interfaces.

It is also predicted that the conductivity mismatch problem can be excluded by the use of a half-metallic ferromagnet (HMF) [65], [74]–[78] with a spin polarization of 100% as a ferromagnetic electrode, in which the addition of a tunnel barrier is not required. However, in practice, this could be challenging, since there is a difficulty in the material formation/processing of completely spin-polarized HMFs. There is also a possibility that the spin polarization of HMF electrodes deteriorates at the interface with a semiconductor [79], [80]. Eventually, a tunnel barrier (formed by an ultrathin insulating film or a Schottky junction) would be required even for an HMF electrode. Nevertheless, HMFs are the most promising material to achieve spin injection with high efficiency, since they can exhibit a very high spin polarization that is inaccessible to ordinary ferromagnets (even if the spin polarization is not exactly 100%). Note that the conductivity of ferromagnetic semiconductors is in the same range of that of semiconductors. Therefore, the ohmic contact between a ferromagnetic semiconductor and a semiconductor is applicable to spin injection without the conductivity mismatch problem [81].

We next consider the problem that arises when the tunnel resistance of TB1 and TB2 is enlarged [73]. In this case, it is necessary to include the effect of the spin-flip phenomenon in the SC region, since a high contact resistance of TB2 can restrict the amount of electrons passing from SC through TB2 to FM2. This situation can be expressed by a bridge circuit shown in Fig. 3(c), where the resistance (R_{SF}) between the spin-up and spin-down channels expresses the effect of the spin flip and the resistances of FM1, SC, and FM2 are neglected. Furthermore, $R_{\mathrm{SF}} \rightarrow 0$ (i.e., a short-circuit) can be assumed when the tunnel resistance of TB1 and TB2 is very high. The circuit shown in Fig. 3(c) represents the case of parallel magnetization, and the case of antiparallel magnetization is indicated in parentheses. The short-circuit has no effect on the current spin-polarization in parallel magnetization, owing to the equilibrium condition of the bridge circuit. However, the short circuit acts on the spin polarization of the current in antiparallel magnetization and thus the magnetoresistance ratio. The combined resistances in the parallel and antiparallel magnetization configurations become equal, and the resulting magnetoresistance ratio is zero. Therefore, when the tunnel resistances of TB1 andTB2 are too high, a sufficient magnetoresistance ratio cannot be obtained by the effect of the spin flip in the SC region. The precise description of the appropriate range of the tunnel resistance was given by [73].

Spin injection into semiconductors have been revealed by optical and electrical methods. Spin light emitting diodes (spin-LEDs) are often used to verify spin injection phenomena. In spin-LEDs, spin polarized electrons are electrically injected from a ferromagnetic electrode to a semiconductor through a Schottky barrier or a tunneling barrier. The spin polarization of the injected electrons (i.e., the spin injection efficiency) can be obtained by analyzing the circular polarized light emitting from the quantum well fabricated in the semiconductor region. The spin injection efficiency from several percent to several tens percent was observed for spin-LEDs using III-V semiconductors [82]. Spin-LEDs were also applied to the verification of spin injection into Si, using a Si n-i-p LED structure [83].

Nonlocal multi-terminal devices [84], [85] are commonly used for studying the spin injection/transport phenomena in semiconductors. Spin-polarized electrons are injected from one ferromagnetic electrode placed in the "local" part of the device and pure spin currents generated by the spin injection are detected by another ferromagnetic electrode placed in the "nonlocal" part. The nonlocal measurement effectively eliminates any spurious

phenomena induced by a stray field from the ferromagnetic electrodes. However, measurements of the Hanle effect (that is, spin precession and dephasing of conduction electrons in a perpendicular magnetic field) would be essential for the verification of spin-current detection. Spin injection and coherent spin transport including the Hanle effect in Si and GaAs were clearly observed by using nonlocal multi-terminal devices [86], [87]. A recently reported measurement technique of the Hanle effect using a hot electron transistor is described in Section III-A.

C. Spin Relaxation in Semiconductors

When spin-dependent transport phenomena are applied to transistors, i.e., spin transistors, the spin relaxation of conduction electrons in semiconductors can play an important role in spin-transistor operations. Spin relaxation in semiconductors can be classified by its mechanism [34]–[36], [88], i.e., Elliott–Yafet (EY) [89], [90], D'yakonov–Perel' (DP) [91], Bir–Aronov–Pikus (BAP) [92], and hyperfine interaction [93] mechanisms. From the viewpoint of spin-transistor applications, the EY mechanism in elemental semiconductors such as Si and the DP mechanism in III-V compound semiconductors such as GaAs, as shown in Fig. 4(a) and (b), respectively, are especially important.

The EY mechanism is a spin relaxation process caused by scattering via phonons, impurities, boundaries and so on. In the electronic band structures of semiconductors, the spin-up and spin-down states are mixed by the spin-orbit interaction of the constituent elements of the host material. As a result, the spin-up state contains a small component of the spin-down state and *vice versa*. (The amplitude of the mixed component depends on the strength of the spin-orbit interaction.) Therefore, spin polarized electrons in a semiconductor will get a chance for a spin flip after many scattering events, although the probability of the spin flip might not be so high. Therefore, the rate of the spin relaxation (that is given by the reciprocal of the spin relaxation time) caused by the EY mechanism is proportional to the rate of the momentum relaxation. A similar spin relaxation is also caused by the spin-orbit interaction induced by the potentials of impurities in highly impurity-doped samples. The EY mechanism appears in elemental semiconductors, such as Si, with a center of inversion symmetry (which is caused in the diamond structure of elemental semiconductors) and in compound semiconductors, such as GaAs, without a center of inversion symmetry (which is caused in the zinc blend structure of compound semiconductors). The EY mechanism can appear in narrow-gap compound semiconductors having a strong spin-orbit interaction, although the DP mechanism described below dominates in middle-gap compound semiconductors, such as GaAs and InGaAs, that have a moderate spin-orbit interaction. The EY mechanism is also a predominant process of spin relaxation in elemental semiconductors (owing to the lack of the DP mechanism in this material system). In phosphorus-doped Si with a dopant concentration lower than $\sim 10^{18}$ cm^{-3}, the spin relaxation time has no dependence on the dopant concentration above 200 K (i.e., the spin relaxation is restricted by phonon scattering), and a fairly long spin relaxation time of about 10 nsec was observed at room temperature [35], [88], [94], which is, of course, due to the very weak spin-orbit interaction in Si. In heavily impurity-doped Si samples, the spin relaxation time decreases with the doping concentration. However, a long spin lifetime greater than 140 ps was observed even in heavily doped n-type silicon at 300 K [95].

The DP mechanism is an important spin-flip process of conducting electrons in compound semiconductors without a center of inversion symmetry. The spin degeneracy in their band structure is lifted by the spin-orbit interaction. Therefore, spin-up and spin-down electrons, even in the same momentum state, experience different energies that depend on the momentum state. This situation is equivalent to causing an internal effective magnetic field depending on the momentum state. The spin moment of moving electrons precesses due to the effective magnetic field until scattering, and then the precession starts again after the scattering. However, the direction and the frequency of the precession change at random, since the effective magnetic field changes with the momentum scattering. Therefore, the spin polarization diffuses with these precession processes. The remarkable feature of the DP mechanism is that the spin relaxation rate is proportional to the momentum relaxation time. The shorter the momentum relaxation time is, the lower the spin relaxation rate is (i.e., the spin relaxation time is longer). In middle-gap III-V semiconductors with a low or moderate impurity concentration, the DP mechanism can dominate in a wide range of temperatures including high temperatures. In quantum well or heterojunction structures, the effective (Bychkov–Rashba) spin-orbit interaction is induced by structural inversion asymmetry, which also causes spin relaxation due to the DP mechanism. This spin relaxation mechanism plays an important role for III-V heterostructure systems (see Section V). The DP mechanism was also found to be dominated in Si quantum well structures at low temperatures [35], [88].

The BAP mechanism is caused in p-type semiconductors. Electrons in p-type semiconductors are coupled with

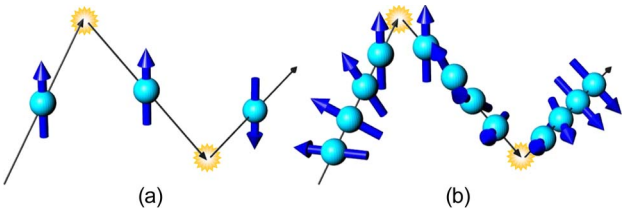


Fig. 4. *Important spin relaxation mechanisms in semiconductors. (a) Elliott–Yafet mechanism, and (b) D'yakonov–Perel' mechanism.*

holes by the exchange interaction between them. The total spin is preserved by this coupling interaction. Since the effect of the spin-orbit interaction is very strong in the valence band, the spin relaxation of holes (that would be caused by the EY mechanism) is very fast in comparison with electrons. Because of the coupling interaction, the spin relaxation of electrons is quickly accompanied by that of holes. The BAP mechanism coexists with the EY and DP mechanisms, and stands out at lower temperatures or in heavily doped p-type samples.

The hyperfine interaction between spin moments of an electron and nuclei causes a spin relaxation for a localized electron such as an electron confined in quantum dots or bound on donors. The wave function of a localized electron is spread over many lattice sites. Therefore, the magnetic moments of many nuclei affect the localized electron through an effective magnetic field induced by the hyperfine interaction, resulting in the spin relaxation of the localized electron. Since the hyperfine interaction is very weak, this spin relaxation mechanism is ineffectual to itinerant electrons. In GaAs the hyperfine interaction is caused by nuclear spins of the lattice nuclei, while in Si it frequently comes from donor ^{31}P due to no nuclear spin of the most abundant isotope ^{28}Si. Therefore, the hyperfine interaction in Si is much smaller than in GaAs. Nevertheless, in phosphorus-doped Si, the spin relaxation of electrons due to the hyperfine interaction was observed at low temperatures below 50 K, where the electrons are bound on the donor levels [35].

D. Current-Induced Magnetization Switching

When spin devices are used in integrated circuits, an important challenge is magnetization switching (reversal). When a magnetic field induced by a current through interconnections placed near the ferromagnetic electrodes of a spin device is used, the current required for magnetization reversal increases as the device size decreases, owing to the demagnetizing field of the scaled-down ferromagnet. This will cause problems of an increase in power dissipation and program disturbs (that is failure mechanisms due to a magnetic field applied from selected interconnections to unselected spin devices). In recent years, current-induced magnetization switching (CIMS) based on spin transfer torque has attracted considerable attention as a scalable means of magnetization reversal in spin devices [96]–[103] (although it is recently recognized that CIMS also induces another type of disturb error in MRAM applications [104]).

CIMS can be caused by injecting a spin-polarized current into a ferromagnetic layer, since the spin-polarized current exerts torque for the magnetization reversal of the ferromagnetic layer. Fig. 5(a) shows a schematic representation of the spin-transfer torque phenomenon, where spin-polarized electrons are incident to a ferromagnet (FM) layer. The incoming electrons are assumed to be spin-polarized on average at an angle θ to the direction of the magnetization of the FM layer. Then, the incident

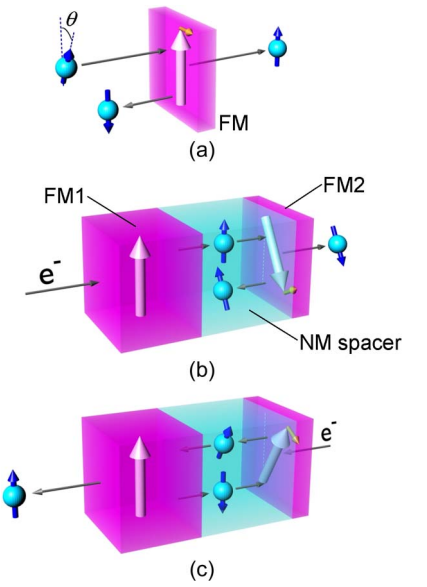


Fig. 5. *(a) Schematic representation of the spin-transfer effect. (b) CIMS mechanism for antiparallel-to-parallel switching. (c) CIMS mechanism for parallel-to-antiparallel switching.*

spin-polarized electrons are scattered by the FM layer, in which the scattering events depend on the relative orientation between the electron spin and the magnetization, i.e., spin-dependent scattering. For the transmitted component through the FM layer, the average spin moment of the electrons is aligned parallel to the magnetization direction of the FM layer due to the ferromagnetic exchange interaction. Namely, the magnetization of the FM layer exerts torque to the spin of the electrons so as to be aligned toward the magnetization direction. At the same time, the magnetization of the FM layer receives the torque from the electrons impinging on the FM layer, owing to the total angular momentum conservation law. This can be more intuitively understood by Newton's third law as a forward push causes the backward thrust. The torque increases with the amount of current (the torque per unit area is proportional to the current density). Although this torque is absorbed in an ordinary-sized ferromagnet, the magnetization reversal will be achieved in a fine deep-submicron ferromagnet. Note that for electrons reflected by the scattering, the average spin polarization is aligned to the opposite direction of the magnetization of the FM layer. This phenomenon is also used for the CIMS of spin devices, as described below.

Fig. 5(b) shows a schematic representation of CIMS in a CPP-SV device. The device is fabricated as a nanopillar structure with a size of around 100 nm or less, where one ferromagnet (FM1) is thickened enough (or pinned) so as to be insensitive to the spin transfer torque effect and the other ferromagnet (FM2) is thinned enough for CIMS. When the magnetization configuration is changed from the antiparallel to the parallel, electrons are injected from FM1

to FM2 for the CIMS (i.e., the resulting current flow from FM2 to FM1). The magnetization of FM2 exerts the torque to align the spin moment of the electrons toward the magnetization direction of the FM2 layer, due to the exchange interaction. Equivalently, this means that the electrons cause the reverse torque to the magnetization of FM2, as described above. When the spin transfer torque can act sufficiently (which requires a high current density over 10^6 A/cm^2), the magnetization of FM2 reverses according to the spin transfer torque and thus the parallel magnetization configuration is established. This parallel configuration stabilizes to the electron flow direction from FM1 to FM2.

When the magnetization configuration switches from the parallel to the antiparallel, the direction of the current is reversed. Namely, electrons are injected from FM2 to FM1. After the spin-dependent scattering by FM1, electrons having the average spin polarization parallel to the magnetization direction of FM1 can transmit through FM1 and thus have no effect on the CIMS. On the other hand, the average spin moment of the electrons reflected by the scattering is aligned antiparallel to FM1 and thus these electrons exert the spin transfer torque to the magnetization of FM2 so as to be aligned antiparallel to the magnetization direction of FM1. When a sufficient amount of the reflected electrons impinges on FM2, the magnetization reversal proceeds and the antiparallel magnetization is established. This CIMS process requires a high current density similar to the antiparallel-to-parallel switching, however its magnitude would be different from the antiparallel-to-parallel switching.

CIMS is also applicable to MTJs [105]–[107] in the same manner as CPP-SV devices. From the view point of integrated circuit applications, reduction of the current densities for CIMS is highly important. Recently, new device structures which use perpendicular magnetization electrodes or half-metallic ferromagnet electrodes have been investigated for reduction of the current densities for CIMS [108], [109].

E. Basic Characteristics of Spin Transistors

In general, spin transistors contain at least two ferromagnetic layers in the device structure, and they are designed to establish two stable states for relative magnetization direction between the two ferromagnetic layers, i.e., the parallel and antiparallel magnetization configurations. The output current or current drivability of the spin transistors can be modified by the magnetization configurations. Fig. 6(a) shows the input/output signal relation of a typical spin-transistor, where I_{O}^{β} represents the output current in the parallel ($\beta = \mathrm{P}$) and antiparallel magnetization ($\beta = \mathrm{AP}$) configurations and V_{O} and V_{I} represent the output voltage and the input voltage, respectively. (Note that in practice, a current bias for the input would be more convenient for the control of output currents in potential-effect spin transistors. However, the voltage bias is used here for the general understanding of spin transistors.) Fig. 6(b) schematically shows the output characteristics of the spin transistor. The output currents are different for the parallel and antiparallel magnetization configurations, even when the same bias condition is applied to the device. This behavior is often referred to as magnetization-configuration-dependent output characteristics or spin-dependent output characteristics. The transconductance, g_{m}^{β}, is defined as the current drivability of the input voltage, i.e., $g_{\mathrm{m}}^{\beta} = \partial I_{\mathrm{O}}^{\beta}/\partial V_{\mathrm{I}}$. Therefore, g_{m}^{β} expresses the sensitivity of the output currents with respect to the input voltage, and g_{m}^{β} is given by the slope of the I_{O}^{β}–V_{I} plot, as shown in Fig. 6(c). The high and low g_{m}^{β} values can be reached in the parallel and antiparallel magnetization configurations, respectively. The variable transconductance of spin transistors gives an additional degree of freedom in controlling the output currents, which is quite useful for nonvolatile logic and reconfigurable logic circuits. In addition, the magnetization configurations of spin transistors can be used as nonvolatile binary information.

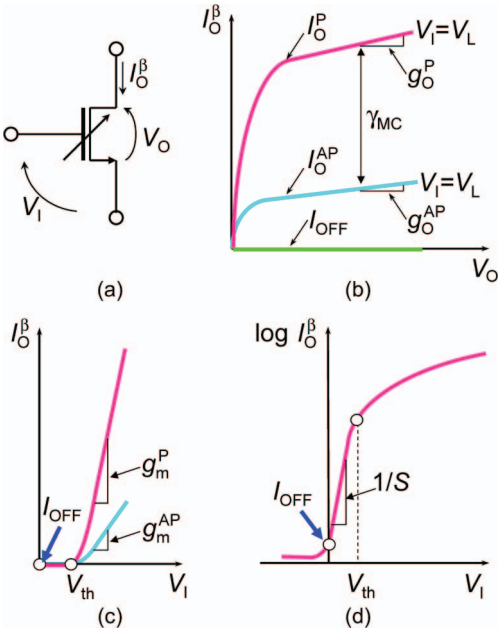


Fig. 6. *(a) Input/output signal relation of a spin transistor. (b) Output characteristics (I_O^β–V_O), (c) transfer characteristics (I_O^β–V_I), and (d) log I_O^β–V_I characteristics of the spin transistor.*

In order to evaluate the magnetization-configuration-dependent output characteristics, the magnetocurrent ratio is commonly used as a performance index for spin transistors. The magnetocurrent ratio, γ_{MC}, is defined by

$$\gamma_{\mathrm{MC}} = \frac{I_{\mathrm{O}}^{\mathrm{P}} - I_{\mathrm{O}}^{\mathrm{AP}}}{I_{\mathrm{O}}^{\mathrm{AP}}}. \tag{1}$$

A suitable magnitude of γ_{MC} depends on the application. A high γ_{MC} value is preferable for nonvolatile memory

applications. On the other hand, a moderate γ_{MC} value is required for logic applications, because of a tradeoff between γ_{MC} and propagation delay. High γ_{MC} means low I_O^{AP}, and thus the low current drivability in the antiparallel magnetization configuration restricts the speed of logic gates, as discussed below. Note that this situation depends on the circuit configuration, and a circuit in which the effect of I_O^{AP} on the circuit performance plays a minor role can be configured, as shown in Section VI.

Hereafter, we consider an integrated logic circuit configured by spin transistors and interconnect wirings. From the viewpoint of circuit performance, the transconductance (g_m^β) and the OFF-state leakage current (I_{OFF}) of the spin transistors are significant, as well as ordinary transistors. Note that I_{OFF} could depend on the magnetization configuration, as described in Section VI, i.e., I_{OFF} should be expressed by I_{OFF}^β. However, I_{OFF} is used here for simplicity. The propagation delay (t_{pd}) and the power delay product ($P \cdot t_{pd}$) are key figures of merit for the circuit performance. These quantities are determined by charging and discharging the load capacitance (C_L) for each spin-transistor. (C_L includes the input capacitance of the next-stage spin transistors, the interconnect capacitance and the parasitic capacitance. However, most of C_L is dominated by the interconnect capacitance.) The situation is the same as in ordinary transistor circuits, and thus transistor behavior with high transconductance is essential even for spin transistors. It should be noted that a spin-polarized current is unnecessary for the interconnections between spin transistors, although it is required for the operation of the spin transistors (i.e., inside of the spin transistors).

The propagation delay required for charging (discharging) C_L is given by $t_{pd} = C_L V_L / I_O^\beta$, where V_L is the logic swing. This is roughly approximated by $t_{pd} \sim C_L / g_m^\beta$. Obviously, a higher g_m^β is effective to reduce t_{pd}. However, t_{pd} depends on the magnetization configuration of the spin transistor. In general, the current drive capability of spin transistors cannot exceed that of ordinary transistors even when the magnetization configuration is parallel. In addition, a high γ_{MC} results in a low I_O^{AP}. Therefore, a high γ_{MC} deteriorates t_{pd} when the corresponding spin transistor is magnetized antiparallel. The power-delay product $P \cdot t_{pd}$, the energy per switching for charging or discharging C_L, is given by $P \cdot t_{pd} = C_L V_L^2 / 2$. The reduction of V_L is the only way to minimize the switching energy. However, in general, a lower V_L causes a lower driving current, resulting in the degradation of t_{pd}. In order to reduce $P \cdot t_{pd}$ without severely degrading t_{pd}, a higher g_m^β is required.

The amplification capability of the spin transistors is also important, since the spin transistors not only perform logical operations but also amplify attenuating signals caused by propagating up to a full logic swing. The voltage gain, G_V, is defined by the change rate of the output voltage to the input voltage, i.e., $G_V = \Delta V_O / \Delta V_I = g_m^\beta / g_O^\beta$, where g_O^β is the output conductance given by $g_O^\beta = \partial I_O^\beta / \partial V_O$. A high g_m^β and a low g_O^β are simultaneously required for a high G_V. In other words, the saturation behavior with a smaller gradient in $I_O^\beta - V_O$ characteristics [Fig. 6(b)] and the steep increase behavior with a larger gradient in $I_O^\beta - V_I$ characteristics [Fig. 6(c)] results in a high G_V. The fan-out is also an important consideration for logic devices. In general logic circuits, the output of one logic gate (driving gate) is connected to the input of one or more gates (load gates). The fan-out is defined by the number of load gates. To ensure an adequate fan-out (typically, four), a sufficiently high current drivability (that is, g_m^β) is necessary.

The leakage current of the spin transistors in the OFF-state cause static power dissipation during the standby mode of the logic circuit. The leakage current exponentially decrease with decreasing V_I [Fig. 5(d)]. The subthreshold swing, S, is defined by the inverse of the slope of the log $I_O^\beta - V_I$ plot, as shown in Fig. 5(d). Although S is commonly used for characterization of a subthreshold leakage current in MOSFETs and other FETs, it is also useful for PETs such as bipolar junction transistors (BJTs). S represents the controllability of the leakage current with respect to V_I, and S depends on the carrier injection mechanism of the transistors, e.g., thermionic or tunneling emission. The minimum S value for ordinary MOSFETs (that employ the thermionic emission of carriers from the source to the channel) is limited to 60 mV/decade at room temperature. BJTs also take the same minimum value of 60 mV/decade owing to the virtually identical mechanism for the carrier injection. Recently researched MOS devices using the tunneling emission for the carrier injection are promising for achieving $S < 60$ mV/decade [110]. A similar restriction for S is imposed on the spin transistors. The ON/OFF ratio between the ON-current (I_{ON}) at $V_I = V_L$ and the OFF-current (I_{OFF}) at $V_I = 0$ is also used to evaluate the leakage current of the spin transistors. Note that although the ON/OFF ratio of FET-type spin transistors depends on the threshold voltage (V_{th}), a ON/OFF ratio over 10^4–10^7 can be achieved. This would be determined by the circuit criteria. [When V_{th} is low (high), both I_{ON} and I_{OFF} are high (low), resulting in a high (low) speed circuit with large (small) standby power.]

The above-described bias-controlled OFF-state is achieved by the same way as ordinary transistors. In this case, we can use the magnetization-*independent* OFF-state, as shown in Fig. 6(b). In other words, the two different ON-states of I_O^P and I_O^{AP} can be employed for circuit operations. This feature is very attractive for complex logic functions. When spin transistors are used in integrated circuits, there is another approach to establish their OFF-state, that is, the usage of the magnetization-controlled OFF-state. In this case, I_O^{AP} is used as I_{OFF}. However, a huge γ_{MC} is required to achieve a high ON/OFF ratio [111]. For example, when γ_{MC} is 100%, the ON/OFF ratio is only 2. If an ON/OFF ratio of 10^4 is needed, a very high γ_{MC} value of 10^6%

is required. Thus, the bias-controlled OFF-state is preferable not only for functionalities but also for achieving sufficient cutoff characteristics.

III. POTENTIAL-EFFECT SPIN TRANSISTORS

A. Hot-Electron Spin Transistors

A variety of spin transistor that replaces part of a hot electron transistor (HET) [112] with a magnetoresistive element has been proposed. Fig. 7(a) shows a schematic energy band diagram of the spin valve transistor (SVT) proposed by Monsma *et al.* [113], [114]. The SVT has a HET structure (with a thermionic-emission-type emitter) with a spin valve (SV) for the base. The emitter and collector barriers are formed by Schottky junctions between the SV base and the silicon emitter/collector. Hot electrons are injected from the emitter to the base by thermionic emission. Although the ballistically conducting hot electrons in the SV base can selectively pass over the collector barrier, the mean free path (MFP) of the hot electrons in the base depends on the magnetization configurations of the SV base, owing to the energy relaxation caused by the spin-dependent scattering. When the SV base is magnetized parallel, the counterpart of the spin-up and spin-down electrons injected from the nonmagnetic emitter is aligned parallel to the magnetization direction of the two ferromagnetic layers in the SV base. On the other hand, in the case of the antiparallel magnetization configuration of the SV base, both the spin-up and spin-down electrons injected into the base region are aligned antiparallel to the magnetization direction of one of the ferromagnetic layers in the SV base, as shown in Fig. 7(a). The MFP of injected electrons with spin moment antiparallel to the magnetization direction is shortened in comparison with the case of the parallel alignment, owing to the spin-dependent scattering effect in the SV base. Therefore, when the SV base is magnetized parallel, more hot electrons can reach the collector than in the case of the antiparallel magnetization configuration of the SV base. The output (collector) current in the parallel magnetization configuration is higher than that in the antiparallel magnetization configuration, i.e, the magnetization-configuration-dependent output characteristics can be established. The most remarkable feature of the SVT is a very high γ_{MC} ($> 300\%$) at room temperature. Nevertheless, the SVT exhibits low output currents and a small current transfer ratio α ($= I_C/I_E$, where I_C is the collector current and I_E the emitter current) of $\sim 10^{-4}$, indicating a very low current drivability. The fairly low α values significantly restrict the transconductance of the SVT, although I_E can nonlinearly increase with an emitter-base voltage. [It should be also noted that for achieving a current gain ($\beta = I_C/I_B$, where I_B is the base current) higher than unity, α must be higher than 0.5 since β is given by $\beta = \alpha/(1-\alpha)$.] Therefore, the SVT would not be suitable as an active device for integrated circuits. Although the barrier heights of the emitter and collector junctions and the width of the base are highly important in order to improve transfer characteristics of the SVT, α would not likely achieve a significantly high value owing to the metallic base layer, as discussed later.

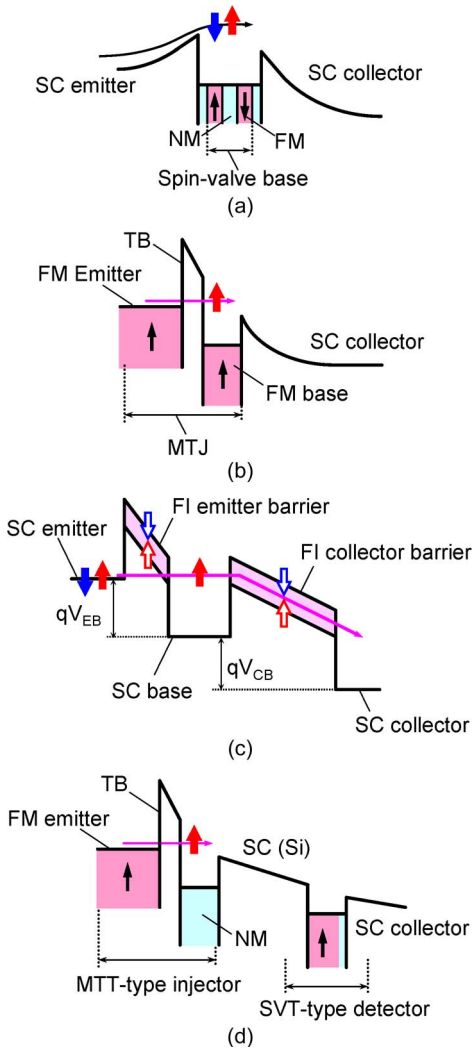


Fig. 7. *Schematic band diagrams of (a) spin-valve transistor (SVT), (b) magnetic tunnel transistor (MTT), (c) spin-filter transistor (SFT), and (d) spin transistor with MTT-type injector and SVT-type detector. The notations are described in the figure captions of Figs. 1 and 2.*

Fig. 6(b) shows a schematic band diagram of the magnetic tunnel transistor (MTT) [115] in which a magnetic tunnel junction (MTJ) is used for the emitter-base junction. The MTT employs a HET structure with a tunneling-emission-type emitter as its basic structure. In the MTT, spin polarized electrons are injected from the ferromagnetic metal emitter to the ferromagnetic metal base through the tunnel barrier of the MTJ. The MFP of the hot electrons injected into the base depends on the

magnetization configuration of the emitter-base MTJ owing to the spin-dependent scattering. When the magnetization configuration between the emitter and the base is antiparallel, the MFP becomes shorter in comparison with the case of the parallel magnetization configuration. Therefore, the magnetization-configuration-dependent output characteristics can also be achieved for the MTT. Although α can be improved for the MTT, owing to the tunneling emission of the spin-polarized electrons from the emitter with a relatively high bias, it is still insufficient ($\sim 10^{-3}$).

It is not so easy in practice for even conventional (nonmagnetic) HETs to achieve a high transfer ratio. In particular, when the base layer is composed of a metal, this has hardly been achieved yet, owing to the short MFP of hot electrons in the metal base. Sufficient transfer characteristics in ordinary HETs were achieved only by using a semiconductor for the base, since the MFP value of semiconductors is a few orders of magnitude more than that of metals [116], [117]. From this point of view, a HET-type spin-transistor with a semiconductor base was proposed, using a ferromagnetic tunnel barrier [118], [119], as shown in Fig. 6(c). HETs have been expected as a high speed integrated device owing to their low input (emitter-base) capacitance and low base resistivity in comparison with BJTs. However, the superiority of HETs as an integrated active device seems to have not been proven yet.

Nevertheless, the device structures of the SVT and the MTT is useful as a spin injector/detector for a semiconductor with high efficiency. Fig. 7(d) shows a schematic band diagram of the spin transistor proposed by Appelbaum *et al.* [120], in which the MTT-type spin injector and the SVT-type spin detector are applied in the device structure. This structure is quite useful for the detection of spin precession of conducting spin-polarized electrons. The coherent spin transport with spin precession induced by the Hanle effect was successfully observed in a Si channel over 350 μm [121].

B. Bipolar Spin Transistors

In contrast to HETs, BJTs can easily achieve a very high α by controlling the doping density of the pn junctions. Moreover, the nonlinear emitter-base diode characteristics in BJTs result in a very high transconductance. Therefore, one can expect that a BJT type of spin-transistor might be promising. Fig. 8 schematically shows a band diagram of the magnetic bipolar transistor (MBT) [122]–[125]. The MBT uses a p-type ferromagnetic semiconductor for the base, and thus the emitter-base and base-collector junctions are ferromagnetic pn junctions consisting of the p-type ferromagnetic semiconductor and an n-type semiconductor. Output characteristics of the MBT can be analyzed by an expanded bipolar transistor model with spin-up and spin-down current components. Like BJTs, excess minority carriers injected from the emitter to the base determine the output characteristics of the MBT. Since the spin-dependent built-in potentials are formed at

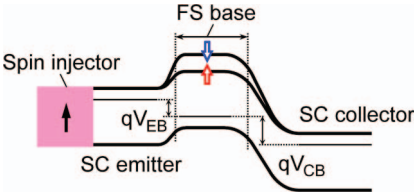


Fig. 8. *Schematic band diagram of magnetic bipolar transistor (MBT).*

the emitter-base junction by the spin-splitting of band edge in the ferromagnetic semiconductor base, one of the spin-up and spin-down electrons that is adapted to the lower built-in potential is preferentially injected into the base layer. The magnetization-configuration-dependent output characteristics can be obtained by installing a spin injector, such as a tunnel contact with a ferromagnetic electrode or an ohmic contact with a ferromagnetic semiconductor, to the emitter. When the magnetization configuration between the emitter spin injector and base is parallel, majority-spin electrons injected in the emitter can pass over the lower built-in potential of the base and thus cause a high collector current. On the other hand, in the case of the antiparallel magnetization configuration, majority-spin electrons in the emitter have to pass over the higher built-in potential (while minority-spin electrons can pass over the lower built-in potential), resulting in a low collector current. Therefore, γ_{MC} depends on the spin splitting of conduction band of the base and the spin polarization of electrons injected from the spin injector to the emitter.

In general, the carrier density of ferromagnetic semiconductors is very high, which causes α to degrade. Therefore, it would be necessary for the MBT to adopt the structure of hetero bipolar transistors (HBTs) [126], [127]. The MBT has the potential to achieve a high α value close to unity and a high transconductance, as noted previously. However, the MBT faces the same situation as ordinary BJT circuits: a serious problem of high power consumption that constrains circuit performance and the degree of device integration. This is due to the high power-delay product of BJT-based devices. It should also be noted that although group-IV- and III-V-based ferromagnetic semiconductors have been developed so far and their Curie temperatures have recently increased [128]–[130], they are still below room temperature.

IV. FIELD-EFFECT SPIN-TRANSISTORS I: SPIN-MOSFET

A. Comparison Between Spin-FET and Spin-MOSFET

Since the scalability and integration ability of spin transistors are essential for integrated circuit applications, spin transistors analogous to FETs are more attractive than

vertical-type devices such as the SVT and the MBT. Furthermore, FET-type devices can suppress the power-delay product to a relatively small value in comparison with BJT-type devices, which is also promising for integrated circuits. The FET type of spin transistor can be classified into two types: the spin-FET proposed by Datta and Das [41] (and its modified versions [131]–[134]) and the spin-MOSFET with several variations [30]–[32], [135]. These spin transistors are comprised of a modulation-doped FET (MODFET) structure or a MOSFET structure in combination with the ferromagnetic source and drain that act as a spin injector and a spin detector, respectively, as shown in Fig. 9. (Furthermore, the quasi-one-dimensional channel structure is necessary to avoid dephasing the spin-polarized channel electrons for the spin-FET, which structure is not required for the spin-MOSFET.) However, their operating principles are quite different. In the spin-FET and its related devices, the switching operation can be achieved by spin precession or dephasing of spin-polarized carriers injected in the channel. On the other hand, the relative magnetization configurations of the source and drain are used to modify output currents for the spin-MOSFET. In this section, the spin-MOSFET is described in detail. The original spin-FET [41] is also briefly reviewed below for comparison, although the spin-FET and its related devices are described in detail in the next section.

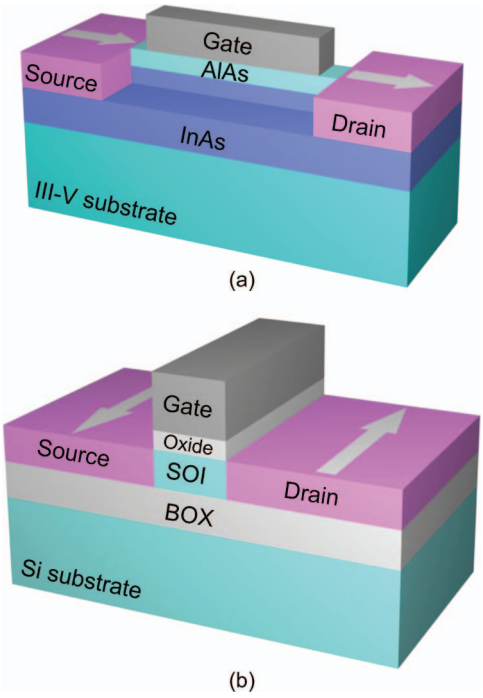


Fig. 9. *Schematic device structures of (a) spin-FET, and (b) spin-MOSFET that are comprised of a MODFET structure or a MOSFEST structure in combination with a ferromagnetic source and drain.*

The spin-FET employs the Rashba spin-orbit interaction for the spin precession of spin-polarized electrons in the channel with the magnetization configuration of the source/drain fixed. The spin moment of the electrons rotates while traveling owing to the effective magnetic field induced by the Rashba spin-orbit interaction. The parallel and antiparallel configurations between the electron spin and the magnetization of the ferromagnetic drain can be achieved by the spin orientation of the conducting electrons reaching the ferromagnetic drain. Since the Rashba spin-orbit interaction can be controlled by a gate bias, the unique output characteristics, including oscillating output currents with respect to a gate bias and the resulting negative transconductance, can be obtained. Particular materials with a strong spin-orbit interaction, such as InGaAs, InAs, and InSb, are required for the channel to sufficiently induce the Rashba spin-orbit interaction. The scalability of the spin-FET depends on the channel material, and a material with a strong spin-orbit interaction can shorten the channel length. However, the scaling is limited to sub-microns or more [136]. A MODFET structure is used as the basic structure of the spin-FET in the original proposal. There is a possibility that a MOSFET structure can be applied according to the future development of recently emerging III-V MOSFET technologies [14]–[17], which would be preferable for integrated circuits. The spin-FET performs the ON/OFF switching by the spin precession of the conducting channel electrons, as described above. In this case, the imperfect OFF-state causes the problem of a low ON/OFF ratio, as described in the Section II-E. The OFF-state of the spin-FET should be achieved by controlling a gate bias for a sufficient cutoff condition.

The channel of the spin-MOSFET is composed of silicon with a very weak spin-orbit interaction. Spin precession of the conducting electrons would be ruled out for short channel devices as long as an external magnetic field is not applied intentionally. Furthermore, the spin relaxation time is expected to be very long in the Si channel, as noted in Section II-C. The output current can be modulated by the magnetization configurations of the ferromagnetic source and drain. Moreover, in contrast to the spin-FETs, the cutoff state of the spin-MOSFET is simply achieved by a gate bias condition in the same manner as an ordinary MOSFET. These features are attractive for reconfigurable logic and nonvolatile logic applications. Since the spin-MOSFET requires no spin precession of spin-polarized electrons in the channel, it has the excellent scalability of ordinary MOSFETs. The spin-MOSFET would have the same degree of performance as metal source/drain MOSFETs and ordinary MOSFETs owing to the similarity in the device structure, although it is necessary to establish ferromagnetic source/drain technology compatible with the present CMOS platform.

It should be noted that there is a very different way for realizing spin transistors. The pseudo-spin-MOSFET [137],

[138] is a simple circuit for reproducing the functions of a spin-MOSFET using an ordinary MOSFET and a MTJ.

B. Classification and Characteristics of Spin-MOSFETs

The basic structure of a spin-MOSFET with several variations [31], [32] is comprised of a MOS capacitor and a ferromagnetic source and drain (S/D), as described above. Spin MOSFETs can be classified by the structure of the ferromagnetic S/D [31], [32]. Fig. 10 shows band diagrams of the various spin MOSFETs. The ferromagnetic S/D should satisfy appropriate contact resistance condition to exclude the conductivity mismatch problem and to generate spin-polarized currents in the channel. The S/D also should act not only as an electrical contact for the channel in the ON-state but also as a blocking contact for leakage currents in the OFF-state.

In a manner analogous to ordinary MOSFETs, ferromagnetic pn junctions using a ferromagnetic semiconductor might be considered promising [Fig. 10(a)]. However, ferromagnetic pn junctions are not practicable at present, since the Curie temperatures of ferromagnetic semiconductors are still lower than room temperature.

Ferromagnetic Schottky junctions using a ferromagnetic metal can be employed for the S/D of a spin MOSFET, which is analous to the recently developed metal S/D (or Schottky barrier) MOSFETs [139]–[142]. The ON/OFF operation of the spin MOSFET is based on the gate-bias-induced modification of the Schottky barrier width at the source/channel junction [Fig. 10(b)]. Although the control of the Schottky barrier height, that is, the tuning of the contact resistance, is required to eliminate the conductivity mismatch problem, the reduction of the Schottky barrier height is rather important since the Fermi level pinning at the junction interface causes a high contact resistance. The reduction of the barrier height is also necessary for high current drivability and high spin injection efficiency [31].

HMFs are also useful for the ferromagnetic S/D. The band structure of HMFs consists of metallic and insulating (semiconducting) spin bands, and thus HMFs show a spin polarization of 100% at the Fermi energy. The metallic spin band of HMF contacts forms a Schottky junction with the Si channel, and the insulating spin band forms an energy barrier whose barrier height is related to the band gap of the insulating spin band. Thus, the spin-dependent barrier structure appears at the source/drain junctions [Fig. 10(c)], and acts as a high efficiency spin filter. In practice, the half-metallicity of HMFs are degraded due to their imperfect quality (such as defects) and the influence of the HMF/Si interface [79], [80]. Nevertheless, high spin polarizations that are inaccessible to ordinary ferromagnets would be achieved in HMFs. Note that the interface effect on the degradation of the half-metallicity can be eliminated by the formation of a HMF(full-Heusler alloy)/Si junction in a particular plane direction [143]. The control of the Schottky barrier height would also be required even for HMFs, as noted in the Section II.

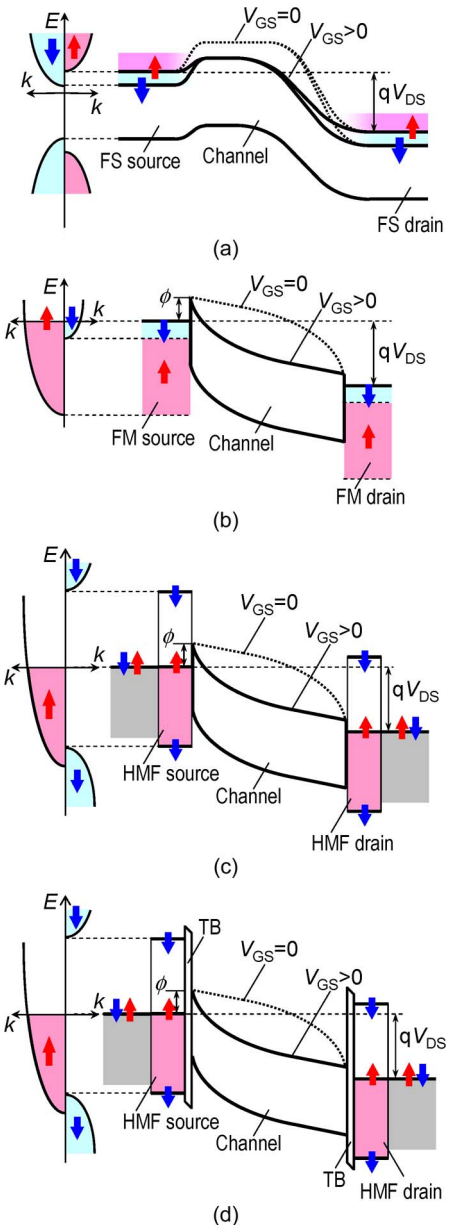


Fig. 10. *Band diagrams of spin-MOSFETs with (a) FS source/drain, (b) FM source/drain, (c) HMF source/drain, and (d) ferromagnetic tunnel contact source/drain. HMF represents half-metallic ferromagnet, and the other notations are described in the figure captions of Figs. 1 and 2.*

Tunnel contacts using an ultrathin insulating barrier are useful for controlling the Schottky barrier height of HMF and FM S/D structures [Fig. 10(d)]. The HMF/Si and FM/Si junctions would induce the Fermi level pinning phenomenon in which the Fermi energy of the HMF or FM electrode is placed to a deep level in the bandgap of Si, regardless the work function of the HMF or FM electrodes.

For highly scaled-down spin-MOSFETs with a nanoscale channel length, the channel conductance is fairly low, which causes the requirement of a considerably low contact resistance to address the conductance mismatch problem. In addition, lower Schottky barrier heights are favorable for the high current drivability. Therefore, the depinning and reduction of the Schottky barrier height are indispensable. A tunnel contact to an n^+—Si region using a ferromagnetic electrode, that is, an application of a common maneuver to achieve an electrical contact, is the easiest way to reduce the Schottky barrier height. However, the highly doped n^+—Si region would affect on a spin flip as noted in Section II, and thus it could be necessary to carefully design the junction structure. Therefore, a tunnel contact with an ultrathin interfacial insulating layer for depinning and a low work-function electrode is attractive [144]–[146]. It should be noted that ferromagnetic insulator barriers [66] with an ordinary metal electrode are also applicable to a tunnel contact type ferromagnetic S/D.

Fig. 11(a) shows the calculated output characteristics of a spin-MOSFET with an HMF S/D [30]. The simulation was performed under the assumptions of ballistic transport and complete spin polarization (100%) without any spin-flip scattering. The spin-MOSFET shows excellent transistor behavior in parallel magnetization (solid curves), and the drain current highly regulates in antiparallel magnetization (broken curves). In practice, it might be difficult to achieve a spin polarization of 100% for the HMF S/D, as noted above, which would affect on the magnetocurrent characteristics (increase the current in antiparallel magnetization). Fig. 11(b) shows the calculated output characteristics of a spin-MOSFET using the ferromagnetic S/D with a spin polarization of 70% [31]. The magnetization-configuration-dependent output characteristics are established even in this case. In the ballistic transport condition, the magnetocurrent ratio (γ_{MC}) given by (1) increases with increasing gate bias V_G and decreasing drain bias V_{DS}. This behavior is adaptable to particular logic applications (nonvolatile bistable circuits), discussed later, in which γ_{MC} under a high V_G and low V_{DS} condition plays an essential role. A moderate γ_{MC} value of ~100% is sufficient for such nonvolatile bistable circuit applications: in the case of the ballistic conduction as shown in Fig. 11(b), this value would be achieved for the ferromagnetic S/D with a spin polarization of 70%–80% [31]. Therefore, HMFs are important as a high spin-polarization S/D material, since such a high spin polarization is inaccessible to ordinary ferromagnets. γ_{MC} depends on the Schottky barrier height of the ferromagnetic S/D [31]. Lower Schottky barrier heights are required for achieving high γ_{MC} and also high current drivability, as described previously. There is a possibility of a decrease in γ_{MC} when a spin flip of the conducting spin-polarized electrons occurs frequently in the channel. However, the remarkably long spin relaxation time in Si at room temperature described in the Section II-C would likely be able

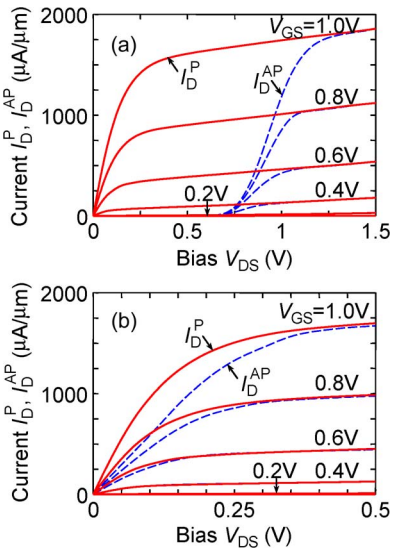


Fig. 11. *Calculated output characteristics of the spin MOSFET (a) with the HMF source/drain and (b) with the FM source/drain.*

to achieve a γ_{MC} value sufficient for circuit applications. The subthreshold leakage current of spin-MOSFETs depends on the magnetization configurations of the ferromagnetic S/D. In particular, when the leakage current is caused by direct tunneling from the source to the drain [147], it would be effectively suppressed by the antiparallel magnetization configuratuion of the HMF S/D.

In spin-MOSFETs, current-induced magnetization switching (CIMS) [101]–[103] is preferred for changing the magnetization configuration of the ferromagnetic S/D, as well as magnetoresistive devices such as CPP-SVs and MTJs. For instance, the CIMS can be performed by installing a CPP-SV (ferromagnet/nonmagnetic metal/ferromagnet) structure to the ferromagnetic drain (or source), in which one of the electrodes in the CPP-SV structure is the ferromagnetic drain (or source) and the other electrode is the pinned layer [i.e., the ferromagnetic drain (or source) is the free layer]. The CPP-SV structure is used as a CIMS device rather than a magnetoresistive device. In this structure, a parasitic resistance induced by the additional structure would be small and thus hardly deteriorate the transistor characteristics, since the spin valve structure consists of the fully metallic layers. Recently, CIMS was observed in a CPP-SV device with half-metallic electrodes, and the possibility of CIMS with a low current density was demonstrated [108].

C. Half-Metallic Source/Drain Technology

HMF S/D technology is an important steppingstone for developing spin-MOSFETs. Co-based full-Heusler alloys, such as Co_2FeSi (CFS), $Co_2FeSi_{1-x}Al_x$ (CFSA) and Co_2MnSi (CMS), are theoretically predicted and experimentally confirmed to exhibit the half-metallicity even at

temperatures greater than room temperature [148]–[155]. Recently very high TMR ratios were observed at room temperature in MTJs with full-Heusler alloy electrodes, and a very high spin polarization of the full-Heusler alloy electrodes, i.e., their half metallicity, was shown [153]–[155]. Therefore, full-Heusler alloys are a feasible candidate for the HMF S/D of spin-MOSFETs. The full-Heusler alloy electrodes of these MTJs were usually formed by a sputtering method at room temperature and successive thermal annealing. In order to establish ferromagnetic S/D technology for spin-MOSFETs adapted to the Si CMOS platform, HMFs should be formed by silicidation induced by rapid thermal annealing (RTA) that is a widely used technique in the present CMOS fabrication process. Full-Heusler alloys containing Si, such as CFS, CFSA and CMS, are considered to be silicides, and thus they could possibly be formed by RTA-induced silicidation. Takamura *et al.* proposed a RTA technique for full-Heusler alloy thin films using a silicon-on-insulator (SOI) substrate [156], [157], in which CFS thin films were formed by RTA-induced silicidation of a Co/Fe/SOI multilayer. Since the diffusion of the transition metal atoms is blocked by the buried oxide (BOX) layer of the SOI substrate, the stoichiometric composition can be achieved by adjusting the film thicknesses of the transition metal layers and the SOI layer. Note that a RTA technique was also applied to MTJs as a thermal annealing treatment [158]. It was confirmed that a high TMR ratio was also able to be achieved by the RTA technique.

The half-metallicity of full-Heusler alloys depends on the degree of order of the atomic arrangement in their structures. The most ordered structure is $L2_1$ (Fig. 12), and it well recognized that other disorder structures such as the *A*2, *B*2, and *DO*3 structures exist. The ordered structure hierarchy is $L2_1 - B2 - A2$, and the *DO*3 disorder is a kind of the *A*2 disorder. The atomic alignment of the $L2_1$ structure is highly important for the half-metallicity. The disordered structures induce gap states in the minority gap, resulting in degradation of the half-metalicity. Note that since CFSA can adjust its Fermi energy by the Al composition so as to lie near the center of the minority gap [150], [151], [159], it can exhibit a half-metallic band structure even in the B2 structure. This structural robustness of CFSA makes it attractive for device applications. The *A*2 and its related *DO*3 disorder structures significantly degrade the half-metallicity of full-Heusler alloys [150], [160]. Furthermore, it is difficult to distinguish the *DO*3 disorder structure from the $L2_1$ structure by the commonly used X-ray analysis. Recently, a new X-ray diffraction analysis technique that can distinguish these structures was developed, and it was revealed that RTA-formed CFS films have the $L2_1$ structure with a very small amount of the *DO*3 disorder [161].

A prototype spin-MOSFET was fabricated using RTA-formed CFS contacts for the S/D [162]. The dopant segregation technique [163] was used in order to reduce the Schottky barrier height of the CFS/Si junctions, i.e., an ion-implantation of As atoms with the relatively small energy and the successive RTA-induced silicidation of CFS was performed. The As atoms were expected to be segregated at the interface of the CFS/Si interface, resulting in the reduction of the barrier height. It was confirmed that the current drivability of the As-segregated device was much higher than that of a reference device without As-implantation. The dopant segregation technique also effectively achieved a high ON/OFF ratio of $\sim 10^5$, and reduced the subthreshold swing. Therefore, the dopant segregation technique would be applicable even for full-Heusler alloy/Si Schottky junctions. It is worthy to note that the RTA-induced formation technique of full-Heusler alloy thin films can also be applied to a tunnel contact with a $L2_1$-ordered full-Heusler alloy electrode [164] and an epitaxial germanidation of Ge-containing full-Heusler alloy (Co_2FeGe) thin films [165].

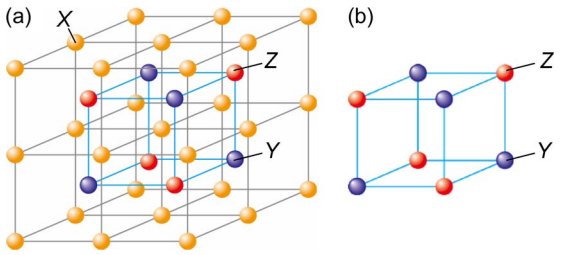


Fig. 12. ***(a) Fully ordered $L2_1$ sturucture of full-Heusler X_2YZ alloys, and (b) its inside sublattice.***

D. Pseudo-Spin-MOSFET Technology

The pseudo-spin-MOSFET (PS-MOSFET) is a circuit for reproducing the functions of spin-MOSFETs using an ordinary MOSFET and a MTJ [137], [138]. Fig. 13(a) shows the circuit configuration of the PS-MOSFET. A MTJ connected to the source of a MOSFET feeds back its voltage drop to the gate, and the degree of negative feedback depends on the resistance states of the MTJ. Therefore, the effective input bias V_{GS0} and also substrate (body-source) bias V_{BS0} can be varied by the magnetization configurations of the MTJ even under a constant gate bias (V_G) condition. Therefore, the PS-MOSFET can possess high and low current drivabilities that are controlled by the magnetization configurations of the MTJ, as shown in Fig. 13(b). In addition, magnetic-field-free CIMS for the MTJ can be established by increasing V_G, as shown in Fig. 13(c). (Note that a V_G value required for CIMS can be designed by the resistance of the MTJ and the size of the MOSFET. Therefore, the raised V_G is not indispensable for CIMS.) Thus, the PS-MOSFET can reproduce the spin transistor behavior and would be the most promising spin transistor based on the present MRAM technology. The desired γ_{MC} can be easily designed by adjusting the TMR and resistance of the MTJ. However, it should be noted that higher resistance values of the MTJ degrade the

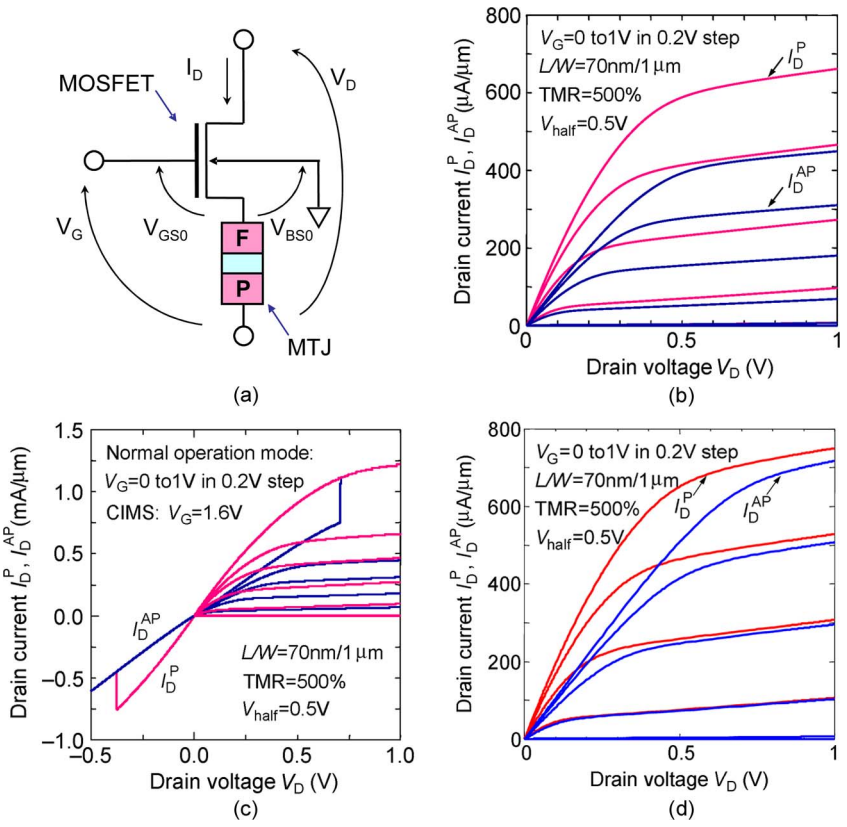


Fig. 13. *(a) Circuit configuration of pseudospin-MOSFET (PS-MOSFET), in which the free layer of the MTJ is connected to the source terminal of the MOSFET. (b) Simulated output characteristics and (c) CIMS behavior of the PS-MOSFET. (d) Simulated output characteristics of another type of PS-MOSFET in which the MTJ is connected to the drain side of the MOSFET. I_D^P and I_D^{AP} represent the drain currents in the parallel and antiparallel magnetization configurations, respectively.*

current drivability of the PS-MOSFET. Also note that when the MTJ is connected to the drain of the MOSFET, the difference in the drain currents between the parallel and antiparallel magnetization configurations decreases with V_{DS}, as shown in Fig. 13(d). This is due to the absence of the feedback effect. However, this causes other features, i.e., the drain currents are higher than those of the PS-MOSFET with the configuration of Fig. 13(a). CIMS is also applicable to this circuit configuration. Although both the configurations can act as spin transistors, the preferable configuration would depend on applications.

A prototype PS-MOSFET was fabricated using a MTJ with a full-Heusler alloy (Co_2FeAl; CFA) electrode and an MgO tunnel barrier [138]. Fig. 14(a) shows the output characteristics of the fabricated PS-MOSFET, in which the red and blue curves show the drain currents I_D^P and I_D^{AP} in the parallel and antiparallel magnetization configurations of the MTJ, respectively. The PS-MOSFET showed high and low current drivabilities that were controlled by the magnetization configurations of the MTJ, i.e., spin-transistor behavior. Fig. 14(b) shows the drain current as a function of magnetic field. The drain current well reflects the resistance change of the MTJ. γ_{MC} increased with decreasing V_D and also increased with increasing V_G. The maximun γ_{MC} value was as high as 45%.

As described above, spin transistors can be virtually realized by PS-MOSFET technology using the present MRAM technology. Design of PS-MOSFETs can be easily achieved using a general circuit simulator such as SPICE with an appropriate circuit model of MTJs [166]. Therefore, we can use spin transistors in logic circuits sooner rather than later, if the MRAM technology is applied to the CMOS logic platform.

V. FIELD-EFFECT SPIN TRANSISTORS II: DATTA–DAS SPIN-FET

A. Spin-Orbit Interaction

Spin-orbit interaction plays an important role in the realization of the electrical manipulation of electron spins. A moving electron in an electric field feels an effective magnetic field even without any external magnetic field. This effective magnetic field acts on the spin magnetic moment of the electron. These are essential for spin-orbit interaction. In III-V compound semiconductor

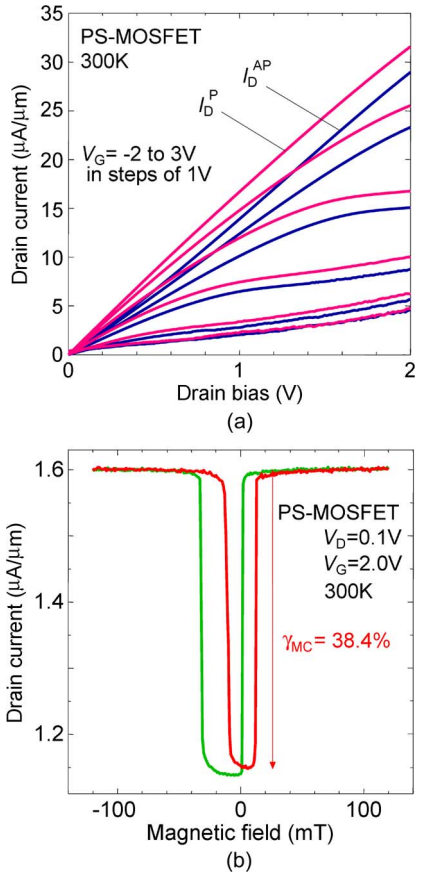


Fig. 14. *(a) Output characteristics of the fabricated PS-MOSFET at room temperature (RT). The drain currents are plotted as a function of drain bias V_D, where gate bias V_G varies from −2 to 3 V in steps of 1 V. Solid curves (I_D^P) and brokencurves (I_D^{AP}) show the drain currents in the parallel and antiparallel magnetization configurations, respectively. (b) Drain current as a function of magnetic field at RT, measured with $V_D = 0.1$ V and $V_G = 2$ V.*

heterostructures, the main contributions of the spin-orbit interaction are the Dresselhaus spin-orbit interaction caused by bulk inversion asymmetry (BIA) [167] and the Rashba (Bychkov–Rashba) spin-orbit interaction caused by structural inversion asymmetry (SIA) [168], [169]. The internal electric field of the Dresselhaus spin-orbit nteraction originates from the microscopic Coulomb potential gradient of the atomic core region, which is generally difficult to modulate. The strength of Dresselhaus spin-orbit interaction is considered to be a material-constant parameter. On the other hand, the internal electric field of the Rashba spin-orbit interaction originates from both the *microscopic* Coulomb potential induced by the atomic core and the *macroscopic* potential gradient caused by the heterointerface and the band bending in the semiconductor heterostructure [170]. Although the microscopic electric field is a material-constant parameter, as is the Dresselhaus spin-orbit interaction, the macroscopic electric field can be modulated by applying an external gate bias voltage on top of the two-dimensional electron gas (2DEG). This enables us to electrically control the effective magnetic field [171], [172]. It should be noted that the spin-orbit interaction effect in solids is much enhanced in contrast to that in vacuum. This is because the electric field near the atomic core is large and the electron wave function varies rapidly in space.

In vacuum, the spin-orbit interaction is described by the Thomas term in the Pauli equation

$$H_{SO} = -\frac{1}{2m_0c^2}\mu_B\sigma\cdot(\vec{p}\times\nabla V_0) = -\mu_B\sigma\cdot\left(\frac{\vec{p}\times\vec{E}}{2m_0c^2}\right). \quad (2)$$

Here μ_B, σ, and V_0 are the Bohr magneton, the Pauli spin matrix, and the scalar potential, respectively. In analogy to the Zeeman Hamiltonian, $H_Z = \mu_B\sigma\cdot\vec{B}$, the strength of effective magnetic field of the spin-orbit interaction is

$$B_{\text{eff}} = \frac{\vec{p}\times\vec{E}}{2m_0c^2}. \quad (3)$$

It is clear that the effective magnetic field is induced perpendicular to both the electron momentum and the electric field. In the relativistic quantum theory, $2m_0c^2$ is the energy gap between an electron and a positron, which is a negative energy particle with the negative mass predicted by Dirac. The energy scale of $2m_0c^2$ is ∼1 MeV; thus, the spin-orbit interaction is negligible for a particle with non relativistic momentum in a vacuum. On the other hand, in crystalline solids, the energy-band gap is reduced to ∼1 eV in typical semiconductors. Since the Dirac gap is replaced by the energy-band gap according to the $k\cdot p$ perturbation theory [170], it results in an enhancement of about six orders of the spin-orbit interaction in semiconductors.

The electron wave function in semiconductors is characterized by both a Bloch function and an envelope function. In the Bloch part, the electron wave is rapidly modulated by the atomic core potential, while the electron wave in the envelope part gradually modulates the rapidly oscillating lattice-periodic part of the Bloch function. Another origin of the enhancement of the spin-orbit interaction in semiconductors is due to the Bloch part, where both the electron momentum and the electric field are enlarged by the fast oscillation of the electron wave and the strong confinement near the atomic core, respectively [170].

In III-V semiconductor heterostructures, the spin degeneracy is lifted not only due to the BIA of the crystal structure, but also due to the SIA of the confining potential

of 2DEG quantum well (QW). Here, we focus on the Rashba spin-orbit interaction. The schematic band profile of QW is shown in Fig. 15. When the confinement potential of QW is symmetric as shown in Fig. 15, the Rashba spin-orbit interaction caused by macroscopic electric field in the QW is zero. By applying an external gate bias on top of 2DEG, the potential profile can be modulated, and the asymmetric QW potential causes a finite Rashba spin-orbit interaction that lifts the spin degeneracy. The advantage of the Rashba spin-orbit interaction is that the strength of spin-orbit interaction can be controlled by the gate voltage [171]. The Hamiltonian of the Rashba spin-orbit interaction in a 2DEG is

$$H_R = \alpha(k_x\sigma_y - k_y\sigma_x) \tag{4}$$

where α is the Rashba spin-orbit interaction parameter, σ_i $(i = x, y)$ are the x and y components of the Pauli spin matrix, and the x and y axes are parallel to the 2DEG plane. The Rashba spin-orbit interaction parameter α depends on the band parameters and the electric field in the QW. The spin splitting energy at the Fermi energy, $\Delta = 2\alpha k_F$, is calculated by (4), where k_F is the Fermi wave number. By comparing the Zeeman energy, an effective magnetic field is given by $B_{\text{eff}} = 2\alpha k_F/\mu_B$, and momentum difference between spin up and down at Fermi energy is described by $k_{F\uparrow} - k_{F\downarrow} = 2\alpha m^*/\hbar^2$, where m^* is an effective mass of electron and $\hbar$ is Planck's constant.

In III-V compound semiconductors, the electric field due to the ionized atoms in the crystal can be an origin of spin-orbit interaction in (2). This is so called Dresselhaus spin-orbit interaction. The derivation of Dresselhaus spin-orbit interaction is obtained from the $\mathbf{k}\cdot\mathbf{p}$ perturbation theory based on Hamiltonian with 14×14 matrix and is too complex. Here, the linear Dresselhaus spin-orbit interaction is given by the following equation.

$$H_D = \beta(k_x\sigma_x - k_y\sigma_y). \tag{5}$$

The Dresselhaus cubic term is negligible when the QW confinement k_z is larger than Fermi momentum.

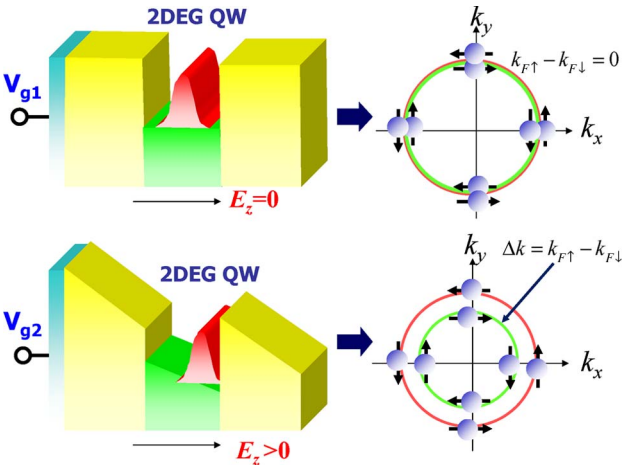


Fig. 15. *Electrical control of the Rashba spin-orbit interaction. The band profile of QW can be tuned by an external gate bias voltage. When the QW potential is symmetric, the Rashba spin-orbit interaction caused by an electric field in QW is zero and spin states are degenerated. An asymmetric potential profile in QW by tuning the gate voltage lifts the spin degeneracy since the electric field in QW is finite. The spin configuration at Fermi energy is shown in right bottom figure. Fermi momentum difference* $\Delta k = k_{F\uparrow} - k_{F\downarrow}$ *between spin up and down is proportional to the Rashba spin-orbit interaction parameter* α.

B. Spin Relaxation and Its Suppression

In epitaxially grown III-V compound QWs such as GaAs and InGaAs, the DP mechanism is generally dominant for spin relaxation. This is because the DP mechanism works in semiconductors without a center of inversion symmetry. The Rashba spin-orbit interaction causes an effective magnetic field B_{eff} which is pointing perpendicular to the momentum direction in the 2DEG plane. The spin of electrons is precessing around the effective magnetic field B_{eff}. In a diffusive 2DEG, the momentum direction of electron changes frequently, and hence so does the direction of B_{eff}. Due to the random change in B_{eff}, the spin orientation is randomized and the spin loses the memory of its initial spin direction. This spin relaxation process is called the D'yakonov-Perel (DP) spin relaxation mechanism [91]. The DP spin relaxation is caused not only by the Rashba spin-orbit interaction but also by the Dresselhaus spin-orbit interaction. Generally speaking, the DP spin relaxation is expected if the system has momentum dependent effective field B_{eff} due to spin-orbit interaction spin splitting energy Δ.

From the above DP spin relaxation picture, we can estimate the spin relaxation time. The spin is initially precessing around a certain effective magnetic field direction with a typical frequency of $\omega = \Delta/\hbar$ and during a typical scattering time τ. After a scattering event, the direction of B_{eff} is randomly changed, and the spin starts to precess around the new B_{eff} direction. Hence, after a certain number of scattering events there is no correlation anymore between the initial and final spin states. The precise time scale on which the spin loses its memory depends on the typical spin precession angle between scattering events $\delta\phi = \omega\tau = \Delta\tau/\hbar$. For $\delta\phi \ll 1$, the precession angle is small between succeeding scattering events, so that the spin vector experiences a slow angle diffusion. During a time interval t, the number of random steps is $N = t/\tau$. For uncorrelated steps in the precession angle, the spread

of the phase will be given by the standard deviation $\phi = \delta\phi\sqrt{N}$. We will call the spin relaxation time τ_s the time at which the standard deviation becomes $\phi \approx 1$. Therefore, we get $(\delta\phi)^2(\tau_s/\tau) = 1$, and the spin relaxation time is given by $\tau_s \approx \hbar^2/\Delta^2\tau$.

Gate controlled spin-orbit interaction which gives rise to an effective magnetic field provides an electrical way to manipulate spins. On the other hand, a momentum-dependent effective magnetic field due to the spin-orbit interaction randomizes spin orientations after several momentum scattering events. The spin-orbit interaction is a double-edged sword because it can be used for spin manipulation, however, at the same time it causes spin relaxation. Therefore, it is very crucial to suppress the spin relaxation while keeping the strength and the controllability of spin-orbit interaction. One of the ways to suppress spin relaxation is to confine electrons to moving one-dimensionally by narrow wire structures whose width is less than bulk spin diffusion length L_{SO} due to Rashba spin-orbit interaction. This suppression of spin relaxation due to lateral confinement effect have theoretically investigated [173], [174] and have experimentally demonstrated with optical way [175] and weak anti-localization analysis [176], [177].

Most effective way to suppress the DP spin relaxation is to utilize the so-call persistent spin helix (PSH) condition [131], [178], where the Rashba spin-orbit interaction strength α is equal to linear Dresselhaus spin-orbit interaction β. In this PSH condition, spin polarization is conserved even after scattering events. This conservation is predicted to be robust against all forms of spin-independent scattering, including electron-electron interaction, but is broken by spin-dependent scattering and cubic Dresselhaus term. Recently, the PSH in semiconductor quantum wells was confirmed by optical transient spin-grating spectroscopy by Koralek *et al.* [179]. They found enhancement of spin life time by two orders magnitude near the exact PSH point. This experimental demonstration is a breakthrough toward minimizing and controlling spin relaxation.

C. Operating Principle and Performance of the Spin-FET

The spin-orbit interaction provides a novel functionality in the spin field-effect transistor (spin-FET) proposed by Datta and Das [41]. Shown in Fig. 16 is the schematic of the spin FET which consists of FM source and drain electrodes and 2DEG channel with the Rashba spin-orbit interaction. The spin polarized carrier should be injected from FM source electrode and transported spin polarized carrier should be detected by FM drain electrode. The key idea of the spin-FET is that the spin orientation can be controlled by the gate electric field instead of the external magnetic field. This gate controlled spin orientation is possible if the Rashba spin-orbit interaction works in the

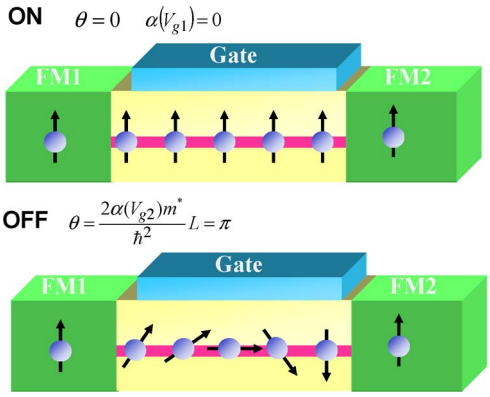


Fig. 16. *Operational principle of spin FET. The key idea of the spin-FET is that the spin orientation can be controlled by the gate electric field instead of the external magnetic field. This gate controlled spin orientation is possible if the Rashba spin-orbit interaction works in the semiconductor 2DEG channel. When the Rashba spin-orbit interaction is zero as shown in top figure, the injected spin polarized carrier is transported without spin precession. Then, drain current is expected since the transported carrier has the same orientation as the FM drain electrode. To make OFF-state, the injected spin polarization in SM 2DEG channel can be reversed by the gate voltage which can tune the Rashba spin-orbit interaction parameter.*

semiconductor 2DEG channel. The spin precession angle $\Delta\theta$ is given by

$$\Delta\theta = \frac{2\alpha m^*}{\hbar^2}L. \tag{6}$$

Here α is the strength of Rashba spin-orbit interaction, m^* is effective mass of electron, $\hbar$ is the Planck's constant, and L is the channel length. When the Rashba spin-orbit interaction is zero as shown in Fig. 16(a), the injected spin polarized carrier is transported without spin precession. Then, drain current is expected since the transported carrier has the same orientation as the FM drain electrode. To make OFF-state, the injected spin polarization in SM 2DEG channel can be reversed by the gate voltage which can tune the Rashba spin-orbit interaction parameter α. Realistic calculation for current modulation in the spin FET device was done by Pala *et al.* [180]. Current modulation due to spin precession is washed out by integration of injection angle. It suggests that a quasi-one dimensional channel is desired to have better performance.

The channel of spin FET should be ballistic since the effective magnetic field is changed after a scattering event. An alternative spin FET which is robust against scattering has been proposed [131], [181] by using the PSH condition. For $\alpha \neq \beta$, the injected spin polarized carriers are randomized because of scattering as shown Fig. 17. When the strengths of the Dresselhaus spin-orbit interaction and the Rashba spin-orbit interaction are balanced, the direction of

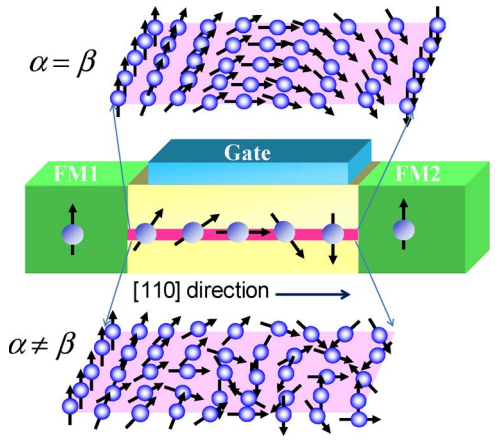


Fig. 17. *Nonballistic spin FET using both Rashba and Dresselhaus spin-orbit interactions. Spin coherent transport is robust against spin-independent scattering when the Rashba spin-orbit interaction parameter is equal to the Dresselhaus spin-orbit interaction parameter.*

effective magnetic field due to spin-orbit interactions becomes uniaxial along $[1, -1, 0]$ orientation and independent of momentum direction. The coherent spin precession even in a diffusive channel is realized for $\alpha = \beta$ case which can be tuned by controlling the Rashba spin-orbit interaction parameter α.

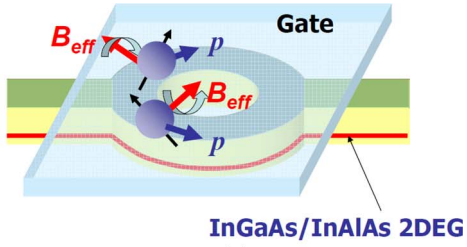
Comparison of performance between the Datta–Das type spin FET and MOSFET is discussed by Bandyopadhyay *et al.* [136]. They suggest that the performance of the spin FET is limited by the channel length needed to make the injected spin polarization reverse. This is because the control of Rashba spin-orbit interaction parameter α by gate electric field is limited in n-channel semiconductor. To make a channel length shorter, it is better to use narrow gap semiconductors such as InAs or InSb. The Rashba parameter α in InGaAs based heterostructures is $1 - 10 \times 10^{-12}$ eVm [35]. According to the above (6), the channel length of spin FET is 260 nm to make π rotation of injected spin orientation with $\alpha = 10 \times 10^{-12}$ eVm and effective mass $m^* = 0.05$. By using PSH condition, the total effective magnetic field induced both by the Rashba spin-orbit interaction and the Dresselhaus spin-orbit interaction is double, reducing the length by half. It is suggested that a better performance in a p-type spin FET with holes can be expected because of larger spin-orbit interaction value and gate controllability [132]. The channel length of p-type spin FET is expected to be as few 10 nm order as the present ordinary FET.

D. Gate Controlled Spin Precession

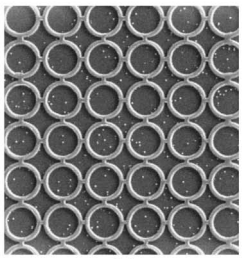
Electrostatic manipulation of spins is of crucial for spintronics. A spin-interference device was proposed to investigate the gate controlled spin precession angle [182]. The schematic structure of the spin interference device is shown in Fig. 18(a). The spin interference can be expected in an Aharonov–Bohm (AB) ring with Rashba spin-orbit interaction because the spins of electrons precess in opposite directions between clockwise and counter clockwise travelling directions in the ring. The relative difference in spin precession angle at the interference point causes the phase difference in the spin wave functions. The gate electrode, which covers the whole area of the AB ring, controls the Rashba spin-orbit interaction, and therefore, the interference. The advantage of this proposed spin-interference device is that conductance modulation is not washed out even in the presence of multiple modes.

The conductance for electrons travelling halfway around the ring at $B_z = 0$ is given by

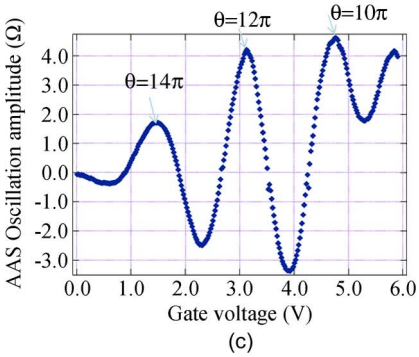
$$G = \frac{e^2}{h}\left[1 - \cos\left\{\pi\sqrt{1 + \left(\frac{2rm * \alpha}{\hbar^2}\right)^2}\right\}\right]. \quad (7)$$



(a)



(b)



(c)

Fig. 18. *(a) Schematic of spin interference device. (b) A SEM picture of an array of rings with 1-μm radius using InGaAs heterostructure. (c) Spin interference controlled by gate voltage on top of the ring array. The oscillation period is consistent with the gate voltage dependence of Rashba spin-orbit interaction parameter. The precession angles are shown in figure.*

Here r is the radius of AB ring. This equation shows that the conductance of the ring oscillates as a function of the strength α of Rashba spin-orbit interaction. This spin-orbit interaction dependence is very similar to the conductance of the spin-FET proposed by Datta and Das, in which they need ferromagnetic electrodes for spin injection and detection. This proposed spin interferometer works without ferromagnetic electrodes.

The spin interference was experimentally demonstrated in small arrays of mesoscopic semiconductor InGaAs rings [183] as shown in Fig. 18(b). By using an electrostatic gate the spin precession rate and the spin phase differences over several interference periods were confirmed at $T = 0.3K$. The second harmonic of the spin interference, oscillating with half the period was also observed. The observed spin interference phase in Fig. 18(c) was consistent with the gate controlled spin-orbit interaction parameter. The precise spin precession control is important in order to realize semiconductor spintronics devices based on spin-orbit interaction, e.g., the Datta–Das transistor.

Recently it was reported that the Datta–Das type spin field-effect transistor was demonstrated below 77K using ballistic InAs 2DEG channel with strong Rashba spin-orbit interaction [184]. They observed an oscillatory channel conductance as a function of gate voltage on top of InAs when the magnetization directions of NiFe injector and detector electrodes are perpendicular to the Rashba effective field. On the contrary, the oscillatory conductance was suppressed when two FM electrodes magnetizations are parallel to the Rashba field.

However, some papers [185]–[187] claim that the experimentally observed amplitudes of spin signal in both parallel and perpendicular magnetizations of FM electrodes can be possible only for one dimensional semiconductor channel. The oscillation amplitude does not increase but gets weaker with increasing mean free path by carrier density. Further experimental study will be required.

VI. INTEGRATED CIRCUIT APPLICATIONS

A. Classification of Nonvolatile Logic

The most attractive applications of spin transistors would be in highly functional logic circuits, although the spin transistors are also applicable to nonvolatile memory. In this section, we discuss nonvolatile logic and reconfigurable logic applications of spin devices including spin transistors. The former is described in Section VI-A and B and the latter in Section VI-C.

Nonvolatile logic is a generic name for logic gates and logic systems that maintain their state despite a power shutdown/failure by using nonvolatile memory or its elements. Nonvolatile logic can be classified into two categories, i.e., 1) logic systems with nonvolatile storage/latch circuits [166], [188] and 2) logic gates that have a type of nonvolatile latch (these are sometimes called nonvolatile logic gates) [189]–[191]. In general, logic systems consist of logic gates and storage/latch circuits, as shown in Fig. 19(a). In the approach 1), only storage circuits (such as caches and registers) and latches are nonvolatilized, as shown in Fig. 19(b). On the other hand, for the approach 2), individual logic gates have a type of nonvolatile latch for input/output data, as shown in Fig. 19(c), which is also referred to as a logic-in-memory architecture. In the approach 2), the logic gates can be comprised of MOS devices and nonvolatile memory elements. The state of the nonvolatile memory elements is used for logic operations so that the logic gates hold input and/or output data without losing them. This method has the following secondary features: The number of transistors in nonvolatile logic gates can be reduced in comparison with their equivalent CMOS design, and computational results will remain in the gates even during an accidental power shutdown. However, nonvolatile logic gates have high energy consumption, since logic operations require rewriting the data in the nonvolatile memory elements at each operation. The energy consumption of data rewriting in nonvolatile memory elements is generally much higher than that of switching operation in ordinary CMOS gates. Therefore, this approach is more suitable for special applications, in which data in the logic gates will not frequently be rewritten. Recently, the energy-performance of nonvolatile logic

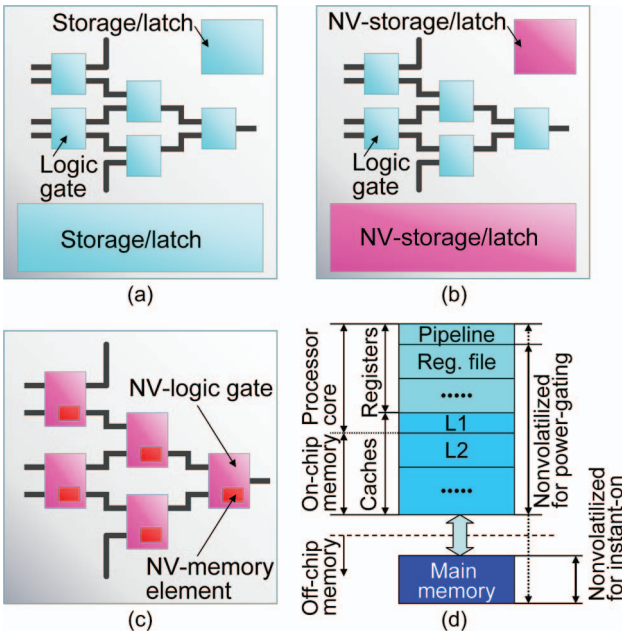


Fig. 19. *(a) Ordinary logic system configured by logic gates and storage/latch circuits, (b) nonvolatile logic system with nonvolatile storage/latch circuits, and (c) nonvolatile logic system configured by nonvolatile logic gates. (d) Hierarchical memory system used in an ordinary/power-gating/instant-on microprocessor.*

gates was evaluated in comparison with its equivalent CMOS design [192].

One of the key factors for the remarkable development of microprocessors is the so-called hierarchical memory system architecture [Fig. 19(d)] that enables high speed operations in spite of its totally large capacity. The hierarchical memory structure is still essential even when microprocessors are comprised of nonvolatile logic gates [approach 2); see Fig. 19(c)], and thus nonvolatile logic gates would be redundant for microprocessor applications. Nevertheless, the concept of nonvolatile logic systems with nonvolatile storage/latch circuits [approach 1); see Fig. 19(b)] can completely comply with the hierarchical memory structure of microprocessors, and leads to the promising low-power architecture described in Section VI-B.

B. Power-Gating Applications for Nonvolatile Logic Systems

In recent years, power dissipation has been one of the most important concerns for highly integrated CMOS logic circuits, such as microprocessors and systems-on-chip (SoCs) [193], [194], since it constrains the performance and the degree of device integration. In general, power dissipation in CMOS logic circuits can be divided into two factors, i.e., dynamic and static power. The former is caused by ON-currents passing through the CMOS logic gates due to logic operations, and the latter by leakage currents in the CMOS gates even during standby mode in which no logical operations are executed. The magnitude of the leakage current for each individual transistor is exponentially small in comparison with the ON-current. However, the static power dissipation gives rise to severe problems for CMOS logic circuits owing to their very large scale integration. Recently proposed power-gating architectures based on multithreshold voltage CMOS (MTCMOS) technology [195]–[198] are expected to be very effective at reducing the static power dissipation in CMOS logic circuits. In this type of architecture, logic circuits on a chip are partitioned into several circuitry domains, so-called power domains that are electrically separated from power-supply lines and/or ground lines by sleep transistors. These domains can be shut down during their standby mode, and the static power is thereby considerably reduced by the power management of the individual domain even during system run-time. A key technology for realizing power-gating systems is the backup of logic information in power domains. Registers and caches that are configured by flip-flops (FFs) and static random access memory (SRAM) arrays, respectively, are used in microprocessors and SoCs as important storage circuits. However they cannot be shutdown without losing their logic data. Therefore, several architectures were developed for realizing power-gating systems, e.g., a regulated power supply for FF/SRAM, data transfers from FF to backup devices through purpose-built interconnects or a commonly used bus line, and balloon FF technology with dual power rails. Although power-gating systems have already been developed with these techniques, disadvantages exist depending on architecture used to achieve power-gating, e.g., nonzero static power dissipation, the addition of purpose-built interconnects for data transfer, extra time for data transfer using a bus line, excess area occupation for backup devices, and greater layout/control complexity due to the dual power rails. These disadvantages would be solved by introducing of nonvolatile SRAM (NV-SRAM) and nonvolatile FF (NV-FF) into power-gating systems [166], [199], [200], as shown in Fig. 20, in which the NV-SRAM arrays and the NV-FFs are applied to the hierarchical memory system. Other registers/latches used in the power-gating systems, such as configuration/context registers, are also nonvolatilized using NV-FFs and related nonvolatile latches (NV-LATs). A concrete architecture for the nonvolatile hierarchical memory system is discussed later.

NV-SRAM and NV-FF circuits can be configured by connecting resistive or capacitive nonvolatile memory elements to the bistable circuit (inverter loop circuit) that is the basic circuit of SRAM and FF cells [201]–[211]. Fig. 21(a)–(c) shows representations of nonvolatile bistable circuits using resistive nonvolatile memory elements, such as MTJs. In these circuits, logic information in the bistable circuit can be stored in the nonvolatile memory elements before suspending operation (or at each execution operation of the bistable circuit). The information stored in the nonvolatile memory elements can be restored to the bistable circuit by the recovery of the power supply. NV-SRAM and NV-FF cells can be configured by these nonvolatile bistable circuits. Nevertheless, the nonvolatile

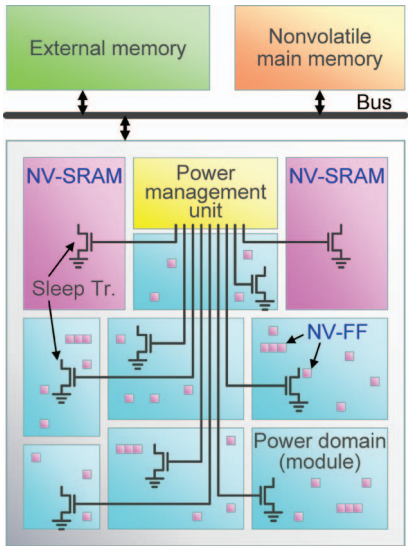


Fig. 20. *Schematic view of a nonvolatile power-gating processor/SoC.*

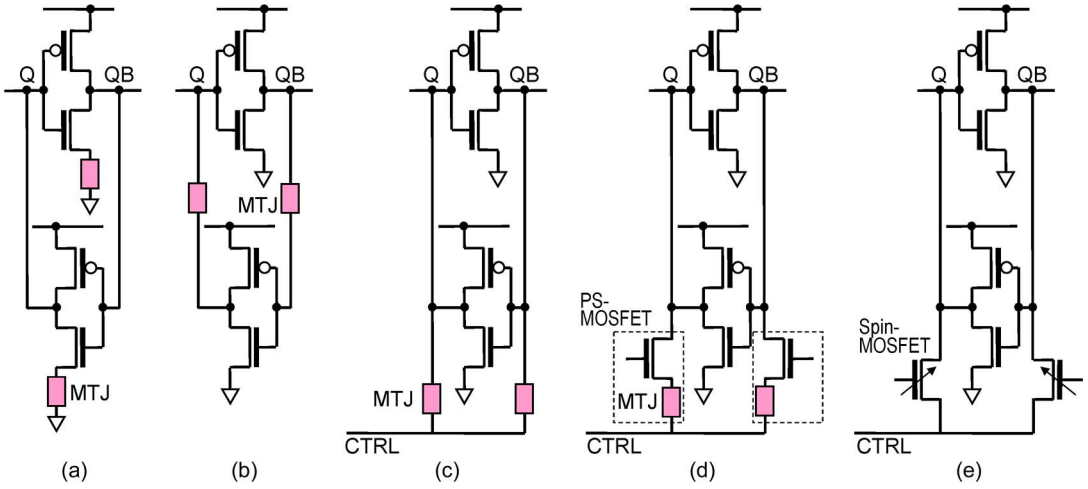


Fig. 21. *Schematic representations of nonvolatile bistable circuitries, in which the MTJs are connected (a) to the source terminal of the inverters, (b) in the inverter loop, and (c) between the storage nodes (Q and QB) and the CTRL line. Nonvolatile bistable circuitries configured by (d) pseudo-spin-MOSFETs (PS-MOSFETs) and by (e) spin-MOSFETs.*

memory elements connected to the cell will deteriorate the circuit performance of NV-SRAM and NV-FF circuits, such as degrading the operating speed, variability tolerance, and static noise margin and also increasing the power dissipation during normal SRAM/FF operations. In order to overcome these problems, a new approach using spin transistors (spin-MOSFETs and PS-MOSFETs) was proposed [166], [199], [200], as shown in Fig. 21(d) and (e). Since the spin transistors can separate the bistable circuit from the nonvolatile memory elements (spin transistors themselves), they have very little deleterious effects on the bistable circuit operation.

Fig. 22(a) shows the circuit configuration of a NV-SRAM cell, in which two PS-MOSFETs are connected to the storage nodes of a standard SRAM cell [166], [199]. When the cell is powered off, the store operation is executed, i.e., data on the storage nodes are stored into the MTJs in the PS-MOSFETs by CIMS. This can be done only by the application of a pulse signal to the CTRL line after the PS-MOSFETs are turned on. After the store operation, the cell can be shut down without losing its logic information. In the case of a restart, the stored data in the MTJs can be restored to the storage nodes by the restore operation in which only the power supply of the inverter loop is pulled up after the PS-MOSFETs are turned on. Since the PS-MOSFETs are turned on only during the store and restore operation modes, currents passing through the MTJs can be completely shut off during the normal SRAM operation mode. NV-LAT and NV-FF circuits can also be configured using PS-MOSFETs in the same manner as the NV-SRAM cell [200]. Fig. 22(b) shows a positive edge triggered masterslave nonvolatile delay-FF (NV-DFF) that consists of a conventional LAT and an NV-LAT, as indicated in the figure. These NV-SRAM and NV-DFF cells have the following features. 1) They can be completely powered off without losing their logic information. 2) The performance of the normal SRAM/DFF operations is hardly degraded, since the PS-MOSFETs can be electrically separated from the bistable circuit. 3) The store/restore operations are quite simple. 4) A moderate TMR

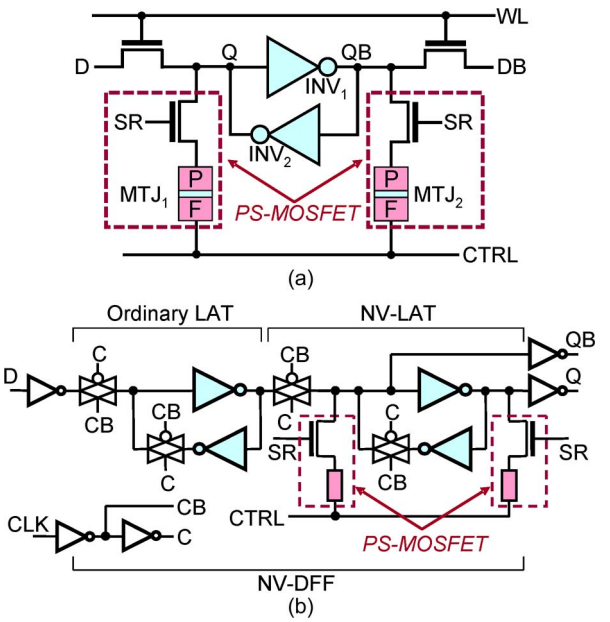


Fig. 22. *Circuit configurations of (a) NV-SRAM and (b) NV-DFF cells using PS-MOSFETs. The direction of the MTJs depends on the power-gating architecture, i.e., the pinned layer of the MTJs is connected the source terminal for the virtual V_{DD} architecture, and the free layer of the MTJs is connected the source terminal for the virtual ground architecture.*

ratio of ~100% and a moderate V_{half} value of ~100 mV are sufficient for the restore operation (a high TMR ratio and a large V_{half} value for the MTJs are not required).

For the application of the NV-SRAM and NV-DFF circuits to power-gating systems, it is important to evaluate the efficiency of power gating for power consumption. Break-even time (BET) is one of important indices of performance for power gating [200], [212], [213]. BET is defined by a shutdown period so that the extra energy required for power-gating operations (such as the store and restore operations) is equal to the static energy not wasted during the shutdown period. Therefore, when the NV-SRAM/NV-DFF cells require a large amount of energy for the store and restore operations, the BET becomes long. If the shutdown period is shorter than the BET, the consumption energy is increased by the power-gating operations. In the NV-SRAM/NV-DFF circuits, most of the BET is dominated by the energy required for CIMS of the MTJs in the cells. Therefore, a reduction of the threshold current for the CIMS is important for shortening the BET. Recently, the BET of the NV-SRAM and NV-DFF cells was analyzed [200], [214]. For the NV-SRAM cells, the calculated BET (ranging from a few microseconds to several tens microseconds) was confirmed to be acceptable for general coarse-grained power-gating architectures. It was also shown that the NV-DFF circuits had a much shorter BET adapted to fine-grained power gating.

A nonvolatile power-gating multicore microprocessor was proposed [215]: it uses nonvolatile caches and nonvolatile registers which are configured by NV-SRAM arrays and NV-FFs, respectively, as shown in Fig. 19(d). The register file, program counter, other program control registers, configuration registers, and higher level caches in the processor cores are nonvolatilized, which is required for core-level power gating. Data in these registers are strongly needed to rapidly restart suspended processing jobs. The nonvolatile higher level caches are also useful for rapid restart to avoid pipeline stalls due to cache misses. However, the pipeline registers should be comprised of ordinary volatile FFs in order to retain the high operating speed (clock frequency) of the critical path. The lower level caches and other configuration resisters in the entire chip are also nonvolatilized for chip- or module-level power gating. In particular, the power gating for the lower level caches is important, since the lower level cashes have high static power dissipation owing to their high degree of device integration. Fine-grained power gating (execution-unit-level power gating in each core and module) can also be established by this processor system. The main memory of the system should also be nonvolatilized, which requires high-density, large-capacity, and low-power nonvolatile memory. The nonvolatile main memory is beneficial for system-level power gating, since it requires no program/data loadings from the external memory (such as a hard disk drive) for system rebooting. Recently, an instant-on (or normally-off) architecture using nonvolatile memory has received renewed interest [216]. Power gating is a superordinate concept inevitably including this architecture, as described above. Instant-on architectures without power gating can be simply achieved with nonvolatile main memory, in which the processor core need not be nonvolatilized [216], [217], as shown in Fig. 19(d). Note that in contrast to power-gating architectures, normally-off architectures with instant-on ability have no effect on the reduction of static power during system run-time.

C. Reconfigurable Logic Applications

Reconfigurable logic applications of spin devices can be classified into the following categories: 1) field programmable gate arrays (FPGAs) constructed by nonvolatile lookup tables (NV-LUTs) that are comprised of spin devices [218]–[223], and 2) reconfigurable logic gates consisting of spin devices and ordinary MOS devices without NV-LUTs [224].

An FPGA consists of configurable logic blocks (CLBs) and programmable connection/switch blocks. In the most general FPGA architectures, each CLB has a lookup table (LUT). The FPGA uses preset "data" for the results (truth table) of logic operations that are stored in LUTs (i.e., logic operations through logic gates are not required). In general, LUTs are configured by SRAM or flash memory. When SRAM is used for LUTs, data in the LUTs disappears with the power shutdown, i.e., the data must be reloaded whenever booting up the system. Therefore, NV-LUTs are attractive owing to the data-reload-free feature for rebooting and thus to instant rebooting. NV-LUTs are considered to be a suitable application of the MRAM technology [50]–[55]. Several types of NV-LUT using MTJs were proposed [218]–[223]. An interesting configuration of the NV-LUTs is that SRAM cells in an ordinary LUT are replaced by MTJs. The number of transistors in the NV-LUT and also the occupied area can be reduced in comparison with ordinary SRAM-based LUTs. However, in this type of NV-LUT, a sense amplifier is required for reading the stored contents of the MTJs. Therefore, the performance, in terms of speed, dynamic/static power, and occupied area merit, would depend on the TMR ratio of the MTJs, since a lower TMR ratio requires a larger sense amplifier for the assured readout operation. In particular, the speed and energy consumption for the readout operation would depend on the design of the sense amplifier. NV-LUTs enable them to be shut down without losing their data during standby mode, which is expected to effectively reduce the static power in an FPGA. Although NV-LUTs can be applied to power-gating architectures [222], a concrete power-gating architecture using MTJ-based NV-LUTs has not been proposed yet. It should be noted that NV-LUTs can also be realized using flash memory technology, and instant-on FPGAs based on this technology are commercially available.

One of the important applications of FPGA is dynamically reconfigurable logic architectures. An FPGA whose

configurations can be changed during runtime is called a dynamically programmable gate array (DPGA). A dynamical reconfiguration capability based on LUTs with a feature of high-speed writing is essential for DPGAs. Therefore, SRAM-based LUTs are used for this application owing to their high speed writing capability. On the other hand, flash-based NV-LUTs would not be suitable for a DPGA because of the low writing speed caused by their constituent flash memory. Nevertheless, MTJ-based NV-LUTs would be applicable to a DPGA owing to their high speed writing ability [220]–[222].

The NV-SRAM architecture based on PS-MOSFETs (or spin-MOSFETs) [166], [199], [200] (described in Section VI-B) would be an alternative approach for realizing a NV-LUT. Although the occupied area of the NV-LUTs cannot be reduced by this approach, the excellent compatibility with the present SRAM-based LUT technology, including the sense-amplifier-free circuit configuration, is attractive. In addition, the nonvolatile and reconfigurable capabilities of the NV-LUT are also suitable for the power-gating architecture of FPGAs/DPGAs. Power gating is also a powerful method for the static power reduction of FPGAs/DPGAs [225], as well as microprocessors and SoCs. In order to achieve the ideal power gating for FPGAs/DPGAs, nonvolatile CLBs (NV-CLBs) and nonvolatile programmable connection/switch blocks are anticipated [226]. In general, CLBs are constructed by a LUT, a DFF for the output latch, and a multiplexer for selection of the sequential/combinational circuit output. Not only the LUT but also the output DFF and the output multiplexer should be nonvolatilized for NV-CLBs, These nonvolatile components of NV-CLBs can be configured by the NV-SRAM and NV-DFF circuits [226]. The programmable connection/switch blocks can also be nonvolatilized by the NV-SRAM cells. Note that for the ideal power gating, each NV-CLB should have an NV-DFF for the output latch from the following reason: when sequential circuits are implemented by CLBs, the operation result of each CLB is stored in the output DFF and would be frequently updated during its execution. These output data of the CLBs are required for the quick restart after suspending.

Spin transistors are also applicable to reconfigurable logic gates in which the logic functions of the hardware can be switched by the magnetization configuration of the spin transistors, i.e., the above-described approach 2). It is known that reconfigurable logic gates can be configured by current-drivability-variable transistors such as neuron MOSFETs [227], [228]. In a manner analogous to neuron MOSFETs, reconfigurable logic gates configured by spin-MOSFETs (or PS-MOSFETs) were proposed [224]. The gates can be shut down without losing their logic functions, since the logic functions are determined by the nonvolatile magnetization configuration of the constituent spin-MOSFETs. However, the circuit speed severely deteriorates when the current drivability of the spin-MOSFETs is low. Furthermore, the gate-level reconfiguration could be highly redundant for general applications. Reconfiguration capability for functional logic blocks/units such as LUT-based CLBs would be more suitable for reconfigurable logic systems than individual reconfigurable logic gates.

VII. CONCLUSION

In this article, we have reviewed the current status and outlook of various spin transistors from the viewpoint of integrated circuit applications. The spin transistors are a potential building block for novel integrated circuits employing spin degrees of freedom. The interesting features of spin transistors are nonvolatile information storage and reconfigurable output characteristics, which are very useful functionalities for new integrated circuit architectures that are inaccessible to ordinary transistor circuits. The spin transistors would open the door to a new development direction for integrated circuit electronics. Nonvolatile logic and reconfigurable logic architectures employing spin transistors would be a promising path for spintronic integrated circuits. ■

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