





AUO PM

CUSTOMER APPROVAL SHEET

C	Company Name	
	MODEL	A090XE02 V3
	CUSTOMER	0)
	APPROVED	
		TIONS ONLY (Spec. Ver. <u>0.3)</u> TIONS AND ES SAMPLE (Spec. Ver. <u>0.3)</u> TIONS AND CS SAMPLE (Spec. Ver. <u>0.3)</u>
P/N : Kei P/N : <u>9</u> Commen	4.09A04.301	

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0.3
38
2012/02/02

Product Specification

9" EPD MODULE

Model Name: A090XE02 V3

Planned Lifetime: From 2011/May. To 2012/Nov.

Phase-out Control: From 2012/May. To 2012/Nov.

EOL Schedule: 2012/Nov

< ◆ >Preliminary Specification

< >Final Specification

Note: The content of this specification is subject to change.

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Record of Revision

Version	Revise Date	Page	Content
0.0	2011/06/15	All	First Draft.
		25	Modify reliability test criteria.
		4	General Information, weight
0.1	2011/11/15	5,6	Ddrawing
		21	Panel Power Consumption
		27	Module/Panel Label Information
0.2	2012/1/12	22	Modify contrast Ratio
0.2	2012/1/12	22	Modify update Time
		7, 8	Modify pin assignment description
		11	Modify Operation rating
0.3	2012/02/02	12	Modify Panel Power consumption
0.3	2012/02/02	17	Modify VCOM_OUT voltage definition, VCOM relationship
		20, 21	Modify power on/off sequence
		29, 30	Modify appilcation circuit
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6.2 Sensing Periodical Mode (INT_MODE[1:0] = [0,0])			36
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A. General Information

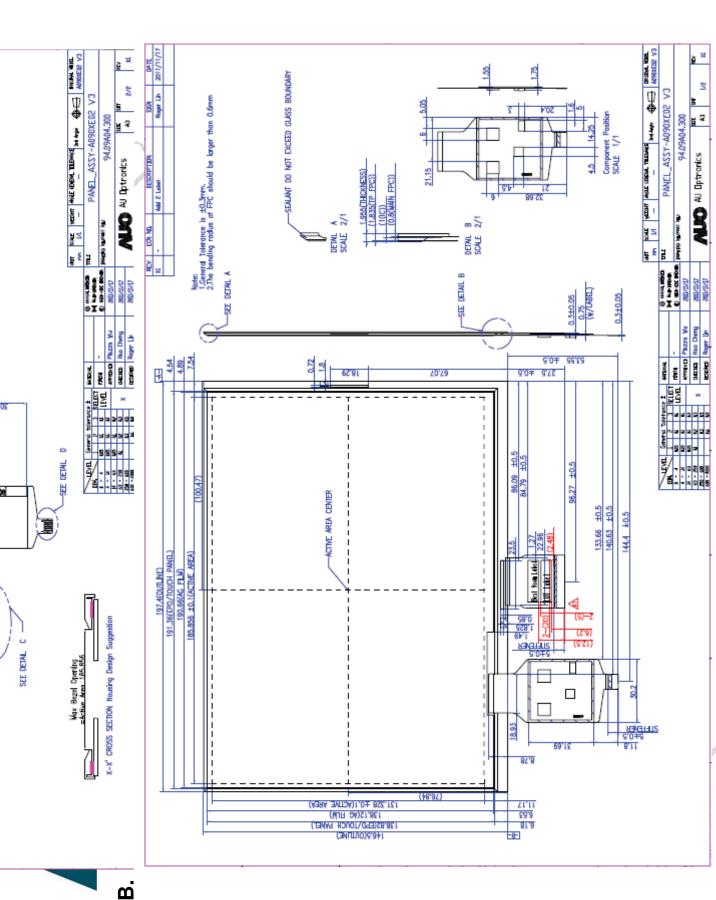
This display is a active matrix electrophoretic display (EPD), which comprises a-si TFT substrace, electrophoretic front plane, protective anti-glare top-sheet, driver ICs, and FPC. It is designed for applications such as e-book or e-reader.

NO.	Item	Unit	Specification	Remark
1	Screen Size	inch	9 (Diagonal)	
2	Display Resolution	dot	1024 (H)× 768(V)	
3	Overall Dimension	mm	197.4(H) × 147.5(V) × 1.955(T)	Note 1
4	Active Area	mm	185.86(H)×131.33(V)	
5	Dot Pitch	mm	0.1815 (H)x 0.171(V)	
6	Gray level		16	
7	Weight	g	121	
8	Surface Treatment		AG (7.5 ± 2%) Hard coating(3H)	Note 2

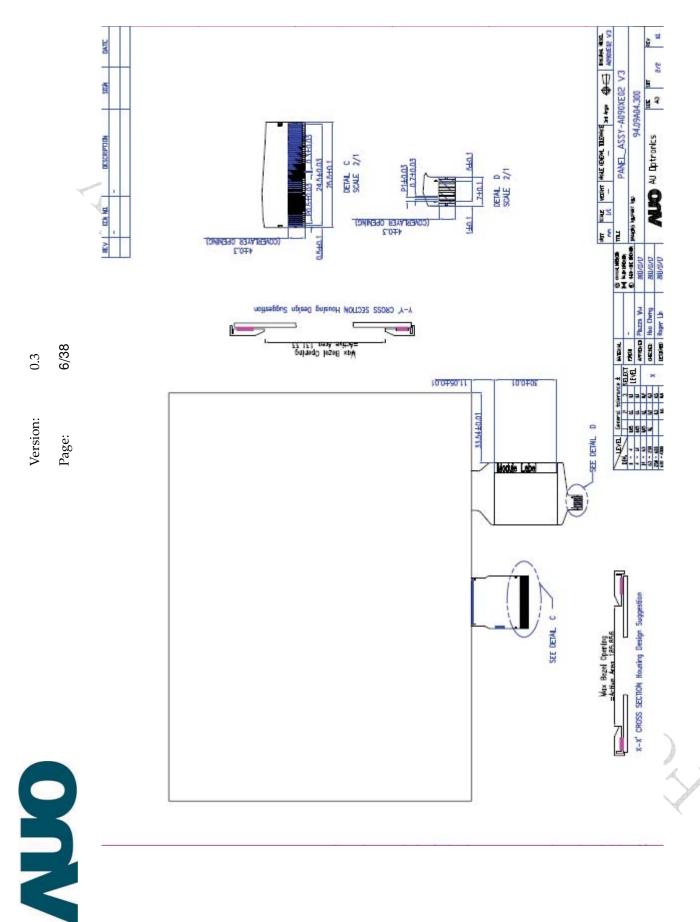
Note 1 : Not include FPC and label. Refer next page to get further information.

Note 2 : 750 g load force on UNI/JPIA 3H pencil, speed is 3.5mm/s on the AG film and scratch length is 1cm and write 5 handwriting, Scratch no. \leq 2 is OK

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C. Electrical Specifications

1. Panel Pin Assignment

Recommended connector : FH12-50S-0.5SH.							
Pin No.	Symbol	I/O	I/O	Description	Remark		
	- ,		Structure	2000			
1	Dummy			Dummy pin			
2	DIODL	I/O	Type 2	Vertical start pulse input/output			
3	VEE	Р		The most negative power supply for gate output			
4	VGG	Р		The most positive power supply for gate output	*		
5	VDD	Р		Digital power			
6	VSS	Р		Digital ground			
7	UDR	I	Type 4	Input pin to select the shift direction of the start pulse. (CMOS signal) (1). UDR="H", DIODL ->G1->G2->>G767->G768->DIODR (2). UDR="L" (Default), DIODR ->G768->G768->>G2->G1->DIODL	Note1		
8	OEDR	I	Type 2	Input pin for the output enable control	Note2		
9	CPVR	I	Type 2	Input pin for the shift clock			
10	DIODR	I/O	Type 2	Vertical start pulse input/output			
11	VCOM_IN	ı	46	To panel VCOM			
12	VCOM_OUT	0	-	VCOM output to system(from driver IC)			
13	VCOMDC	Р	Type 2	External voltage for VCOMDC			
14	VCOMH	Р		External voltage for VCOM high power			
15	VCOML	Р	/	External voltage for VCOM low power			
16	VSS	Р		Digital circuit ground supply for source driver			
17	SHD_N	I	Type 4	DC-DC converter shut down pin. "0": Enable.(Panel shut down; Default) "1": Disable.			
18	PWR_RDY	0	Type 1	Power ready output. When SHD_N from "1" to "0": PWR_RDY will become "0". When SHD_N from "0" to "1": after 100ms, PWR_RDY will become "1".			
19	VCOMIN_0	I	Type 2	Logic Input for VCOM_OUT voltage generate.			





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20	VCOMIN_1	ı	Type 2	Logic Inpu	t for VCOM_	OUT voltag	e generate.			
21	XDIOL	I/O	Type 5	These pins	izontal start pulse input/output. se pins are used to input and output shift data. These s are switched as input or output by setting the SHL pin					
22	XDIOR	I/O	Type 5	as ionow.	SHL XDIOL XDIOR L Input Output H Output Input					
23	LD	ı	Type 3	Latch data					Note3	
24	D0	Ι	Type 3	Data input	, First pixel L	SB				
25	D1	I	Type 3	Data input	, First pixel M	1SB)		
26	D2	Ι	Type 3	Data input	, Second pix	el LSB				
27	D3	I	Type 3	Data input	, Second pix	el MSB	A			
28	D4	ı	Type 3	Data input	, Third pixel I	_SB				
29	D5	I	Type 3	Data input	ata input, Third pixel MSB					
30	D6	I	Type 3	Data input	ata input, Forth pixel LSB					
31	D7	ı	Type 3	Data input	Pata input, Forth pixel MSB					
32	SHL	1	Туре 3	SHL = "L":	lorizontal (left/right) scan direction. SHL = "L": Shift right to left. SHL = "H": Shift left to right. Default					
33	XCLK	ı	Type 3	Horizontal	Clock input				Note3	
34	Dummy	D	7. 6	Dummy pii	ı					
35	VREF	O	-7	For power	setting capa	ctor connec	ted pin.			
36	AVDD	O		For power	setting capa	ctor connec	ted pin.			
37	C1P	C	2	For charge	pump capa	ctor connec	ted pin.			
38	C1N	С		For charge	pump capa	ctor connec	ted pin.			
39	VSS	Р		Digital gro	und					
40	VSSA	Р		Analog gro						
41	VDD	Р		Digital pow						
42	VREF_POS			· ·	For power setting capactor connected pin.					
43	VREF_NEG				For power setting capactor connected pin.					
44	VDDX8	Р		•	itive voltage					
45	NVDDX8	Р		DCDC negative voltage						
46	VDPS	Р		External voltage for source postive power.						
47	VDNS	Р		External voltage for source negative power. For power setting capactor connected pin.						
48	VDNG	C -				ctor connec	tea pin.			
49	VCOM_IN	ı		To panel V	COM					





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50 Dummy pin Dummy

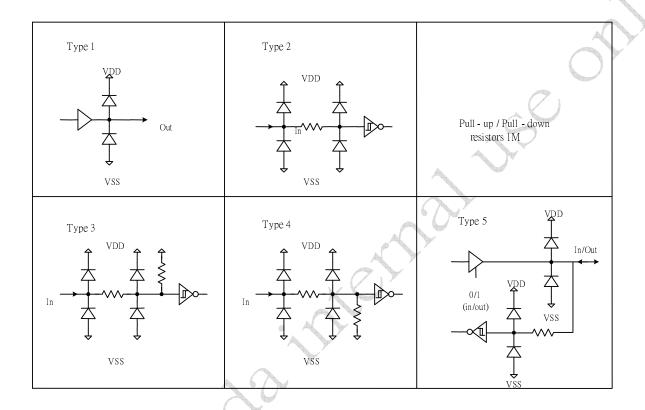
I: Input pin; O:output pin, I/O: Input / Output; P: Power pin; C: capacitor pin; D: Dummy

Note 1: Scanning up to down must to set UDR="H"

Note 2: Please reference chapter E

Note 3: Please reference chapter E

I/O Pin Structure:







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2. Touch Panel Pin Assignment

 $Recommended\ connector: FH12-6S-1SH.$

Pin No.	Symbol	I/O	Description	Remark
1	GND	Р	Touch panel ground.	
2	VDD_TP	Р	Touch panel power.	
3	TP_INT	0	Touched Interrupt Indicator pin.	
4	IICSCL	I	Serial input clock in I2C-Bus interface operation pin.	
5	IICSDA	I/O	Serial input/output data in I2C-Bus interface operation pin.	
6	RST_TP	I	Touch panel reset pin.	

3. Absolute Maximum Ratings

J. ADSOIDLE ME	ixiiiidiii i t	atiiigo					
Item	Symbol	Condition	Min.	Max.	Unit	Remark	
Power voltage	VDD	VSSA=VSS= 0	-0.3	+5.0	V		
Digital input voltage	VI	GND =0	-0.3	VDD+0.3	٧		
	VDPS	VSSA=VSS=0	0	VDDX8-1	٧		
	VDNS	VSSA=VSS=0	NVDDX8+1	0	٧		
Source voltage	VDDX8	VSSA=VSS=0	0	22	٧		
	NVDDX8	VSSA=VSS=0	-22	0	٧		
	VDNG	VSSA=VSS=0	NVDDX8	0	٧		
Gate voltage	VGG	VSS=0	-0.3	VEE+55	٧		
Gate voltage	VEE	VSS=0	VGG-55	+0.3	٧		
	VCOMH	VSSA=VSS=0	0	VDDX8-1	٧		
VCOM_OUT voltage	VCOML	VSSA=VSS=0	NVDDX8+1	0	٧		
A	VCOMDC	VSSA=VSS=0	-5	0	٧		
Storage temperature	Tstg	-	-55	125	$^{\circ}$		
Operating	Topa	-	-30	85	$^{\circ}$		





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Operation Ratings

Item	Symbol	Min.	Typical	Max.	Unit	Remark
Power voltage	VDD	3.0	3.3	3.6	V	
	VDPS	14.5	15	15.5	٧	
	VDNS	-15.5	-15	-14.5	٧	4
Source voltage	VDDX8	14.5	15	15.5	٧	Short with VDPS
	NVDDX8		-15		٧	Short with VDNS
	VDNG		-15		V	Short with VDNS
Gate voltage	VGG	19	19.5	20	V	
date voltage	VEE	-22	-21.5	-21	N	1
	VCOMH	1	0	(V	
VCOM_OUT voltage	VCOML	1	0	-	V	
	VCOMDC		0		V	
VCOM voltage	VCOM_IN	-5		0	V	





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D.Electrical Characteristics

1 Panel Power Consumption

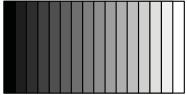
Item	Symbol	Condition	Min.	Typical	Max.	Unit
Supply Voltage	VDD	VSSA=VSS= 0V	3	3.3	3.6	V
Low Level Input	VDD	V33A=V33= 0V	3	3.3	3.0	V
Voltage	Vil	Digital input pins	GND	-	0.3xVDD	V
High Level Input						
Voltage	Vih	Digital input pins	0.7xVDD	-	VDD	V
Operating temperature	T _{op}		-	25	O- ^y	℃
		VDD=3.3V		1.61	3.2	mA
		VDPS=15V		1.71	2.5	mA
		VDNS=-15V		1.26	2.5	mA
		VDDX8=15V		0.19	0.4	mA
		NVDDX8=-15V	7	0.19	0.4	mA
Operation Power Dissipation	r P	VGG=19.5V		1.48	2.5	mA
		VEE=-21.5V		1.48	2.5	mA
		VCOMH=0V		0	0	mA
		VCOML=0V		0	0	mA
		VCOMDC=0V		0	0	mA
	A	VCOM_IN=TBD V		TBD	TBD	mA
		VDD=3.3V		0.03	0.1	mA
	. 6	VDPS=0V		0		mA
		VDNS=0V		0		mA
		VDDX8=0V		0		mA
Cton dlay Dayya		NVDDX8=0V		0		mA
Standby Power Dissipation	Р	VGG=0V		0		mA
Dissipation		VEE=0V		0		mA
		VCOMH=0V		0		mA
		VCOML=0V		0		mA
		VCOMDC=0V		0		mA
		VCOM_IN=TBD V		0		mA





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Note: Typical power consumption measured by following pattern



2. Touch Panel Power Consumption

Mode	Symbol	Condition	Min.	Тур.	Max.	Unit	Remark
Active	Ptp_a		1	18	20	mA	>
Sleep	Ptp_s	VDD= 5.0V	-	1.6	2	mA	7
Deep Sleep	Ptp_dp		-	0.8	1	mA	

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E. Input timing AC Characteristics

1. Horizontal input timing

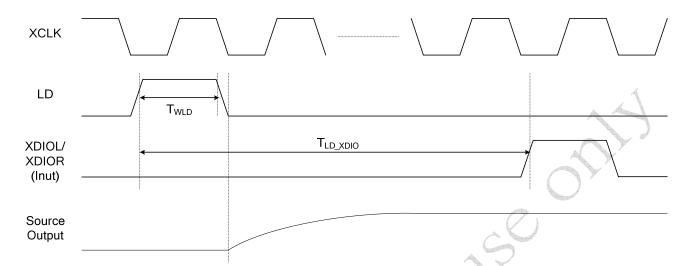


Figure 1: LD input timing

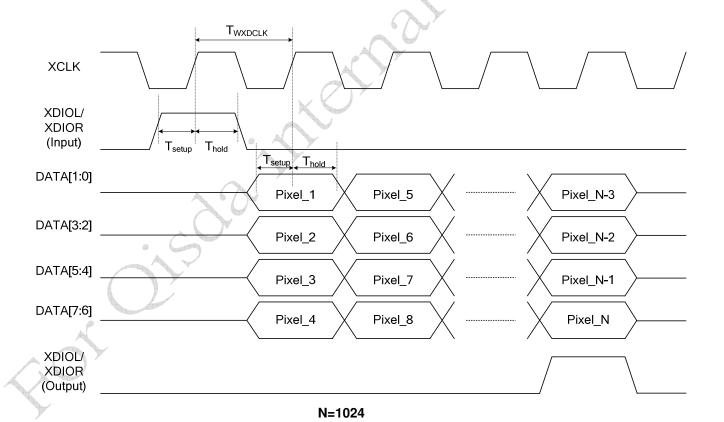


Figure 2: Horizontal data Input timing





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$(\mathsf{VDD} \texttt{=} \mathsf{VDD} \texttt{_} \mathsf{DRV} \texttt{=} 3.3 \mathsf{V}, \, \mathsf{VSSA} \texttt{=} \mathsf{VSS} \texttt{_} \mathsf{DRV} \texttt{=} \mathsf{0V}, \, \mathsf{TA} \texttt{=} 25 ^{\circ} \mathsf{C})$

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Clock pulse width	T _{WXDCLK}	13			ns
Data setup time	T _{setup}	2	-	-	ns
Data hold time	T_{hold}	2	-	-	ns
LD pulse width	T _{WLD}	1	-	-	XCLK
Time from LD to XDIOL/XDIOR	T _{LD_DIO}	5	-	-	XCLK

1.1 Relation ship of input data and source output voltage

The source driver output voltage will base on input 2 bits data, and the relationship is as below:

MSB	LSB	Function
0	0	Source output is 0V
0	1	Source output is VDPS(+15V)
1	0	Source output is VDNS(-15V)
1	1	Source output is floating

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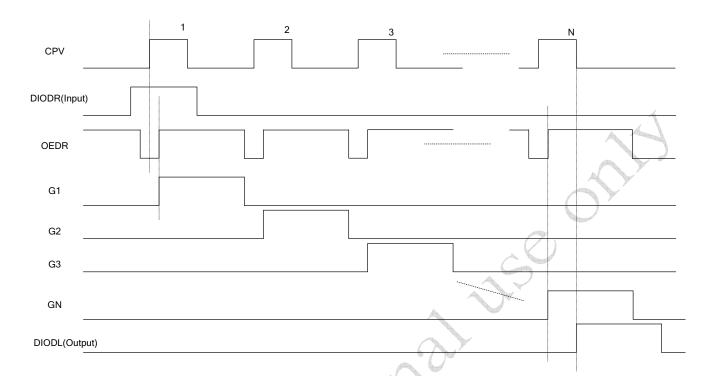




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2. Vertical input timing



N=768

Figure 3: Vertical input timing



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3. VCOM_OUT voltage definition

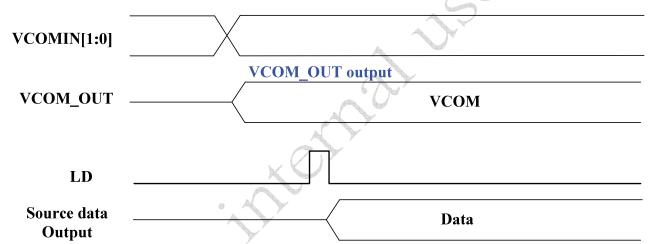
The VCOM output voltage will base on input pins VCOMIN[1:0], and the relationship is as below:

VCOMIN[1:0]	Function
00	VCOM_OUT output is VCOMDC v
01	VCOM_OUT output is VCOMH v
10	VCOM_OUT output is VCOML v
11	VCOM_OUT output is floating

4. VCOM_OUT relationship

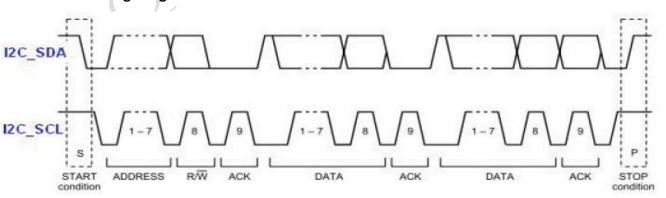
VCOM_OUT will change while VCOMIN[1:0] change

Source output will change while LD signal falling edge.



5. Touch panel timing

5.1. I2C Timing Diagram



Note: Slave address is 1001100.



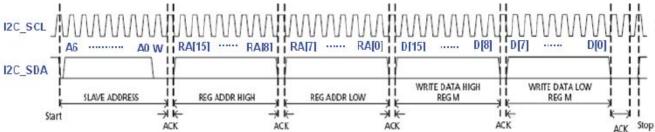


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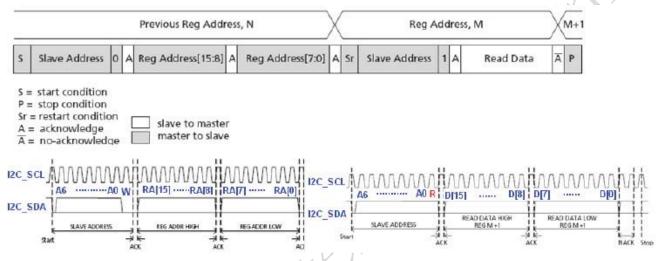
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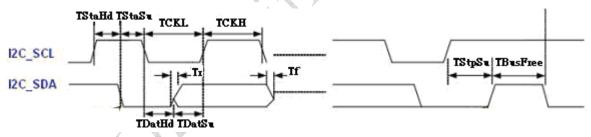
5.2. Register Write Sequence



5.3. Register Read Sequence



5.4. I2C Timing Characteristics



VDDI=1.65~3.3V, VCI=2.5~3.3V, TA=25℃

Item	Symbol	Min.	Тур.	Max.	Unit					
Working Frequency	Fclk	-	-	400	KHz					
I2C Clock Low	TckL	1250	-	-	ns					
I2C Clock High	TckH	1250	-	-	ns					
I2C Data ring time	Tr	-	-	300	ns					
I2C Data falling time	Tf	-	-	300	ns					
I2C Data hold time	TDatHd	0	-	-	ns					
I2C Data setup time	TDatSu	100	-	-	ns					
I2C Start Condition hold time	TStaHd	600	_	-	ns					
I2C Start Condition setup time	TStaSu	600	-	-	ns					





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I2C Stop Condition setup time	TStpSu	600	ı	-	ns
I2C Bus free time	TBusFree	1300	-	-	ns





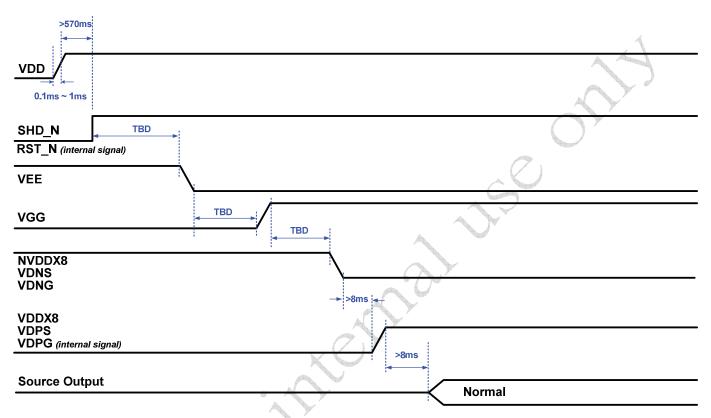
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F. Power On/Off Characteristics

1. Recommended Power On/off Sequence

The suggested power on/off sequence is below:

1.1 Power on sequence:



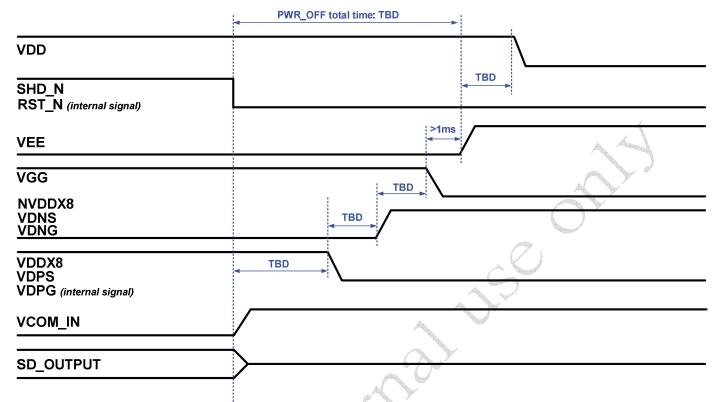
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1.2 Power off sequence:







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G. Optical Specification

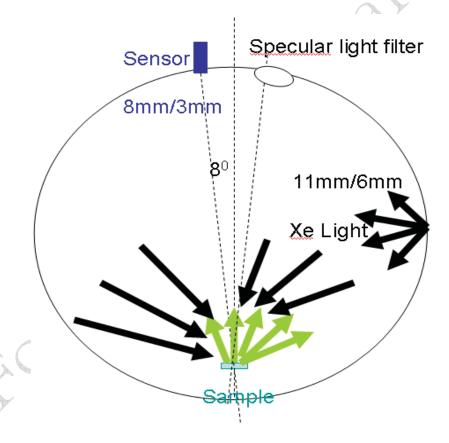
All optical specification is measured under typical condition (Note 1, 2)

Item	Symbol	Condition	Min.	Min. Typ.		Unit	Remark
Reflectance	R	white	25	34		%	Note1,2,3,4
Contrast Ratio	CR	At optimized viewing angle	8	11			Note1,2,3,5
Update Time	Т	T=25℃ T=10℃ T=0℃		600 1100 1500	700 1210 1650	ms	Note 3

Note 1. Ambient temperature =25 $^{\circ}$ C

Note 2. Reflectance and constrast ratio are measured by KONICA MINOLTA spectrophotometer CM-2600d.

Note 3: The measurement shall be conducted under AUO specificed driving condition, including LUT and TCON codes.





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Note 4. Definition of Reflectance:

The Reflectance is expressed as:

 $R = Reflectance \ Factor_{white \ board} \, x \ (L_{center} \, / \, L_{white \ board})$

 L_{center} is the luminance measured at center in a white area. $L_{white\ board}$ is the luminance of a standard white board.

Note 5. Definition of contrast ratio:

The contrast ratio (CR) is the ratio between the reflectance in a full white area (RI) and reflectance in a dark area (Rd).

Contrast ratio (CR) =
$$\frac{Rl}{Rd}$$





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H. Reliability Test Items

	Test	Condition	Condition	Remark
1	High-Temperature Operation	Tamb=+50℃, RH=30% for 240hrs	IEC 60068-2-2Bp	Update pattern four times per minute.
2	Low-Temperature Operation	Tamb=0℃ for 240hrs	IEC 60068-2-2Ab	Update pattern four times per minute.
3	High-Temperature Storage	Tamb=+60℃, RH=23% for 240hrs		
4	Low-Temperature Storage	Tamb=-25℃ for 240hrs	IEC 60068-2-2Ab	
5	High-Temperature, High-Humidity Operation	Tamb=+40℃, RH=90% for 168hrs	IEC 60068-2-3CA	Update pattern four times per minute.
6	High-Temperature, High-Humidity Storage	Tamb=+60℃, RH=80% for 240hrs	IEC 60068-2-3CA	
7	Temperature Cycle	1 Cycle : [-25° C 30min] → [+60° C 30min] : 100 cycles	IEC 60068-2-14	
8	UV Exposure Resistance	Condition: 765W/m2, 40℃ Test Duration: 7 cycles (Definition of 1 cycle: 8 hr at exposure state and 16 Hr at non-exposure state)	IEC 60068-2-5Sa	
9	Package Vibration	1.04G, Frequency: 10 ~ 500HZ Direction: X, Y, Z Duration: 1 hours in each direction		
10	Package Drop Impact	Drop from height of 100 cm on concrete surface. Drop sequence : 1 corner, 3 edges, 6 faces one drop for each.		
11	Electrostatic discharge	Air-mode: +/- 6kV Contact-mode: +/- 2kV	IEC 61000-4-2	
12	FPC Bonding Strength	Pull the FPC Stiffener part with a force of 500gf in the horizontal and vertical directions		





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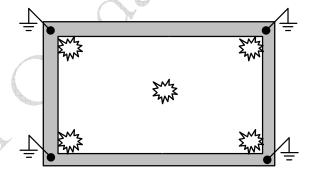
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13	3	Apply MIT method. Bending rate radius: 1.0mm Weight 500gf, Bending angle: ± 135° Bending cycle: 20 times	
14	Stylus Tapping	POLYACETAL Pen: Top R0.8mm Load: 300gf Speed: 2 times/sec Total 13,500 times	Pass criteria - no glass breakage or damage to micro-cups.
15	Altitude test Operation	700hPa(=3,000m) 48hrs	
16	Altitude test Storage	260hPa(=10,000m) 48hrs	

Note 1. The test modules will be kept at 25℃ environment for 4 hours after finish the environmental test and make measurement after AUO specified TCON code and waveform re-driving, there is no display function NG issue occurred. All the cosmetic specification is judged before the reliability stress.

Note 2. ESD testing method.

- Ambient: 24~26°C, 56~65%RH, atmospheric pressure: 940~960hPa
- 2. Instruments: Noiseken ESS-2000,
- 3. Operation System: AUO pattern generator
- Test Mode: Non-operating mode, test pattern: chess 4.
- Test Method:
 - a. Contact Discharge: 150pF(330Ω) 1sec, 5 points, 10 times/point
 - b. Air Discharge: 150pF(330Ω) 1sec, 5 points, 10 times/point
- Test point:



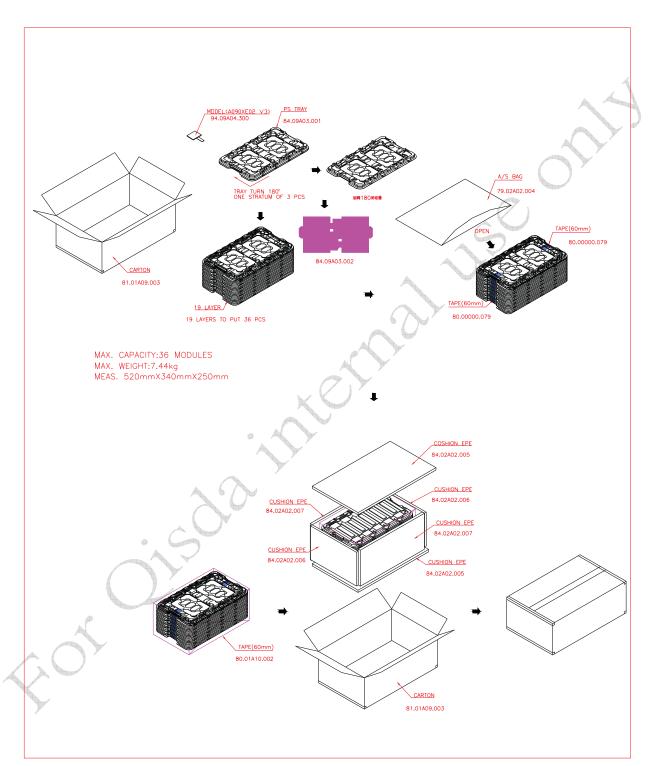




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I. Packing and Marking

1. Packing Form







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2. Module/Panel Label Information

The module/panel (collectively called as the "Product") will be attached with a label of Shipping Number which represents the identification of the Product at a specific location. Refer to the Product outline drawing for detailed location and size of the label. The label is composed of a 22-digit serial number and printed with code 39/128 with the following definition:

ABCDEFGHIJK(LMN)

AB Weekcode C Year code D Fab code Ε Version code

For internal system usage and production serial numbers **FGHIJK**

LMN Version control code

3. Carton Label Information

The packing carton will be attached with a carton label where packing Q'ty, AUO Model Name, AUO Part Number, Customer Part Number (Optional) and a series of Carton Number in 13 or 14 digits are printed. The Carton Number is apparing in the following format:

ABC-DEFG-HIJK-LMN

DEFG appear after first "-" represents the packing date of the carton Date from 01 to 31

- Month, ranging from 1~9, A~C. A for Oct, B for Nov and C for Dec.

A.D. year, ranging from 1~9 and 0. The single digit code reprents the last number of the year

Refer to the drawing of packing format for the location and size of the carton label.

ABC-DEFG-HIJK-LMN

DEFG appear after first "-" represents the packing date of the carton Date from 01 to 31

Month, ranging from 1~9, A~C. A for Oct, B for Nov and C for Dec.

A.D. year, ranging from 1~9 and 0. The single digit code reprents the last number of the year

Refer to the drawing of packing format for the location and size of the carton label.





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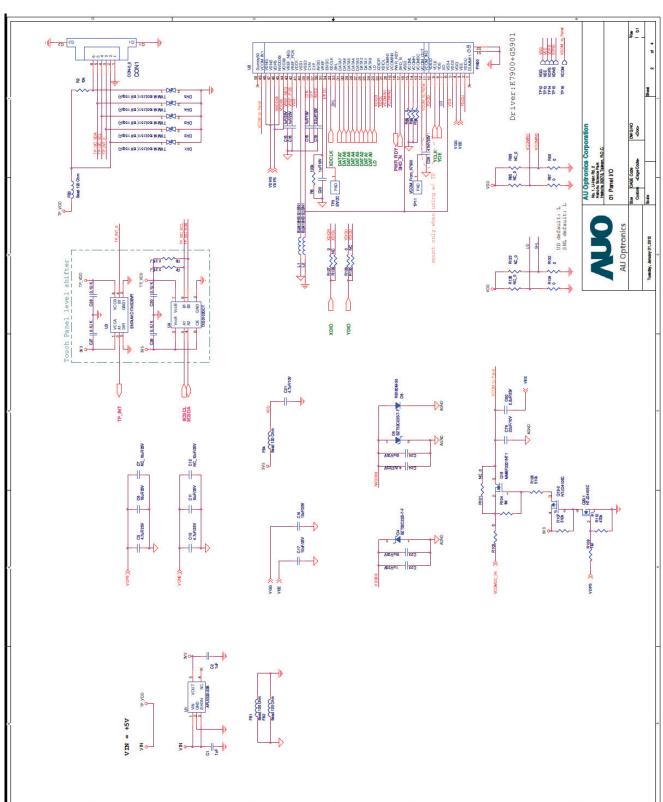


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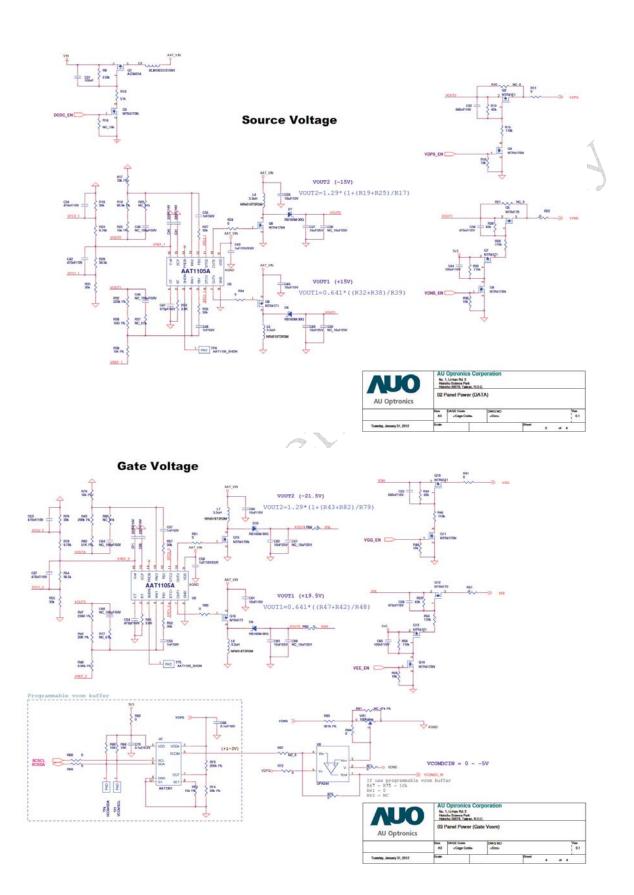
J. Application Note

1. Application Circuit





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2. Touch panel pin assign circuit







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K. Precautions

- Do not twist or bend the module and prevent the unsuitable external force for display module during assembly.
- 2. Adopt measures for good heat radiation. Be sure to use the module with in the specified temperature.
- 3. Avoid dust or oil mist during assembly.
- 4. Follow the correct power sequence while operating. Do not apply the invalid signal, otherwise, it will cause improper shut down and damage the module.
- 5. Less EMI: it will be more safety and less noise.
- 6. Please operate module in suitable temperature. The response time & brightness will drift by different temperature.
- 7. Be sure to turn off the power when connecting or disconnecting the circuit.
- 8. Display surface never likes dirt or stains.
- 9. A dewdrop may lead to destruction. Please wipe off any moisture before using module.
- 10. High temperature and humidity may degrade performance. Please do not expose the module to the direct sunlight and so on.
- 11. Acetic acid or chlorine compounds are not friends with display module.
- 12. Static electricity will damage the module, please do not touch the module without any grounded device.
- 13. Do not disassemble and reassemble the module by self.
- 14. Be careful do not touch the rear side directly.
- 15. No strong vibration or shock. It will cause module broken.
- 16. Storage the modules in suitable environment with regular packing.
- 17. Be careful of injury from a broken display module.
- 18. Please avoid the pressure adding to the surface (front or rear side) of modules, because it will cause the display non-uniformity or other function issue.
- 19. Application under direct sunlight is strongly not recommended as it would result in display performance degradation.
- 20. It is highly recommended that the display is exposed to an even lighting condition to ensure a good display uniformity.
- 21. Elimination of light exposure to the display by applying proper means, e.g. lighting shielding cover is suggested when the display is not being used to extend the life performance of the device.
- 22. Heat isolation or heat sink to control uniformity of panel temperature should smaller than 1 °C
- 23. Any performance degradation or display distortion which can be eliminated by display refreshing should not be regarded as a defect

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L. Touch Panel Command and Register Map

1. I2C Protocol Definition

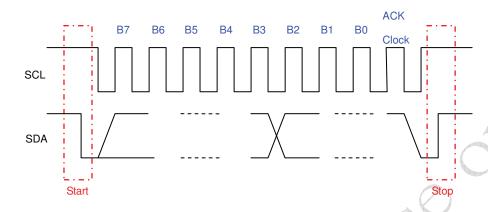


Figure 1. Standard I²C Transaction Unit

The sensor controller supports standard I²C protocol with SCL up to 400KHz. The device address is 0x5C. The chip also provides both single and sequential access. Figure 2 shows the write operation using single or sequential mode. Figure 3 also depicts the standard I2C transaction for single for sequential read mechanism.

Write Operation															
Single	Start	Device Address (W)	Α	Mem Addr	Α	Data[0]	Α	Stop							
Sequential	Start	Device Address (W)	Α	Mem Addr	Α	Data[0]	Α	Data[1]	Α		Α	Data[n]	Α	Stop	

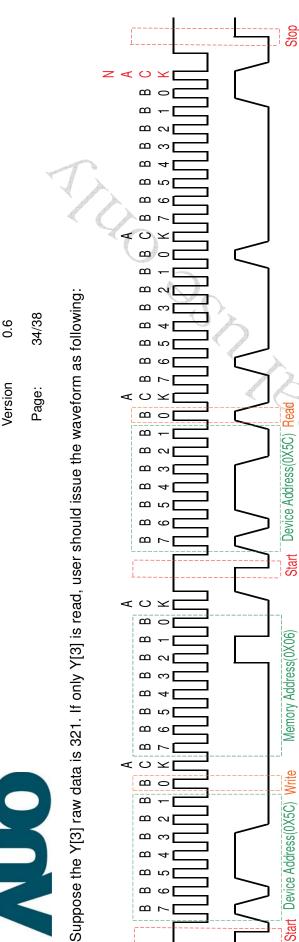
Figure 2. Write Operation with Single/Multiply Access

Read Oper	Read Operation													
Single	Start Device Address (W) A Mem Addr A Start Device Address (R) A Data[0]] NA Stop												
Sequential	Start Device Address (W) A Mem Addr A Start Device Address (R) A Data[0	A A Data[n] NA Stop												

Figure 3. Read Operation with Single/Multiply Acce

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2. Coordinate Register Map

Add r.	Addr.(HEX)	Description	R/W	B7	B6		B4	B3	B2	B1	B0
0	00	X1 (LSB)	R	X1[7]	X1[6]	X1[5]	X1[4]	X1[3]	X1[2]	X1[1]	X1[0]
1	01	X1 (MSB)	R	0	0	0	0	0	0	X1[9]	X1[8]
2	02	Y1 (LSB)	R	Y1[7]	Y1[6]	Y1[5]	Y1[4]	Y1[3]	Y1[2]	Y1[1]	Y1[0]
3	03	Y1 (M SB)	R	0	0	0	0	0	0	Y1[9]	Y1[8]

Note: (1) (X1, Y1) means the touched point

- (2) The coordinate of X1 = X1(LSB) + X1(MSB)*256, Y1 = Y1(LSB) + Y1(MSB)*256
- (3) If no touch, (X1, Y1)=(0,0)

3. Display and Touch Resolution

If screen resolution (blue) is 1024x768, and touch resolution (yellow) is the same (1024x768)

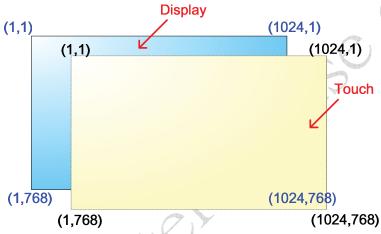
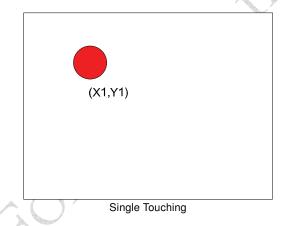


Figure 4 Reference of touched point diagram

4. Single Touch



First Touch Point
(X1,Y1)

Second Touch Point
(X2,Y2)=(0,0)

5. Sensitivity

Addr.	Addr. (HEX)	Description	R/W	B7	B6	B5	B4	B3	B2	B1	B0
111	6F	X_SENSITIVITY (THRESHOLD)	R/W				X_SENSI	TIVITY[7:0]			
112	70	Y SENSITIVITY (THRESHOLD)	R/W				Y SENSI	TIVITY[7:0]			

Note: (1) The default value for X/Y SENSITIVITY is 0X14



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6. Interrupt Operation Mode

This chip should support both polling and interrupt way to get the coordinate and raw data by I2C interface. The figure below depicts the interruption operation.

6.1 Interrupt Mode Setting

Addr. (HEX)	Description	R/W	B7	B6	B5	B4	B3	B2	B1	B0			
113 71	INT_SETTING	R/W	TP_NUM[2]	TP_NUM[1]	TP_NUM[0]			INT_POL	INT_MODE[1]	INT_MODE[0]			
114 72	INT_WIDTH	R/W				INT_WI	DTH[7:0]		***				
Note: (1)	TP_NUM[2:0]									2			
	TP_NUM means how many fingers touched on the panel												
	000: No finger			001: One finge	er								
	010: Reserved			others: Reserv	/ed	7							
(2) INT_RELEASE							4					
	Under Touch Periodical Mode, once the behaviour of finger touched and then left was established, sensing IC will stop to scan until INT_RELEASE be modified INT_RELEASE default is 0												
(3) EN_INT												
	0: Disable interrup	ot		1: Ena	1: Enable interrupt								
(4) INT_POL							7					
	0: The interrupt is	low-a	ctive (default)	1: the	interrupt is hig	h-active							
(5) INT_ MODE[1:0]												
	00: INT assert per	iodica	lly	01: IN	T assert only v	vhen coordinate	e difference						
	10: Touch Indicate	e (defa	ault)	11: IN	T assert only w	vhen INT_RELI	EASE be modif	fied					
(6) The default value t	or IN	_SETTING is	0X0A;INT_W	IDTH is 0X64								

6.2 Sensing Periodical Mode (INT_MODE[1:0] = [0,0]).

For sensing periodical mode, the INT_MODE[1:0] should be [0,0].

The data must be ready (including coordinate and raw data) before signal 'INT' rising.

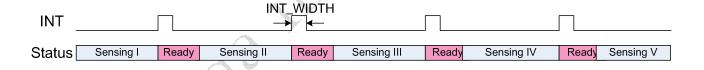


Figure 5: Interruption with INT_R auto-reset

6.3 Coordinate Compare Mode (INT_MODE[1:0] = [0,1]).

The INT signal will be asserted while coordinate changes under comparison mode $(INT_MODE[1:0] = [0,1])$.

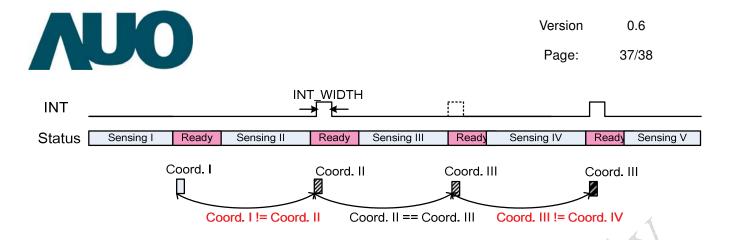


Figure 6: Interruption Flag under Coordinate Compare Mode

6.4 Touch Indicate Mode (INT_MODE[1:0] = [1,0]).

The interrupt will assert when the touch is valid. The interrupt should keep high until the touch is released.

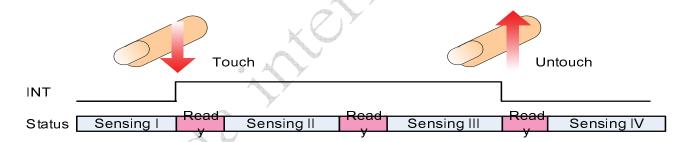


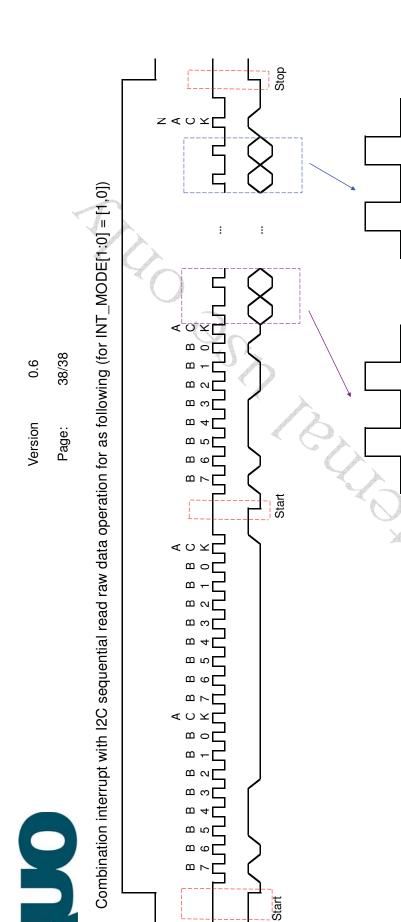
Figure 7: Touch Indicate Mode

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B0 X[n]_MSB

B7 Y[0]_LSB





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7. Power Mode

	Addr.	Addr.(HEX)	Description	R/W	B7	B6	B5	B4	B3	B2	B1	B0
ſ	115	73	Power Mode	R/W	IDLE_PERIOD[3]	IDLE_PERIOD[2]	IDLE_PERIOD[1]	IDLE_PERIOD[0]	0	ALLOW_SLEEP	POWER_MODE[1]	POWER_MODE[0]

The capacitive sensor controller support 3 steps of power saving: Active, Sleep, Deep Sleep, the following section describe relative scan rate and power consumption:

The default value is 0X50

Active Mode:

The scan speed will reach 60Hz, this mode makes full-speed sensing and data process to provide best performance. the Power Mode is '0'.

Sleep Mode:

This mode will lower the scan speed down to 10Hz. Active Mode can enter sleep mode automatically or by command. When the system issues a command to change power mode to '1', the scan rate will switch to 10Hz at next scan cycle. When allow_sleep parameter is given, and user don't touch the screen longer than IDLE_PERIOD ms. the controller should also enter sleep mode directly and change the scan rate to 10 Hz immediately.

When user touches the screen in active region, the controller should return to Active mode. besides, when system assert a command to change the power mode to '0', the scan rate should also rise to 60Hz

Deep Sleep Mode:

When the chip enter deep sleep mode, the scan speed will reduce to 1Hz to achieve minimum power consumption. While deep sleep mode, all the registers are accessible during 4 ms, and it start from end of interrupt transition. The figure 13 and figure 14 shows a example to reference.

The only way to leave/enter deep sleep mode is change the power mode by specific command. The power mode is defined as '2'



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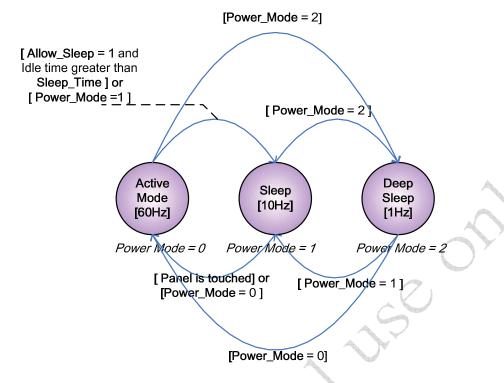


Figure 8 Power Mode Diagram

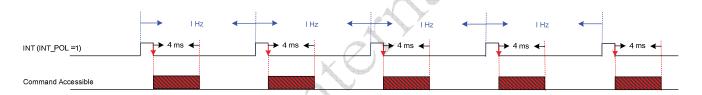


Figure 9 Command Accessible in Deep Sleep Mode (INT_POL=1)

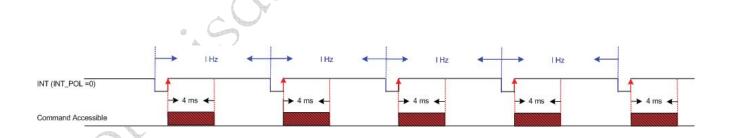


Figure 10 Command Accessible in Deep Sleep Mode (INT_POL=0)





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8. Calibration

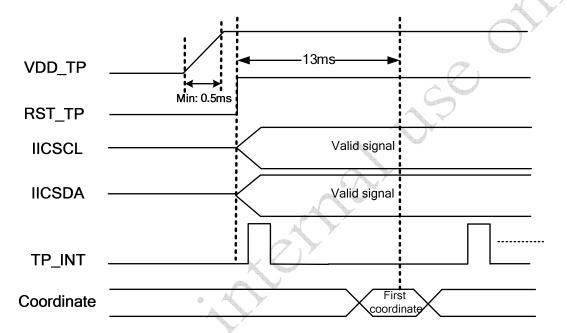
Add	Addr. (HEX)	Description	R/W	B7	B6	B5	B4	B3	B2	B1	B0
120	78	Calibration	W	0	0	0	0	0	0	1	1

"Calibration" procedure has to be done once after assembly

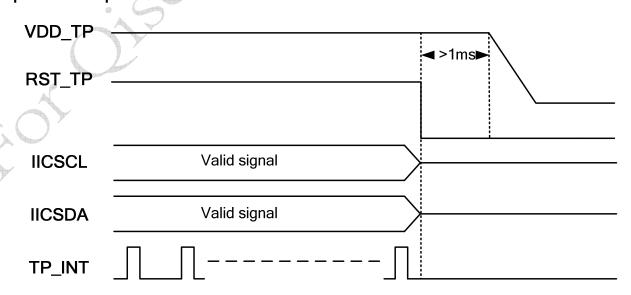
Set address 0x78 as a 0x03 and wait 500ms, "Calibration" procedure will be done

9. Power On/Off Sequence

9.1 power on sequence



9.2 power off sequence



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