CS224

Lab No: 06

Section No: 04

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No.	Cache Size KB	N way cache	Word Size	Block size (no. of words)	No. of Sets	Tag Size in bits	Index Size (Set No.) in bits	Word Block Offset Size in bits ¹	Byte Offset Size in bits ²	Block Replacement Policy Needed (Yes/No)
1	128	1	32 bits	4	213	15	13	2	2	NO
2	128	4	32 bits	16	2 ⁹	17	9	4	2	YES
3	128	Full	32 bits	16	20	26	0	4	2	YES
4	256	2	64 bits	8	211	47	11	3	3	YES
5	256	4	64 bits	32	28	48	8	5	3	YES
6	256	Full	16 bits	16	20	11	0	4	1	YES

Word Block Offset Size in bits: Log₂(No. of words in a block)

Byte Offset Size in bits: Log₂(No. of bytes in a word)

Q2)

Memory accessed	Set no.	Hit
00 00 20 24	0	no
00 00 20 42	0	yes
00 00 20 68	1	no
00 00 20 04	0	no
00 00 20 0C	1	yes
00 00 20 4C	1	no

Q3)

Memory accessed	Set no.	Hit
00 00 00 2C	1	no
00 00 00 48	2	no
00 00 00 44	1	no
00 00 00 0C	0	no
00 00 00 04	2	no
00 00 00 0C	0	yes

Q4)

a)

Total Physical Memory Size: 4 GB=2^32 bytes

Word Size: 2 bytes=2^1 bytes

- Block Size: 32 words × 2 bytes/word=64 bytes=2^6
- Cache Memory Data Area Size: 1 KB=2^10 bytes
- Number of Blocks in Cache: Cache Memory Data Area Size/Block Size=2^10/2^6=2^4 Blocks
- Number of Sets (N): 8 sets

Subfields in Physical Address:

- 1. Block Offset: 6 bits (log2(Block Size))
- 2. Set Index: 3 bits (log2(N))
- 3. Tag: Remaining bits after accounting for Block Offset and Set Index

Sizes in Number of Bits:

- Block Offset: 6 bits
- Set Index: 3 bits
- Tag: 32-(6+3)=23

So, the physical address structure is 6 bits for Block Offset, 3 bits for Set Index, and 23 bits for Tag.

b)

- Data Area: 32 words×2 bytes/word=64 bytes=512 bits
- Tag: 23 bits
- **D (Dirty Bit)**: 1 bit

Total Size of a Block: 512 bits (Data Area)+23 bits (Tag)+1 bit (D)=536 bits

c)

- Size of a Set: 536 bits/block×24 blocks/set=8,576 bits
- Total SRAM Size: 8,576 bits/set×8 sets=68,608 bits

d)

- If random replacement is made, it doesn't directly affect the SRAM size.
- SRAM size is determined by the number of sets and the size of each set.
- Changing the replacement policy does not change the number of bits in the SRAM, but it may affect the cache's performance characteristics (e.g., hit rate, miss rate).