ZEESHAN RAFIQUE

Karachi, Pakistan ◇ zeeshanrafique.me ◇ (+92) · 344 2350520 ◇ zeeshanrafique23@gmail.com

EDUCATION

Usman Institute of Technology (NED), Karachi *July 2021*
B.E. in Computer Engineering *CGPA: 3.4*

EXPERIENCE

Xcelerium Nov 2021 - Present (Part-time)
Hardware Engineer *Irvine, CA (Remote)*

- Responsible of doing co-simulations & AFI generation to emulate RISC-V System-on-Chip (SoC) on AWS-FPGA.
- Vectorized Floating Point Unit (FPU) for high bandwidth data for RISC-V vector SoC.
- Redesigned existing non-multi-precision FPU to support multi-precision operations to increase resource sharing.

Micro Electronics Research Lab (MERL) Oct 2019 - Present
Hardware Researcher *Karachi, PK*

- Worked on designing and verification of embedded RISC-V processors.
- Involved in the complete development cycle of SoC from designing to chip bring-up.
- Part of a team who has collectively done 6 tape-outs on SKY130nm open-source PDK with the addition of new features in each revision. Also, done one commercial SoC tape-out on TSMC65nm PDK.
- Managed Git organization and repositories. Also introduced automation in workflows.

Google Summer of Code Jun 2021 - Aug 2021
Contributor *Remote*

- Worked on a RISC-V CPU called SERV to add support for Multiplication and Division operations to optimize the execution of the programs having Mul/Div instructions.
- The project was completed in 3 months along with documentation.

PROJECTS

Azadi-SoC https://github.com/merledu/azadi-soc
SystemVerilog, Tcl, Python, Makefile, RV GCC *MERL*

Azadi-SoC is an embedded low-power 32-bit SoC that integrates a RISC-V processor with peripherals using Tilelink(UL) bus. I was involved in the RTL front-end of this SoC, system-level verification, emulation on FPGA, and in Synthesis flow to hand over a clean netlist to the back-end team. We taped out this SoC on TSMC-65nm.

Multi-precision FPU
SystemVerilog, RISC-V, Cocotb *Xcelerium*

Rewrote the existing FPU modules to support multi-precision and to increase resource sharing. Also, designed a wrapper for vectorized floating point unit to handle a high bandwidth input data stream. The unit testing was performed using Cocotb (Python lib.) based test benches.

Buraq-mini-RV https://github.com/merledu/Buraq-mini
SystemVerilog, RISC-V, C++ *MERL*

A 32-bit 5-stage pipelined core designed in SystemVerilog. It implements the RISC-V base ISA and multiply/divide instructions. Basic assembly tests were executed on the core for verification. This project was intended for learning the execution of instructions in a pipelined environment.

TECHNICAL STRENGTHS

Hardware Descriptive Languages	SystemVerilog, Verilog, CHISEL
Interconnect & Peripheral Protocols	AXI4, APB, TileLink, SPI, UART, PWM
Computer Languages	Python, C/C++, Tcl, Shell scripting, RISC-V Assembly
Concepts	RISC-V ISA, MMIOs, STA, Synthesis
Tools	Cadence(Xcelium, Genus), Verilator, Xilinx-Vivado, Git, Linux, Vim, RV GCC Compiler