A Low Phase-Noise SiGe Colpitts VCO with Wide Tuning Range for UWB Applications

Alexander Esswein [#1], Gunther Dehm-Andone [#2], Robert Weigel [#3], Anna Aleksieieva [*4], Martin Vossiek [*5]

[#] *Friedrich-Alexander University of Erlangen-Nuremberg, Institute for Electronics Engineering*
Cauerstr. 9, 91058 Erlangen, Germany
[1] esswein@lte.eei.uni-erlangen.de
[2] dehm-andone@lte.eei.uni-erlangen.de
[3] weigel@lte.eei.uni-erlangen.de

[*] *Institute of Electrical Information Technology, Clausthal University of Technology*
Leibnizstr. 28, 38678 Clausthal-Zellerfeld, Germany
[4] aleksieieva@iei.tu-clausthal.de
[5] vossiek@iei.tu-clausthal.de

***Abstract*—An integrated differential common collector Colpitts VCO with a wide tuning range is presented in this paper. The circuit was designed and fabricated in the IHP Technologies SGB25V 250 nm SiGe:C BiCMOS process. It provides a superior low phase noise performance of -115 dBc/Hz covering the frequency range of 6.7 to 8.7 GHz for UWB pulsed frequency modulated secondary radar application. An additional common collector output buffer was implemented as well. The circuit provides an overall output power of -10 dBm single-ended with a power dissipation of 47 mW including the on-chip buffer. This paper also shows the modifications and improvements done at the mmwave topology to reduce size and to improve the tuning range.**

***Index Terms*—Voltage controlled oscillators, Ultra wideband, Phase noise, Analog integrated circuits**

I. Introduction

There are two main approaches to achieve ultra broadband signals: frequency modulation and pulses. But another possibility is often neglected - a combination between both systems. This concept operates with pulsed frequency modulated signals which was implemented in [1] for use as a high precision local positioning system. The interested reader can find detailed information in [2] and [3]. The FMCW (frequency modulated continous wave) is chopped to short pulses thereby broadening in spectrum as well as reducing the output power. This enables to fulfill the emission limits given by the official regulatory authorithies while maintaining the advantages of both systems. Due to the fact that a discrete implementation cannot reach a pulse width below approx. 1 ns, the bandwidth is limited to 1 GHz. But if an integrated solution can be achieved, the bandwidth could be increased beyond 1 GHz only limited by the speed of the chopping switch. Therefore, the main focus of our efforts were integrated transmitter key components such as the VCO with a wide tuning range of at least 25% of the oscillation frequency and the fast RF switch. The goal of research is to implement a complete pulsed FM transmitter for 7 to 9 GHz in a single chip. This includes other components such as PLL/DDS and spectral signal forming by filters.

The IHP Technologies SGB25V 250 nm SiGe:C BiCMOS process was chosen. It provides a cheap and flexible platform including one or two thick top metal layers consisting of aluminum. The advantage of using a BiCMOS process for a transmitter circuit is the possibility to build a system-on-a-chip (SoC) solution that integrates digital baseband and analog RF circuits. For the VCO design the high performance bipolar transistors with f_T = 75 GHz and f_{max} = 95 GHz were selected.

II. Circuit Topology and Design Aspects

This work is based on a frequently employed common collector Colpitts oscillator design ([4],[5] and [6]) including a second varactor diode pair at the base transistor. Several enhancements that are presented here have been implemented to use this topology in the required frequency range of 7 to 9 GHz.

The main goal of the changes done to the topology were to reduce size respectivly cost, but while maintaining the overall RF and bias performance over the whole tuning range. The simplified VCO topology is given in Fig. 1.

A current mirror with bipolar transistors is used to drive the oscillator core. Additionally, a common collector (emitter follower) output buffer was implemented to decouple the output load from the VCO core.

As described in [4], the VCO frequency defining series resonant circuit consists of L_B and C_{in} (see equation 1).

$$f_{res} = \frac{1}{2\pi\sqrt{L_B C_{in}}} \tag{1}$$

L_B is realized as a spiral inductor without tuning capability, so C_{in} has to be tuned over a wide tuning range (see Fig. 2) using a varicap diode circuit.

For a minimum influence on the tuning range, C_P, which is mainly the collector base capacitance C_{CB} of transistor T, has to be minimized. As discussed in [4], C_S which is determined mainly by C_{BE}, has to be maximized. Additionally, both varactor capacitance ranges have to be maximized.

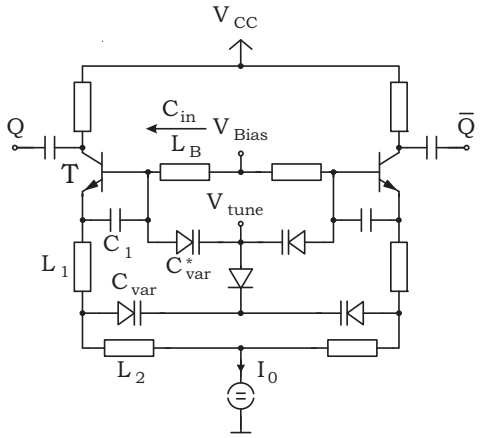

Fig. 1. Common Collector Colpitts VCO topology used in mm-Wave range with two varactor tuning pairs

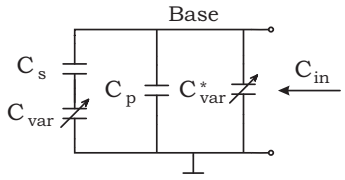

Fig. 2. Equivalent circuit for input capacitance C_{in} of topology of Fig. 1

These constraints lead to an additional capacitance C_1 between base and emitter of T which increases C_S, whereas C_P is given by the transistor size and bias current capability and cannot be improved further. Only an increase of the varactor capacitance reduces the influence of C_P but this improvement possibility is also limited by losses and wiring inductances as discribed in [4]. The varactor capacitance ratio of 3.1:1, together with the presented measures, results in a wide tuning range.

In contrast to [4], the emitter inductance L_2 is replaced by a resistor to save space admitting a loss in performance of phase noise and loop gain but still remaining in the required constraints. L_1 was neglected due to the fact that [4] found few influence on performance if done so. For compensating the negative effect of exchanging the inductors by a resistor, filtering capacitors (without complementary inductance) are added at the current source (C_2) and between the the collector of T and the supply voltage (C_4), which lowers the phase noise by approx. 2 dB in simulation. The principle is also described in [7].

As a further step of optimization, the possibility of differential tuning, was skipped to reduce space (connector/pad count) and the number of tuning voltages. The diode in the tuning voltage concept of [4] was skipped, resulting in a lower K_{VCO} but also reducing the minimum to maximum K_{VCO}-ratio.

Fig. 3 shows the resulting schematic after the enhancements for the size and frequency range.

Including all parasitics, a tuning range of 3.0 GHz at 8.19 GHz center frequency can be obtained in simulation. This corresponds to a relative bandwidth of 36 % within a tuning voltage range of only 0 to 4 V.

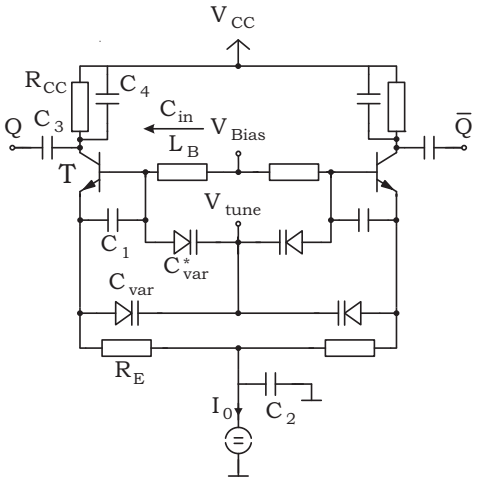

Fig. 3. Common Collector Colpitts VCO topology used in this work

TABLE I
COMPONENT PARAMETERS

Parameter Name	Value
$C^*_{var,min}$	65 fF
$C^*_{var,max}$	200 fF
$C_{var,min}$	145 fF
$C_{var,max}$	455 fF
L_B	0.41 nH
R_E	200 Ω
R_{CC}	200 Ω
C_1	700 fF
C_2	200 fF
C_3	300 fF
C_4	300 fF
V_{Bias}	1.8 V
V_{CC}	3.3 V
V_{tune}	0 to 4 V

The parameters depicted in Table I are chosen to achieve this performance.

III. Simulation Results and On-Chip Characterization

The simulation of the chip was done with the Cadence Virtuoso Spectre Circuit Simulator[1]. Post-layout simulation showed promising results, with a simulated phase noise of -112.5 $\frac{\text{dBc}}{\text{Hz}}$ at 1 MHz offset and a relative tuning range of 36%. Simulated output power ranged from -2.8 to 0.5 dBm with a differential load of 100 Ω. The oscillator draws a bias current of 7.1 mA from the 3.3 V supply.

For the on-chip characterization, the chip was measured using a spectrum analyzer, with Picoprobe GSG DC-probes with a 150 μm pitch width for supply, ground and biasing voltages and a Picoprobe GSSG RF-probe with a 150 μm pitch

[1]Cadence, Spectre and Virtuoso are registered trademarks of Cadence Design Systems, Inc.

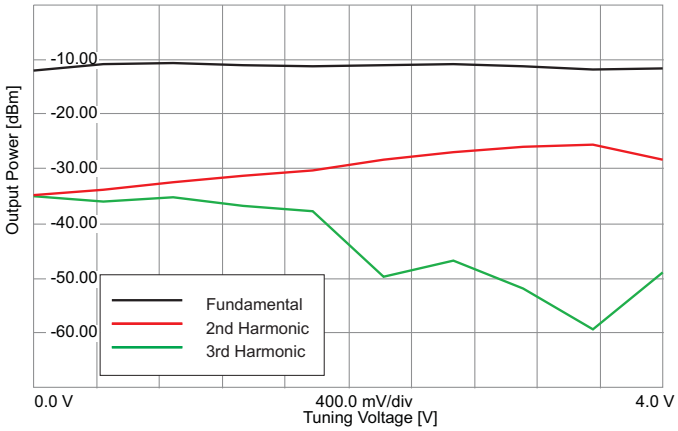

Fig. 4. Harmonic power of output

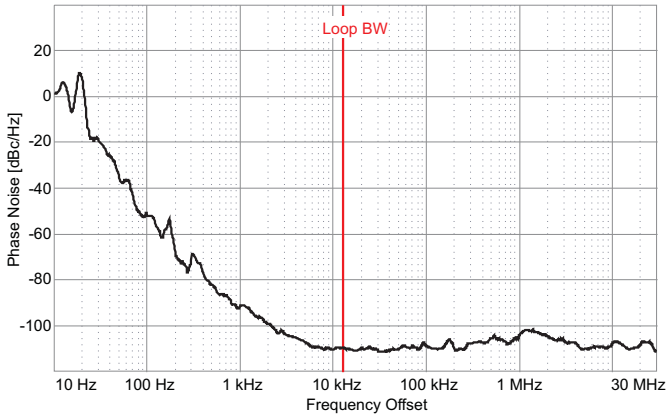

Fig. 5. Phase noise measurement results. The vertical line indicates the loop bandwidth of the spectrum analyzer's internal loop filter. Note that the measurement is only valid from the loop bandwidth up to one to two decades of higher frequency

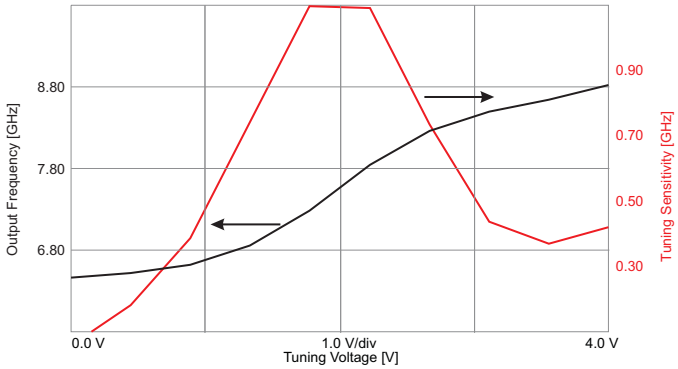

Fig. 6. Output frequency and sensitivity over tuning range

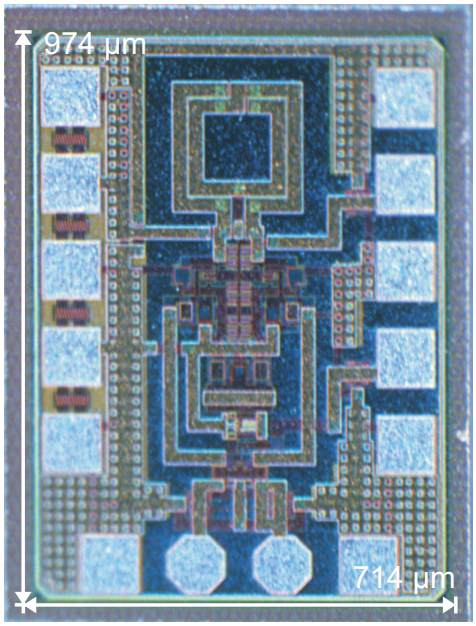

Fig. 7. Microphotograph of the improved Colpitts oscillator

width for the signal output. As no differential measurement equipment was available, the measurements had to be done single-ended. The negative output was terminated with a 50 Ω.

The output power was measured with the integrated harmonic output power measurement function of the spectrum analyzer. As the measurement was done single-ended, 2nd harmonic power was not suppressed as it is in a differential configuration. 3rd harmonic power suppression was found better than 25 dB over the whole tuning range (see Fig. 4). The fundamental ouput power of -10 dBm single-ended is close to the simulated value. Taking into account the theoretical 6 dB improvement of output power in a differential compared to a single-ended configuration, the difference of 1.2 to 3.5 dB is attributed to imperfect matching and the uncertainties of manufacturing.

Phase noise was measured with the internal PLL measurement configuration of the spectrum analyzer. It was found to be -115 $\frac{\text{dBc}}{\text{Hz}}$ at an offset of 1 MHz from the center frequency, at 2 V tuning voltage (resulting in an output frequency of 7.5 GHz), as can be seen in Fig. 5.

VCO tuning range was found to be from 6.4 to 8.7 GHz with a 0 to 4 V tuning voltage, equivalent to a relative tuning range of 30 percent. The measurements of the tuning sensitivity resulted in a K_{VCO} between 300 $\frac{\text{MHz}}{\text{V}}$ and 1.1 $\frac{\text{GHz}}{\text{V}}$. Refer to Fig. 6.

The edge length of the chip die is $714\,\mu\text{m} \times 974\,\mu\text{m}$. As Fig. 7 illustrates, the inductor spiral takes up a very large portion of the die. This substantiates our point that reducing the number of integrated inductors, as proposed in this work, saves valuable wafer space while retaining competitive performance.

IV. Comparison to State-of-the-Art VCOs

In order to compare the manufactured VCO to other topologies, a common figure of merit including tuning range was employed. It is defined as

$$FOM_T = \mathcal{L}(\Delta f) - 20\log\left(\left(\frac{f_0}{\Delta f}\right)\cdot\left(\frac{FTR}{10}\right)\right) + 10\log\left(\frac{P_{diss}}{1\,\text{mW}}\right), \quad (2)$$

TABLE II
VCO COMPARISON

Oscillator	$\mathcal{L}(\Delta f)$ @ 1 MHz [$\frac{\mathrm{dBc}}{\mathrm{Hz}}$]	f_0 [GHz]	FTR [%]	P_{diss} [mW]	FOM_T [$\frac{\mathrm{dBc}}{\mathrm{Hz}}$]
[8]	-116	5.7	8.8	10.8	-179
[9]	-108	8.5	12	4.75	-181
[10]	-85	5	180	13.2	-173
[11]	-87	11.25	45.3	46.8	-164
[12]	-106	7.95	15.1	36	-172
This work	-115	7.55	30	47	-185

where $\mathcal{L}(\Delta f)$ is the phase noise at a specified offset Δf from center frequency, f_0 is the center frequency, FTR is the frequency tuning range in percent and P_{diss} is the power consumption of the oscillator.

The comparison to different circuits is found in Table II. As can be seen, the proposed circuit compares favorably to other topologies, especially for the target application which requires the wide tuning range.

V. CONCLUSION

A fully integrated SiGe VCO for an UWB application at 6.4 to 8.7 GHz with low phase noise of -115 $\frac{\mathrm{dBc}}{\mathrm{Hz}}$ and ultra wide tuning range of 30 percent has been designed, fabricated and characterized. It shows an excellent FOM_T of -185 $\frac{\mathrm{dBc}}{\mathrm{Hz}}$. By simplifying and enhancing a millimeter-wave topology, a superior performance with small size has been achieved, compared to state-of-the-art VCOs. Measurements confirmed this behavior. Additionally, a common collector output buffer was implemented in the same IHP Technologies SGB25V 250 nm SiGe:C BiCMOS process.

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