Design of Low Phase-Noise Oscillators and Wideband VCOs in InGaP HBT Technology

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***Abstract*—A method for design of low phase-noise balanced-Colpitts (BC) fixed-frequency oscillators (FFOs) and wideband voltage-controlled oscillators (VCOs) is presented. Analytical expressions describe how to design an oscillator for best phase noise, given a limited Q factor and a certain active device. The theory needs only two free parameters: the impedance level (Z_c) and tapping ratio (n) of the resonator. It is described how to chose Z_C and n for low phase noise and large tuning range, respectively.**

The design method is verified with a low phase-noise FFO and a wideband VCO, both designed in InGaP HBT technology. The BC FFO presents a phase noise of −112 dBc/Hz at 100-kHz offset from a 9.2-GHz carrier. The wideband VCO implemented in the same technology presents a minimum phase noise of −106 dBc/Hz at 100-kHz offset from a 9-GHz carrier. Over the frequency range of 8.4–9.7 GHz, the phase noise is better than −102 dBc/Hz and the output power is 7 ± 0.5 dBm. The wide tuning range, constant output power, and relatively constant and low phase noise are achieved due to double pairs of tuning varactors, one between emitters and one between collectors. To the authors' best knowledge, this type of double-tuned BC VCO topology has not been previously published.

***Index Terms*—Balanced Colpitts (BC), double tuned, oscillator, phase noise, voltage-controlled oscillator (VCO), wideband.**

I. Introduction

LOW phase-noise voltage-controlled oscillators (VCOs) with sufficient tunability (about 10%–20%) is a bottleneck in high data-rate wireless communication systems. With cost as the driving factor, there is a strong demand for fully integrated monolithic microwave integrated circuit (MMIC) VCOs with low phase noise. It has been shown that InGaP HBT technology, with its low flicker-corner frequency and high breakdown voltage, is a good choice for design of low phase-noise VCOs. In particular, balanced Colpitts (BC) or Hartley VCOs in InGaP HBT present state-of-the-art phase noise for MMIC VCOs [1], [2].

The good phase-noise performance of Colpitts oscillators is associated with superior cyclostationary noise properties [3]. The cyclostationary properties depend in turn on the capacitive division ratio for the feedback resonator. The optimum phase noise is achieved for a specific division ratio [3], [4] that generally cannot be maintained over a VCO's tuning range if the oscillator is tuned with a single tuning varactor.

The single-ended Colpitts topology is extended to a balanced version in [5]. To avoid tuning the capacitors in the feedback network, and thus affecting the optimum feedback condition, the oscillator is proposed to be tuned with additional varactors in parallel to the resonant tank [5]. This implementation, which is not a true Colpitts oscillator, has the drawback of rather small tunability as varactors constitute only a fraction of the total tank capacitance. If the size of the tuning varactors is increased in comparison to the capacitances in the feedback network, the modified Colpitts topology will deviate considerably from a true Colpitts, the waveforms will be distorted, and phase noise degraded.

Tuning range can be significantly improved by utilizing hyperabrupt varactors [6]. However, hyperabrupt varactors are generally not available in commercial MMIC processes, where the base–collector junction is normally utilized as tuning element. To achieve higher tunability in a conventional MMIC process with an abrupt collector junction, the varactor must contribute to a larger fraction of the total tank capacitance. A solution is to tune more than one circuit element. A very wideband single-ended VCO with three tuning elements was presented in [7] and a double-tuned common-collector BC VCO integrated in SiGe HBT technology was presented in [8]. Besides increasing the tuning range, tuning several circuit elements also allows for balancing of resonator impedance level (Z_C) and capacitance division ratio (n) so that the oscillator can maintain good cyclostationary properties over the tuning range without being voltage limited [9].

This paper presents a simple and systematic method to determine optimum Z_C and n for a common-base BC oscillator. The two parameters Z_C and n, together with the angular oscillation frequency ω_0, are sufficient to calculate the component values of the oscillator. The theory is then extended to tunable oscillators. A novel double-tuned balanced Colpitts (DTBC) topology with tuning varactors between both collectors and emitters is proposed, and it is shown how the optimum component values of this topology can be determined. The two BC oscillators are implemented in a GaAs–InGaP HBT MMIC technology.

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This paper is organized as follows. Section II presents the design methods describing how to chose the circuit elements for low phase noise and wide tuning range. Section III presents how the theory is applied to implement the circuits in GaAs–InGaP HBT MMIC technology. Section IV presents the experimental result. Finally, Section V concludes this study.

II. Theory and Simulations

A single-sideband phase-noise spectrum is qualitatively described by Leeson's equation [10]

$$L = 10\log_{10}\left[\frac{2FkT}{P_{\rm sig}}\left(1+\left(\frac{\omega_0}{2Q\Delta\omega}\right)^2\right)\left(1+\frac{\Delta\omega_{\frac{1}{f^3}}}{|\Delta\omega|}\right)\right] \quad (1)$$

where Q is the quality factor of the resonator, $P_{\rm sig}$ is the oscillation power, F is the effective noise factor, and $\Delta\omega_{1/f^3}$ is the corner frequency between the 20- and 30-dB/decade slope.

From (1), the efficiency of increasing Q for improved phase noise is evident, any doubling of Q will theoretically result in a 6-dB improvement in phase noise at a given offset frequency.

Several papers have investigated how to improve Q for integrated inductors, particularly for Si where substrate loss degrades Q significantly. For III–V technologies, as discussed in this paper, the substrate is essentially lossless and the Q factor is limited primarily by metal loss.

In reality, the achievable Q factors are limited by technology, e.g., substrate loss tangent and metal sheet resistance. For an oscillator with integrated resonant tank, the Q factor is typically <50 in the frequency range of 5–10 GHz. Further, the active device is generally decided when the designer starts the design of his oscillator. Left to be controlled are the topology and values of the passive components.

The time-invariant expression in (1) is sufficient for qualitatively predicting the shape of the phase-noise spectrum in an oscillator. A quantitative prediction of phase-noise levels requires time-variant analysis [3], [4]. The goal of this paper is not to come up with another theory for calculation of phase noise, but rather to propose a design methodology for minimum phase noise, when technology and topology for the oscillator are chosen. A question to be answered is: *How to systematically determine the optimum values of the passive components without using an optimization routine?* The topology to be examined is the BC oscillator [5] that is theoretically [3] and experimentally [1] proven to provide good phase noise.

Firstly, the question: *How to minimize phase noise of an oscillator based on a resonator with fixed Q factor?* is addressed. The investigation is then extended to tunable oscillators with the question: *How to maintain phase noise and signal power over the tuning range?*

A. Models and Simulations

The subsequent analysis relies on a good harmonic balance (HB) simulation algorithm and accurate models for active and passive components. In this section, passive elements are assumed to be ideal with no self-resonant frequency. Losses in reactive elements are expressed in terms of a finite Q factor that, for simplicity, is assumed to be frequency independent and constant for all elements.

Tuning varactors are described with a linear model

$$C(V) = \frac{C_0}{n_T(V)} \quad (2)$$

where $C(V)$ is the capacitance under tune voltage V, C_0 is the maximum varactor capacitance, i.e., when a semiconductor varactor is near forward bias, and $n_T(V)$ is fractional tunability of the varactor.

The active device is a four-finger GaAs–InGaP HBT from WIN Semiconductors, Tao Yuan Shien, Taiwan. It has emitter-finger width and length of 1 and 20 μm, respectively. The HBT is represented by an in-house developed model, the Chalmers–Mitsubishi HBT model [11]. To improve phase-noise simulations, the model is complemented with low-frequency noise sources at the base and collector, respectively [12].

A limitation in the analysis is that the used computer-aided design (CAD) software, Agilent Advanced Design System (ADS), treats noise sources linearly and not cyclostationary [13]–[17], which would give more accurate near-carrier phase-noise predictions. However, as previously mentioned, the focus of this paper is not on modeling accuracy, but rather on topology and how to systematically chose the circuit elements for optimum performance. To keep things simple, we thus stick to the linear noise representation, which is straightforward to implement in the used model and CAD software. In this case, the limitation in accuracy, focusing on phase noise at 100-kHz offset, is also minor as the used device has a flicker-corner frequency in the order of 40 kHz. If the focus is phase noise closer to carrier or if another technology, e.g., CMOS, with higher corner frequency is used; the procedure in this paper is still applicable, but cyclostationary device models are mandatory.

B. Low Phase-Noise BC Oscillator

Fig. 1 shows a common-base BC oscillator that is the basis of this study. Its resonator, including feedback tapping capacitors, can be characterized by only three parameters: characteristic impedance

$$Z_C = \sqrt{\frac{L}{C}} \quad (3)$$

angular center frequency

$$\omega_0 = \frac{1}{\sqrt{LC}} \quad (4)$$

and capacitive division ratio

$$n = \frac{C_1}{C_1 + C_2}. \quad (5)$$

Using (3)–(5), the component values in the tank can be calculated

$$L = \frac{Z_C}{\omega_0} \quad (6)$$

$$C = \frac{1}{Z_C\omega_0} \quad (7)$$

$$C_1 = \frac{C}{1-n} = \frac{1}{Z_C\omega_0(1-n)} \quad (8)$$

$$C_2 = \frac{C}{n} = \frac{1}{Z_C\omega_0 n}. \quad (9)$$

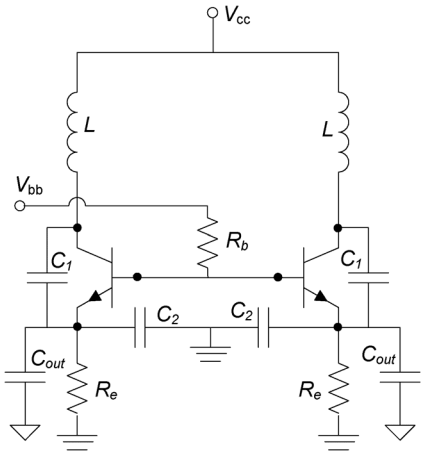


Fig. 1. Schematics of common-base BC oscillator.

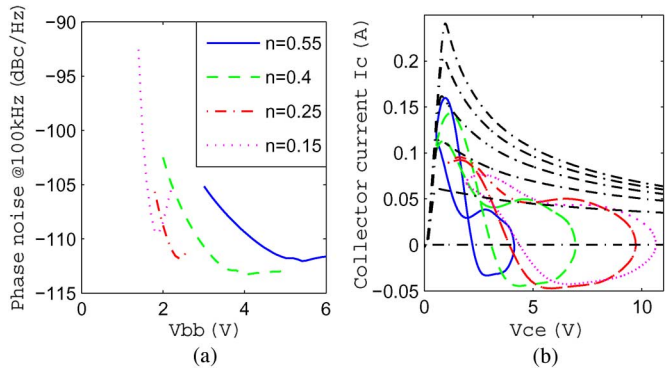


Fig. 2. Influence of capacitive division ratio n. (a) Phase noise versus base-bias voltage with n as a parameter. (b) Oscillator load lines captured at optimum bias for different values of n.

The resonator loss is characterized by Q that, for simplification, is assumed to be the same for all components. If the tank is depicted as a parallel resonator, the loss may be represented by a parallel resistor

$$R_p = Z_C * Q. \tag{10}$$

Other elements in the oscillator, e.g., R_b for the base bias, R_e for the dc current, and $C_{\rm out}$ for extraction of the output signal, should be chosen so that they will not affect the oscillator's performance. R_b can easily be chosen sufficiently high so that its influence on the oscillator can be neglected. Similarly, $C_{\rm out}$ can be chosen small enough in order to eliminate any pulling effects. The major complication is the emitter resistance R_e that will appear in parallel to C_2, and thus load the resonator's Q factor (see Fig. 1). R_e has to be chosen sufficiently high in order to have little influence on the Q factor, but still not too high, as it will then consume significant dc power as it carries all current of the oscillator.

The influence of each parameter will be investigated by simulations based on the models in Section II-A. The target is to design the oscillator for minimum phase noise at a given Q factor. In the subsequent simulation, $Q = 20$ is assumed, which is a reasonable value in a III–V technology with semi-insulating substrate. The resonant frequency of the tank is set to $\omega_0 = 2\pi \times 10$ GHz. The base resistance is set to $R_b = 1000\ \Omega$, which is quite sufficient to isolate the voltage source used for bias. The emitter resistance R_e deserves some considerations before presenting the simulation results; it has to be set properly. As seen in Fig. 1, R_e appears parallel to C_2 so its resistance should be higher than, or at least equal to, the equivalent parallel resistance of C_2. Utilizing $Q = R\omega_0 C$ inserted in (9), the emitter resistance can be expressed as

$$R_e \geq \frac{Q}{\omega_0 C_2} = \frac{Q}{\omega_0 \frac{1}{Z_C \omega_0 n}} = Q Z_C n. \tag{11}$$

For a given ω_0, the oscillator synthesis is now about determining only two parameters: n and Z_C. The target parameter in this study is oscillator phase noise. Besides, output power and harmonic content are also important parameters. However, it will turn out that all parameters of the oscillator generally are good when phase noise reaches its optimum, occurring right before the transistor goes into compression.

The first parameter to be investigated is n. Increasing n reduces the conduction angle and the impulse sensitivity function (ISF) [3] with lower phase noise as a result. However, the voltage swing over the tank is also affected by n. For large n values, the phase noise will increase due to reduced voltage swing over the resonant tank [compare (1)]. There exists an optimum value of n, representing the best tradeoff between ISF and power swing. In [3], Hajimiri and Thomas demonstrate with simulations that the optimum is about $n \approx 0.2$ for a bipolar oscillator. In a later study by Andreani *et al.*, the optimum is analytically shown to be $n \approx 0.3$ [4]. In both [3] and [4], a constant dc current is assumed, and the target is to minimize an oscillator figure-of-merit (FOM) trading phase noise versus dc power consumption [18]. In this study, the target is on minimum phase noise, a slightly higher value of n can then be expected, as reduction in voltage swing may be partly compensated by increased dc current and larger current swing.

To deduce the optimum value of n, phase noise is plot versus base-bias voltage V_{bb} (the parameter determining collector dc current) with n as a parameter. Fig. 2 shows phase noise at 100-kHz offset versus V_{bb} for different n, in the simulation $Z_C = 10\ \Omega$ and $Q = 20$. The lowest phase noise is obtained for $n = 0.4$ at a bias voltage $V_{bb} = 4$ V. Fig. 2(b) shows load lines captured at the bias points for minimum phase noise, it is seen that the voltage swing is reduced, but current swing increased as the value of n is increased. It can also be noted that the minimum phase noise does not differ much when n is changed from 0.25 to 0.55, i.e., the phase-noise minimum is flat, as stated in [4].

Once an optimum n is found, the next step is to determine impedance level Z_C that was fixed to $Z_C = 10\ \Omega$ in the search for optimum n (presented in Fig. 2). Z_C also has a strong effect on voltage and current waveforms, the higher Z_C, the higher the current and lower the voltage swing. To investigate the effect of Z_C, n is fixed to $n = 0.4$, and phase noise simulated versus V_{bb} with Z_C as a parameter (the results are shown in Fig. 3), note that the emitter resistance is changed according to (11). It is found that phase noise is improved with lowered

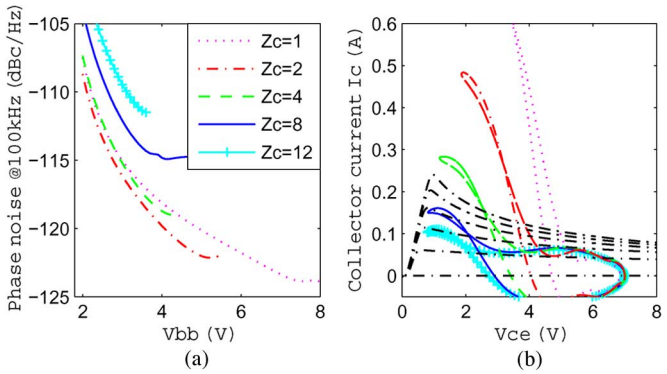


Fig. 3. Influence of the resonator impedance level Z_C when capacitive division ratio is $n = 0.4$. (a) Phase noise versus base-bias voltage with Z_C as a parameter. (b) Oscillator load lines for different Z_C, captured at optimum bias points.

Z_C. Until $Z_C \approx 2\ \Omega$, the improvement is independent of V_{bb}, while for $Z_C = 1\ \Omega$, the phase noise at low bias voltages is degraded, but a lower minimum value is reached at a higher bias. Fig. 3(b) shows load lines captured at bias points of minimum phase noise, according to Fig. 3(a). It is obvious that for high-resistance load lines, the oscillator is voltage limited, while for the lowest resistance $Z_C = 1\ \Omega$, it is current limited. Due to finite on-resistance, the voltage swing is also reduced as Z_C is lowered. The careful reader may object that the optimum n may change as Z_C is changed. However, that is not the case, which is easily verified by repeating the sweep in Fig. 2 for a lower value of Z_C, Z_C and n can be considered as independent parameters with reasonable accuracy.

The above simulations are completely theoretical without taking into account any practical issues with component values. In reality, too low values of Z_C and n may result in physically too large/small components and/or currents exceeding the breakdown limitations of the given technology. For $Z_C = 4\ \Omega$, $n = 0.4$, and an oscillation frequency of 10 GHz, the component values become $L = 64$ pH, $C_1 = 6.6$ pF, $C_2 = 9.9$ pF, and $R_e = 32\ \Omega$, values that are realizable in MMIC technology. The simulated performance for an oscillator with these component values is shown in Fig. 4, as base bias is chosen as $R_b = 1000\ \Omega$, and the output is taken through $C_{\text{out}} = 0.2$ pF. Note, as mentioned in the beginning of this section, that all parameters are well optimized, despite that phase noise was the only target parameter in the optimization. The minimum phase noise of -119 dBc/Hz @ 100-kHz offset from the carrier occurs for a bias current $I_{C0} = 160$ mA, which is right where the transistor enters the compression region and the output power is maximized. Fig. 5(a) shows waveforms and the load line at the phase-noise minimum for the optimized oscillator. It is seen that the oscillator operates in class-C with the current peak well centered around the voltage minimum.

C. Wideband VCOs

The optimum condition for a fixed-frequency oscillator was derived in Section II-B. To make this oscillator tunable, the best would be a frequency-invariant active element and a tunable resonator maintaining its impedance while the frequency is tuned. In this case, the load line of Fig. 5(b) and all oscillator

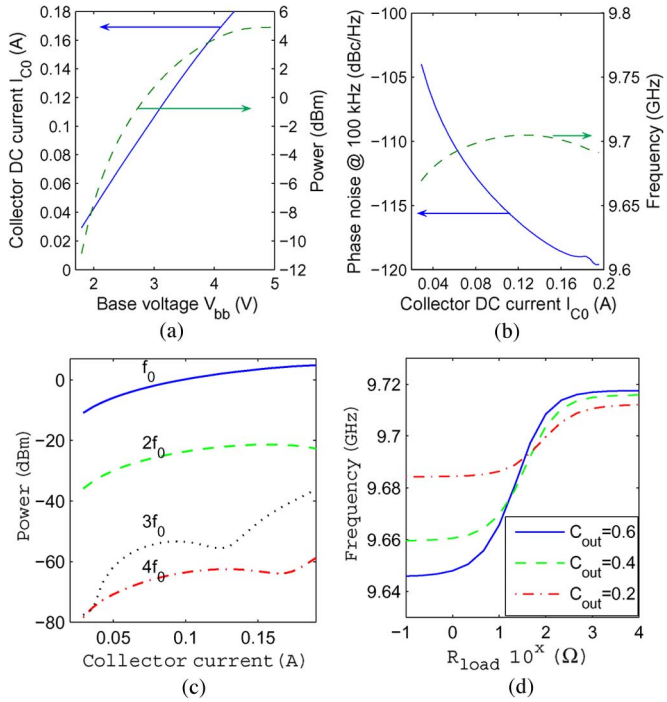


Fig. 4. Simulated performance of the optimized fixed-frequency oscillator. (a) Oscillation power versus base-bias voltage. (b) Phase noise and pushing characteristics. (c) Harmonic content. (d) Pulling figure for different C_{out} [pF].

characteristics in Fig. 4, except for frequency and phase noise, would remain unchanged when the oscillator is tuned. Phase noise would change according to (1), i.e., 6-dB increase each time frequency is doubled. However, in real VCOs, there are generally no tunable resonators maintaining impedance while frequency is tuned. Instead VCOs are generally based on varactors, i.e., variable capacitors. Its capacitance can be described by the simple relation in (2), where the fractional tunability $n_T(V)$ can have different voltage dependence, as will be discussed in Section III. In this section, the voltage dependence is not discussed.

In an oscillator, the tunability of the varactor translates to a fractional frequency tuning of $f_{\max}/f_{\min} = \sqrt{n_T(V_{\max})}$ if the varactor capacitance is the only capacitance in the tank.

In a Colpitts oscillator, the capacitance is divided between C_1 and C_2. Tuning both C_1 and C_2 is practically difficult due to arrangement of the bias network. In particular, the bias network for C_1 is complicated to arrange, while the supply for C_2 is straightforward, as it is symmetrically placed between the two emitters and ground [see Fig. 6(a)]. An example of a VCO tuned by C_2 was presented in [19]. Tuning C_2, but not C_1, is not utilizing the tuning varactor fully, the effective tunability is reduced and can be expressed as follows:

$$n_{\text{eff},C2} = 1 + n\left(n_T(V) - 1\right) \xrightarrow{n \to 0} n_T(V). \qquad (12)$$

Besides, reduced tuning efficiency, tuning only C_2 has the drawback of changing the division ratio n so the oscillator will deviate from the optimum with respect to phase noise, as derived in Section II-B. Fig. 7(a) shows how output power and phase noise varies with frequency for different values of n as C_2 is

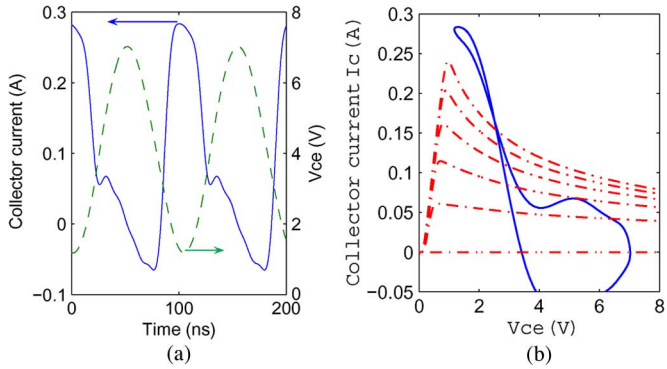


Fig. 5. Waveforms of the optimized oscillator. (a) Voltage and current in time domain. (b) Load line of the oscillator.

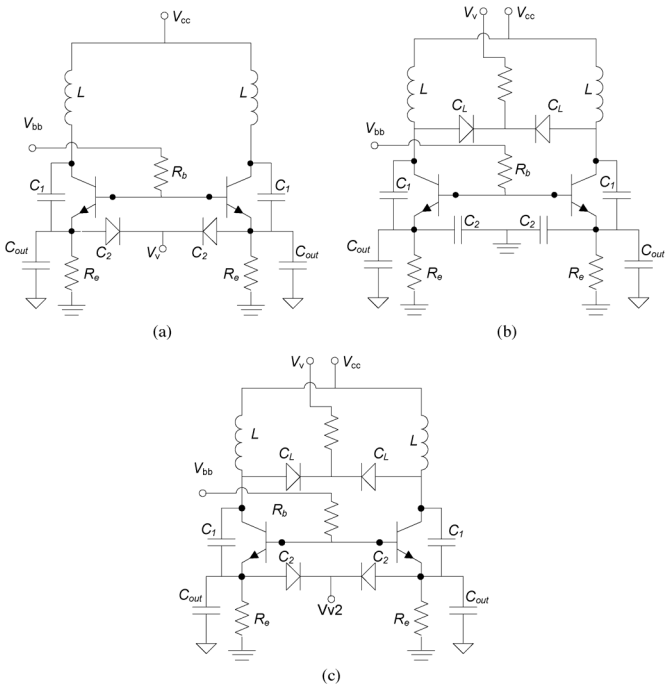


Fig. 6. Common-base BC VCOs. (a) True Colpitts tuned by C2. (b) Modified Colpitts with effectively tunable inductance. (c) DTBC VCO.

tuned, a fractional tunability $n_T(V_{\max}) = 2$ is assumed for C_2, and it is stepped in linear steps. If the untuned value of n is lower than the optimum $n = 0.4$, the phase noise will initially drop as n is increased when C_2 is reduced. The maximum output power occurs about $n = 0.55$ for larger n the slopes $\partial P/\partial f < 0$ and $\partial \mathrm{PN}/\partial f \gg 0$.

To avoid the large variations in phase noise and output power occurring when C_2 is tuned, BC oscillators are, instead, often tuned by a varactor C_L in parallel to the tank inductance [5], this implementation can be seen as an effectively tunable inductance

$$L_{\text{eff}}(V) = \frac{L}{1 - \omega^2 L C_L(V)}. \tag{13}$$

As seen from (13), the effective inductance is reduced as C_L is reduced, and the oscillation frequency is correspondingly increased. In the schematics [see Fig. 6(b)], the capacitance C_L appears in parallel to the series combination of C_1 and C_2. To

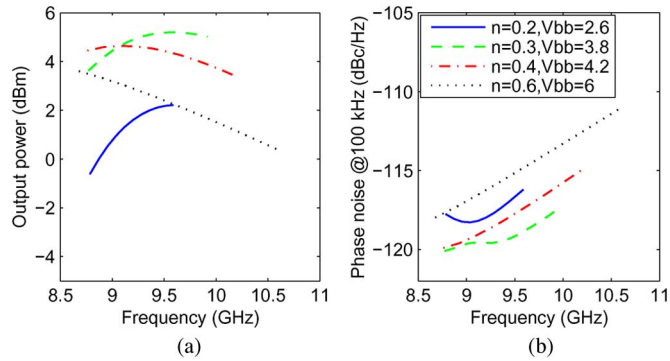


Fig. 7. Simulated tunability for true-Colpitts oscillator tuned by C_2 that is changing a factor $n_{T,\max} = 2$ [see Fig. 6(a)]. (a) Output power versus frequency. (b) Phase noise versus frequency.

maintain ω_0 and Z_C constant, C_1 and C_2 have to be correspondingly reduced as C_L is increased. Defining a ratio

$$n_R = \frac{C_L}{C_L + C_1 C_2/(C_1 + C_2)}. \tag{14}$$

The symbolical expressions (8) and (9) for the capacitance values of the Colpitts oscillator can be recalculated as capacitance is gradually moved to C_L. The new values become

$$C_1 = \frac{1}{Z_c \omega_0} \frac{1 - n_R}{1 - n} \tag{15}$$

and

$$C_2 = \frac{1}{Z_c \omega_0} \frac{1 - n_R}{n}. \tag{16}$$

The larger n_R, the better the tunability of the oscillator in Fig. 6(b). However, the introduction of C_L is a deviation from the true Colpitts topology in Fig. 1 with its good waveforms previously discussed. Increasing n_R will distort the waveforms; the peak current will no longer be centered at the voltage minimum. Fig. 8 shows that the waveforms of the modified Colpitts topology in Fig. 6(b) deviates little from a true Colpitts if $n_R \leq 0.5$. For larger values of n_R, the deviation will be significant and the phase noise considerably worse compared to a true Colpitts oscillator [see Fig. 9(a)]. To illustrate how an inductively tuned oscillator is changed while C_L is tuned, Fig. 10 shows phase noise and power variation with frequency for different n_R. For the oscillator tuned by C_2, the effective tunability was given in (12). For an oscillator tuned by C_L, the varactor appears in parallel to the series combination $C_1 - C_2$ and the effective tunability can be expressed

$$n_{\text{eff},CL} = \frac{n_T(V)}{n_R + n_T(V)(1 - n_R)} \xrightarrow[n_R \to 1]{} n_T(V). \tag{17}$$

Neither of the two different ways of tuning the BC VCO, tuned by C_2, as in Fig. 6(a), or effectively tuned inductance, as in Fig. 6(b), takes full advantage of the varactor, i.e., the varactor tunability is diluted by fixed capacitance. Both tuning methods also causes variations in phase noise and output power, which is a problem in wideband applications.

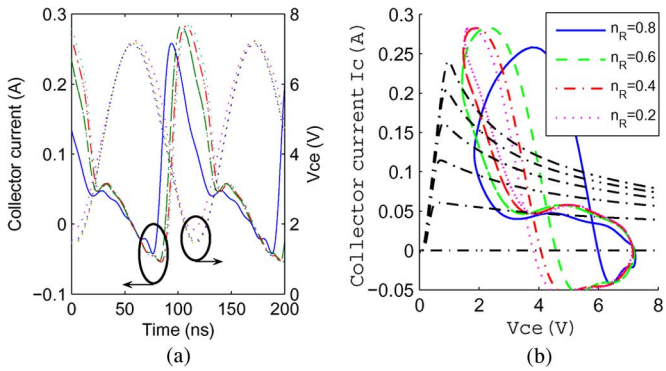


Fig. 8. Oscillator waveforms for fixed-frequency modified Colpitts oscillators with different values of n_R. (a) Voltage and current in time domain. (b) Oscillator load lines

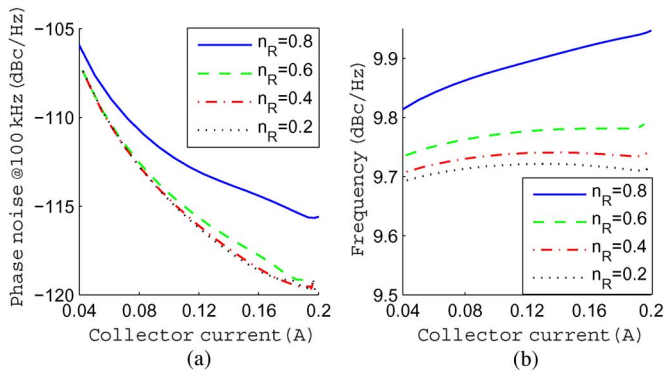


Fig. 9. Phase noise versus collector current fixed-frequency modified Colpitts oscillators with different values of n_R. (a) Phase noise. (b) Frequency.

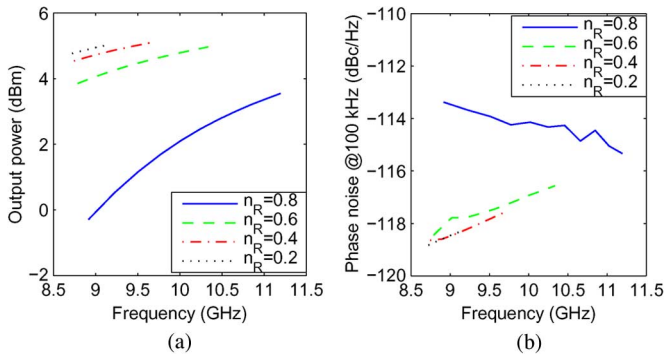


Fig. 10. Simulated tunability for modified Colpitts oscillator [see Fig. 6(b)] with a varactor C_L changing a factor $n_{T,\max} = 2$. (a) Output power versus frequency. (b) Phase noise versus frequency.

From (12) and (17), it is realized that the tunability of the VCOs in Fig. 6(a) and (b) can be improved by increasing either n or n_R. It is also seen in Figs. 7 and 10 that the two parameters n and n_R affects the variations in phase noise and output power.

An improved tuning range can be achieved with a DTBC, e.g., as the common-collector implementation proposed in [8]. A DTBC in a common-base configuration, where both C_2 and C_L are implemented as varactors, can be designed as in Fig. 6(c). Tuning the two varactors simultaneously improves not only the tuning range, but also allows for flattening the output power and trading phase-noise variations over the tuning range by changing the proportions between n and n_R. The

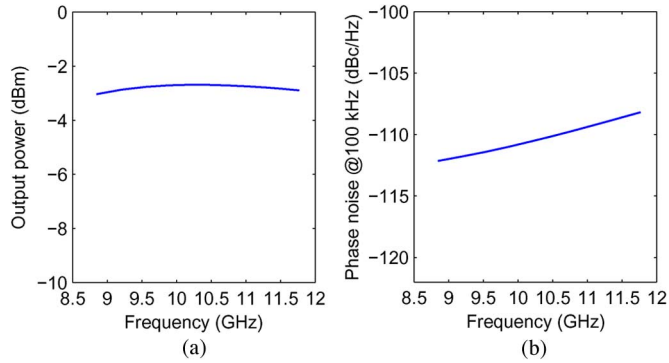


Fig. 11. Simulated tunability for wideband double-tuned VCO [see Fig. 6(c)], $n = 0.6$, $n_R = 0.8$. The two varactors are tuned a factor $n_{T,\max} = 2$. (a) Output power versus frequency. (b) Phase noise versus frequency.

effective capacitance tunability in an oscillator tuned by C_L and C_2 can be expressed as follows:

$$n_{\text{eff},CL,C2} = \frac{n_T(V)\left(1 + n_0\left(n_T(V) - 1\right)\right)}{n_R\left(1 + n_0\left(n_T(V) - 1\right)\right) + n_T(V)(1 - n_R)}. \tag{18}$$

It is not possible to derive any optimum n and n_R for an optimum tradeoff between phase noise and flat output power, as these factors both also strongly depend on the physical properties of the varactors. However, as an example of the potential for a DTBC VCO, Fig. 11 shows phase noise and output power versus frequency for the VCO with $n = 0.6$, $n_R = 0.8$, and $Z_C = 4\ \Omega$. From (18), the capacitance tunability for $n = 0.6$ and $n_R = 0.8$ is $n_{\text{eff}}(V_{\max}) = 1.9$, corresponding to a fractional frequency tunability of $f_{\max}/f_{\min} = 1.38$ that is near $\sqrt{n_T(V)}$, which would be obtained if the varactor tunability was fully utilized. In Fig. 11, the fractional frequency tunability is slightly lower, $f_{\max}/f_{\min} = 1.33$.

III. Circuit Implementations

The theories presented in Section II describe how to chose the optimum component values for oscillators and VCOs. Simply implementing these values in MMIC technology is not straightforward. Lumped elements, e.g., capacitors and inductors, are associated with parasitics, resulting in effective inductance/capacitance deviating from given values. Further, interconnecting lines will also act as series inductances adding to the given values. A commonly used approach in MMIC design is to start from analytical formulas, e.g., (6)–(9), and then optimize and tune the solution using CAD software to compensate for parasitic effects and layout constraints. This approach has the problem that the designer will never know or be able to verify whether he is near the optimum solution in any other way than just judging the achieved performance. Further, multidimensional optimization of nonlinear circuits (like oscillators) is time consuming and may be associated with convergence problems.

This paper proposes that the passive resonator is analyzed individually and its target parameters ω_0, Z_c, and n matched to the optimum solutions, as presented in Section II. Removing active elements and bias circuitry, the passive resonant tank of the BC oscillator in Fig. 1 can be drawn as in Fig. 12(a). The

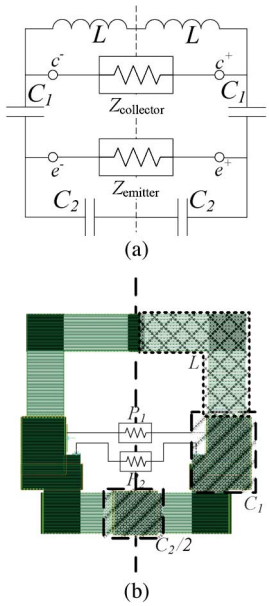


Fig. 12. Schematic and layout of balanced resonators.

critical parameters of the resonator can then be calculated from impedances $Z_{\text{collector}}$ and Z_{emitter}

$$Q = \frac{\omega_0}{2}\frac{d\phi(Z_{\text{collector}})}{d\omega}\Big|_{\omega=\omega_0} \tag{19}$$

$$Z_c = \frac{\Re\{Z_{\text{collector}}\}}{2Q} \tag{20}$$

$$n = \sqrt{\frac{\Re\{Z_{\text{emitter}}\}}{\Re\{Z_{\text{collector}}\}}}. \tag{21}$$

A. Low Phase-Noise MMIC Oscillator

The realization of a low phase-noise MMIC oscillator can be reduced to the design of a layout that mimics the ideal tank in Fig. 12(a) in terms of Z_C and n, as derived in Section II-B with as high a Q factor as possible. Fig. 12(b) shows the layout of a resonator implemented in WIN Semiconductors' InGaP HBT technology. The inductance is realized as a 50-μm-wide transmission line, utilizing metal 1 and 2 in parallel for maximum Q factor. The capacitances C_1 and C_2 are implemented as metal–insulator–metal (MIM) capacitors. For a compact layout, C_1 is designed and electromagnetic (EM) simulated. The midpoint grounding between the two capacitors (C_2) connecting the emitters is removed and the capacitors are replaced with one capacitor of half the size. The resonator is EM simulated and the results matched to an ideal resonator in Fig. 14(a)–(c). It is clearly seen that, around the oscillation frequency, the layout can be represented by the ideal lumped resonator as far as it concerns the critical parameters Q, Z_c, and n. At other frequencies, there are significant differences between the layout and the ideal resonator, e.g., there is a series resonance in the C_2 branch that the careful reader can identify in Fig. 14(a). However, at a first approximation, the waveforms and the oscillator's performance are determined primarily by the behavior around the oscillation frequency. Commenting on Fig. 14, the ideal resonator also shown in the figure has $Q = 23$, $Z_c = 4$, and $n = 0.25$. The value of n is ironically close to the conventional rule-of-thumb [3]. According to Section II-B, $n = 0.4$ is better, but when coming to the physical implementation, the Q factor is reduced with increased n due to increased size of C_1.

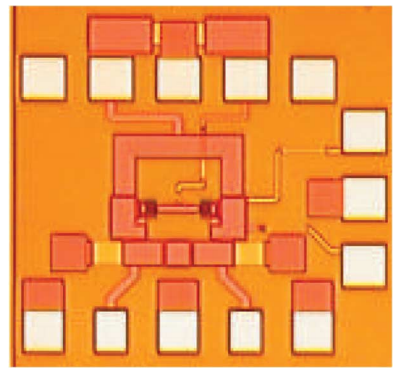


Fig. 13. Micrograph of low-impedance oscillator.

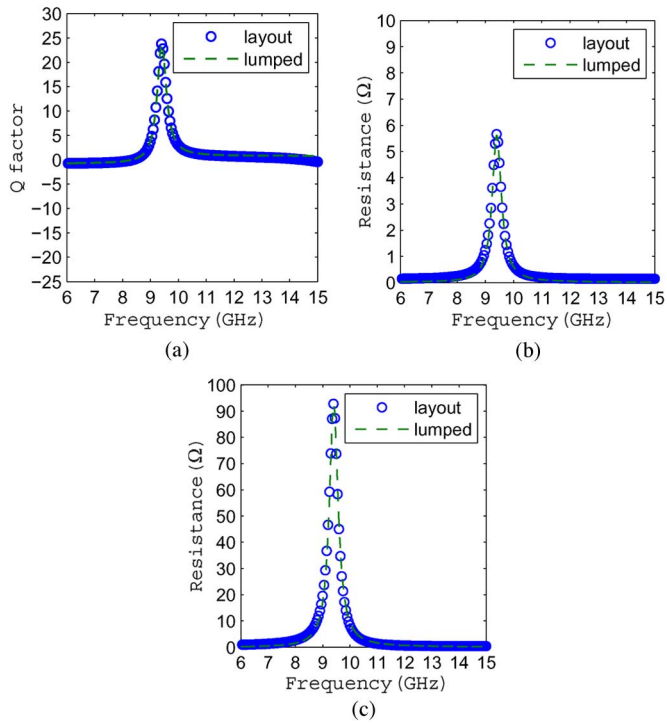
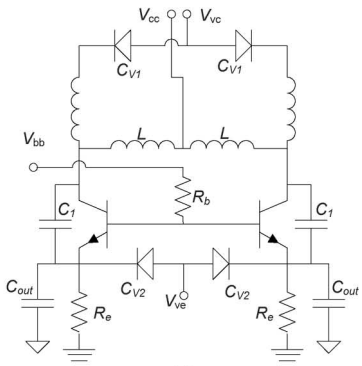


Fig. 14. Comparison of ideal lumped resonator and layout of the low impedance resonator. (a) Q factor. (b) Resistance at the emitter port. (c) Resistance at the collector port.

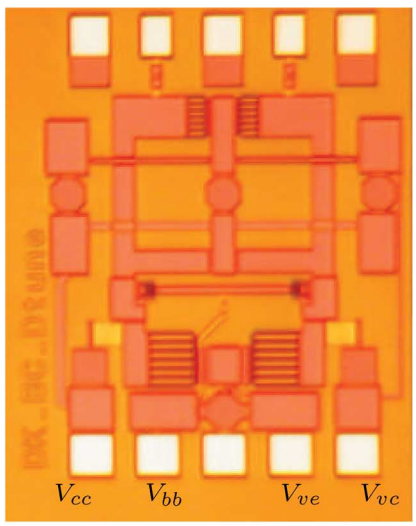
The simulations of the low phase-noise MMIC oscillator are shown together with the measurements in Fig. 18. The simulated phase noise is -117 dBc/Hz @ 100-kHz offset, which compares well to the simulations of the ideal resonator in Section II-B.

B. DTBC VCO

To demonstrate the design of wide-tuning range oscillators, a DTBC VCO was implemented in WIN Semiconductors' dedicated InGaP HBT VCO process (H01U-10). The design [see



(a)



(b)

Fig. 15. DTBC VCO. (a) Schematics. (b) Micrograph.

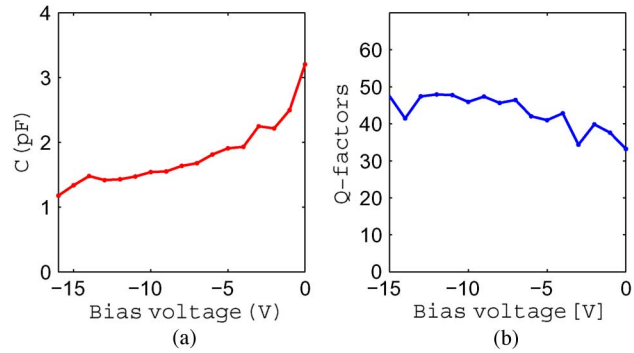


Fig. 16. Measured performance of a varactor with seven fingers of length 60 μm and width 15 μm. (a) CV. (b) Q factor at 7 GHz extracted from the Deloach structure.

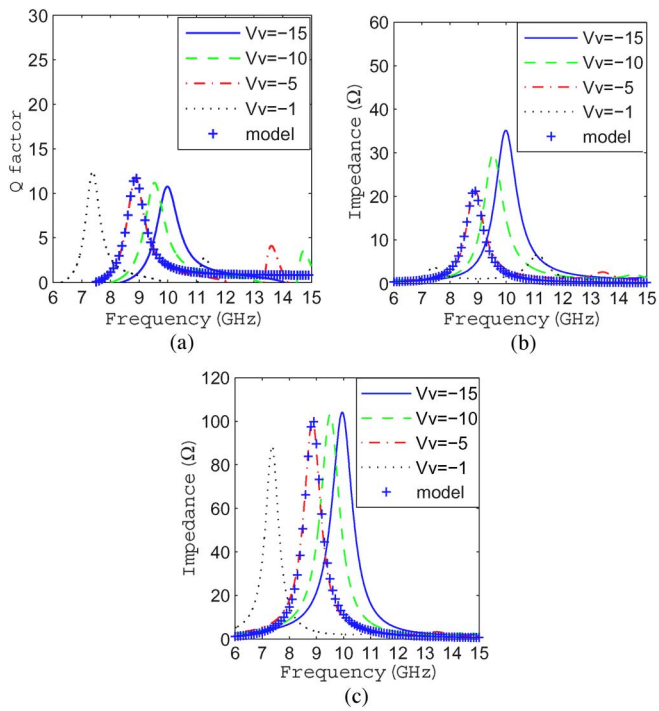


Fig. 17. Simulation of the resonator in the double-tuned VCO. (a) Q factor. (b) Resistance at the emitter port. (c) Resistance at the collector port.

Fig. 15(b)] utilizes the same four-finger HBT as the fixed-frequency oscillator in Section III-A. For lowest phase noise, special high-Q finger varactors are utilized. Fig. 16 shows varactor capacitance (C_V) and Q factor versus bias voltage for a $7\times15\times60$ μm^2 varactor. The Q factor, measured from a 6-GHz Deloach structure, is better than 30 for all tuning voltages, and the varactor's tuning ratio is about $n(V_{\max}) = 2.4$ for tuning voltages between $V_V = 0$ and -15 V. The capacitance per unit area of these varactors is lower compared to MIM capacitors. For this reason, the varactor C_L is complemented with a series inductance to achieve an effective capacitance that is larger than the varactor capacitance. This implementation has the drawback of reducing the tank-Q factor that will be limited by series resistance from the sheet resistance in the metal strip constituting the series inductance. As the tank-Q factor is limited by inductance rather than varactor capacitance, the highest Q factor occurs when the varactor bias voltage approaches the forward region where the varactor capacitance is the highest. The top varactors, between the collectors, have six fingers of width 10 μm and length 40 μm, while the varactors between the two emitters have six fingers of width and length 12 and 100 μm, respectively. The inductance is realized with 50-μm wide transmission lines. Fig. 17 shows the simulated Q factor and impedance at three different varactor-bias conditions. The quality factor is about $Q \approx 12$, the impedance level $Z_C = 4-5\ \Omega$, and the tapping ratio $n = 0.1$–0.6, depending on bias voltage. The performance at $V_V = -5$ V is fit with an ideal resonator with parameters $Q = 20$, $Z_C = 4.2\ \Omega$, $n = 0.46$, and $n_R = 0.4$.

The prototype VCO [see Fig. 15(b)] is designed with different bias pads for base, collector, and the two tuning varactors. The tuning varactors are tuned relative to the emitter and collector, respectively. In order to suppress noise from bias lines, the layout [see Fig. 6(c)] is highly symmetrical with custom-designed decoupling capacitors. The design is also very compact, occupying an area of only 800 $\times$ 1050 μm^2. Simulated performance of the VCO are shown together with measurements in Fig. 20.

IV. Experiments and Results

The fixed-frequency oscillator and the double-tuned VCO were characterized on-wafer. Phase noise was measured with the Agilent E5500 phase-noise system using the discriminator

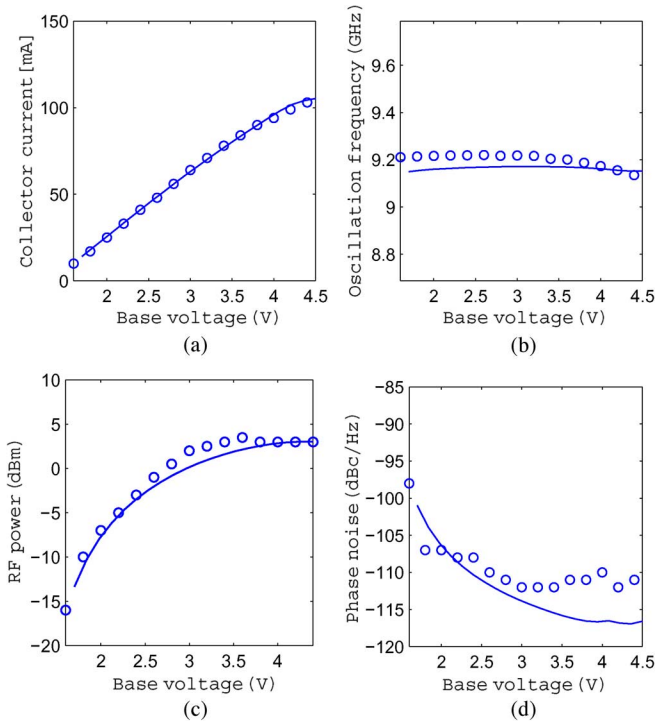


Fig. 18. Measured (markers) and simulated (lines) performance versus base-bias voltage for the low-impedance oscillator under bias point of $V_{cc} = 7$ V. (a) Collector current. (b) Frequency. (c) Output power. (d) Phase noise.

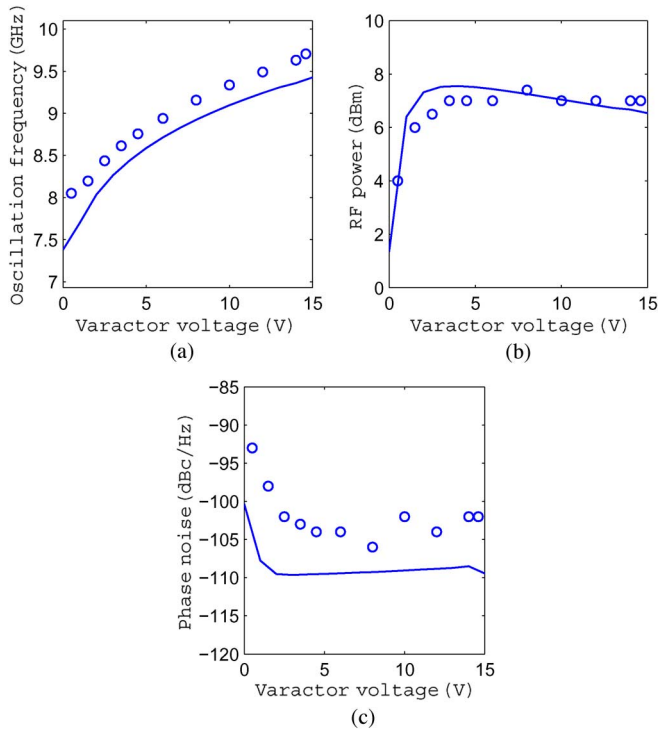


Fig. 20. Measured characteristics versus varactor voltage for the DTBC VCO under bias point of $V_{cc} = 7$ V and $I_C = 95$ mA. (a) Oscillation frequency. (b) Output power. (c) Phase noise.

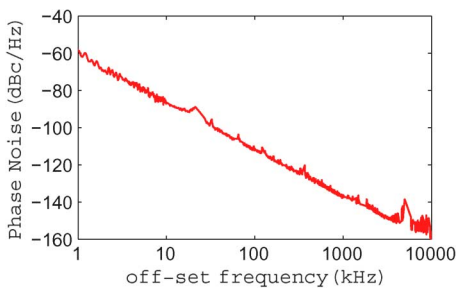


Fig. 19. Phase noise versus offset frequency for low-impedance oscillator at $V_{CC} = 7$ V and $V_{bb} = 3$ V.

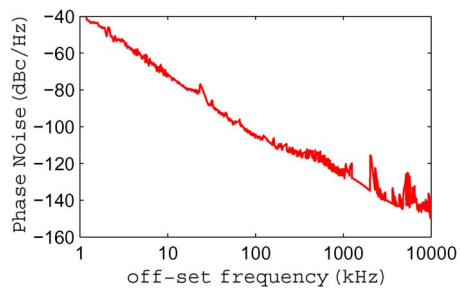


Fig. 21. Phase noise versus offset frequency for the DTBC VCO, measured at a bias point of $V_{cc} = 7$ V, $I_C = 95$ mA, and $V_V = -7$ V.

method. Frequency and output power were measured with an Agilent 8565EC spectrum analyzer, power calibrated using an E4419B power meter. The output power of the differential circuits was measured from one output while the other was terminated in 50 Ω, combining the two outputs in a balun would give nearly 3-dB higher output power. Firstly, the base voltage (V_{bb}) was tuned with respect to phase noise and output power.

Fig. 18 shows measured characteristics of the fixed frequency oscillator compared to simulations. The agreement between simulations and measurements is good; collector current, oscillation frequency, and power are all well predicted. The phase noise is well predicted until a collector current of 60 mA, corresponding to $V_{bb} = 3$ V, where the transistor enters the compression region with less accurate prediction of phase noise. As previously mentioned, the accuracy in this region can probably be improved if noise sources are treated cyclostationary [13]. Fig. 19 shows measured phase noise versus offset frequency at a collector current of 60 mA for the fixed-frequency oscillator.

The double-tuned VCO was measured with the same setup as the fixed frequency oscillator. First the varactor voltage was set to $V_V = -2$ V for both varactors and the base voltage increased until minimum phase noise was reached at $V_{bb} = 4.9$ V, corresponding to $I_C = 95$ mA. The collector voltage was $V_{cc} = 7$ V. Finally, after fixing V_{bb} and V_{cc}, the varactor voltages were tuned, and the VCO characteristics recorded for each tuning voltage.

Measured frequency and output power versus varactor voltage are compared to simulated results in Fig. 20. The results are presented as a function of varactor voltage (V_V); the actual tuning voltages are $V_{Tc} = V_V + 7$ V and $V_{Te} = V_V + 1.5$ V. Under all bias conditions, the measured and simulated output power agrees within the measurement accuracy and the measured oscillation frequency is about 0.2–0.3 GHz higher than

TABLE I
STATE-OF-THE-ART LOW PHASE-NOISE MMIC VCOs, BENCHMARKED WITH RESPECT TO TUNING BANDWIDTH

Techology	Frequency (GHz)			Phase noise (dBc/Hz)@		Δf (kHz)	$P_{\rm out}$ (dBm)	FOM	[**ref**]
	$f_{\rm min}$	$f_{\rm max}$	$f_{\rm BW}$	min	max				
InGaP HBT	12.8	13.0	0.2	-120	-110	100	-10	196	[1]
InGaP HBT	25.35	1.4	26.1	-106	-95	100	-10	197	[2]
InGaP HBT	6.7	8.7	2.0	-100	-94	100	-5	200	[6]
InGaP HBT	6.1	7.5	1.4	-102	-99	100	-5	102	[6]
SiGe HBT	6.7	8.7	2.0	-115	-115	1000	-10	201	[8]
InGaP HBT	23.5	28.0	4.5	-95	-88	100	-2	201	[21]
InGaP HBT	19.9	28.2	8.4	-93	-87	100	-8	205	[21]
SiGe HBT	2.8	3.1	0.3	-105	-103	100	0	193	[22]
CMOS	3.1	5.2	2.1	-95	-90	100	N/A	196	[23]
CMOS	1.2	2.4	1.2	-108	-101	100	N/A	203	[24]
InGaP HBT	8,4	9.7	1.3	-106	-102	100	7	204	This work $V_V \leq -2.5V$
InGaP HBT	8.2	9.7	1.5	-106	-98	100	7	202	This work $V_V \leq -1.5V$
InGaP HBT	8	9.7	1.7	-106	-93	100	7	198	This work $V_V \leq -0.5V$

in simulations, indicating a too low estimate of the varactor capacitance. The measured phase noise is about 5 dB higher than in simulations, associated with the inaccurate prediction when the transistor goes into compression. However, as predicted by simulations in Section II, the phase noise and output power are both rather invariant over the tuning range. Fig. 21 shows phase noise versus offset frequency for $V_V = -7$ V, the varactor voltage providing the best phase noise. It is seen that the measured $1/f^3$ corner frequency is located about $\Delta f = 100$ kHz, which is rather high compared to conventional BC VCOs in InGaP HBT, e.g., for the fixed-frequency oscillator in Fig. 19, no corner-frequency is detected. This may indicate that the varactors are at least partly responsible for the up-conversion of low-frequency noise [20].

Despite the slightly high $1/f^3$ corner frequency, the DTBC VCO presented in this paper presents state-of-the-art low phase noise for wideband VCOs. Table I benchmarks VCOs in open literature versus a FOM

$$\text{FOM} = -\text{PN} + 20\log_{10}\left(\frac{f_{\rm BW}}{\Delta f}\right) \tag{22}$$

where PN is the highest phase noise measured within the tuning bandwidth $f_{\rm BW}$ and Δf is the offset frequency where PN is measured. The DTBC VCO reported in this paper is the only VCO maintaining a phase noise better than -102 dBc/Hz at 100-kHz offset over a frequency range of 1.3 GHz or more. Note that the FOM in (22) excludes the dc power consumption, in contrast to the power-normalized FOM [18] often used for VCOs in CMOS technology. The reason for excluding the power consumption is that this paper focuses on absolute performance rather than low power consumption. The power consumption of the DTBC VCO is 7×95 mW which is high compared to many other oscillators, but not disqualifying in applications, e.g., microwave links.

V. CONCLUSIONS

Methods for design of low phase-noise and wide-tuning range BC oscillators and VCOs have been presented. The validity of the methods is verified by implementations in InGaP HBT technology. A novel DTBC VCO with varactors between both emitters and collectors presents a phase noise better than -102 dBc/Hz at 100-kHz offset, over a 1.3-GHz tuning range with a nearly constant output power about 7 dBm. To the authors' best knowledge, no other VCO published maintains such low phase noise over that tuning bandwidth.

ACKNOWLEDGMENT

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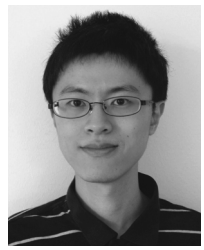

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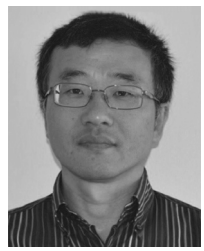
Mr. Lai was the recipient of the Transistor Modeling Competition of the 2012 IEEE Microwave Theory and Techniques Society (IEEE MTT-S) International Microwave Symposium (IMS).



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