Description of the microscope control software (LabVIEW)

The virtual instrument (VI) file '*whole_setup_control_RT_v1229.vi*' is implemented on the real-time target (RT) of the CompactRIO controller (cRIO-9038).

The VI file '*whole_setup_control_FPGA_v1229.vi*' is implemented on the FPGA target of the CompactRIO controller.

In addition, the FPGA target also contains

- RT to FPGA FIFO: a FIFO transferring data from RT to FPGA.
- FPGA to RT FIFO: a FIFO transferring data from FPGA to RT.
- Blocks of memory for storing pre-calibrated waveforms.

Pre-calibrated waveforms, formatted as text, are written into the file '*20231229_4980us_output_signal.dat*' on the RT. Upon the initialization of the control software, the RT VI file reads this file, then transfers the waveform values to the FPGA through the 'RT to FPGA FIFO'. These values are stored in the FPGA's memory blocks for high-speed readout and output.

The software allows for real-time adjustment of the driving voltage signals for the piezo scanner, the galvo mirror, and the trigger signals for cameras and lasers. Initially stored in the FPGA's memory, the waveforms undergo multiple computational steps, such as phase shifting, linear transformations, and combinations. The processed waveforms are then output through analog and digital I/O devices. The parameters used for these computational steps are dynamically set through the user interfaces of the RT VI ('*whole_setup_control_RT_v1229.vi*' front panel).

For non-linear adjustment of the galvo mirror's driving signals, our software allows real-time modifications to the waveform values in the FPGA memory. This is achieved by superimposing a pulse waveform onto the existing waveforms. Users can set the phase and amplitude of these pulse signals in real-time through the RT VI front panel. We use a Gaussian-shaped pulse waveform as the correction waveform to ensure the updated waveforms remain smooth.

Moreover, the timing of the trigger signals for the cameras and laser, as well as the duration of the laser pulse, can be adjusted in real-time via the RT VI front panel.

Finally, our software offers two operational modes: a recording mode and a debugging mode. In the debugging mode, the laser activates only at a user-specified time, set through the RT VI front panel, and for a duration also determined by the user in each volumetric scanning cycle. This feature enables real-time visualization of the raw images of a specific z plane during volumetric scanning.

The FPGA of the cRIO-9038 controller operates at a clock rate of 40 MHz, corresponding to a clock cycle of 25 ns (one tick). Our software updates the output signals every 160 ticks (4 μs). Each of the pre-calibrated waveforms contains 1245 values, taking 4980 μs to complete a full output cycle.