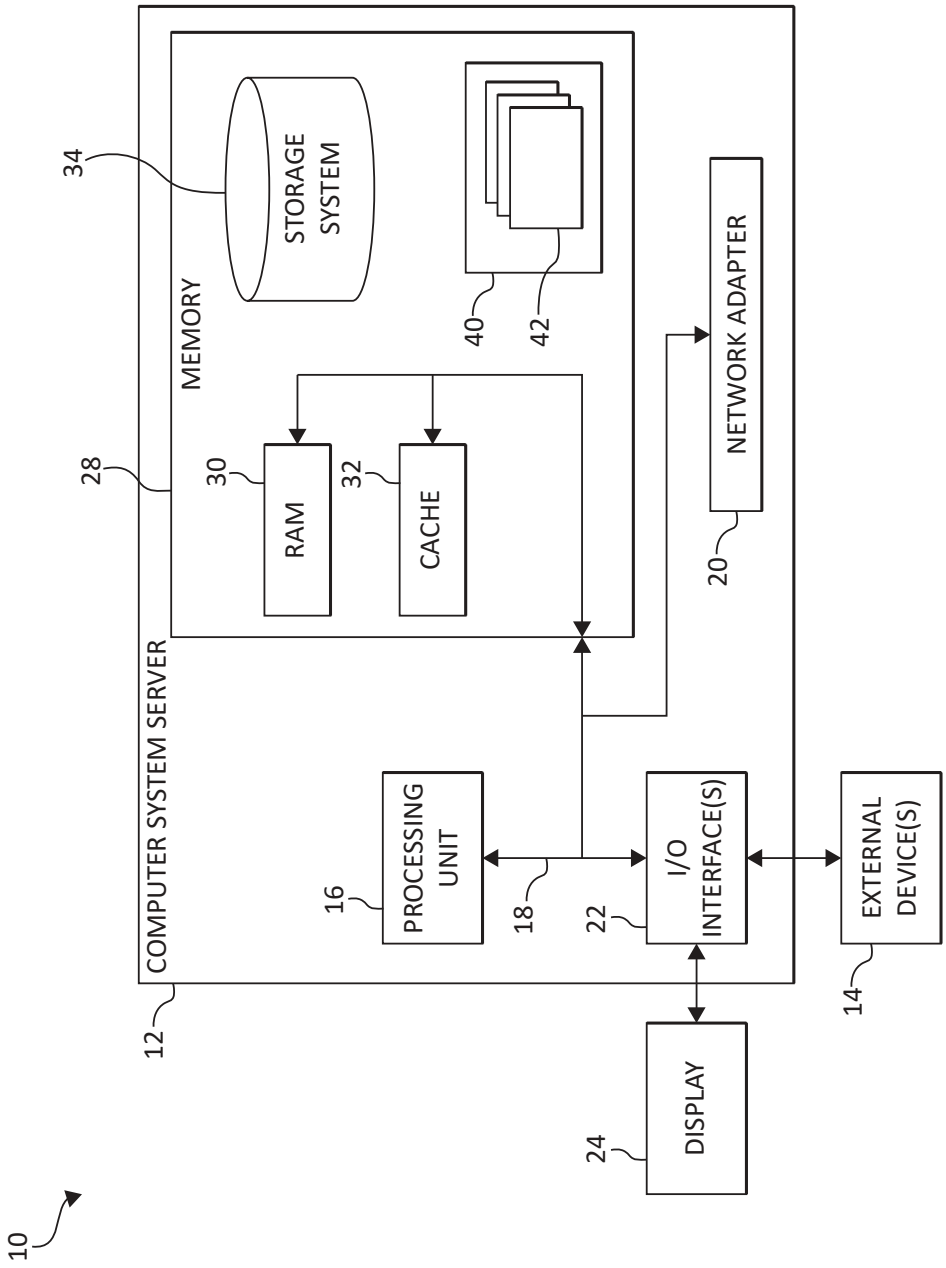
10
12
COMPUTER SYSTEM SERVER
28
MEMORY
34
STORAGE SYSTEM
40
42
30
RAM
32
CACHE
NETWORK ADAPTER
20
16
PROCESSING UNIT
18
22
I/O INTERFACE(S)
EXTERNAL DEVICE(S)
14
24
DISPLAY

FIG. 1

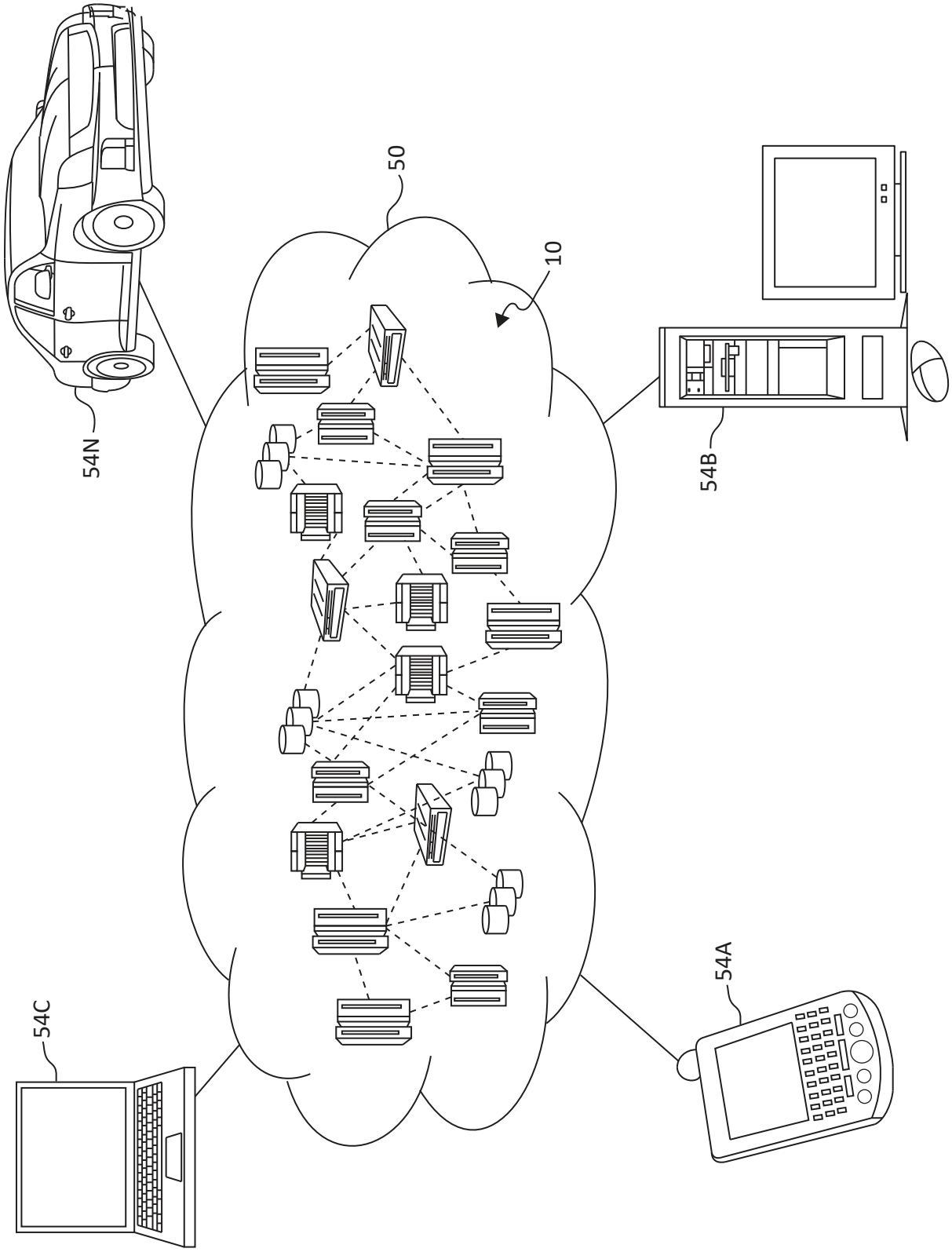

FIG. 2

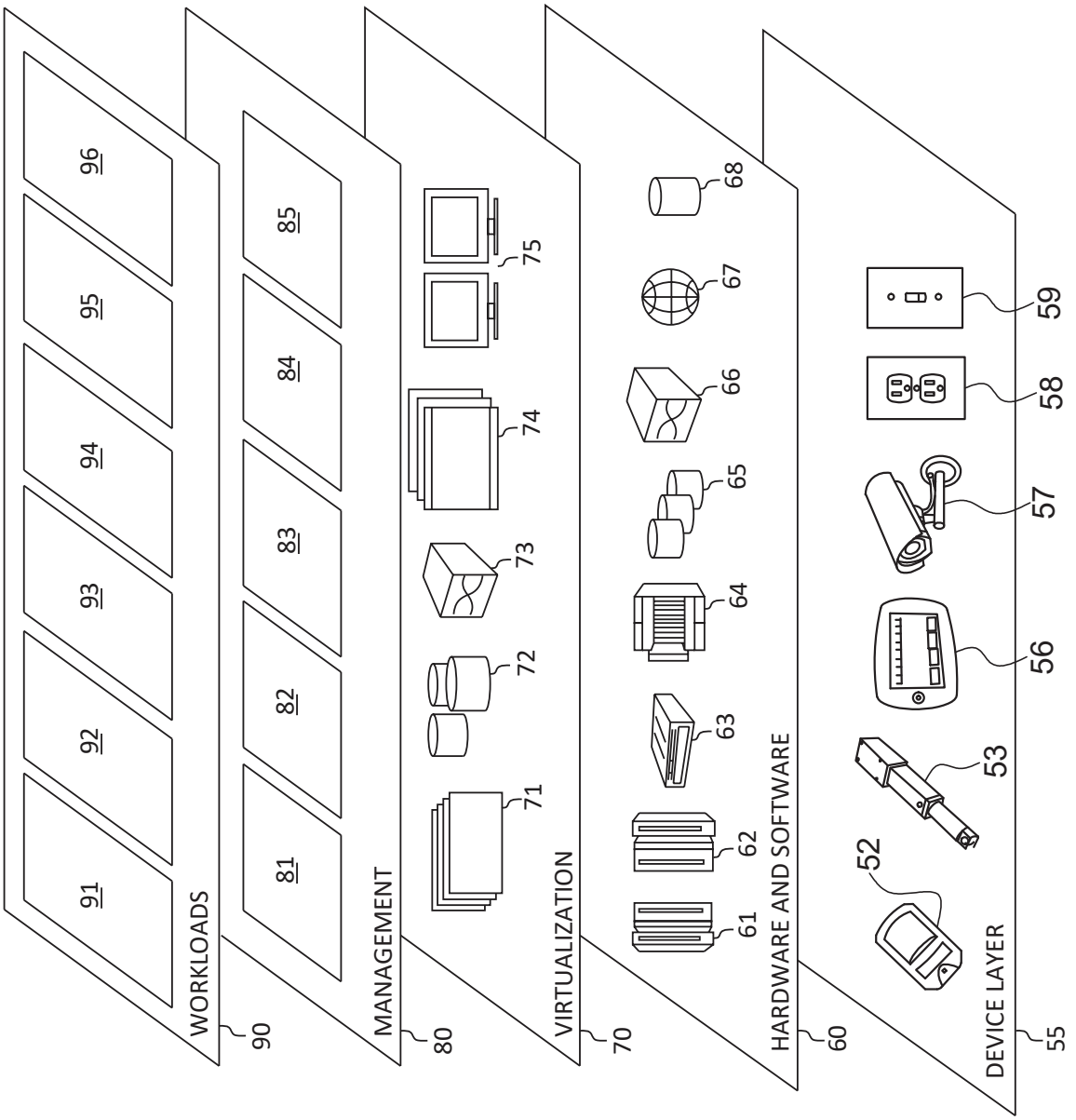
WORKLOADS
90
91
92
93
94
95
96
MANAGEMENT
80
81
82
83
84
85
VIRTUALIZATION
70
71
72
73
74
75
HARDWARE AND SOFTWARE
60
61
62
63
64
65
66
67
68
DEVICE LAYER
55
52
53
56
57
58
59

FIG. 3

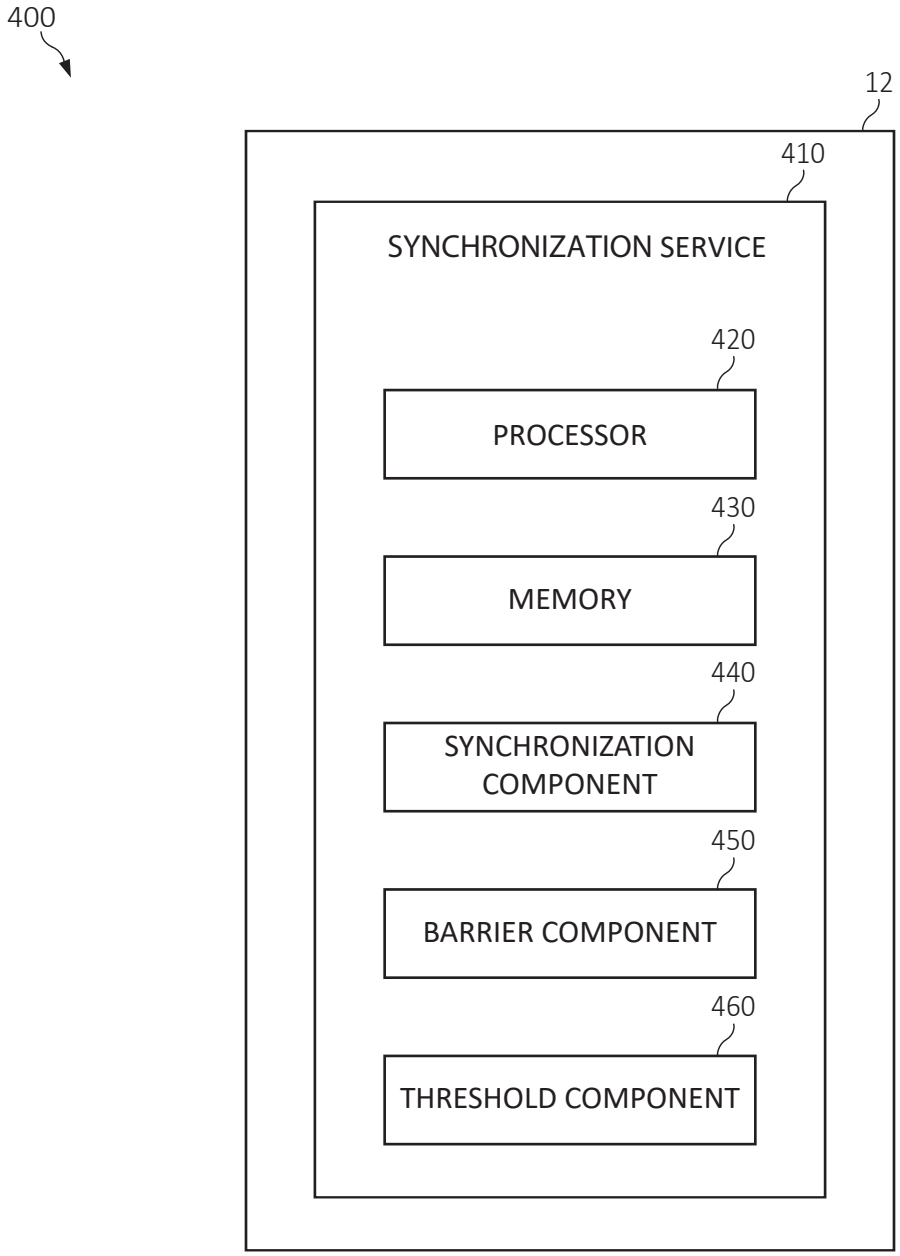
400
12
410
SYNCHRONIZATION SERVICE
420
PROCESSOR
430
MEMORY
440
SYNCHRONIZATION COMPONENT
450
BARRIER COMPONENT
460
THRESHOLD COMPONENT

FIG. 4

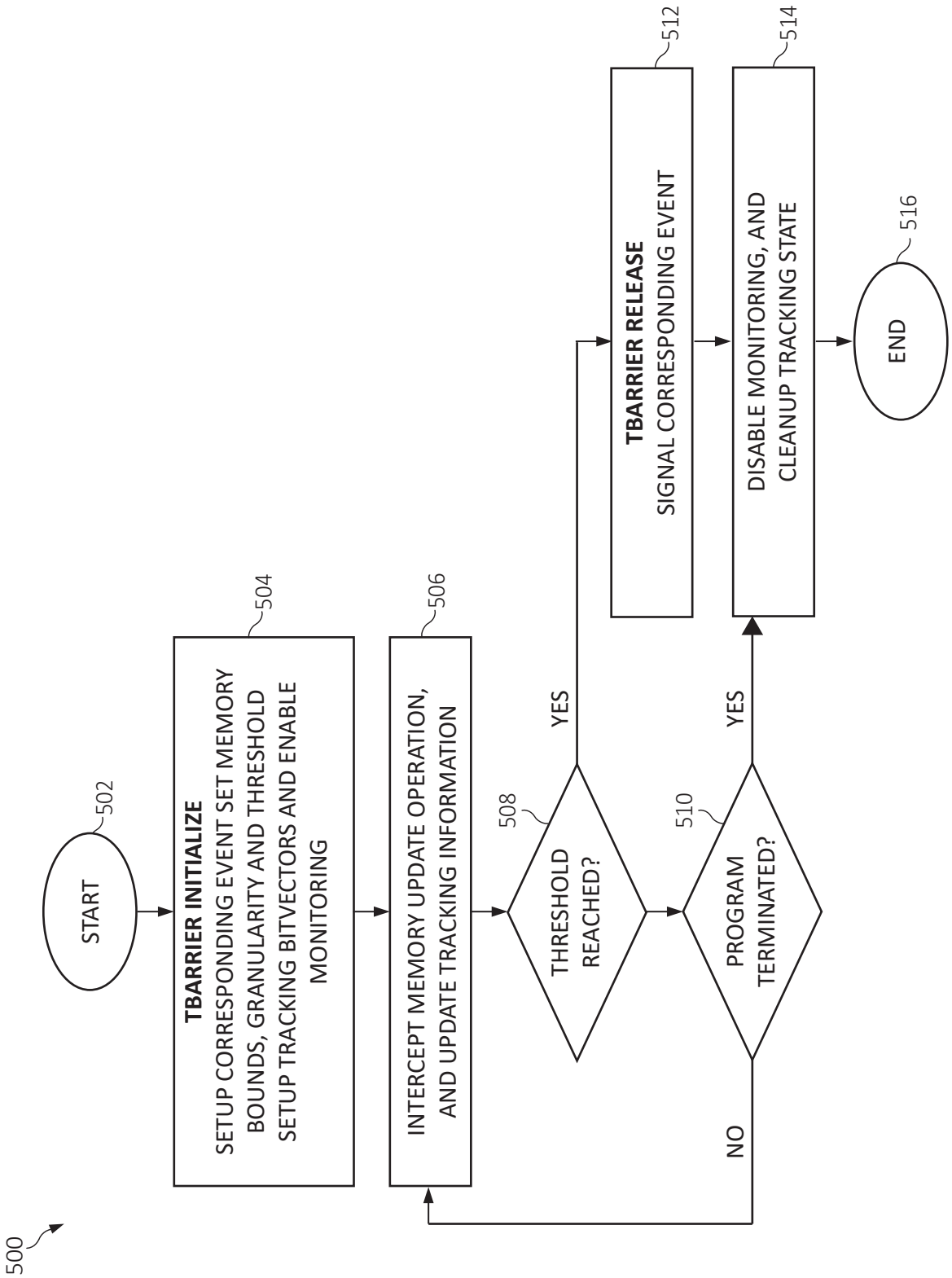
500
START
502
TBARRIER INITIALIZE
SETUP CORRESPONDING EVENT SET MEMORY BOUNDS, GRANULARITY AND THRESHOLD
SETUP TRACKING BITVECTORS AND ENABLE MONITORING
504
INTERCEPT MEMORY UPDATE OPERATION, AND UPDATE TRACKING INFORMATION
506
THRESHOLD REACHED?
508
YES
TBARRIER RELEASE
SIGNAL CORRESPONDING EVENT
512
PROGRAM TERMINATED?
510
YES
NO
DISABLE MONITORING, AND CLEANUP TRACKING STATE
514
END
516

FIG. 5

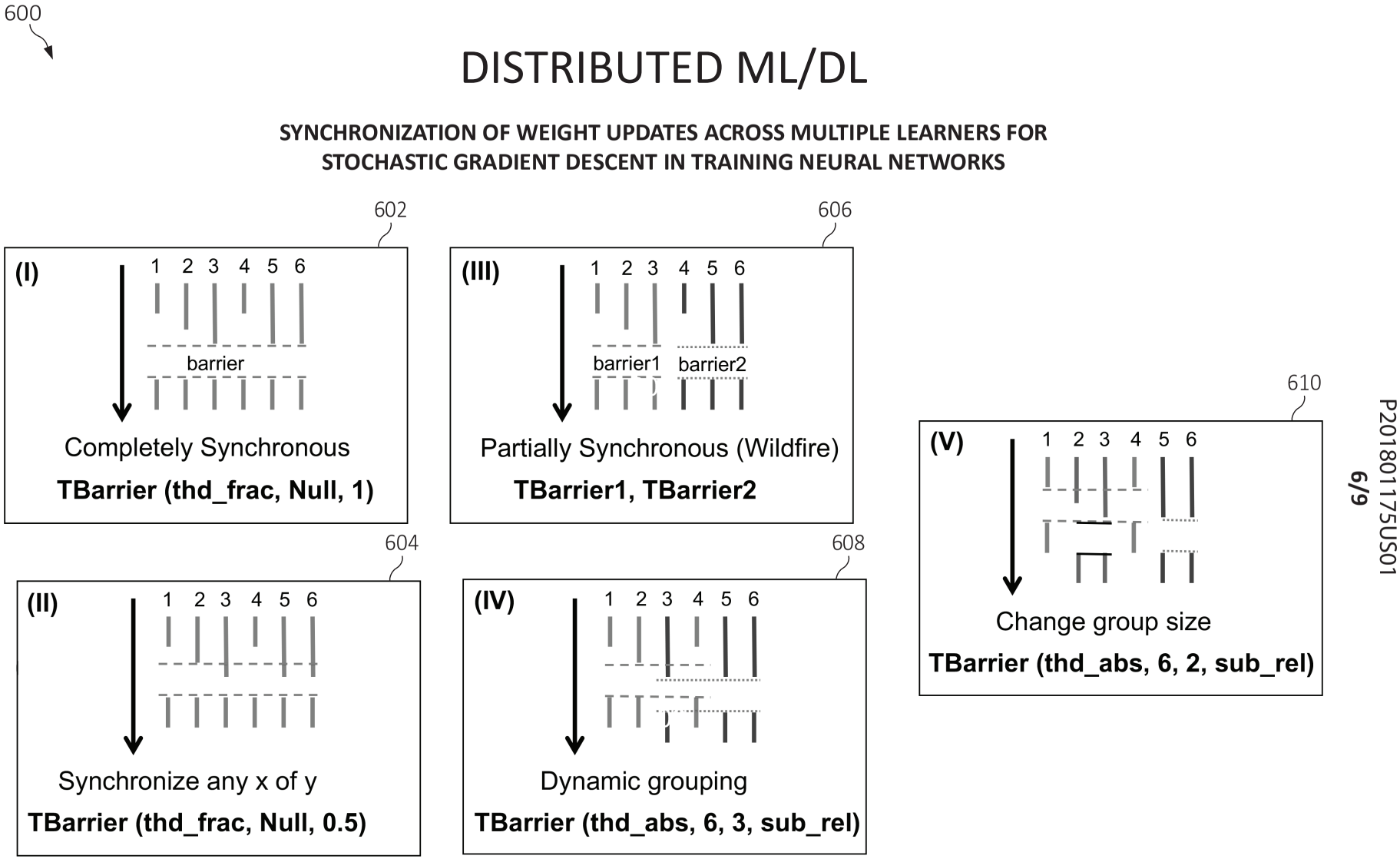
600
DISTRIBUTED ML/DL
SYNCHRONIZATION OF WEIGHT UPDATES ACROSS MULTIPLE LEARNERS FOR STOCHASTIC GRADIENT DESCENT IN TRAINING NEURAL NETWORKS
602
(I)
1 2 3 4 5 6
barrier
Completely Synchronous
TBarrier (thd_frac, Null, 1)
606
(III)
1 2 3 4 5 6
barrier1
barrier2
Partially Synchronous (Wildfire)
TBarrier1, TBarrier2
610
(V)
1 2 3 4 5 6
Change group size
TBarrier (thd_abs, 6, 2, sub_rel)
604
(II)
1 2 3 4 5 6
Synchronize any x of y
TBarrier (thd_frac, Null, 0.5)
608
(IV)
1 2 3 4 5 6
Dynamic grouping
TBarrier (thd_abs, 6, 3, sub_rel)

FIG. 6

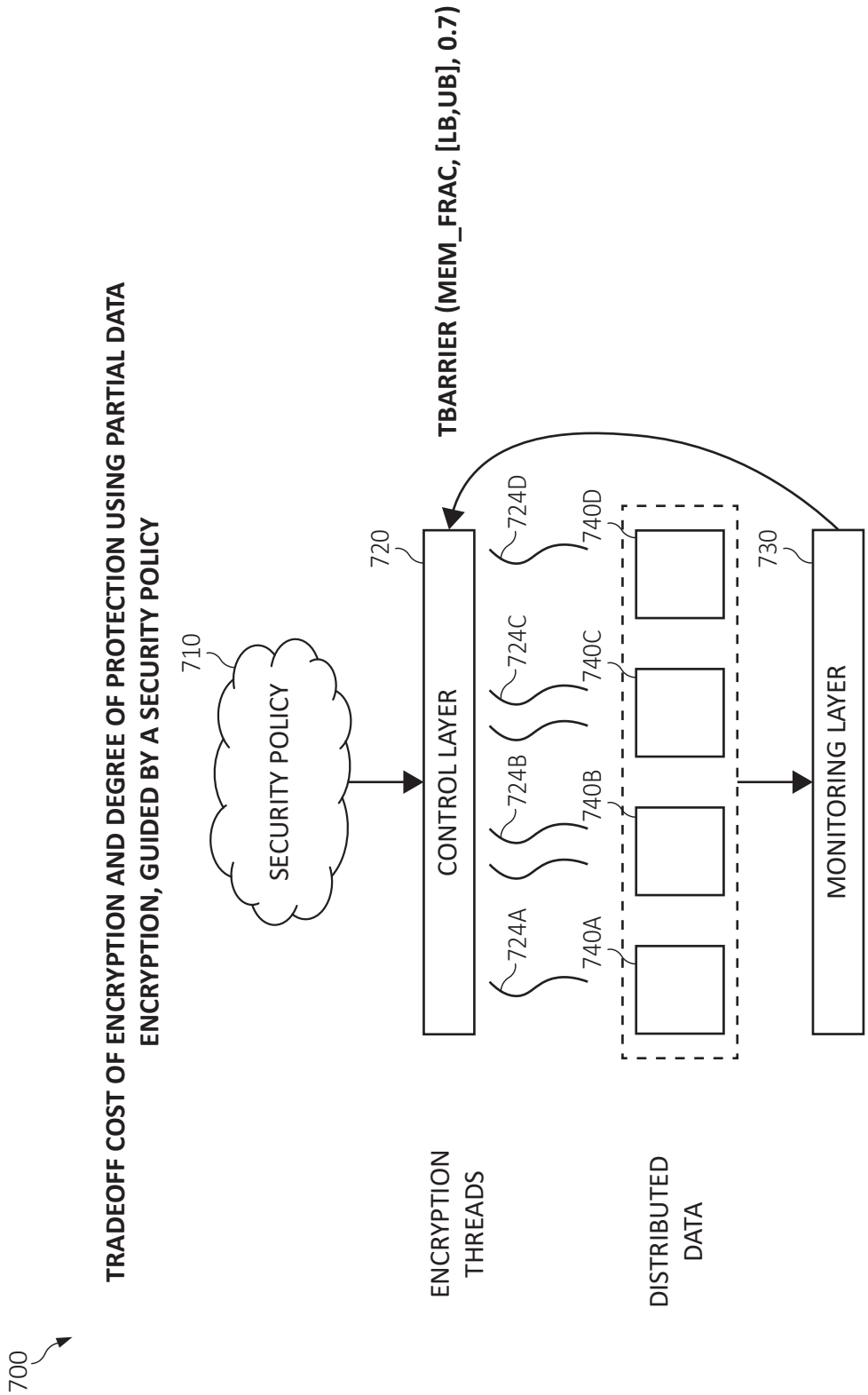
700
TRADEOFF COST OF ENCRYPTION AND DEGREE OF PROTECTION USING PARTIAL DATA ENCRYPTION, GUIDED BY A SECURITY POLICY
710
SECURITY POLICY
720
CONTROL LAYER
TBARRIER (MEM_FRAC, [LB,UB], 0.7)
724A
724B
724C
724D
740A
740B
740C
740D
730
MONITORING LAYER
ENCRYPTION THREADS
DISTRIBUTED DATA

FIG. 7

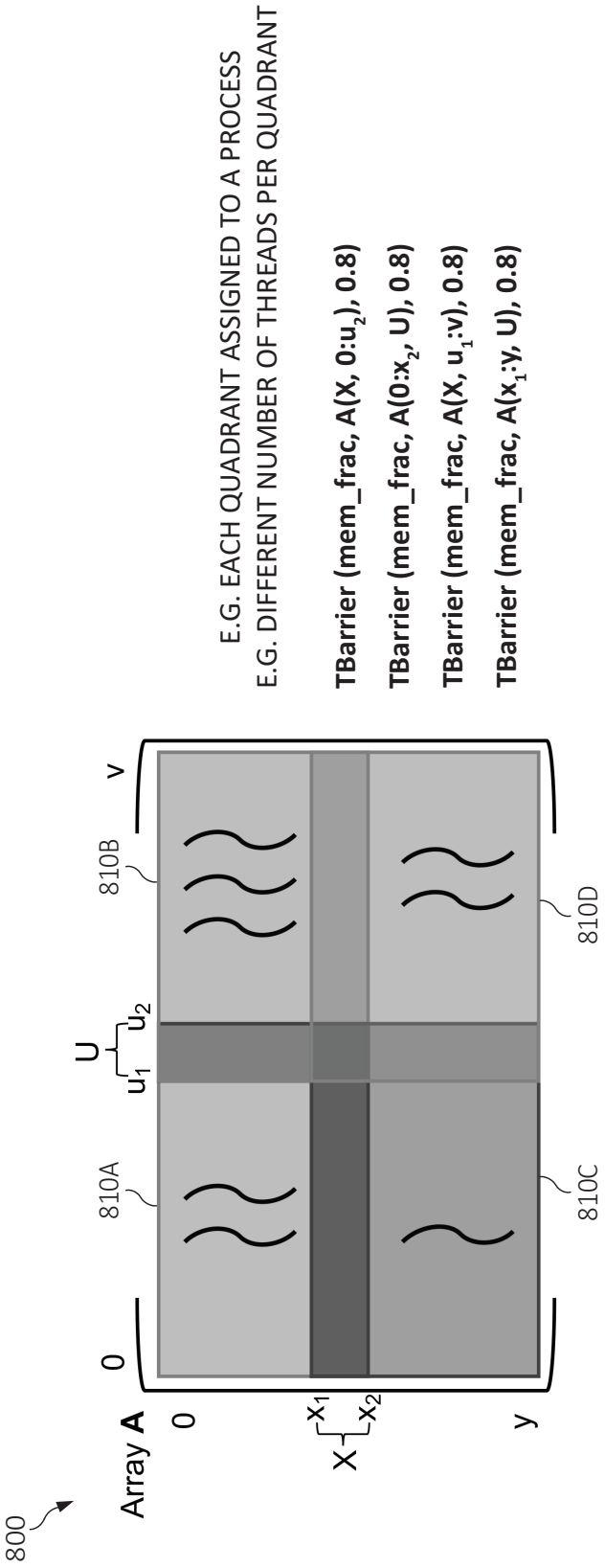
800
Array **A**
0
0
X
x_1
x_2
y
U
u_1
u_2
v
810A
810B
810C
810D
E.G. EACH QUADRANT ASSIGNED TO A PROCESS
E.G. DIFFERENT NUMBER OF THREADS PER QUADRANT
TBarrier (mem_frac, A(X, 0:u_2), 0.8)
TBarrier (mem_frac, A(0:x_2, U), 0.8)
TBarrier (mem_frac, A(X, u_1:v), 0.8)
TBarrier (mem_frac, A(x_1:y, U), 0.8)

FIG. 8

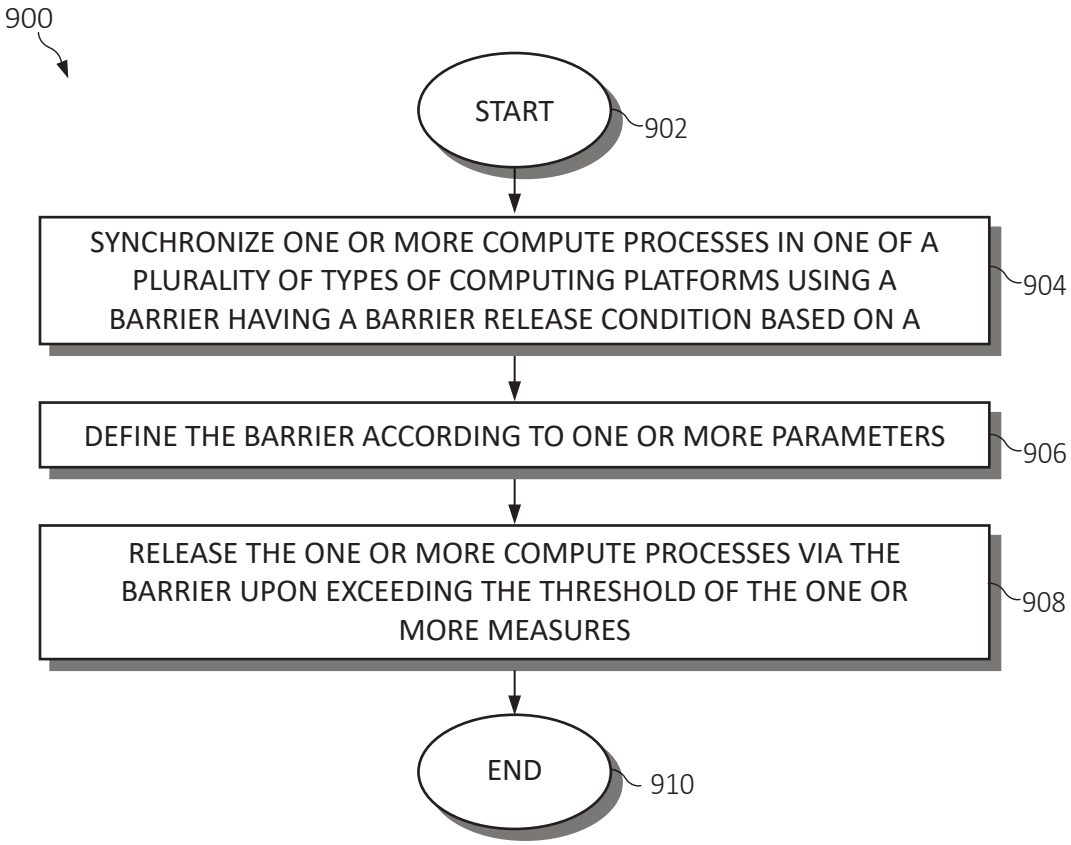
900
START
902
SYNCHRONIZE ONE OR MORE COMPUTE PROCESSES IN ONE OF A PLURALITY OF TYPES OF COMPUTING PLATFORMS USING A BARRIER HAVING A BARRIER RELEASE CONDITION BASED ON A
904
DEFINE THE BARRIER ACCORDING TO ONE OR MORE PARAMETERS
906
RELEASE THE ONE OR MORE COMPUTE PROCESSES VIA THE BARRIER UPON EXCEEDING THE THRESHOLD OF THE ONE OR MORE MEASURES
908
END
910

FIG. 9