ERIC ZHOU

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Java • Go • C • C++ • Scala • Python • JavaScript • SQL • Assembly • SPICE • Verilog

EDUCATION

August 2015 - May 2019 (Expected Graduation)
University of California, Berkeley
B.S. Electrical Engineering and Computer Sciences
GPA 3.91
Awards: Honors to Date • Dean's List • Eta Kappa Nu
Relevant Courses: **CS61B** (Data Structures) • **CS61C** (Machine Structures) • **CS162*** (Operating Systems and Systems Programming) • **CS70** (Discrete Mathematics) • **CS186** (Databases) • **CS170** (Efficient Algorithms and Intractable Problems) • **CS189*** (Machine Learning) • **CS161** (Computer Security) • **EECS151** (Digital Design and Integrated Circuits) • **EE16** (Information Devices and Systems) • **EE105** (Microelectronic Devices and Circuits) • **EE140** (Linear Integrated Circuits)
* Currently enrolled

EXPERIENCE

Research
Robot Arm (*Fall 2017 - Spring 2018)*
I am working on firmware for the microcontrollers that are running on a work-in-progress, next generation robot arm, as well as the software that controls it. I am on a team with one post-doc, one PhD student, and six other undergraduates, working under the supervision of Professor Pieter Abbeel.
Internships
Software Development Engineer Intern at ***Amazon*** *(Summer 2017)*
I developed a web UI for Amazon Fresh internal usage that allows for safe and quick updates to merchant schedules. One of the impacts of this tool is that it increases the speed at which Fresh can launch in new regions. The application uses a Scala backend with an AngularJS frontend.
Software Intern at ***Rently*** *(Summer 2016)*
I created support for controlling Rently Keyless smart home devices (mainly locks) on the Amazon Echo. I created an Amazon Alexa Skill that forwards raw English text to a custom natural language parser, which processes the command and makes HTTP calls to Rently's servers.

PROJECTS

Course Projects
CPU *(Fall 2017)*
A fully tested and functional 32-bit RISC-V CPU with a 3-stage pipeline and cache written in Verilog and pushed through the ASIC design flow with Synopsys Design and IC Compiler.
Mixed Signal Chip *(Spring 2017)*
The analog parts of a mixed-signal chip in 90nm process for embedded *IOT* applications, including an 8-bit successive-approximation analog to digital converter, a programmable gain amplifier, bandgap voltage reference and temperature sensor, and an analog multiplexer. Final design was simulated and tested in Cadence.
SIXT33N *(Spring 2016)*
A mobile robot on 3 wheels that moves around according to speech input. It uses a TI-Launchpad along with some circuitry for driving the motor and filtering audio input. Voice recognition is implemented with PCA.
Personal Projects
grocery-split
A simple web server written in Go that allows for uneven bill splitting. Parses generic HTML containing a list of items with prices and allows users to select which items they want to pay for.