MS FACULTY OF ENGINEERING AND ARCHITECTURE
AMERICAN UNIVERSITY OF BEIRUT

MIDTERM - PREVIOUS

DIGITAL SYTEMS DESIGN (EECE320)

NAME: _____ ID: _____

CLOSED BOOK (90 MINUTES)

CALCULATORS ARE NOT ALLOWED.

PROVIDE YOUR ANSWERS IN THE SPACE PROVIDED ON THE QUESTION SHEET.

THE SCRATCH BOOKLET WILL NOT BE CONSIDERED IN GRADING.

BE AS NEAT AND CLEAR AS POSSIBLE.

GOOD LUCK!

Problem	Total Points	Earned Points
1	20	
2	4	
3	6	
4	8	
5	8	
6	8	
7	8	
8	8	
9	6	
10	12	
11	12	
Total	100	

Problem 1 (20 points)

a) Convert the following binary number to Hexadecimal:

1001110010110 10.101111 = (_____)16

b) Convert the following binary number to Octal:

11101110100.01101 = (_____)8

c) Convert this hexadecimal number, 3D7C, to Octal: (_____)8

d) Represent the following decimal numbers using **two's complement** with just **enough bits**:

+ 77 = (_____) - 59 = (_____)

e) The **10's complement** of the decimal number 9039700 is: _____

f) Just apply DeMorgan to complement the following expression and **DO NOT** simplify it:

F = Z+Y'(Z'+W)' + X'Y

Answer: _____

g) One solution of the quadratic equation ($x^2 - Bx + 16 = 0$) **is x=2**. Accordingly, the base used is:_____ (**Note: B is equivalent to 11 decimal**)

h) Using 5 bits, N = 11010. What is the decimal value of **N** if the representation is:

Sign/Magnitude _____ 2's comp _____

i) The **Decimal** number **864** is represented in **Excess-3** code as:

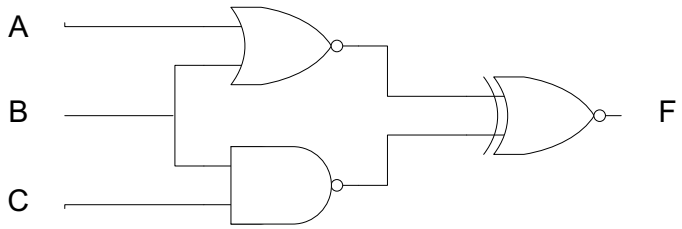
_____

Problem 2 (**4 points**)

Given **F(A,B,C) = AB' + A'C**, express F as a product of **MAXTERMS**.

Problem 3 (**6 points**)

Write the Boolean expression of the following circuit and **reduce it using Boolean algebra**. The expression should contain only AND, OR and NOT operations.



F = _____

Problem 4 (**8 points**)

We want to design a circuit with 4 inputs (A,B,C,D) and 1 output that will be set to 1 if the number of "**zeros**" in the inputs is **equal or greater to 3**. Otherwise, it produces a 0. Complete the K-map and derive a minimum **SOP** expression. Finally, implement this function **using only NAND gates**.

CD \ AB	00	01	11	10
00				
01				
11				
10				

SOP of F =

_____

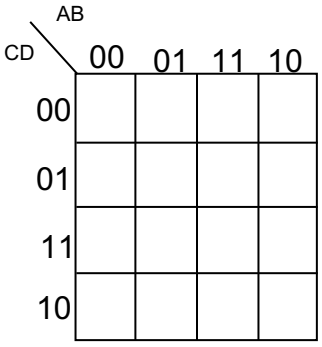
_____

_____

Problem 5 (8 points)

Use the Karnaugh map to obtain a minimum **SOP** expression of the following logic function:

$F = \Sigma_{ABCD}(2, 3, 5, 6, 13, 14, 15) + \Sigma d(1, 8, 9, 11)$



F = _____

Problem 6 (8 points)

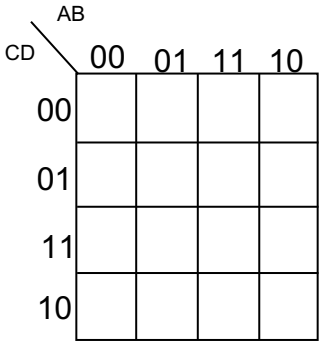
Consider the function: $F = \Sigma_{A,B,C,D}(0, 1, 2, 4, 5, 6, 7, 9, 11, 12, 13, 14)$

a) What are the essential prime implicants of F?

_____

b) What are **ALL** the **OTHER** prime implicants of F?

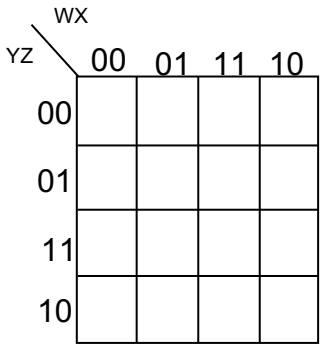
_____



Problem 7 (8 points)

For the following logic expression (F), indicate all the transitions that cause a static hazard in the corresponding two-level AND-OR circuit, and suggest a new expression for a hazard-free circuit that realizes the same logic function.

F = W'.X + Y'.Z + W.X.Y.Z + X'.Y.Z'



Transitions causing hazards are:

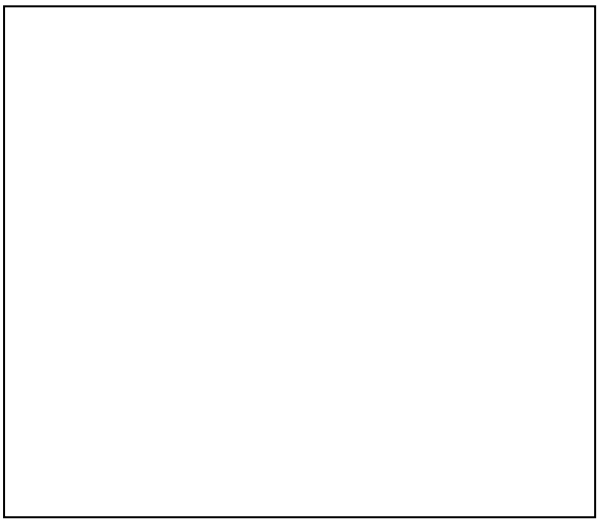
_____

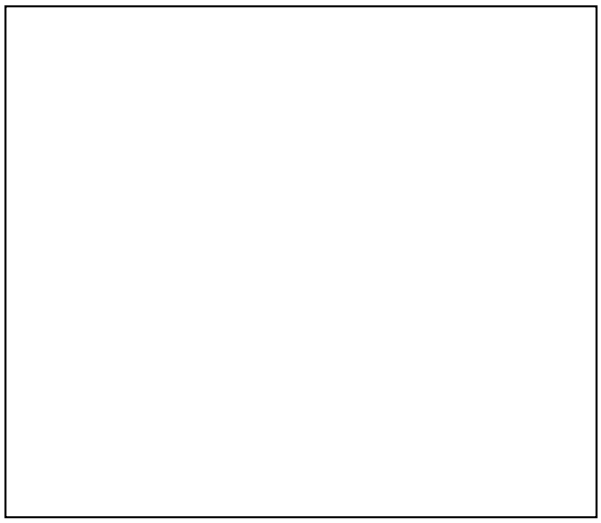
_____

Minimum Hazard-Free F = _____

Problem 8 (8 points)

Implement the function **F = A'C + ABC'** using a **3-to-Decoder** using additional gates. Then Implement F using a **4-input** multiplexer with controls B and C. (**Remember Shanon**)





Problem 9 (6 points)

A half-adder adds only two bits (A and B, without carry-in) and produces two outputs, the sum (S) and carry (C). Write the expressions of S and C in terms of A and B and then implement the following four functions using **ONLY THREE half adders**. You have to show the inputs that are connected to each half adder and what are the outputs of the adders.

D = A ⊕ B ⊕ C E = A'BC + AB'C F = ABC' + (A'+B')C G = ABC

Problem 10 (12 points)

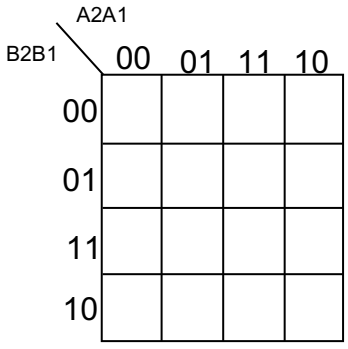
We would like to design a circuit that adds two words (A and B) each with two bits (A_2A_1) and (B_2B_1). We want to design the circuit as one block and not as two full bit adders as we did in class. The circuit will have 4 inputs (A_2, A_1, B_2, B_1) and three outputs that represent the sum (S) and the carry (C) (C, S_2, S_1). Start by completing the truth table below, then fill the corresponding K-maps and finally derive the SOP expressions for C, S_2 and S_1.

Hint: You can fill out the table by considering any row like:

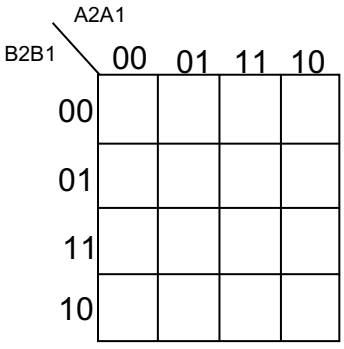
1	0	1	1

As (10) + (11) that is 2+3 = 5 = (101)

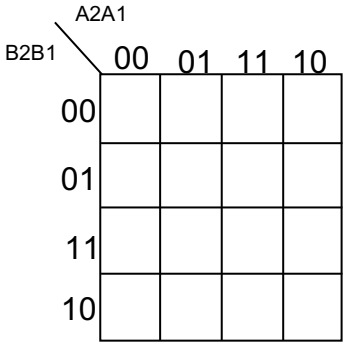
A2	A1	B2	B1	C	S2	S1
0	0	0	0	0	0	0
0	0	0	1	0	0	1
0	0	1	0			
0	0	1	1			
0	1	0	0			
0	1	0	1			
0	1	1	0	0	1	1
0	1	1	1			
1	0	0	0			
1	0	0	1			
1	0	1	0			
1	**0**	**1**	**1**	**1**	**0**	**1**
1	1	0	0			
1	1	0	1			
1	1	1	0			
1	1	1	1			



C



S2



S1

C = _____

S_2 = _____

S1 = _____

Problem 11 (12 points)

Write a VHDL entity and architecture to implement a 2-to-4 decoder with enable using the **behavioral style**. The decoder has an active-high enable signal (EN). Then, write a testbench to the test the decoder with 2 cases, one with enable low and one with enable high.

Library ieee;