Mini Project#3

Finalizing Chip

Overview:

This step is the final step to make sure the design is complete and functioning.

Requirement:

1. Using Phase One adder and Phase two multiplier.
2. Perform DRC checks using updated rules (attached).
3. Perform LVS checks using the same rules used in the lab.
4. Modify design and add wellTaps (updated lib,lef,gds,spi files attached) & perform DRC & LVS again.
5. [Bonus] get DRC clean design. (Fix DRC errors)
6. [Bonus] get LVS clean design. (Fix LVS errors)

Deliverables:

- DRC & LVS reports from 2 and 3 steps.
- GDS with wellTaps.
- [Bonus] DRC & LVS reports from 2 and 3 steps.

Due Dates:

- All files should be zipped together and uploaded on GoogleClassroom by only one team member
- Due Date is the 3rd **of JAN at midnight**. Discussion will be at 4th of JAN.