Hanqing Zhu

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Education

Shanghai Jiao Tong University **Shanghai, China**
B.E. in Microelectronics science and technology *Sept 2016- Jul 2020(expected)*
Zhiyuan Honors Program of Engineering (An elite program for top 10% students in SJTU)

- Ranking: 2nd/57 (Sophomore, junior GPA Ranking 1st/57)
- Major GPA: 89.25/100, Overall GPA: 89.12/100, Advanced GPA (for last four semesters): 91.65/100
- **Core Courses(Selected):** Probability and Statistics (100, rank 1st),Circuit Theory (94), Signals and Systems (95, rank 1st), Design of Digital Integration Circuits (94, rank 1st), Chip Design Methodology for Advanced Logic System (91, rank 1st), Digital Signal Processing (98, rank 1st), Computer Processors and System(89)

Peter the Great St. Petersburg Polytechnic University **Saint Petersburg, Russia**
Summer School of Information Technology Module(Modern SAP Technologies) *Aug 2018- Sept 2018*
Modern SAP Technologies and Russian Course (Grade:98/100)

Internship

University of Texas at Austin **Austin,USA**
Summer Research Intern in Department of Electric and Computer Engineering *July 2019- Sept 2019*

- Research on Fundamental Graph Partition Problem in Pysical Design and Robust Optical Nerual Network
- Advisor: Prof. David. Z. Pan, IEEE fellow & SPIE fellow

Honors and Awards

- Overall GPA Ranking 2 out of 57(Sophomore and Junior GPA Ranking 1^{st}), Department of Microelectronics Science and Technology, Shanghai Jiao Tong University 2016-2019
- Outstanding undergraduate scholarship (¥30,000, awarded to only 5 undergraduate students) 2019
- The Samsung Scholarship(top2%, only one in our department) 2018
- The First & Second Prize Scholarship of Shanghai Jiao Tong University 2017 & 2018 &2019
- Zhiyuan College Honors Scholarship (Top 10% students of Shanghai Jiao Tong university) 2016
- The scholarship for academic progress 2018
- Excellent league cadre of Shanghai Jiao Tong University 2019
- First Prize in China Undergraduate Mathematical Contest in Modeling, Shanghai Division 2018
- Full scholarship for summer school funded by SPbPU (Only two students among C9 universities' applicants in China got full scholarship) 2018
- "Color for love" bronze prize of Chinese college students' rural supporting education 2017

Research Experience

Wireless Near-Field Thin-Film Integrated Antenna Design[J1]
Research Assistant, supervised by Prof. Li Duan, Shanghai, China *Sept 2017 - Oct 2018*

- Designed and fabricated three integrated antennas with a shape of Shanghai Jiao Tong University's logo pattern with a maximum size of 22mm and lowest echo lost -21.93dB.
- Analyzed the collected data and extracted relationship between basic parameters (length, width, ground…) and some performance characteristic such as resonant frequency.
- Found the interactive superposition effect between multiple integrated antennas influenced by common ground.

MIMO Detection Algorithm Optimization and Corresponding VLSI Structure

Research Assistant, supervised by Prof. Guanghui He, Shanghai, China *Nov 2018 - present*

- Tried to optimize traditional MPD algorithm taking advantage of deep learning based on the similarity between message passing scheme and DNN structure.
- Reproduced a low complexity MPD algorithm with a serial message updating which only use the up to date possibility instead of original method.
- Explored optimizing space of DNN-aided MPD algorithm and further VLSI implementation.

A New GPU-Friendly Heuristic Algorithm for Graph Partitioning(Independent Work)

Research Intern, supervised by Prof. David.Z.Pan, Austin, USA *July 2019 - Sept 2019*

- Adopted a **heuristic** for fundamental Graph Partitioning problem based on **K-means algorithm** which divides data into cluster based on the distance between centroid and point and **load-balancing mechanism** in parallel computing which serves as a means to introduce "Distance" into graph.
- Modified seed selection scheme by using BFS to take graph structure into account when selecting initial seeds instead of randomly selection.
- Adopted **GPU** to accelerate current methodology since load-balancing is based on linear equation Ax=b solver which is GPU-friendly and used **parallel computing** by taking advantage of algorithm inner parallel structure for further accelerating and got about k times acceleration if we need k partition.
- Outperformed state-of-art tool like **Metis** and in current implementation have about 5% performance improvement on edge-cut in current implementation and run-time is acceptable compared to Metis (with acceleration).
- This work is planned to submit to IPDPS.

A Noise-Aware Quantization Scheme Towards Robust ONN with low-bit[C1](Cooperative Work)

Research Intern, supervised by Prof. David.Z.Pan, Austin, USA *July 2019 - Sept 2019*

- Proposed a protective Group Lasso regularization technique to boost noise-robustness of quantized ONNs
- Mainly worked on experiment part and realised traditional iterative methods in ONN as baseline on the basis of senior's work

Academic Projects

CNN-Classification on FPGA Platform *Course Project*

- Reproduced a fast FPGA prototyping framework for high performance CNN deployment on PYNQ platform.
- Performed MINIST and Cifar-10 classification on PYNQ aided by caffe framework to train basic model
- Tried to transplanted PYNQ kernel to ZYNQ-7000 board and successfully implemented some basic functions through Jupyter in Python.

High Performance VLSI Architecture for HEVC Motion Estimation *Course Project*

- Proposed an efficient VLSI architecture compatible for HEVC (High Efficiency Video Coding) ME full search algorithm targeting processing 1920×1080p video @30fps and supporting 4*4 pixels block size and [-8,8) search range under SMIC 0.18um technology (The frequency requirement is 100MHz).
- Adopted 16 Processing Elements as SAD computing core module where each one computes 4*4 pixels computing and local memory to reduce the off-chip bandwidth and serve as data buffer for further computing using ping-pong mechanism.
- Used SMIC 0.18um technology, the proposed architecture is synthesized at the maximum work frequency of about 74MHz and power of 845.18mW and used ICC compiler to to complete physical design part.

Convolutional Layer Hardware Design for CNN *Course Project*

- Proposed three possible hardware structure of the 2nd convolutional layer in VGGNet and refered to Eyersis as a row stationary hardware design in the third design
- Completed function verification by comparing results from MATLAB and Modelsim simulation

Publications

[C1] ROQ: A Noise-Aware Quantization Scheme Towards Robust Optical Neural Networks with Low-bit Controls

- Jiaqi Gu, Zheng Zhao, **Hanqing Zhu**, Chenghao Feng, Ray T. Chen, David Z. Pan
- In submission to Design, Automation and Test in Europe Conference, DATE 2020

[J1] Design and Manufacturing of Near-Field Thin-Film Integrated Antenna for Wireless Romote Sensing on Turbine Blade Surface by MEMS technology

- In submission to The Journal of Shanghai Jiao Tong University as a co-author

Leadership and Activities

Siyuan Commonweal Organization **Shanghai Jiao Tong University, Shanghai**
Project Director *Sept 2017 - July 2019*

- Took efforts to improve education quality in China's poorest places with my heart of gratitude as one who also comes from rural and poverty-stricken areas
- Responsible for the Rural Support Education Program of Siyuan Commonweal Organization for two years
- Chaired three support education seminars and more than thirty interviews to select about 110 volunteer teachers from Shanghai Jiao Tong University, East China Normal University and Shanghai International Studies University
- Established collaboration with three new support schools and offered free summer class for more than 700 students in rural China during 2018 summer

Supporting Education volunteer **Eryuan, Yunnan Province**
Teacher Volunteer *Aug 2017- Sept 2017*

- Offered more than 30 kinds of class for 113 students in Eryuan No.2 high school included the Themes-Based-Teaching class for over one month
- Responsible for the investigation about traditional Chinese villages and cultural heritage by the national ministry of housing and urban-rural development
- Offered complete survey on the local villages and suggestions on how to develop the local economy
- Awarded with "Color for love" bronze prize of Chinese college students' rural supporting education for extraordinary volunteer performance

SKILLS

- **Programming Languages:** python, C++, MATLAB, Verilog, CUDA
- **VLSI Tools:**
  - Cadence tools & Xilinx FPGA board development tools & Hspice
- **Others:** Latex & Git