Group 45:
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Lab 05 - Combinatorial Logic

In this lab, you've learned real world applications of digital logic, as well as how to assemble your own Verilog modules. In addition, you've learned how the constraints file maps your inputs and outputs to real pins on the FPGA.

Rubric

Item	Description	Value
Summary Answers	Your writings about what you learned in this lab.	25%
Question 1	Your answers to the question	25%
Question 2	Your answers to the question	25%
Question 3	Your answers to the question	25%

Lab Summary

We learned about verilog programming to build a digital circuit using XOR logic. We learned how to declare inputs, outputs and assign them to the hardwear. We had a stairway light example for adding 2 bits together, then used carry logic to add more than two bits together. Lastly we programmed it on the circuit to double check everything was working properly.

Lab Questions

1 - Explain the role of the Top Level file.

The top level file serves as the main module in order to integrate all lower-level modules within the project. It describes how all the files connect together and interact with each other.

2 - Explain the function of the Constraints file.

The contrants file is used to map verilog modules to the specific hardwear you are using and the location/functions within the hardwear. Sets pin numbers, switches, lights, to verify that your verilog project is working as intended.

3 - How might one add more than two bits together?

You can use the carry logic to determine the carry bits in order to add them together.

Code Submission

Upload a .zip of all your code or a public repository on GitHub.