Group 45

Lab 10 - Synchronous Circuits

In this lab, you've learned about behavioral Verilog and how to use it to implement circuits with memory. You've also learned how to utilize this memory in conjunction with multiplexers and demultiplexers to make a simple storage system.

Rubric

Item	Description	Value
Summary Answers	Your writings about what you learned in this lab.	25%
Question 1	Your answers to the question	25%
Question 2	Your answers to the question	25%
Question 3	Your answers to the question	25%

Lab Summary

We dealt with synchronous circuits and digital logic design.We used some of the material we did in Lab 09 for the mux and demux. We designed a single bit memory to implement a D-Latch and then a four byte by using the D-Latch, 8-bit memory block, demux, and mux.

Lab Questions

1 - Why can we not just use structural Verilog to implement latches?

We can't just use structural Verilog to implement latches because there is a limitation to combination loops and things like D-Latches and SR-Latches aren't synthesizable. So in verilog we use behavioral Verilog to allow synthesis tools to map logic.

2 - What is the meaning of `always @(*)` in a sensitivity block?

The always @(*) in a sensitivity block means to run the logic in this block whenever any signal used in the block changes. It ensures that there isn't unintended latching behavior.

3 - What importance is memory to digital circuits?

Memory is very important because it lets the circuits store data for future use, helps with multi-step operations, and to use timers, state machines, and more.

Code Submission

Upload a .zip of all your code or a public repository on GitHub.