Group 45

Lab 10 - Edge Sensitivity

In this lab, you've learned about edge sensitive circuits and explored some of the power therein.

Rubric

Item	Description	Value
Summary Answers	Your writings about what you learned in this lab.	25%
Question 1	Your answers to the question	25%
Question 2	Your answers to the question	25%
Question 3	Your answers to the question	25%

Lab Summary

We learned how to build and use edge-sensitive circuits with D Flip-Flops, JK Flip-Flops, and T Flip-Flops. We figured out that edge-sensitive circuits are better for clocked and synchronized behavior in digital circuits/systems. Also we learned how to use the keyword posedge to detect rising clock edges.

Lab Questions

1 - What is the difference between edge and level sensitivecircuits?

Edge synthetic circuits only respond to changes in a signal, for example when the clock goes from low to high. Level sensitive circuits respond as long as a signal is active, which means it can continuously update while enabled. But for edge-sensitive circuits update only once per clock cycle.

2 - Why is it important to declare the initial state?

Declaring an initial state makes sure that the circuit starts in a known condition when the FPGA is programmed. Without it, the flip-flops could start in a random start, which can result in incorrect behavior.

3 - What do edge sensitive circuits let us build?

They let us build a clock system. Like counters, memory, and full CPUs. These systems only change their state on clock edges, which allows them to work in sync with the rest of the system.

Code Submission

Upload a .zip of all your code or a public repository on GitHub.