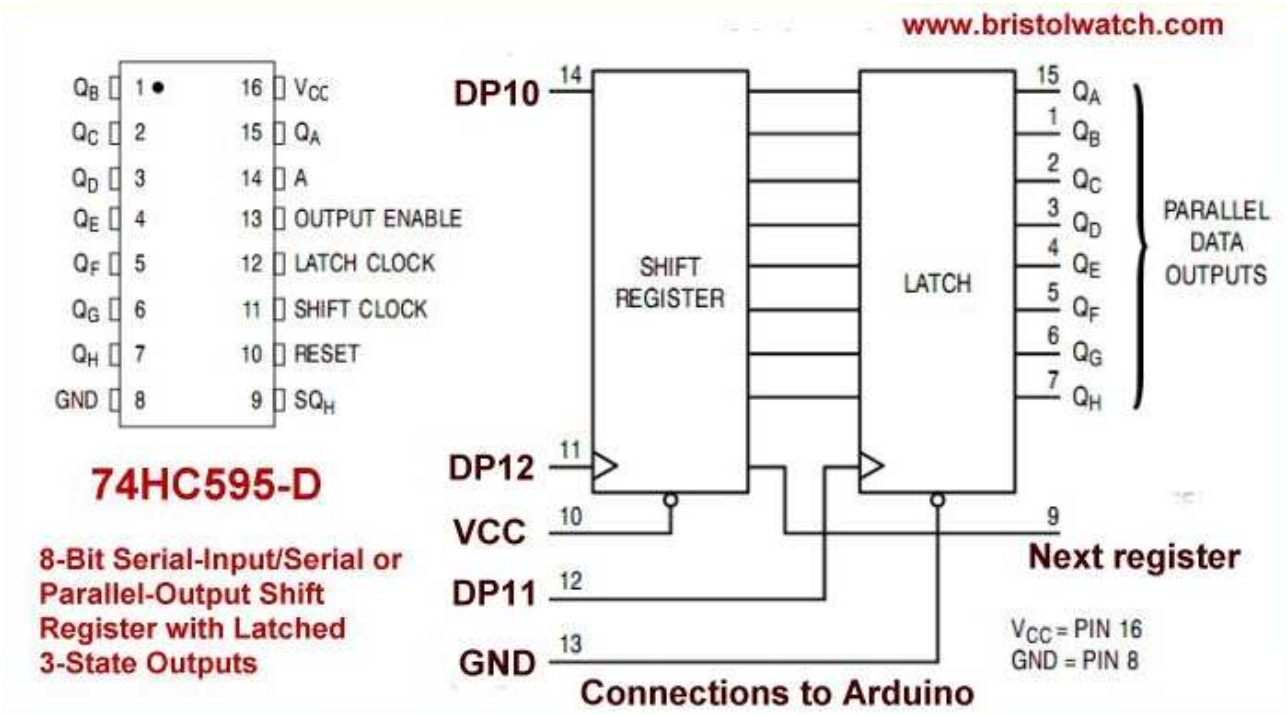
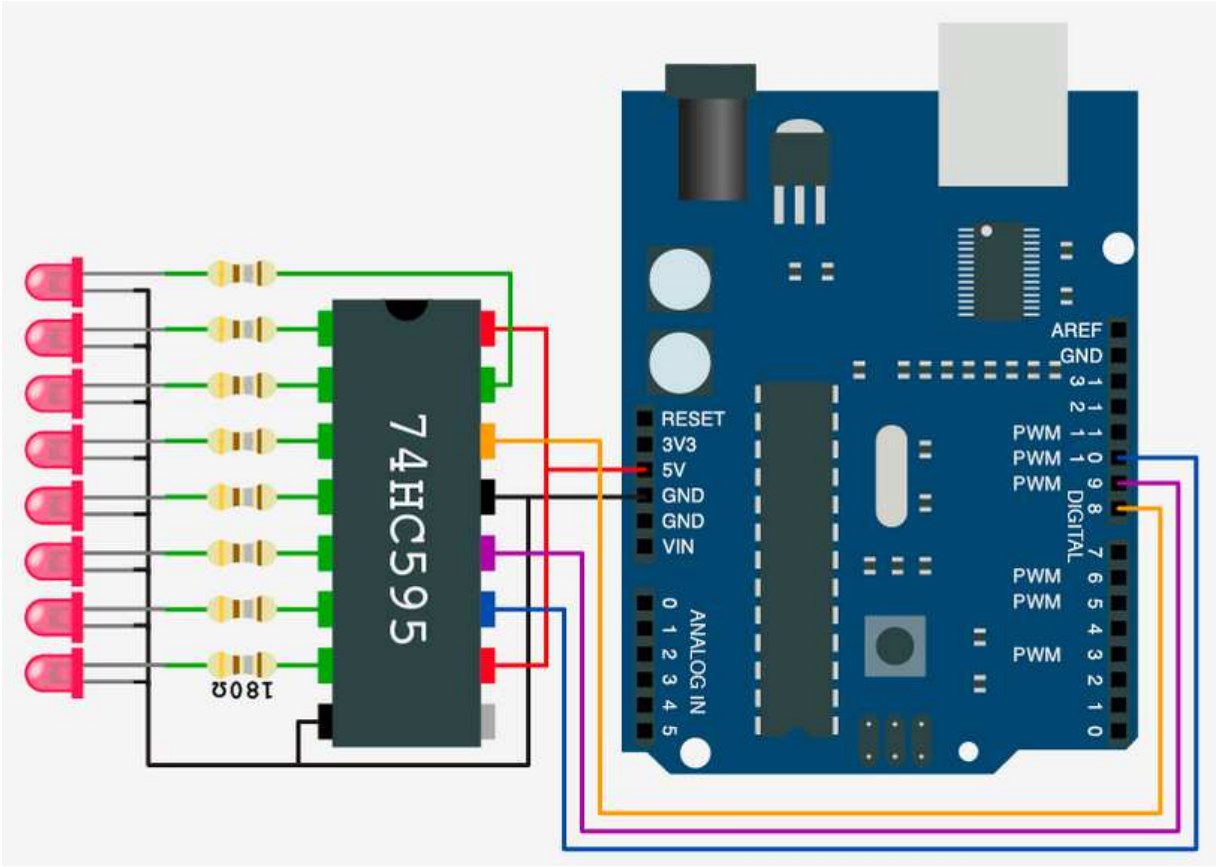
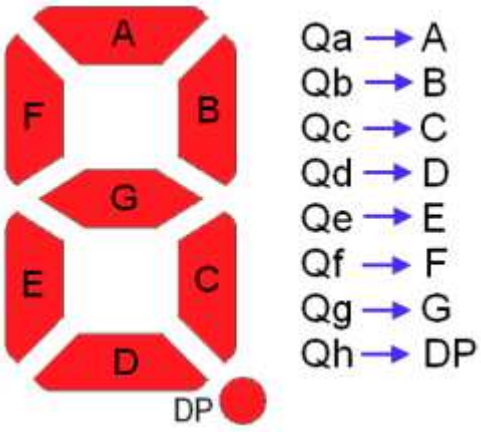
Aufbau mit D-FlipFlops:

Aufbau eines 8-bit Schieberegisters mit D-FF; Aufbau eines 8-bit Speichers (Latch) mit D-FF; Beschriftung der Signalleitungen anhand 74HC595.





Elektronikschule Tettnang	**Arduino - µController** Schieberegister 74HC595	Name : _____ Datum: _____



Schaltplan:

SYMBOL	PIN	DESCRIPTION
Q_0 to Q_7	15, 1 to 7	parallel data output
GND	8	ground (0 V)
Q_7'	9	serial data output
$\overline{MR}$	10	master reset (active LOW)
SH_{CP}	11	shift register clock input
ST_{CP}	12	storage register clock input
$\overline{OE}$	13	output enable (active LOW)
D_S	14	serial data input
V_{CC}	16	positive supply voltage

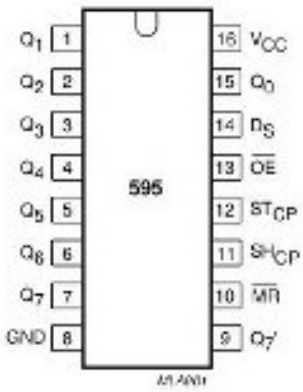


Fig.1 Pin configuration.

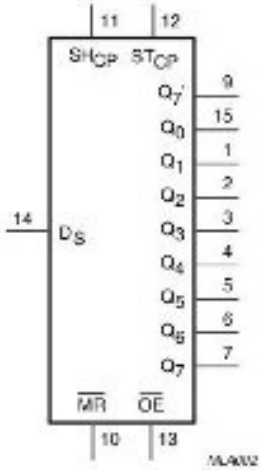


Fig.2 Logic symbol.

Software: z.B.: https://www.youtube.com/watch?v=hUZCrba93pU

www.makerblog.at