105-2 CA with Embedded DSD Homework 3 Report

Hardware Implementation of Single Cycle MIPS

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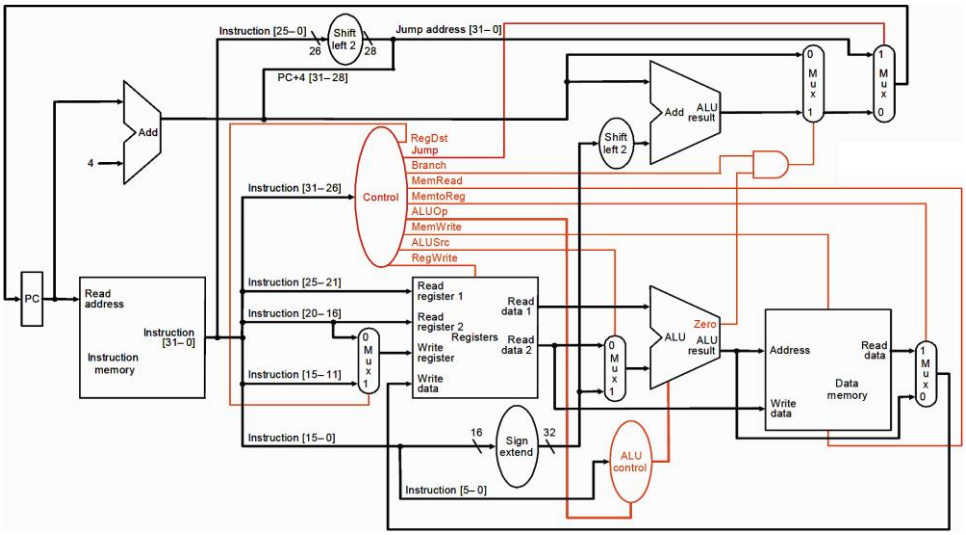
1. RTL simulation

The implementation of module SingleCycle_MIPS :

According to the datapath on the below, I implemented several sub modules at the first, and then utilize them in module SingleCycle_MIPS.



Sub modules:

a. PC (Program Counter)
b. Add_ALU
c. register_file
d. mainControl
e. ALU
f. ALUControl
g. signExtend
h. Mux

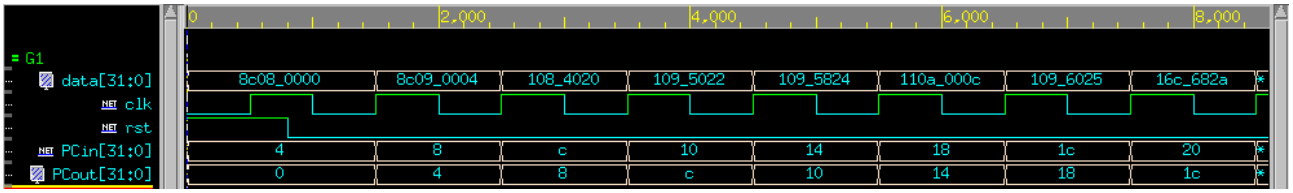
In module SingleCycle_MIPS:

Cell	Reference
_PC	PC
_mainControl	mainControl
_ALU	ALU
_ALUControl	ALUControl
_signExtend	signExtend
_regFile	register_file
MUXX_RegDST	Mux_WIDTH5_0
MUXX_Src	Mux_WIDTH32_0
MUXX_MemToReg	Mux_WIDTH32_5

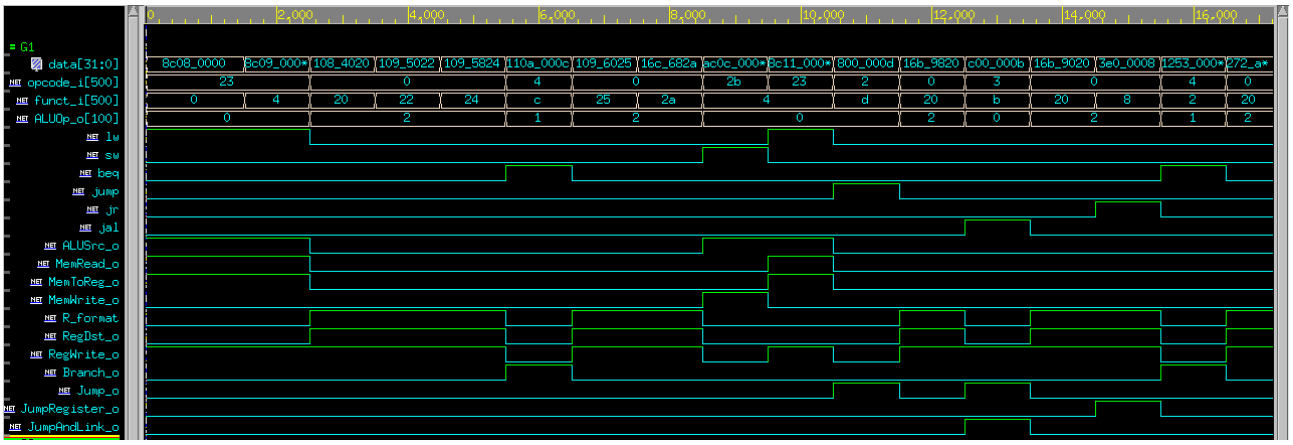
PC_adder	Add_ALU_0
branch_adder	Add_ALU_1
MUXX_Branch	Mux_WIDTH32_4
MUXX_JumpRegister	Mux_WIDTH32_2
MUXX_Jump	Mux_WIDTH32_3
MUXX_JumpAndLink_1	Mux_WIDTH5_1
MUXX_JumpAndLink_2	Mux_WIDTH32_1

而每個cell所得波形圖如下所示:

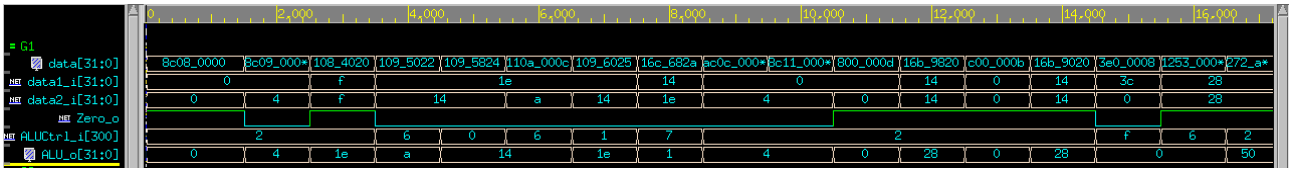
a. _PC



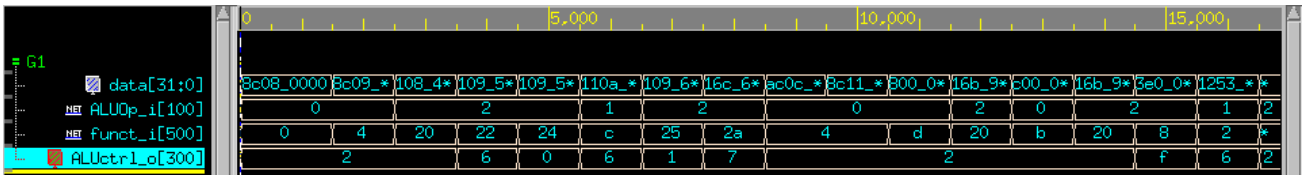
b. _mainControl



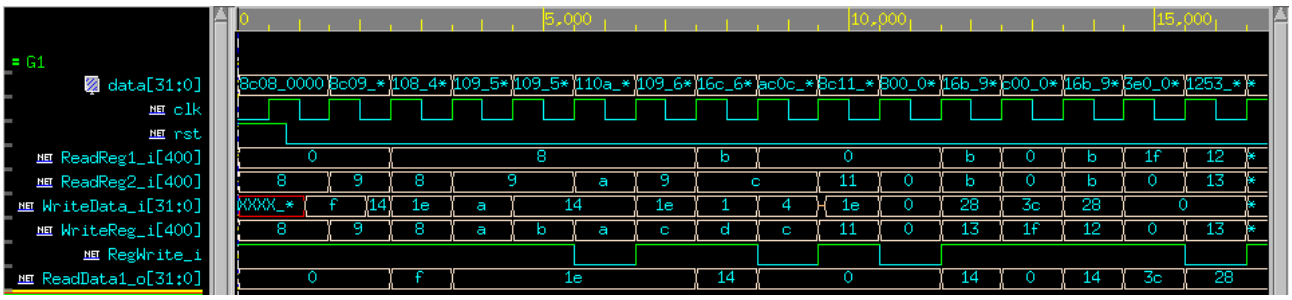
c. _ALU



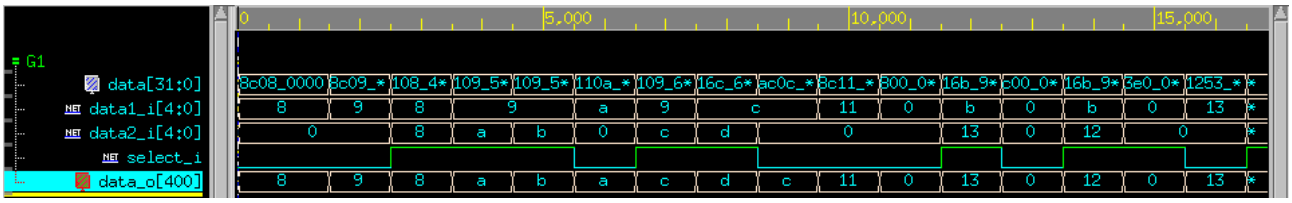
d. _ALUControl



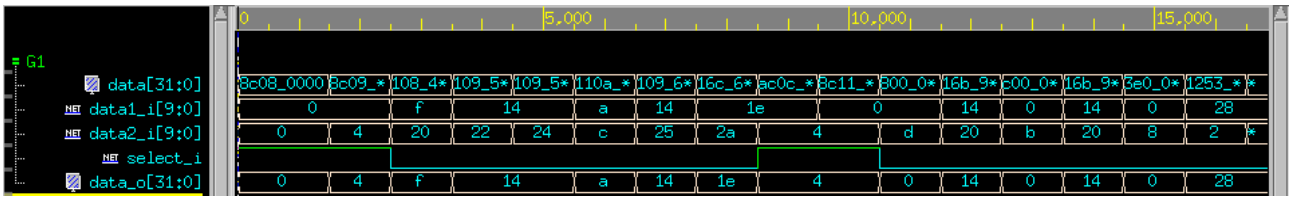
e. _regFile



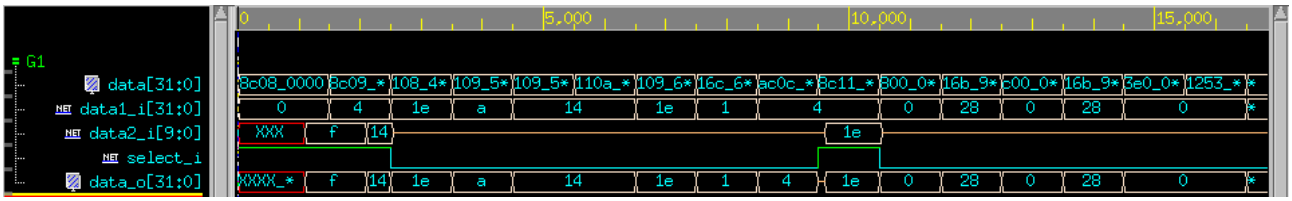
f. MUXX_RegDST



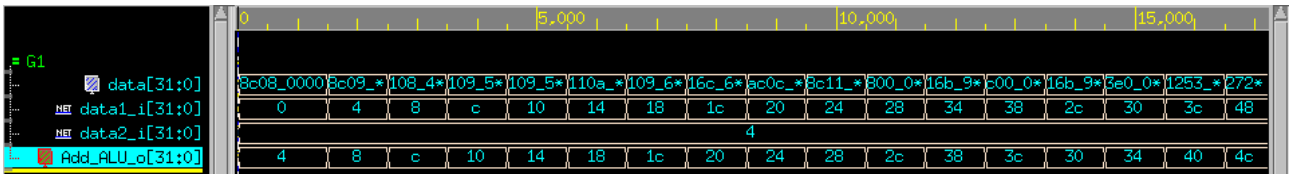
g. MUXX_Src



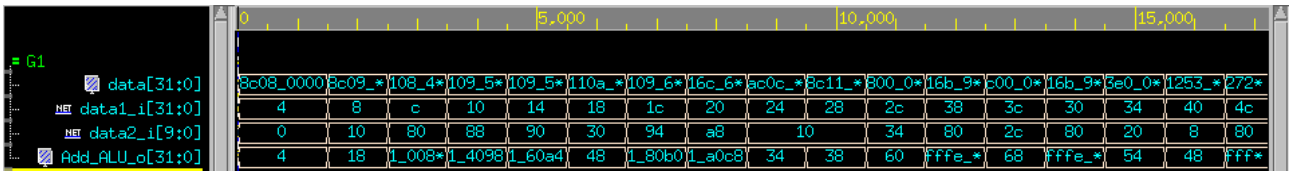
h. MUXX_MemToReg



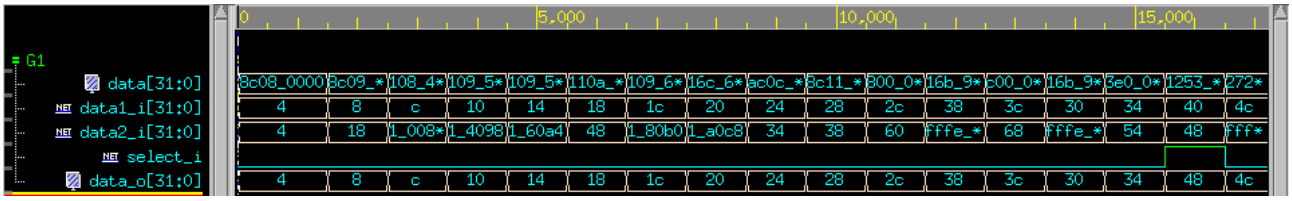
i. PC_adder



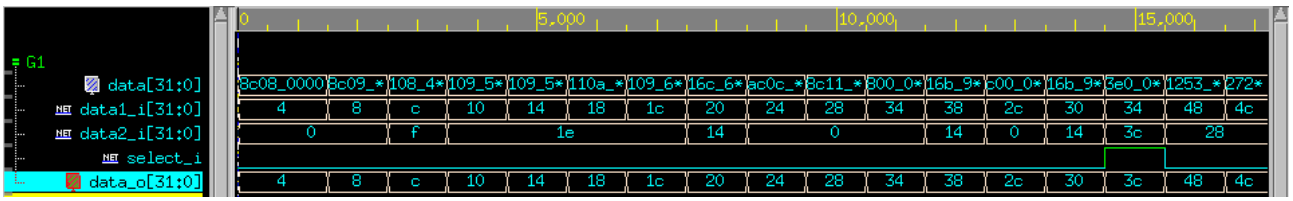
j. branch_adder



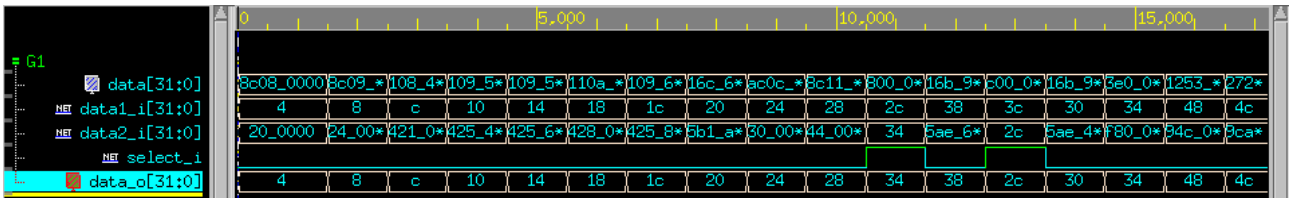
k. MUXX_Branch



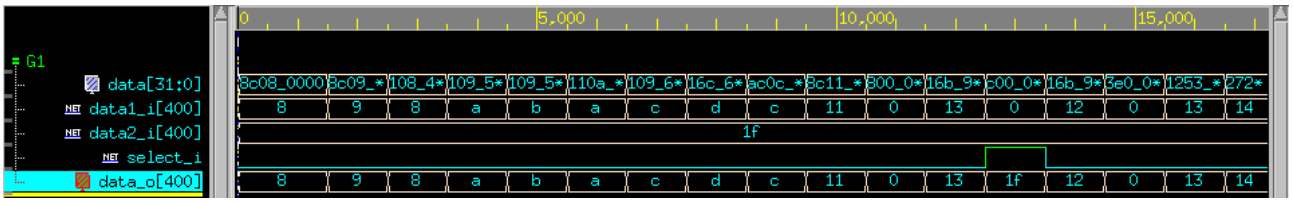
l. MUXX_JumpRegister



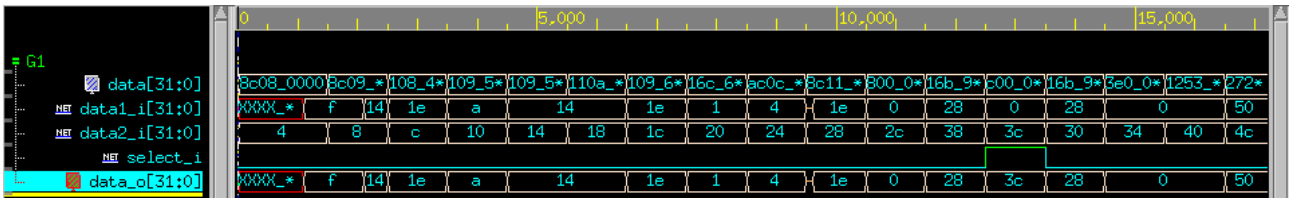
m. MUXX_Jump



n. MUXX_JumpAndLink_1



o. MUXX_JumpAndLink_2



2. Synthesis

Area Report:

```
****************************************
Report : area
Design : SingleCycle_MIPS
Version: G-2012.06
Date   : Thu Apr 20 03:26:55 2017
****************************************

Library(s) Used:

    typical (File: /home/raid7_2/course/cvsd/CBDK_IC_Contest/CIC/SynopsysDC/db/typical.db)

Number of ports:                          172
Number of nets:                           533
Number of cells:                           38
Number of combinational cells:             22
Number of sequential cells:                 0
Number of macros:                           0
Number of buf/inv:                         20
Number of references:                      21

Combinational area:          45503.898122
Noncombinational area:       34056.632446
Net Interconnect area:       undefined  (No wire load specified)

Total cell area:             79560.530569
Total area:                  undefined
```

Timing Path Report:

```
****************************************
Report : timing
         -path full
         -delay max
         -max_paths 1
         -sort_by group
Design : SingleCycle_MIPS
Version: G-2012.06
Date   : Thu Apr 20 03:28:45 2017
****************************************
 # A fanout number of 1000 was used for high fanout net computations.
Operating Conditions: slow     Library: slow
Wire Load Model Mode: top
  Startpoint: _regFile/register_reg[31][1]
              (rising edge-triggered flip-flop clocked by CLK)
  Endpoint: A[6] (output port clocked by CLK)
  Path Group: CLK
  Path Type: max

  Point                                                  Incr       Path
  -----------------------------------------------------------------------------------------------------------
  clock CLK (rise edge)                                  0.00       0.00
  clock network delay (ideal)                            0.50       0.50
  _regFile/register_reg[31][1]/CK (DFFRX1)               0.00 #     0.50 r
  _regFile/register_reg[31][1]/Q (DFFRX1)                0.26       0.76 r
  _regFile/U732/Y (MXI4X1)                               0.20       0.96 f
  _regFile/U676/Y (MX4X1)                                0.16       1.12 f
  _regFile/U674/Y (MXI2X1)                               0.07       1.20 r
  _regFile/ReadData2_o[1] (register_file)                0.00       1.20 r
  MUXX_Src/data1_i[1] (Mux_WIDTH32_0)                    0.00       1.20 r
  MUXX_Src/U14/Y (AO22X1)                                0.19       1.39 r
  MUXX_Src/data_o[1] (Mux_WIDTH32_0)                     0.00       1.39 r
  _ALU/data2_i[1] (ALU)                                  0.00       1.39 r
  _ALU/sub_371/B[1] (ALU_DW01_sub_0)                     0.00       1.39 r
  _ALU/sub_371/U4/Y (CLKINVX1)                           0.04       1.43 f
  _ALU/sub_371/U2_1/CO (ADDFXL)                          0.38       1.81 f
  _ALU/sub_371/U2_2/CO (ADDFXL)                          0.22       2.04 f
  _ALU/sub_371/U2_3/CO (ADDFXL)                          0.22       2.26 f
  _ALU/sub_371/U2_4/CO (ADDFXL)                          0.22       2.48 f
  _ALU/sub_371/U2_5/CO (ADDFXL)                          0.22       2.71 f
  _ALU/sub_371/U2_6/CO (ADDFXL)                          0.22       2.93 f
  _ALU/sub_371/U2_7/CO (ADDFXL)                          0.22       3.16 f
  _ALU/sub_371/U2_8/S (ADDFXL)                           0.14       3.30 f
  _ALU/sub_371/DIFF[8] (ALU_DW01_sub_0)                  0.00       3.30 f
  _ALU/U20/Y (AOI221XL)                                  0.19       3.49 r
  _ALU/U18/Y (OAI211X1)                                  0.07       3.56 f
  _ALU/ALU_o[8] (ALU)                                    0.00       3.56 f
  A[6] (out)                                             0.00       3.56 f
  data arrival time                                                 3.56
  clock CLK (rise edge)                                  10.00      10.00
  clock network delay (ideal)                            0.50       10.50
  clock uncertainty                                      -0.10      10.40
  output external delay                                  -6.00      4.40
  data required time                                                4.40
  -----------------------------------------------------------------------------------------------------------
  data required time                                                4.40
  data arrival time                                                 -3.56
  -----------------------------------------------------------------------------------------------------------
  slack (MET)                                                       0.84
```

3. **Gate-level simulation**

Simulated timing (ns) : 10ns