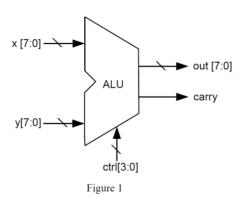
105-2 CA with Embedded DSD Homework 1 Report

B03901156 電機三 黄于瑄

1. 8-bit arithmetic logic unit(ALU)



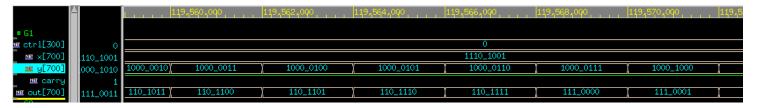
The implementation of alu_rtl_tb2.v and alu_tb2.v:

参考 Lab2 中 Lab2_test_alu.v 的寫法,對於每個operation皆考慮x及y所有可能的組合情形,並在console上印出test通過或失敗的訊息;以Addition的test pattern 為例:

```
// test for Add
#(`CYCLE);
ctrl = 4'b0000;
for(i=0;i<256;i=i+1) //x's all situations
begin
    for(j=0;j<256;j=j+1) //y's all situations
begin
    x=i[7:0];y=j[7:0];
#20    true_out=x+y; tmp ={x[7],x}+{y[7],y}; true_carry=tmp[8];
    if(out !== true_out[7:0]) //check if "out" is the same as the ture output
    begin
        $display(" %b + %b should be %b. But your output is %b",x,y,true_out,out);
    end
    else $display( "ADD ----- PASS" );
    if(carry !== true_carry) //check if "carry" bit is the same as the ture carry
        $display(" %b + %b's carry should be %b. But your output is %b",x,y,true_carry,carry);
end
else $display( "ADD_carry ----- PASS" );
end
end</pre>
```

而每個operation所得波形圖如下所示: (case ctrl)

a. $(ctrl == 4'b0000) \rightarrow out = x + y$;



b. $(ctrl == 4'b0001) \rightarrow out = x - y$;

			199,420,00	70, , , 199,422,00	0, , , 199,424,00	70, , , 199,426,00	0 , , , 199,428,00	70, , , , 199,430,090,
= G1								
± ctr1[300]	1					1		
MEI ×[700]	.000_0101					1000_0101		
<u>м</u> пу[700]	111_1100	111_10*	111_1100	111_1101	111_1110	111_1111	1000_0000	1000_0001
ME carry	1	- :						
<u>ME</u> out[700]	1001	1010	1001	1000	111	110	101	100

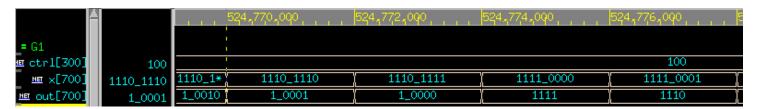
c. $(ctrl == 4'b0010) \rightarrow out = x \& y;$

			387,342,000,,,,,	387,344,090 , , , ,	387,346,090 , , ,	387,348,000 , , , ,	387,350,090,,,,38:
= G1							
ш ctr1[300]	10					10	
<u>ы</u> ×[700]	1111_0100					1111_0100	
<u>м</u> пу[700]	1000_1100	1000_0100	1000_0101	1000_0110	1000_0111	1000_1000	1000_1001
ΜEI out[700]	1000_0100			1000_0100		X	1000_00

e. $(ctrl == 4'b0011) \rightarrow out = x | y;$

			, , , 511 ₃ 746 ₃ 09	0, , , , 511,748,00	90,,,,,511,750,00	70, , , 511,752,09	0, , , , 511,754,00	10, ,
- 04								
= G1								
ı ctr1[300]	11					11		
<u>мет</u> ×[700]	1110_0111					1110_0111		
<u>м</u> пу[700]	1000_0101	111_1101	111_1110	111_1111	1000_0000	1000_0001	1000_0010	1
<u>ы</u> out[700]	1110_0111		1111_1111				1110_0111	

f. $(ctrl == 4'b0100) \rightarrow out = ~x$;



g. $(ctrl == 4'b0101) \rightarrow out = x ^ y;$

			637,410,00	0, , , 637,412,00	90, , , 637,414,00	0, , , , 637,416,00	90, , , 637,418,090,
- 01							
= G1						404	
: ctr1[300]	101					101	
ыш ×[700]	1101_1011					1101_1011	
<u>на</u> у[700]	1110_1101	1110_1*	1110_1101	1110_1110	1110_1111	1111_0000	1111_0001
₫ out[700]	11_0110	11_0111	11_0110	11_0101	11_0100	10_1011	10_1010

h. $(ctrl == 4'b0110) \rightarrow out = -x \& -y$;

			77,1,066,000,,,,	77,1,068,090,,,,	77,1,07,0,090	77,1,07,2,090 , , , ,	77,1,07,4,090
= G1							
: ctr1[300]	110					110	
<u>№</u> ×[700]	1110_0000					1110_0000	
<u>м</u> ш у[700]	1111_1001	1111_1*	1111_1001	1111_1010	1111_1011	1111_1100	1111_1101
ш out[700]	110	111	110	101	100	11	10

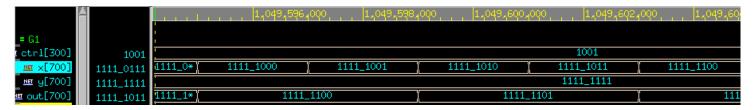
i. $(ctrl == 4'b0111) \rightarrow out = y << x[2:0];$

			, , , 909,308,00	0 909,310,00	70 909,312,00	0	0
= G1		1					
:ctr1[300]	111					111	
<u>м</u> х[700]	1110_1110					1110_1110	
<u>м</u> в у[700]	1111_1001	1111_1*	1111_1001	1111_1010	1111_1011	1111_1100	1111_1101
虹 out[700]	100_0000	0	100_0000	1000_0000	1100_0000	0	100_0000

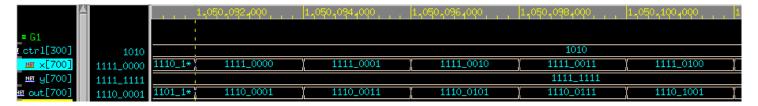
j. $(ctrl == 4'b1000) \rightarrow out = y >> x[2:0];$

			1,032,682,000	1,032,684,000	1,032,686,000	1,032,688,000	1,032,690,000, , , :
= G1		1					
: ctr1[300]	1000					1000	
<u>ы</u> ×[700]	1101_1111	1				1101_1111	
<u>м</u> ш у[700]	1111_0000	1110_1*	1111_0000	1111_0001	1111_0010	1111_0011	1111_0100
⊈ out[700]	1	!				1	

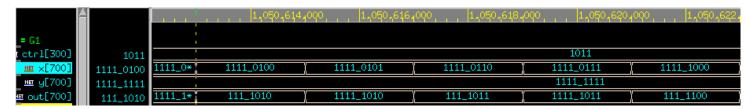
k. $(ctrl == 4'b1001) \rightarrow out = \{x[7], x[7:1]\}$;



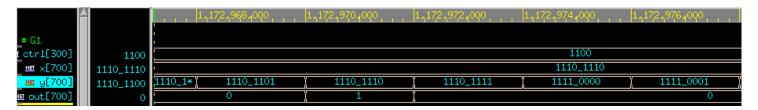
1. $(ctrl == 4'b1010) \rightarrow out = \{x[6:0], x[7]\};$



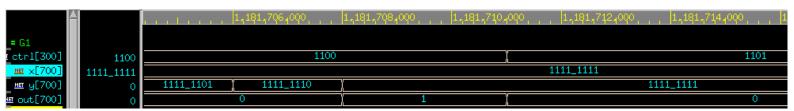
m. $(ctrl == 4'b1011) \rightarrow out = \{x[0], x[7:1]\};$



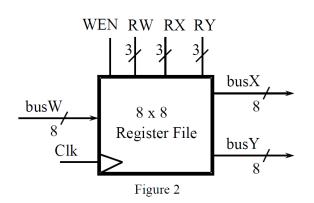
n. $(ctrl == 4'b1100) \rightarrow out = (x==y) ? 1 : 0;$



o. $(ctrl == 4'b1101 \text{ or } 4'b1110 \text{ or } 4'b1111) \rightarrow out = 0$;



2. 8x8 Register File



關於 \$r0 = constant zero:

```
//==== sequential circuit ==== register file
    reg [7:0] registers[7:0];

always@(posedge Clk) begin
    if(WEN)
        registers[RW] <= busW;
end

always@(RX or registers[RX])begin
    if(RX == 0) busX <= 0;
    else busX <= registers[RX];
end

always@(RY or registers[RY])begin
    if(RY == 0) busY <= 0;
    else busY <= registers[RY];
end</pre>
```

3. Simple Calculator

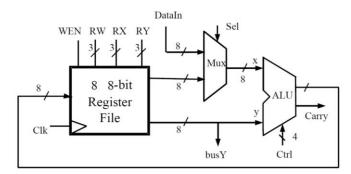


Figure 3

Design:

```
always@(Ctrl,x,busY)
begin
42
43
44
45
46
47
48
49
50
51
52
53
54
55
60
61
62
63
64
65
                                tmp ={x[7],x}+{busY[7],busY};
Carry = tmp[8];
busW = x+busY;
                      end
4'b0001: begin
    neg = ~busY + 00000001;
    tmp ={x[7],x}+{neg[7],neg};
    Carry = tmp[8];
    busW = x-busY;

                                                   = x & busY;
= x | busY;
                        4'b0011: busW
                        4'b0100: busW
                                         busW
                        4'b0110: busW
4'b0111: busW
4'b1000: busW
4'b1001: busW
                                                      4'b1010: busW
                        4'b1011: busW
                         4'b1100: busW
                         4'b1101: busW
                                         busW
                         4'b1111: busW
```

波形圖:

