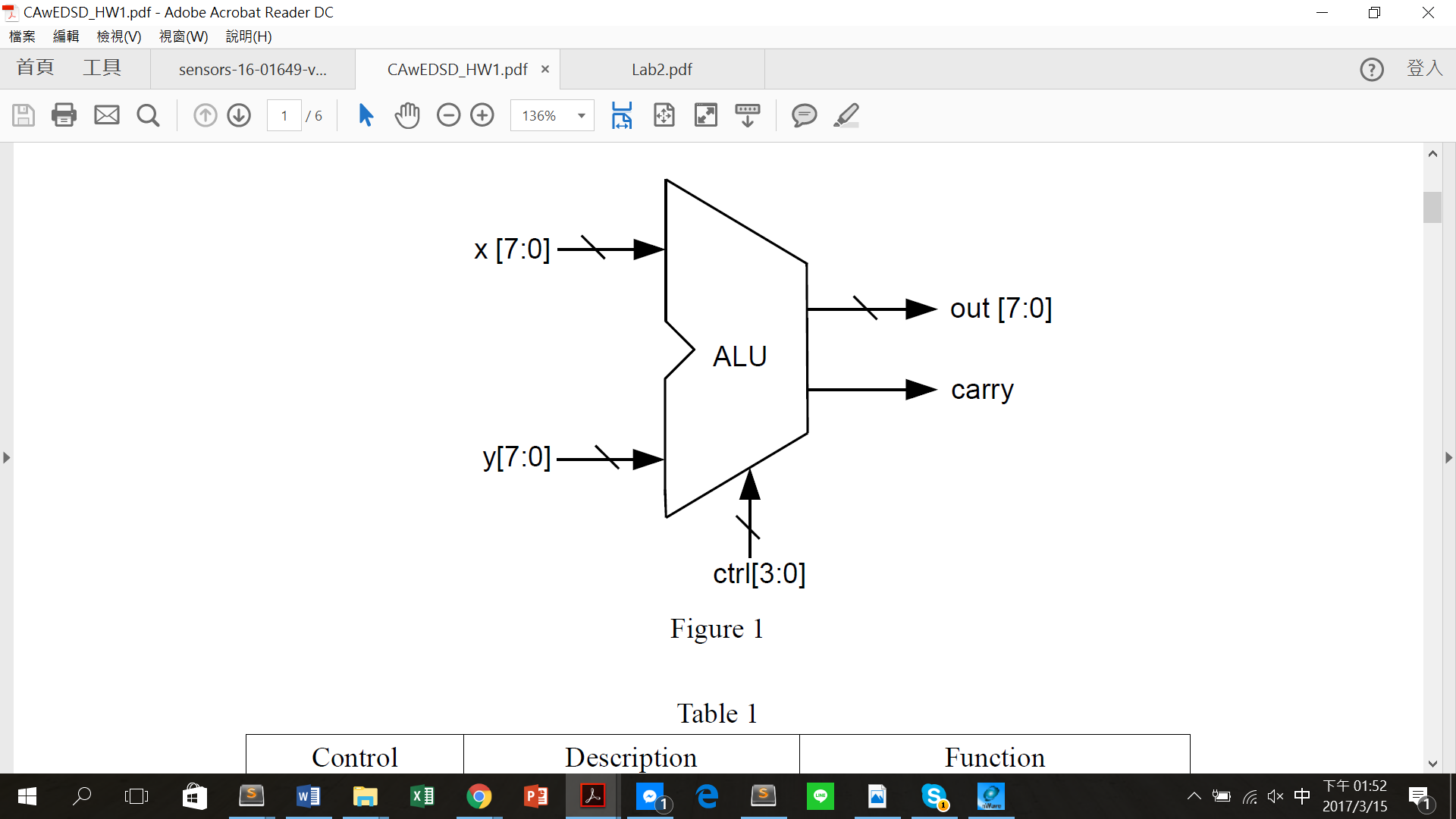
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| B03901156 電機三 黃于瑄 |

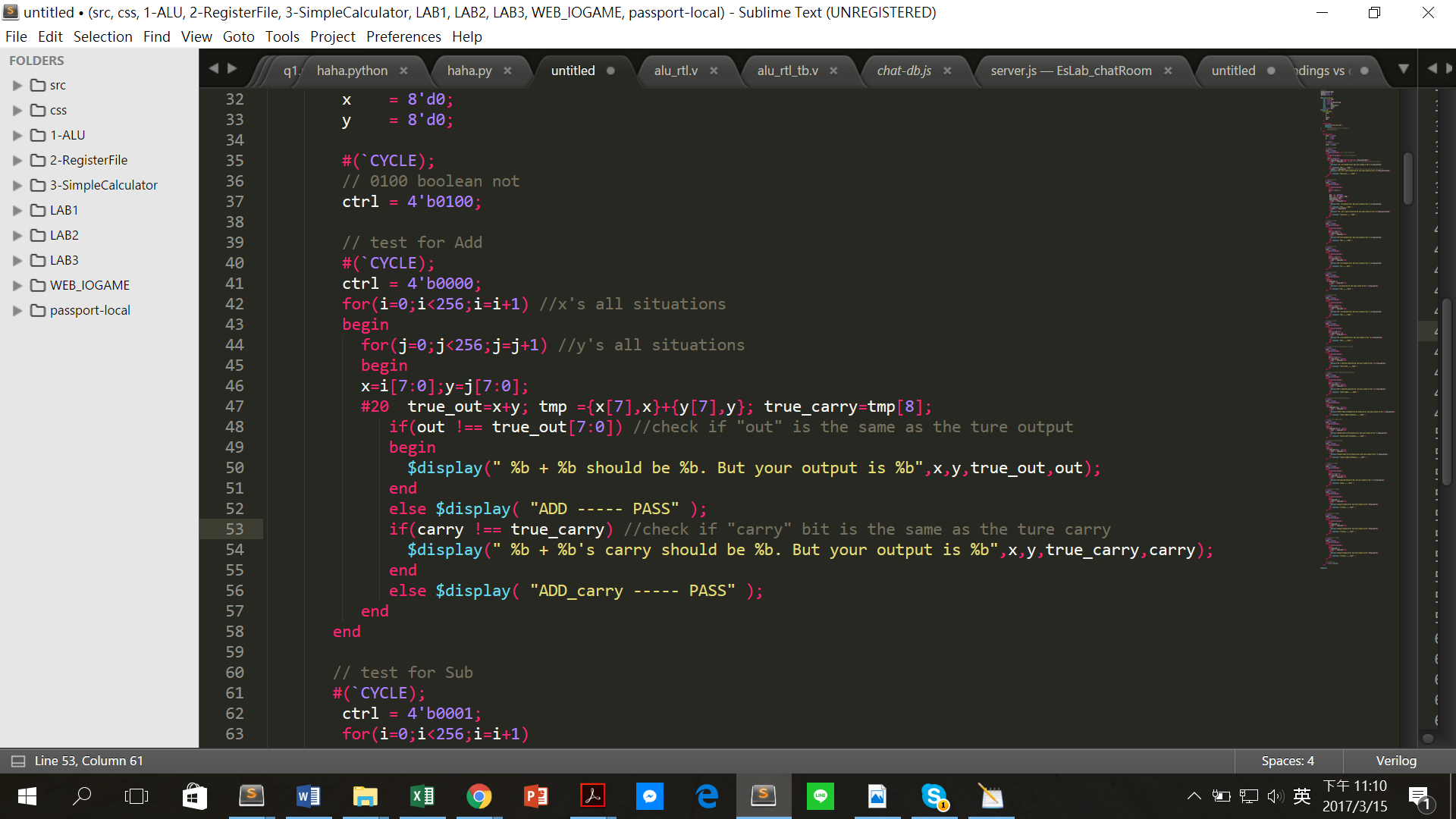
**105-2 CA with Embedded DSD Homework 1 Report**

1. **8-bit arithmetic logic unit(ALU)**



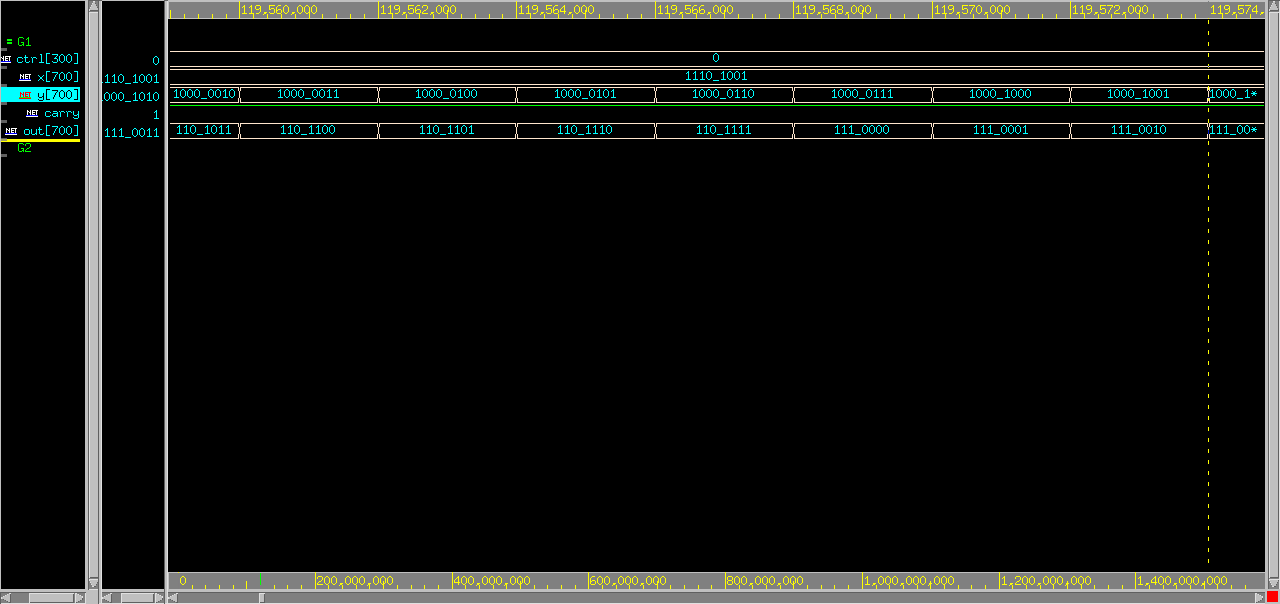
**The implementation of alu\_rtl\_tb2.v and alu\_tb2.v :**

參考 Lab2 中 Lab2\_test\_alu.v 的寫法，對於每個operation皆考慮x及y所有可能的組合情形，並在console上印出test通過或失敗的訊息；以Addition的test pattern 為例:

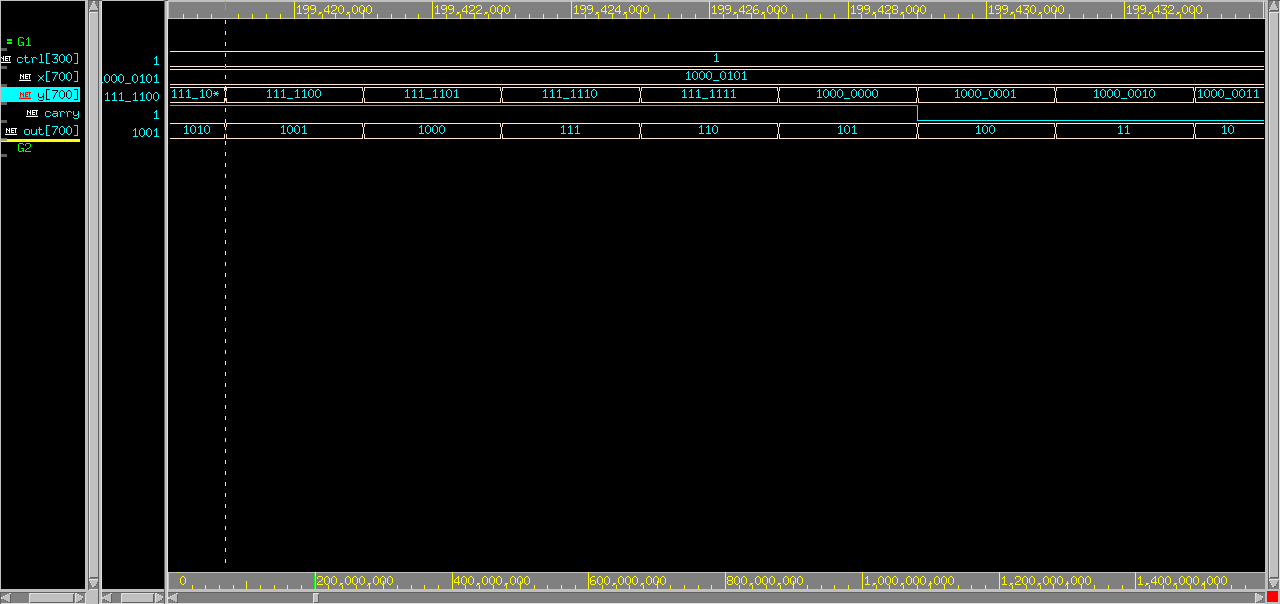


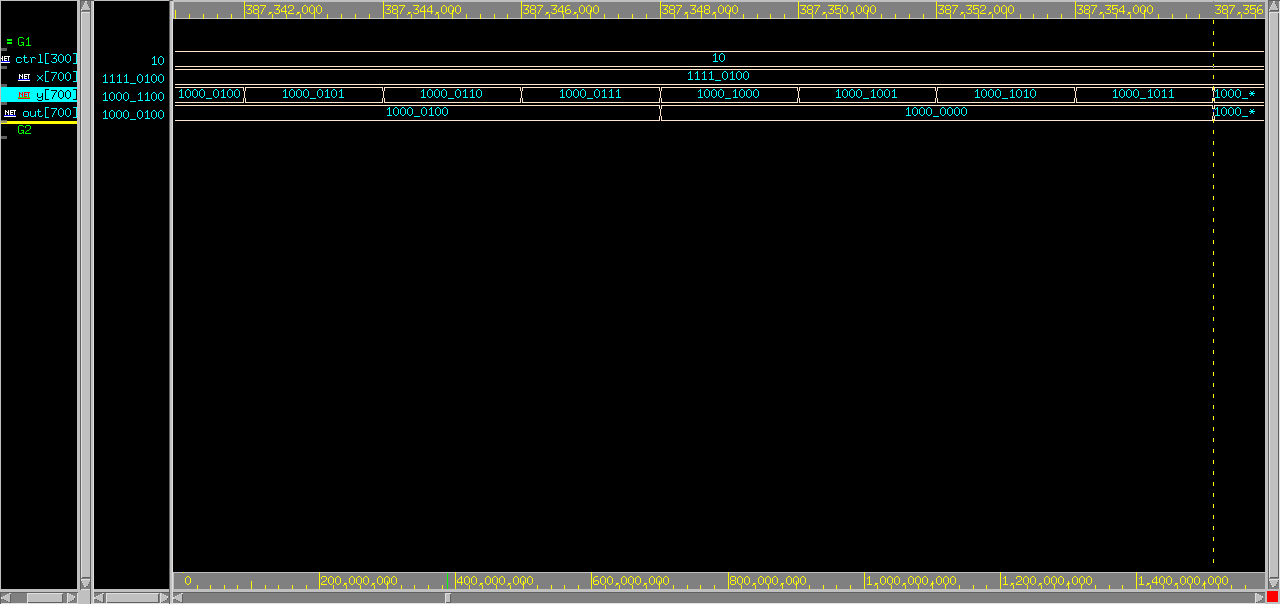
而每個operation所得波形圖如下所示: (case ctrl)

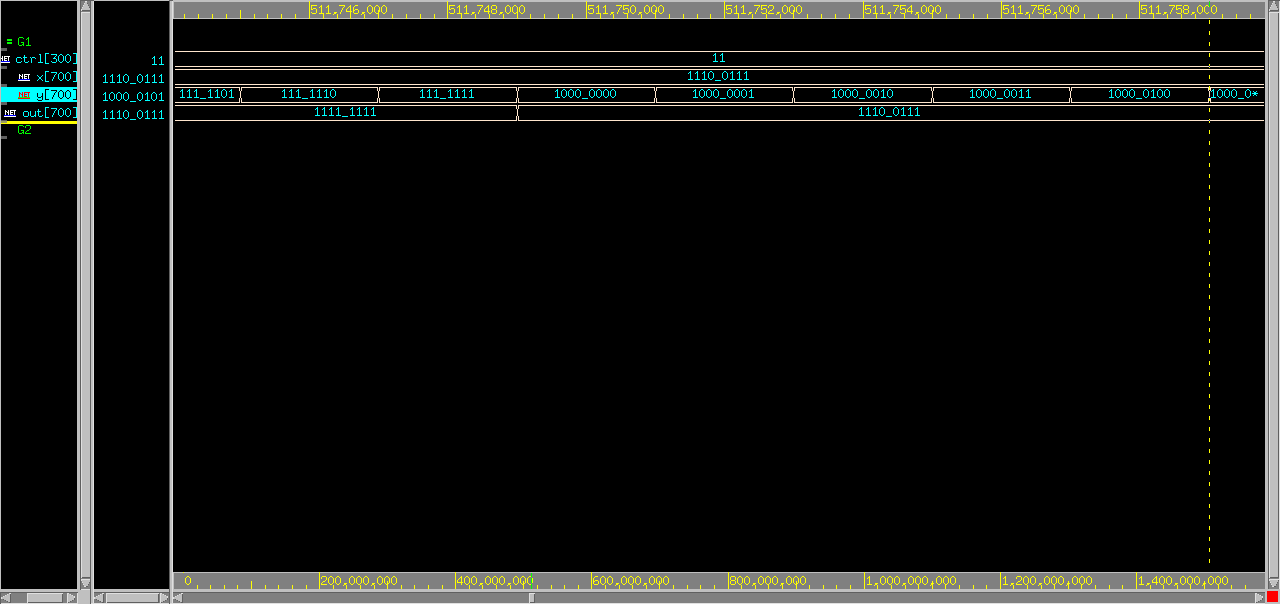
1. (ctrl == **4'b0000**) 🡪 out = x **+** y ;



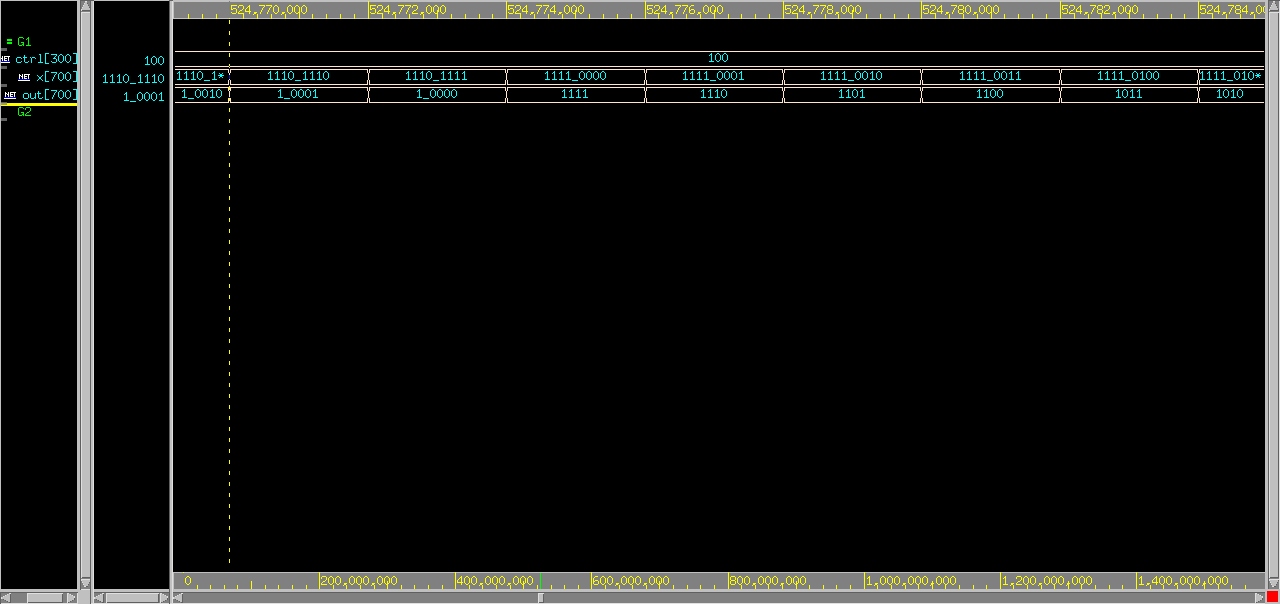
1. (ctrl == **4'b0001**) 🡪 out = x - y ;

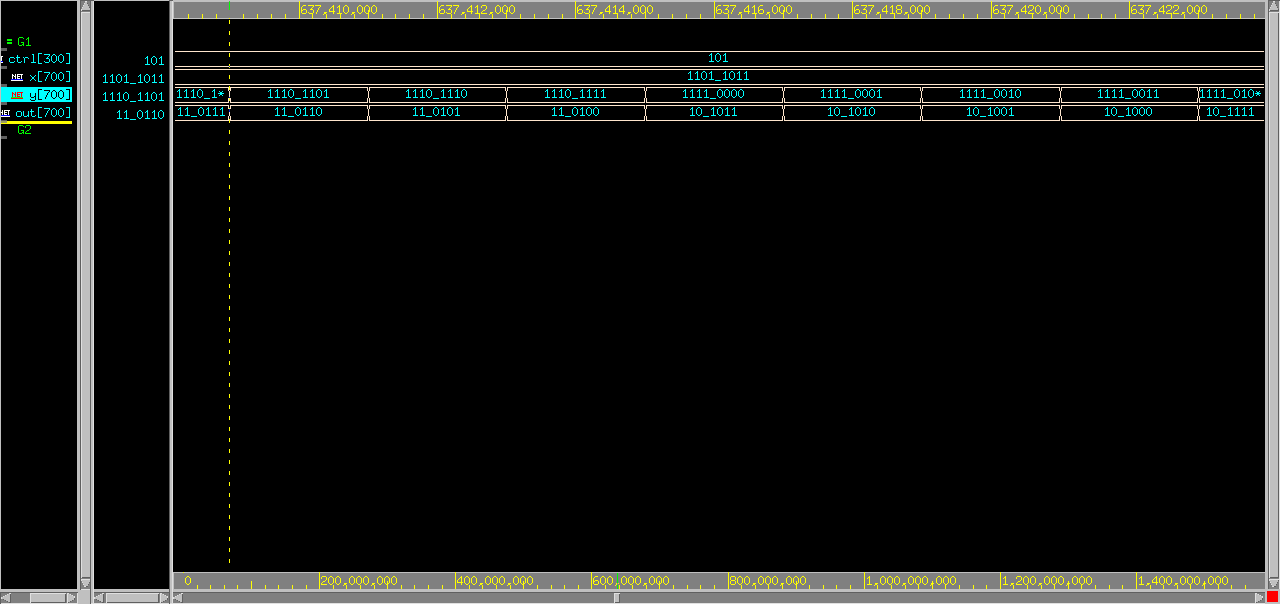


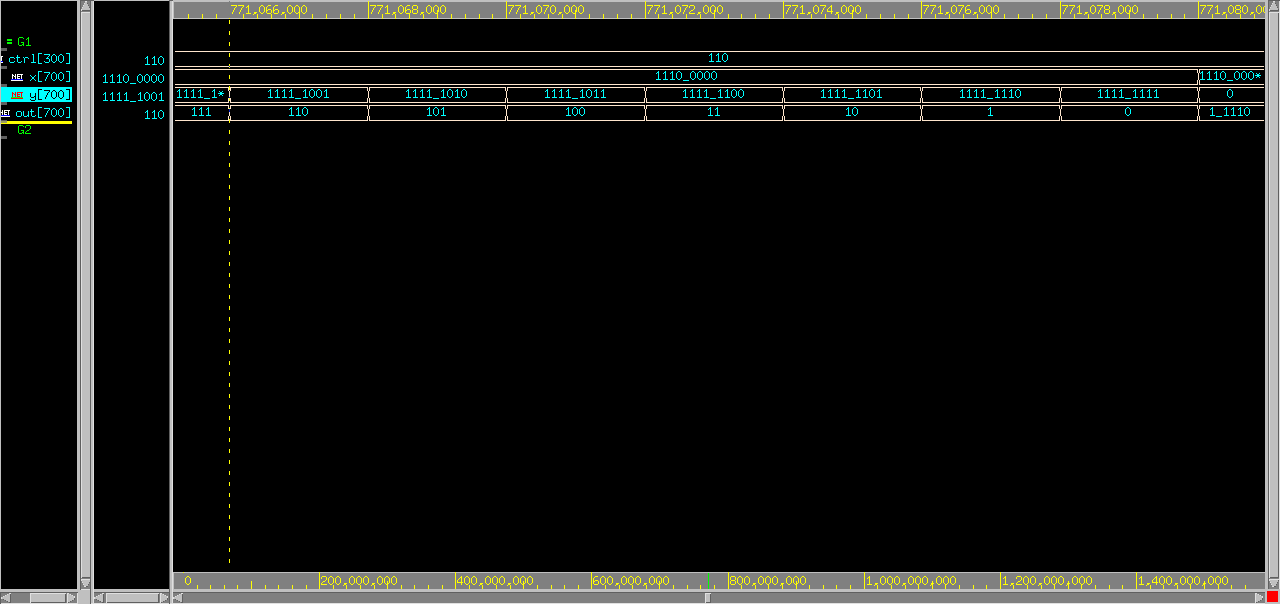
1. (ctrl == **4'b0010**) 🡪 out = x **&** y ;
2. 
3. (ctrl == **4'b0011**) 🡪 out = x **|** y ;



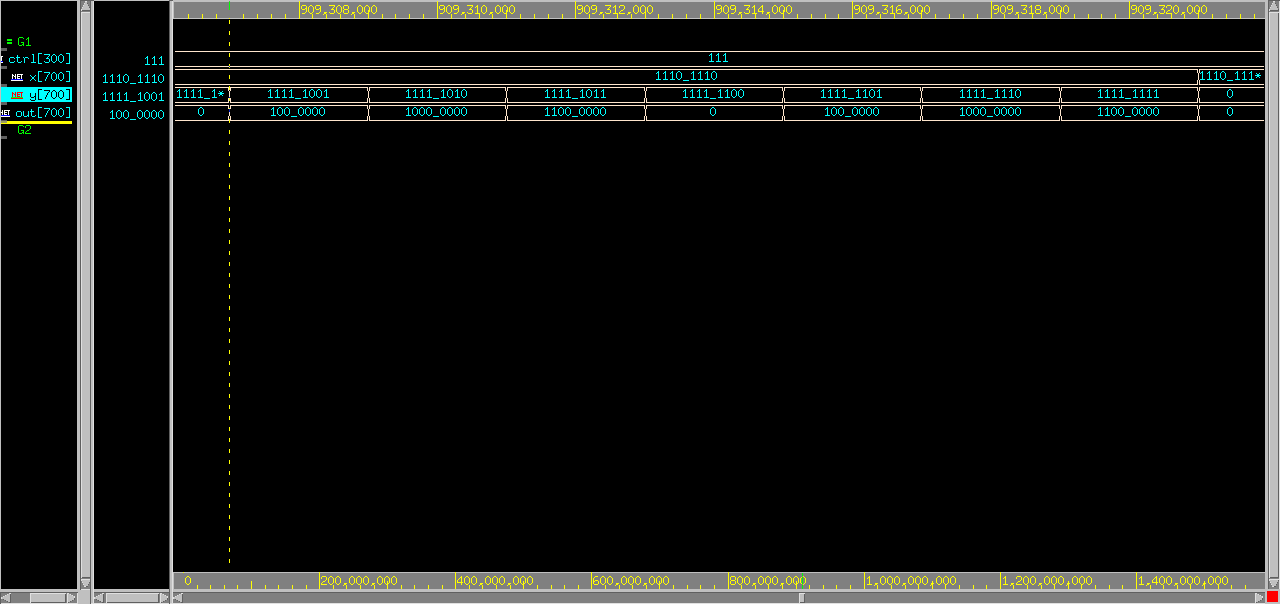
1. (ctrl == **4'b0100**) 🡪 out = **~** x ;

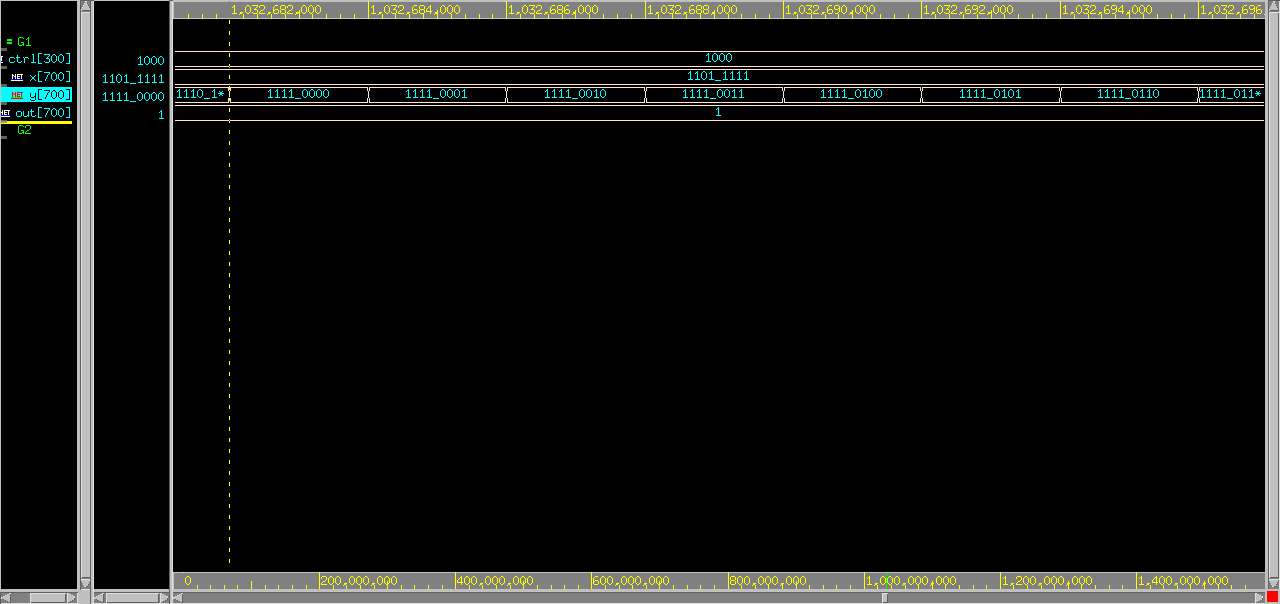


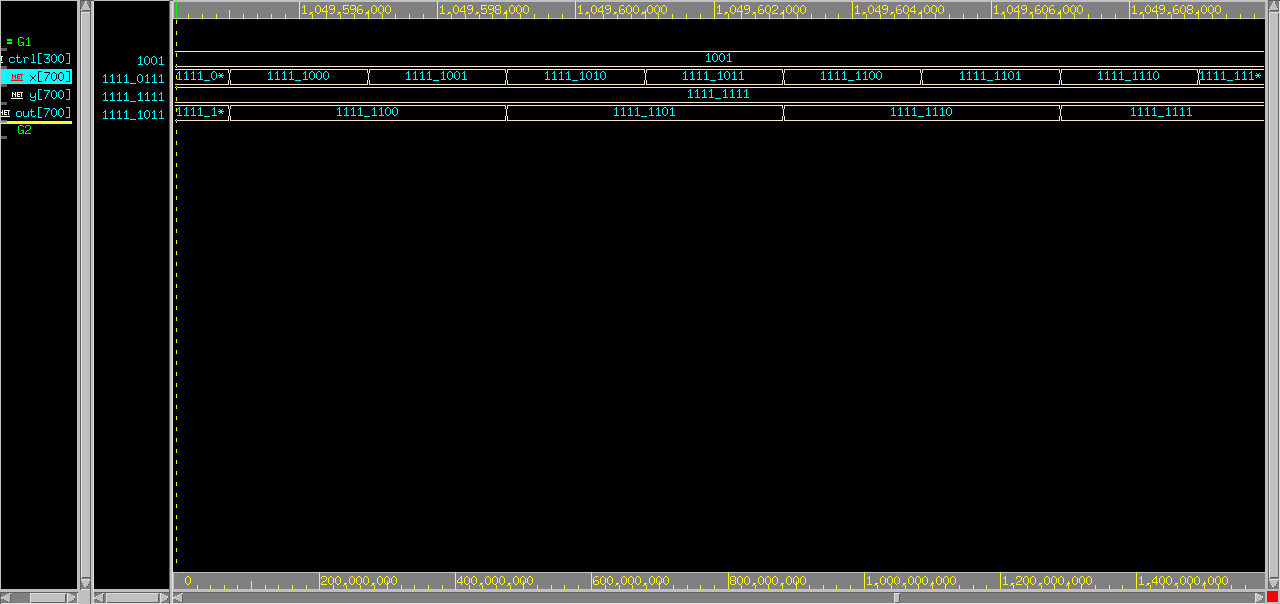
1. (ctrl == **4'b0101**) 🡪 out = x **^** y ;
2. (ctrl == **4'b0110**) 🡪 out = **~**x **&** **~**y ;



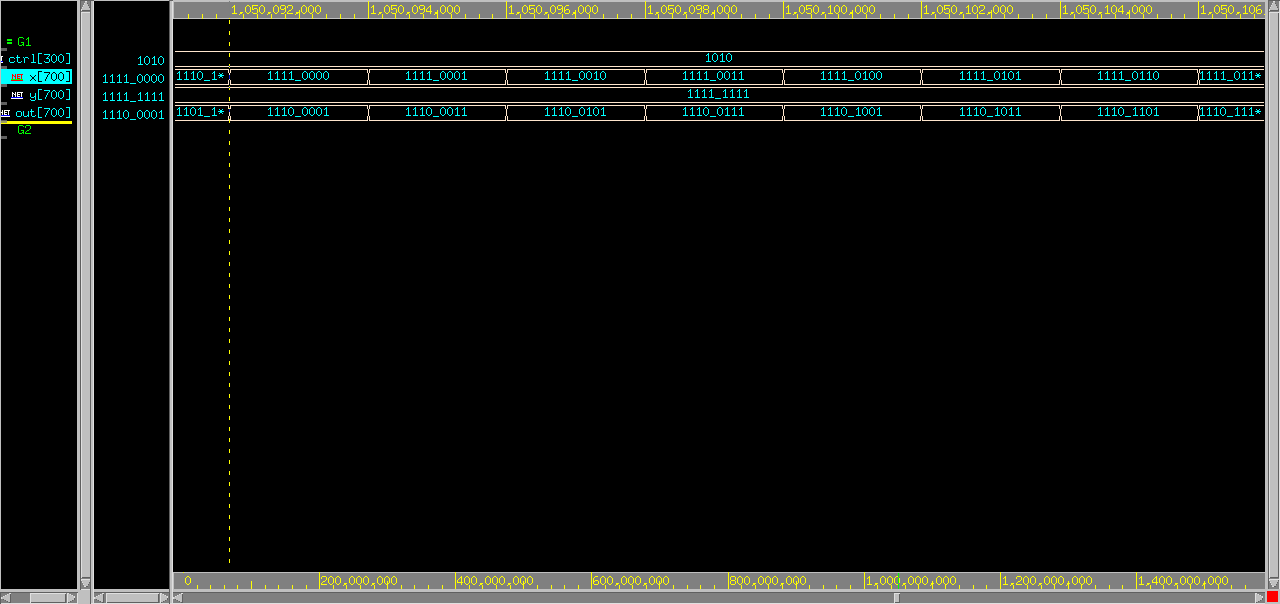
1. (ctrl == **4'b0111**) 🡪 out = **y << x[2:0]** ;



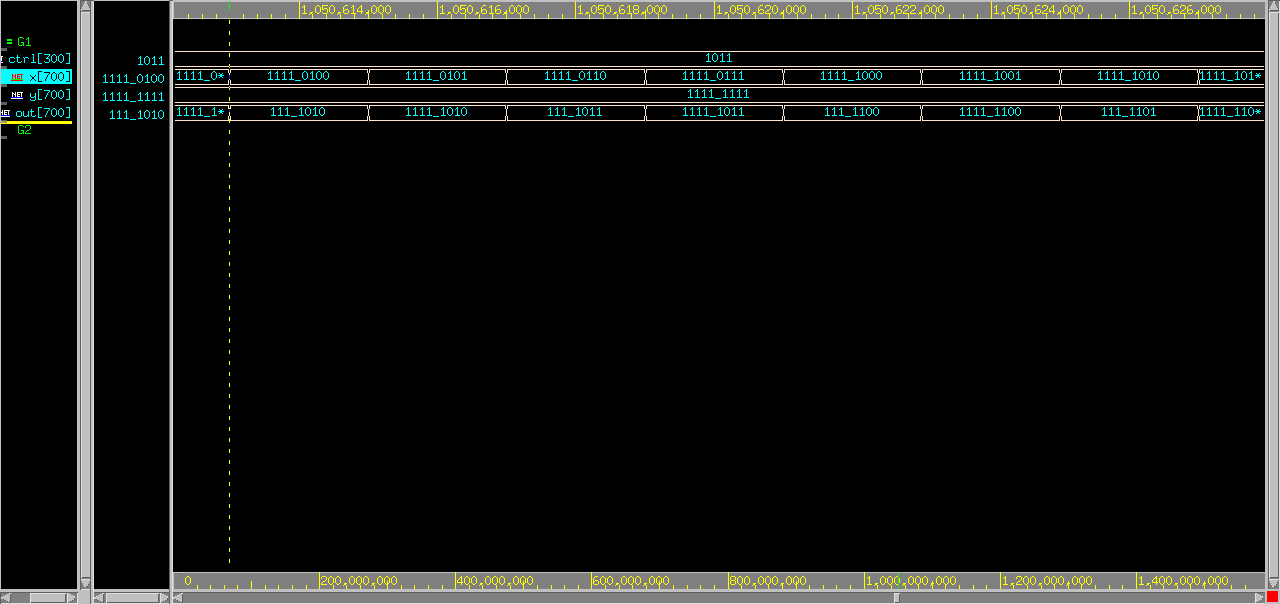
1. (ctrl == **4'b1000**) 🡪 out = **y >> x[2:0]** ;
2. (ctrl == **4'b1001**) 🡪 out **= {x[7],x[7:1]}** ;



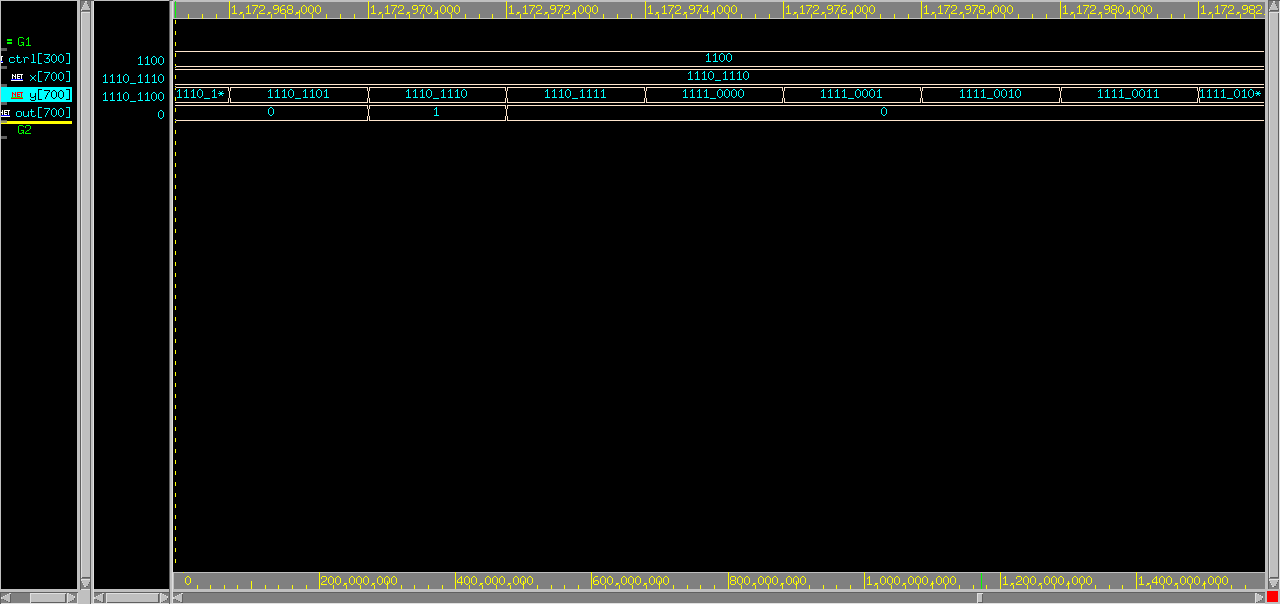
1. (ctrl == **4'b1010**) 🡪 out **= {x[6:0] , x[7]}** ;



1. (ctrl == **4'b1011**) 🡪 out **= {x[0] , x[7:1]}** ;



1. (ctrl == **4'b1100**) 🡪 out **= (x==y) ? 1 : 0** ;

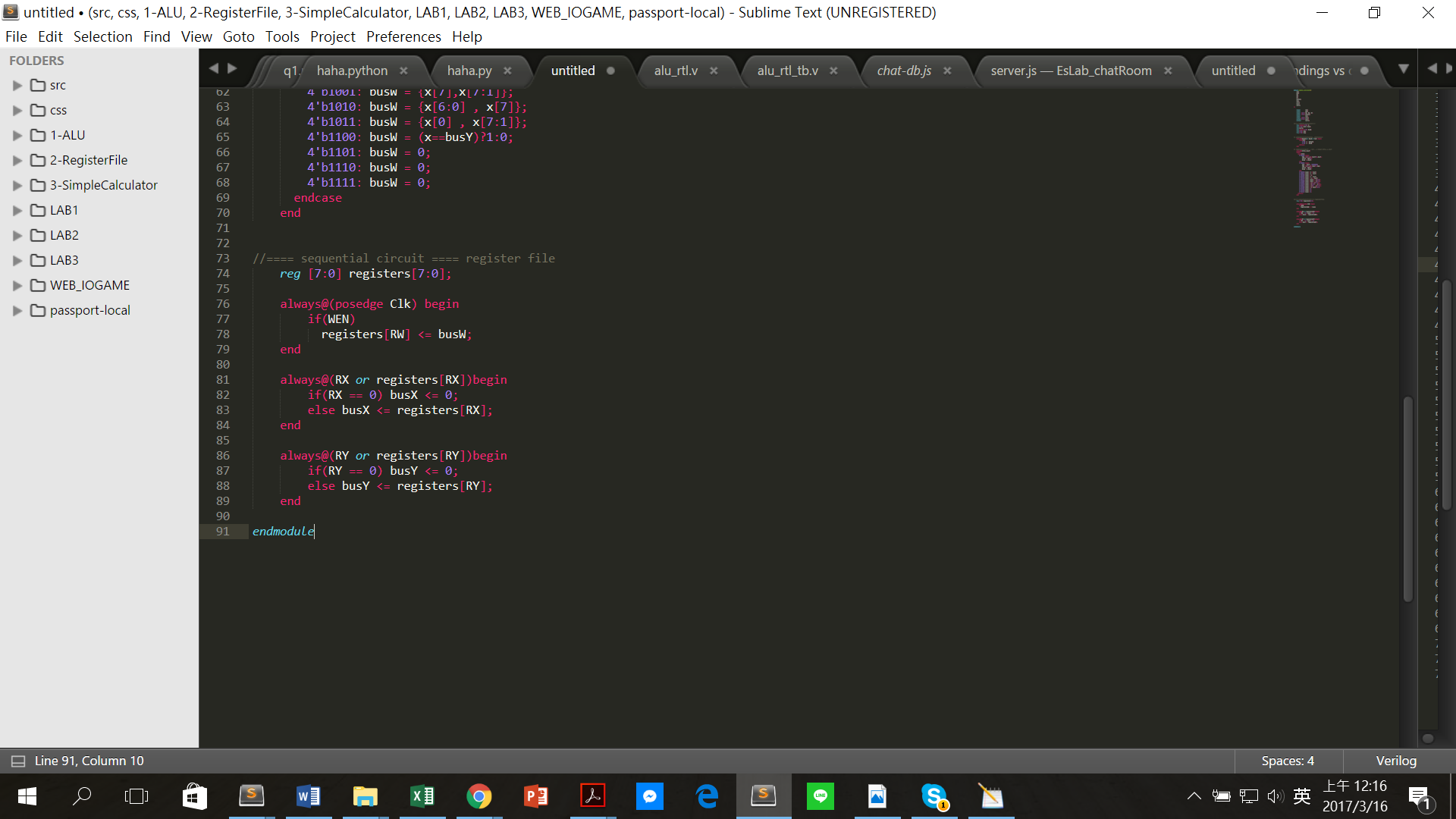
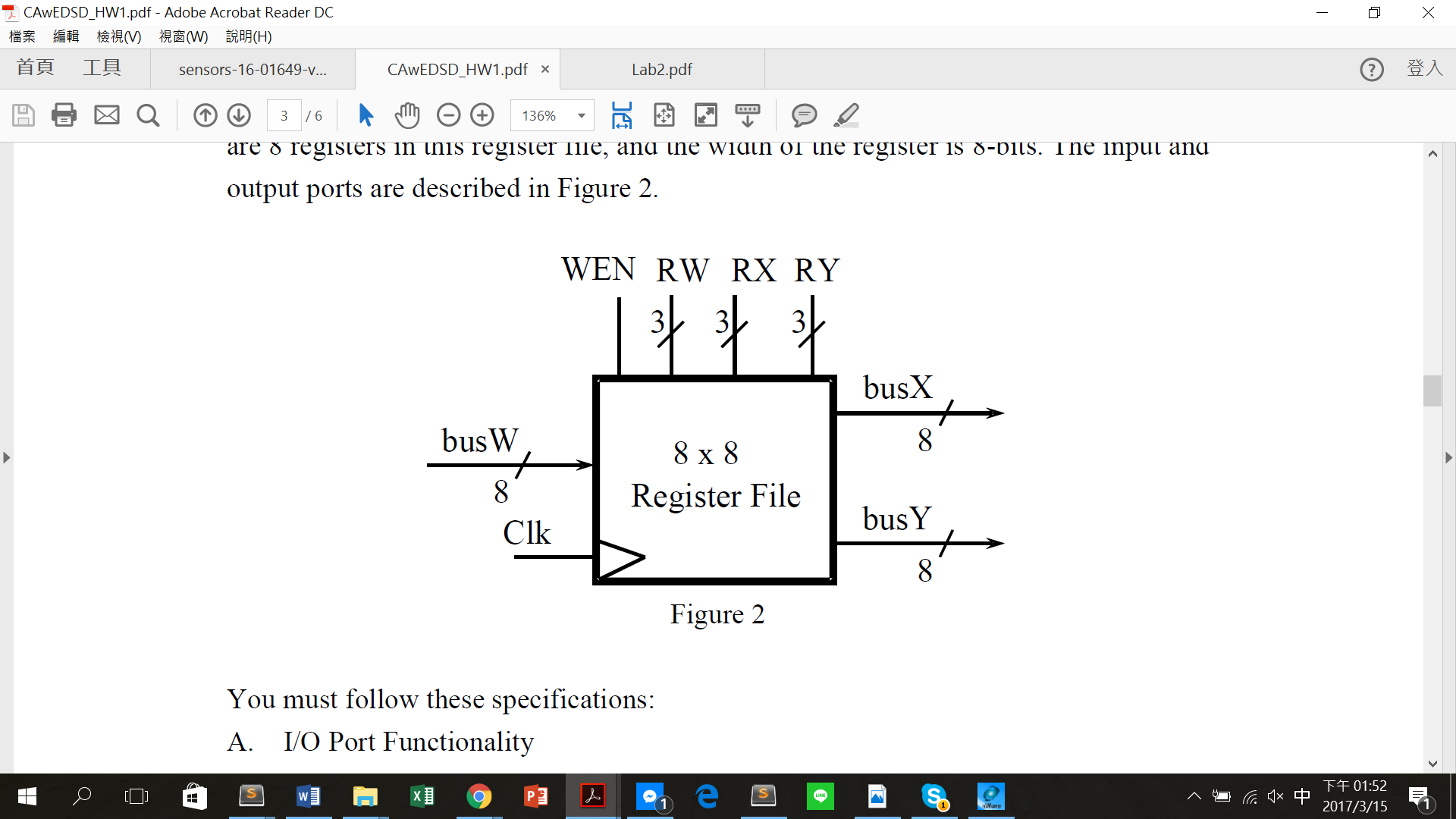


1. (ctrl == **4'b1101** or **4'b1110** or **4'b1111**) 🡪 out **= 0** ;

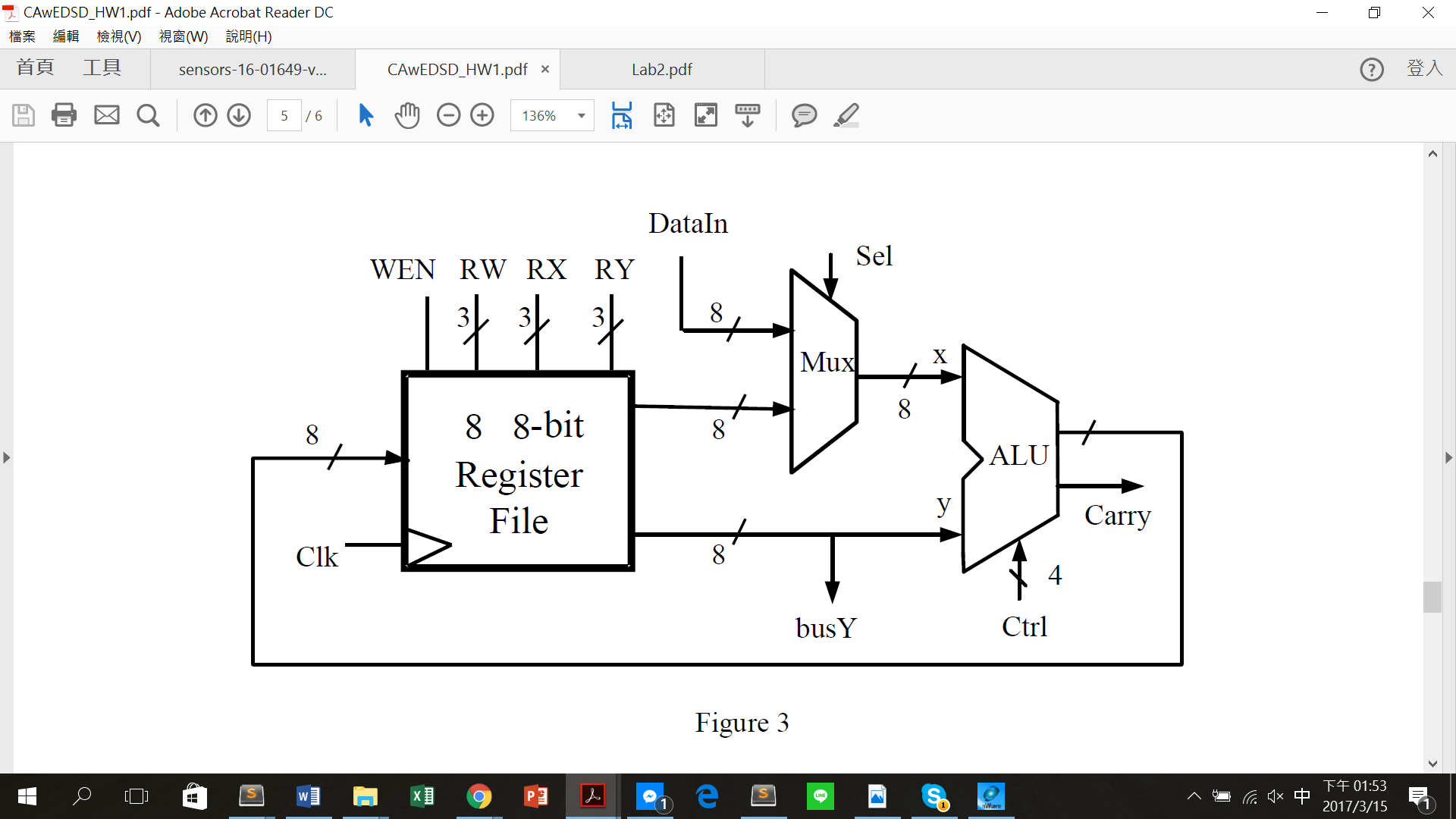


1. **8x8 Register File**

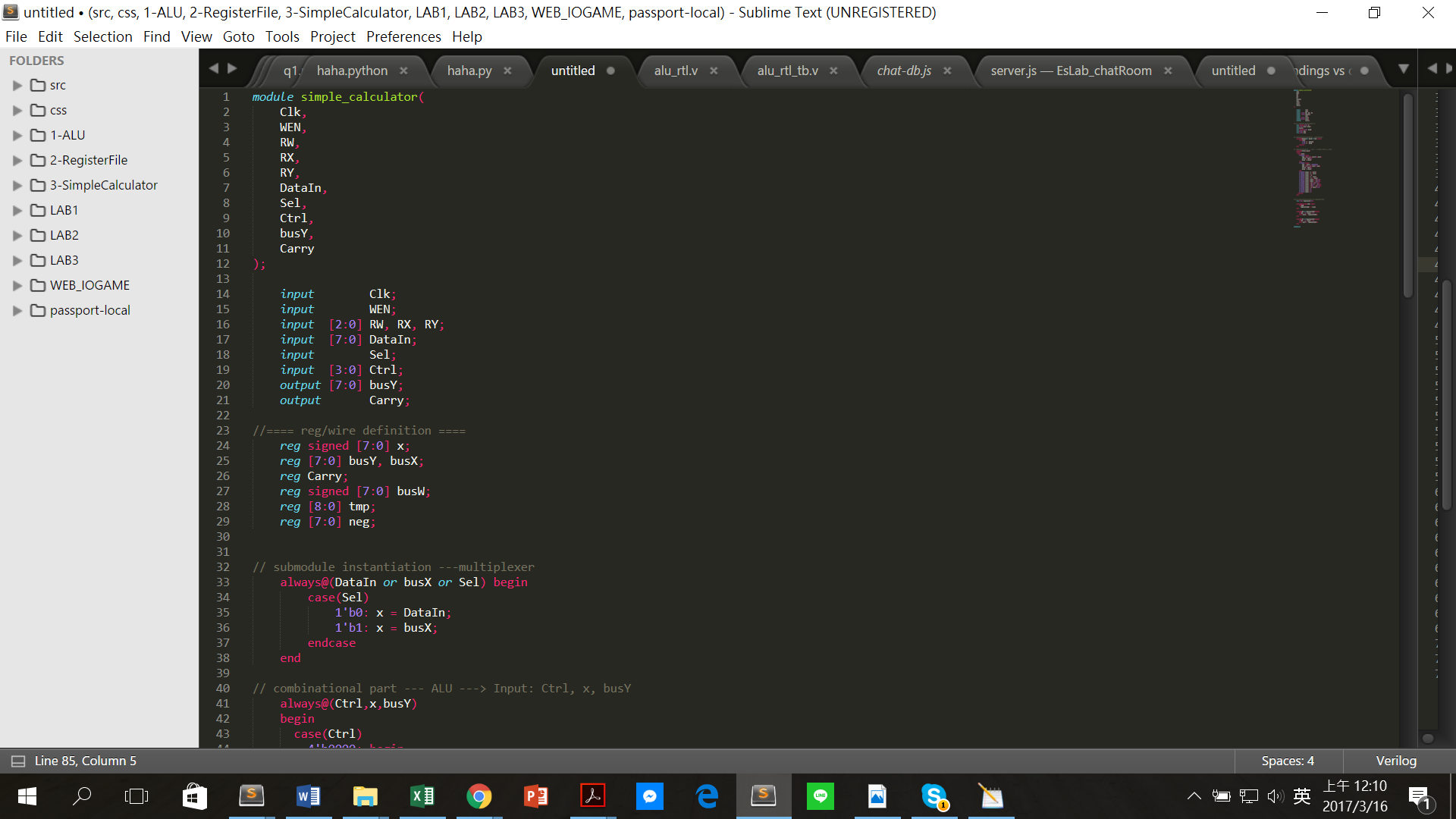
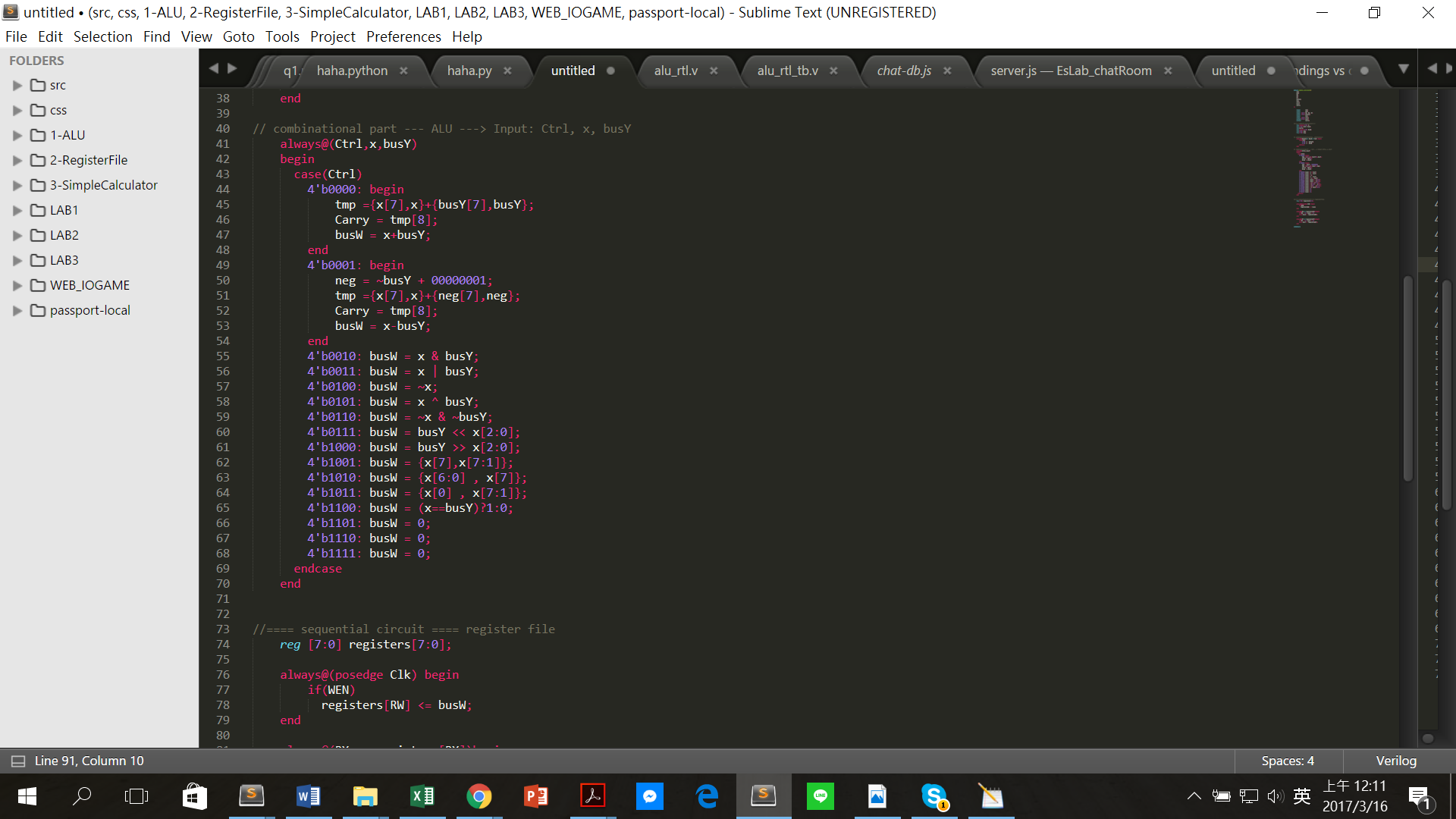
關於 $r0 = constant zero :

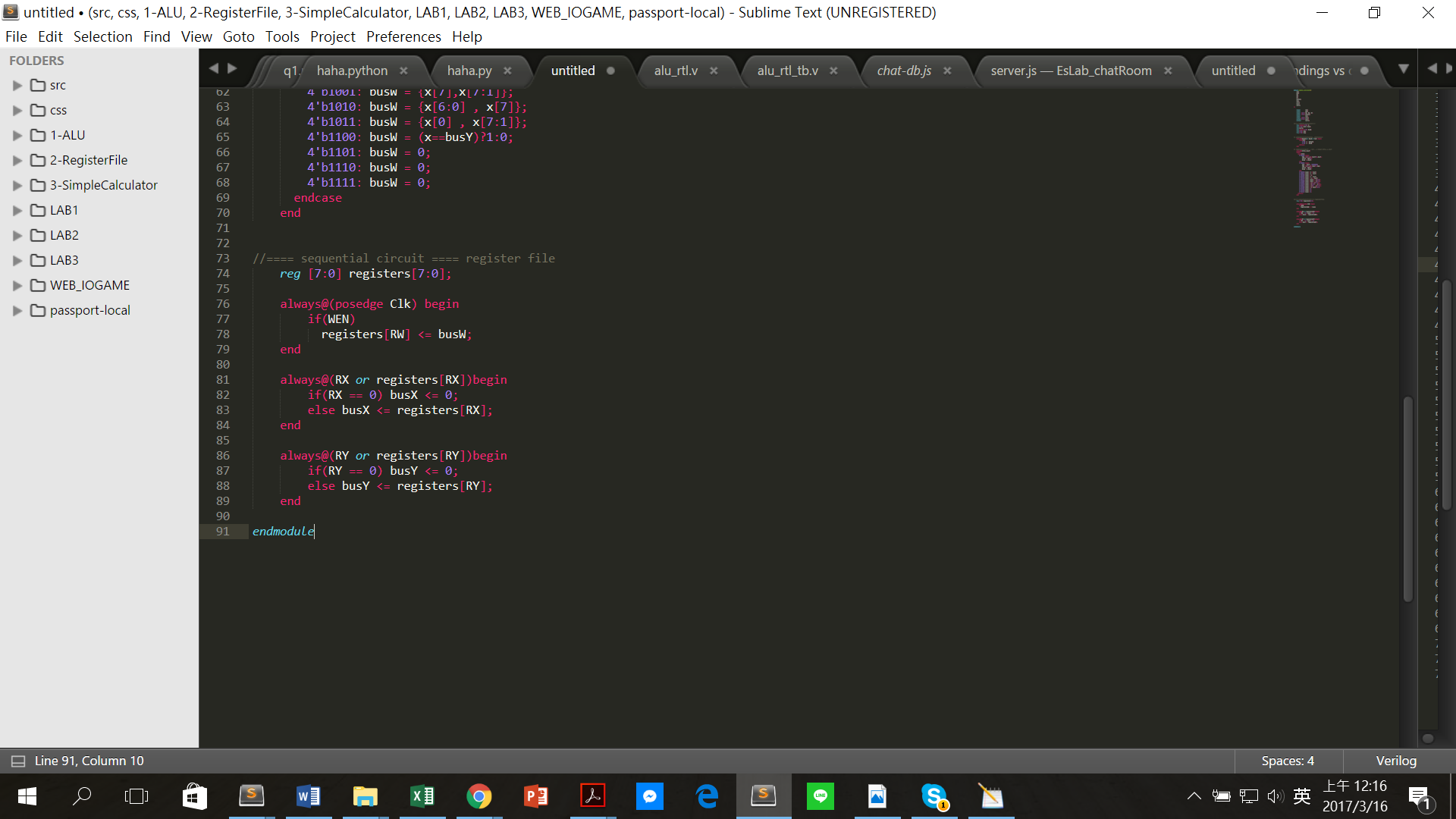


**3. Simple Calculator**



Design:





波形圖:

